PL23B3
Single-chip USB HID to UART Bridge Controller

USB Interface

- Fully Compliant with USB 2.0 specification (Full-Speed Mode).
- UHCI/OHCI (USB 1.1), EHCI (USB 2.0), xHCI (USB 3.1) Host Controller Compatible.
- USB Human Interface Device (HID) class:
  - No driver installation needed for Windows, Mac, Linux, and Android.
  - Provides HID-to-UART SDK libraries for application development.
- Integrated termination resistors and pull-up resistor on USB signal pins to reduce external components.
- Supports 256-byte OTPROM (One-Time Programmable ROM) programming by software tool via USB interface for USB device descriptors and GPIO configuration. Each IC has unique ID (for Serial Number).
- Supports USB power configuration (bus-powered, self-powered)

GPIO Interface

- Total 2 General Purpose I/O (GPIO) pins with Versatile functions can be configured by software tool via USB interface
- Optional Clock Output for external MCU.[1]
- A trigger pin to control the USB device attachment to USB host controllers.

UART Interface

- Supports Serial UART Interface:
  - TXD and RXD UART pins
  - Flexible baud rate up to 115200 Mbps
  - 5, 6, 7 or 8 data bits
  - Odd, Even, Mark, Space, None parity mode
  - One, one and a half, or two stop bits
- 1024-byte bi-directional data FIFO buffers (768-byte receive/256-byte transmit) for faster data throughput. Configurable in OTPROM.
- Configurable Transmit and Receive access pins for LED indicators.[1]

Miscellaneous

- Integrated self-generated precise clock generator (No external crystal required).
- Integrated Power-on-Reset (POR) circuit.
- Wide operating voltage 2.8V – 5.5V(VIN)
- Low operating power and USB suspend current.
- -40°C to 85°C Operating Temperature.
- Available in 8-pin SOP package (RoHS compliant and Pb-free Green Compound).

Prolific Technology Inc.
7F, No.48, Sec. 3, Nan Kang Rd., Nan Kang, Taipei 115, Taiwan
Tel：+886-2-2654-6363; Fax：886-2-22654-6161
Website：http://www.prolific.com.tw/

Document Version：v0.4

Product Data Sheet PL23B3

1. Product Applications

- USB to UART converters/cables/ adapters
- Extension of UART interface for MCU and CPU ICs data transferring and device control for Healthcare/Medical/GPS Navigator …etc. portable devices and instrumentation and industrial and automation equipment.

2. HID to UART API Library Support

Human Interface Device (HID) class is natively supported in almost all operating systems. No custom driver is required to be installed. Prolific provides Dynamic-Link Library (DLL) API libraries for customers to develop their application software. Refer to the PL23B3 HID to UART SDK documentation on how to control the PL23B3 using the DLL.

- Windows 10, 8, 7, Vista, XP
- Windows Server 2003, 2008, 2008 R2, 2012, 2016
- Mac OS X
- Linux OS
- Android 3.2 and above

3. Ordering Information

Chip Product Name	Package Type	Ordering Part Number	MPQ
PL23B3	8-pin SOP (Lead Free)	PL23B3G3PEG7P1	100pcs / tube
		PL23B3G3PEG8P1	2500pcs / reel

Prolific Technology Inc.
7F, No.48, Sec. 3, Nan Kang Rd., Nan Kang, Taipei 115, Taiwan
Tel：+886-2-2654-6363; Fax：886-2-22654-6161
Website：http://www.prolific.com.tw/

Table of Contents

List of Figures

List of Tables

4. Block Diagram

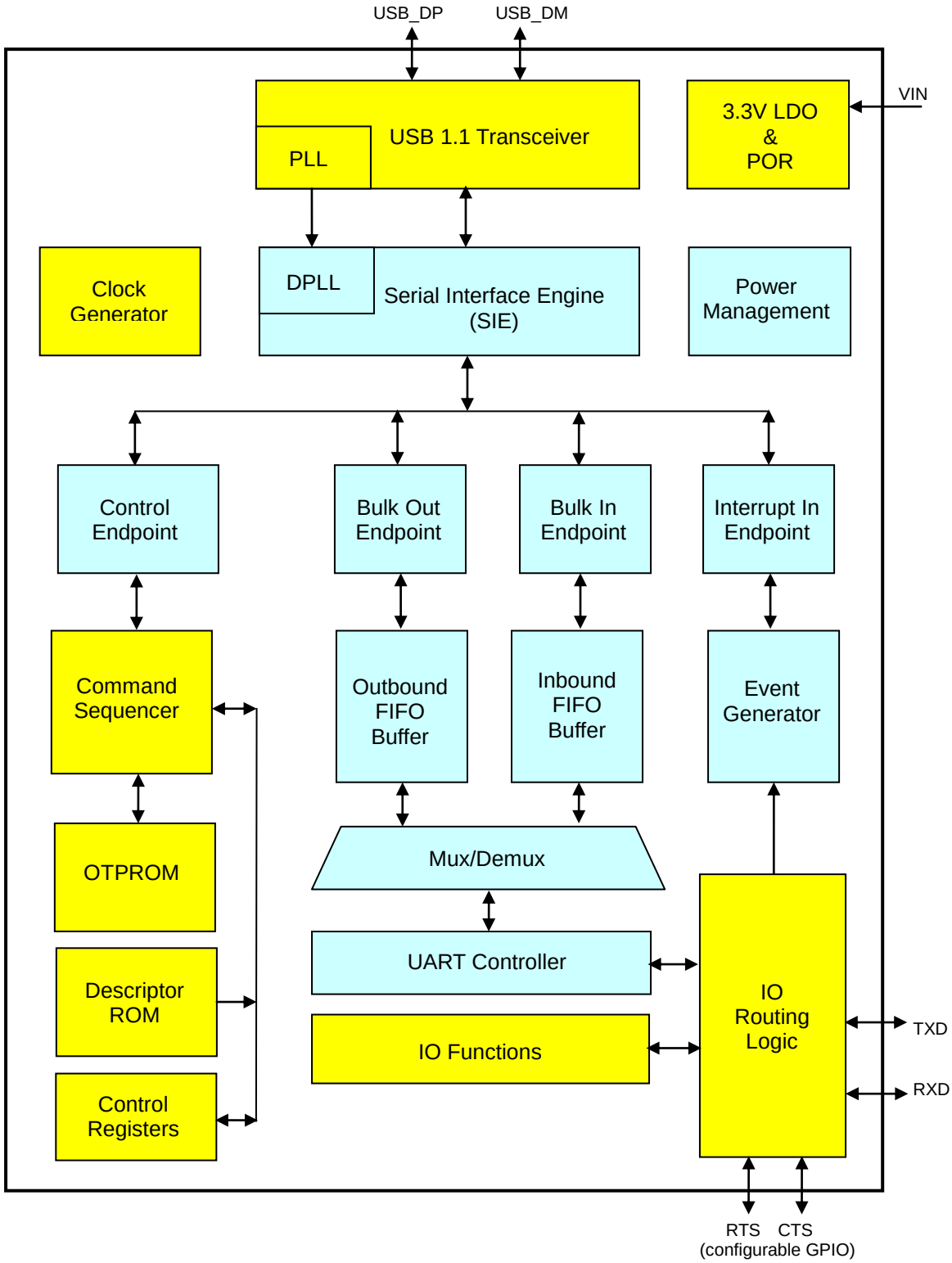


Figure 4-1 PL23B3 Block Diagram

5. USB Logo Certification

T.B.D

6. Overview

The PL23B3 is an USB HID to UART bridge controller for bridging an UART asynchronous serial interface device to any Universal Serial Bus (USB) capable host. The PL23B3 implements the standard USB Human Interface Device (HID) device class which is natively supported in most operating systems; so the PL23B3 does not need any custom driver installation. The operating system or USB host communicates with the PL23B3 through HID application software developed based on Windows/Mac/Linux DLL libraries provided by Prolific.

The PL23B3 UART interface provides TX and RX signals to implement USB to UART bridging and full controls including baud rate support up to 115200 Kbps, data/parity/stop bit configuration.

The PL23B3 integrates an internal precise clock generator (no external crystal required), USB 1.1 transceiver, Serial Interface Engine (SIE), LDO voltage regulator, power-on- reset (POR), FIFO data buffers, and One-Time Programming ROM (OTPROM). The OTPROM allows product vendors to customize some USB descriptors and configurations like USB Vendor ID (VID), Product ID (PID), Manufacturer and Product strings, USB Serial Number, power configuration as well as GPIO configurations.

Key feature:

- USB1.1/Full speed HID class to UART bridge
- Baud rate: 1-115200 Kbps
- 2.8V to 5.5V operating voltage
- No external crystal required
- 8 pin SOP packages available
- Operating temperature: -40°C to +85°C

Enhanced feature:

- 2 GPIO pins can be configured with the following versatile functions:
  --clock output
  --UART accessing LED indicator(output)
- Trigger input to control PL23B3 attachment to USB host controllers.
- Detection output when device attachment detection When device is attached to USB host and configured by USB host
- Detection output to indicate that the chip is in the un-configured state or suspend state

PL23B3 is designed to support a wide-range of serial application domain including mobile, embedded, industrial, consumer, healthcare, navigation, and wearable devices. With very small power consumption in either operating or suspend mode, PL23B3 is perfect for self-powered operation can reserve power for the attached UART devices. PL23B3 is available in 8-pin SOP RoHS compliant and Pb-free green compound package.

7. Pin Diagram and Description

7.1 SOP8 Pin Diagram

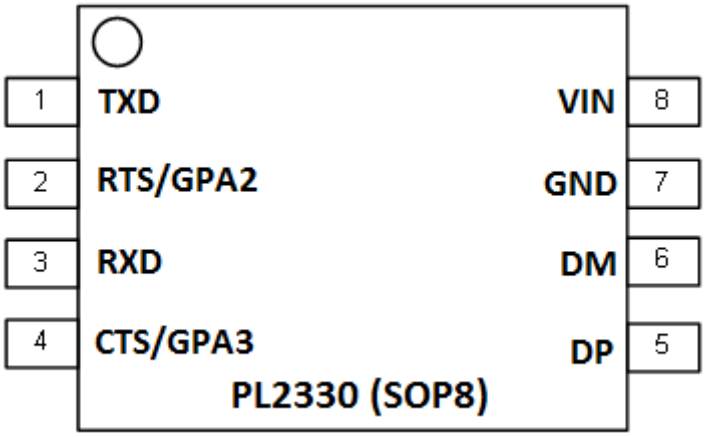


Figure 7-1 PL23B3 Pin Diagram

7.2 Pin Out Description

Table 7-1: USB Data Interface Pins

Pin Name	SOP8 Pin No.	Type	Description
DP	5	I/O	USB Port Data Plus (D+) Signal
DM	6	I/O	USB Port Data Minus (D-) Signal

Table 7-2: UART (Serial Port) Interface Pins

Pin Name	SOP8 Pin No.	Type	Description
TXD	1	Output	Serial Port: Transmitted Data Output
RXD	3	Input	Serial Port: Received Data Input (5V tolerant)

Table 7-3: Configurable GPIO Pins

Pin Name	SOP8 Pin No.	Type	Description
RTS/GPA2	2	I/O	Configurable GPIO Pin. (see Section 7.3)
CTS/GPA3	4	I/O	Configurable GPIO Pin. (see Section 7.3)

Table 7-4: Power and Ground Pins

Pin Name	SOP8 Pin No.	Type	Description
GND	7	Power	Ground
VIN	8	Power	USB port VBUS input power supply.

7.3 GPIO Multi-Function Options

The PL23B3 chip provides a total of 2 configurable GPIO (General Purpose I/O) pins. The table below shows the possible functions that can be configured for each GPIO pin. These special functions can be easily configured in the OTPROM of the PL23B3 using the PL23B3 OTPROM utility tool. When these pins are configured as standard GPIO pins, customers can refer to the PL23B3 HID to UART SDK to develop software to control the GPIO pins for customer application desired functions.

Table 7-5: Configurable GPIO Multi-Function Pins

GPIO	SOP8 Pin No.	Factory Default	Configurable Options (using OTPROM Tool)				
GPA2	2	RTS	TX_LED	CLK_OUT	SUSP_N	USB_CFG	GPIO
GPA3	4	CTS	RX_LED	TRX_LED	VBUS_DET	GPIO	

Table 7-6: GPIO Multi-Function Option Descriptions

GPIO Function	GPIO Pins	Type	Description
TX_LED	GPA2	Output	Serial Port: TXD Access LED.
RX_LED	GPA3	Output	Serial Port: RXD Access LED.
TRX_LED	GPA3	Output	Serial Port: TXD and RXD Access LED.
VBUS_DET	GPA3	Input	When this pin is set to VBUS_DET mode, the device will not attach to USB until VBUS_DET input pin goes to high level. NOTE: Only one pin can be configured as VBUS_DET pin.
USB_CFG	GPA2	Output	When device is attached to USB port and configured by USB host, this USB_CFG pin will output to high level. This pin can be used to enable system function after USB is configured.
SUSP_N	GPA2	Output	Active low Shutdown control pin. This pin has two options to choose. One is to indicate chip suspend state by USB bus state. The other option (factory default) is to indicate chip un-configured state and chip suspend state.
CLK_OUT	GPA2	Output	This pin can generate clock output up to 12MHz. Clock rates can be configured in OTPROM.

8. Functional Description

This section details the functional block diagram description of the PL23B3.

8.1 USB 1.1 FS Transceiver

The USB Transceiver provides the USB full-speed electrical signal requirements and USB physical interface (DP/DM). This block also includes one precise internal oscillator for PLL. The PLL provides the clock to other logic functions. This block also includes the internal USB series termination resistors on the USB data lines and pull-up resistor for the DP signal.

8.2 LDO Regulator

This block is the 5V to 3.3V LDO regulator to power and drive the USB transceiver. It also includes 3.3V brownout detection output signals that will be used by digital circuit to reset the chip.

8.3 Clock Generator

The clock generator module generates the 48MHz and 12MHz reference clock signals for internal chip logic. The internal clocks will be stopped while in suspend state.

8.4 USB FS SIE

The USB Full-Speed Serial Interface Engine (SIE) block performs the processing of USB DP/DM signals. It translates the internal parallel data to serial data and outputs to USB FS transceiver to generate external USB DP/DM signals timing. It also translates external USB DP/DM signals pass through USB FS transceiver to parallel data for internal circuit. This block supports USB packet decoding and encoding. It also generates and check packet CRC, bit stuffing, SYNC and EOP frame signal. The DPLL module will use the internal 48MHz clock to synchronize external DP/DM transitions to generate 12MHz clock for USB interface related circuit.

8.5 Power Management

This module will monitor the USB attachment and DP/DM signals state to create reset state, running state, suspend state, wakeup state, etc. Reset and suspend signals are generated from this module.

8.6 Control Endpoint

The Control Endpoint module handles control endpoint packet transfer protocols such as SETUP packet, DATA packet and return status packet.

8.7 Bulk Out Endpoint

The Bulk Out Endpoint module handles bulk-out endpoint packet transfer protocols such as DATA packet and return status packet. It also transfers USB host bulk-out data to chip outbound FIFO.

8.8 Bulk In Endpoint

The Bulk In Endpoint module handles bulk-in endpoint packet transfer protocols such as DATA packet and return status packet. It also transfers data inside the chip inbound FIFO to USB host through bulk-in DATA packet.

8.9 Interrupt In Endpoint

The Interrupt In Endpoint module handles interrupt-in endpoint packet transfer protocols such as DATA packet and return status packet. It transfers interrupt data generated inside the chip to USB host through interrupt-in DATA packet.

8.10 Command Sequencer

This module handles the USB standard requests and vendor requests. It dispatches control signals to relative peripheral modules and gather information from peripheral modules. When it received USB standard request commands, it may check ROM data or data latched from OTP and return them to USB host. When vendor requests are received, it dispatches to peripherals to set or get something.

8.11 Outbound FIFO

This buffer receives data from Bulk Out Endpoint and provides data to peripheral modules. It handles read and write pointers and calculate full and empty conditions. There are also near empty threshold check to notify peripheral module that FIFO is going to empty.

8.12 Inbound FIFO

This buffer receives data from peripheral modules and provides data to Bulk In Endpoint. It handles read and write pointers and calculate full and empty conditions. There are also near full threshold check to notify peripheral module that FIFO is going to full.

8.13 Event Generator

This module provides interrupt data to Interrupt In Endpoint. This module senses interrupt event toggle from UART peripheral.

8.14 Internal OTPROM

The OTPROM (One-Time Programming Read-Only Memory) for the PL23B3 is used to store chip function settings and USB descriptor related data. A one-time programming user area of the memory is available to allow customization of settings. The user area of the PL23B3 OTPROM can now be easily programmed using the Prolific OTPROM utility tool through USB port without any additional voltage converter requirement. Refer to Section 9.0 for more information on the OTPROM configuration settings.

8.15 Mux/Demux

This module is designed to pass data between FIFO and UART peripheral module.

8.16 Descriptor ROM

This block contains the USB descriptor data for returning to USB host.

8.17 UART Control

The UART Control module handles the data transfer according to UART format and interface. This module also includes a precise baud rate generator.

8.18 Control Registers

The Control Registers module contains the chip control registers read and set, and initially loads from OTPROM. USB host will use USB vendor command to read and write control registers to set chip function.

9. Chip Function Configuration

The default configuration descriptors are stored in the chip internal memory which will be loaded during power-on reset or USB bus reset whenever OTPROM (One-Time Programmable ROM) is empty. Several of the USB and configuration descriptors could be modified and programmed one-time into the chip's OTPROM using the PL23B3 OTPROM Writer tool. These descriptors include Vendor ID, Product ID, Serial Number, Product String, and other USB configuration descriptors.

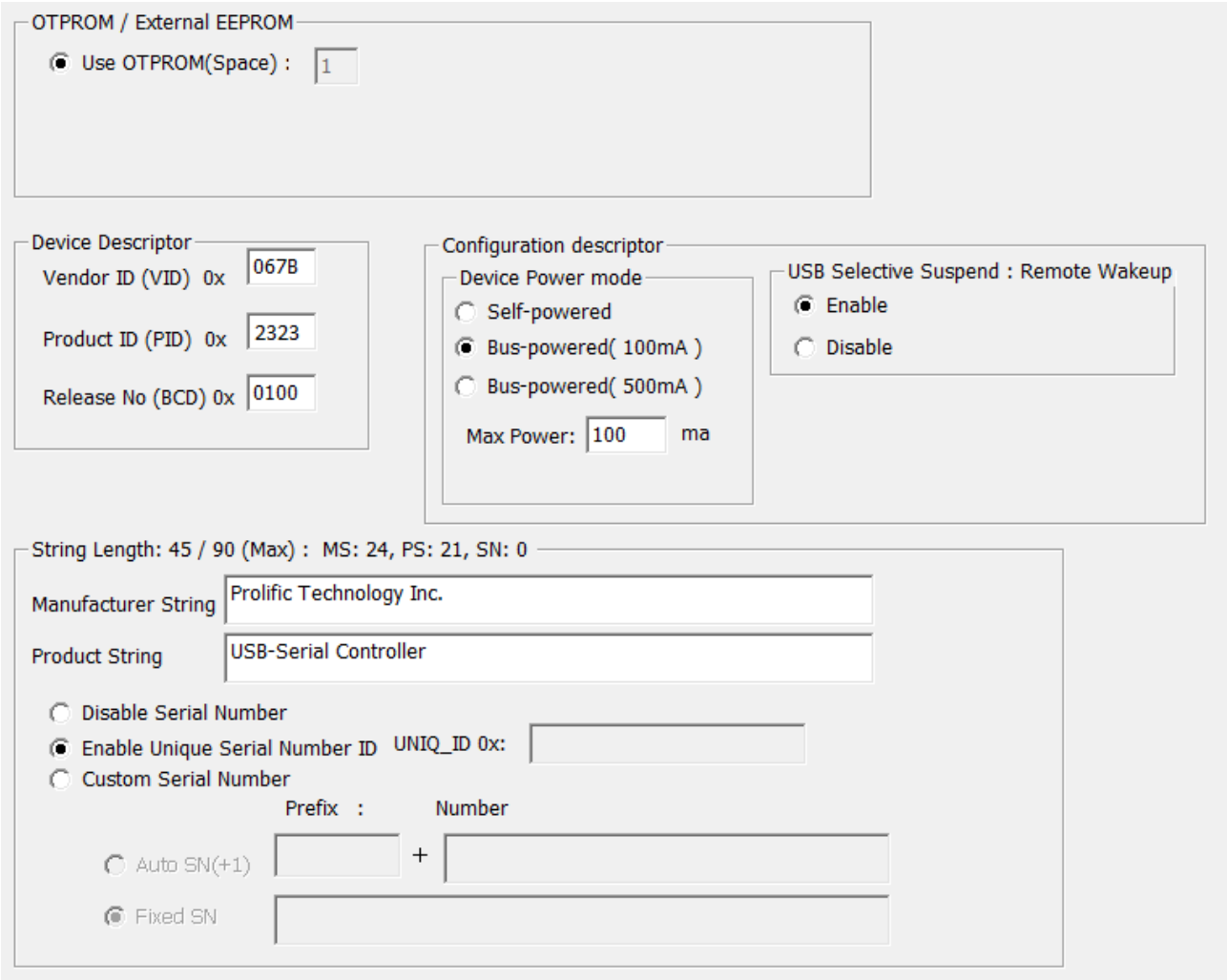


Figure 9-1 PL23B3 OTPROM Writer Tool

9.1 USB Data Configuration

Table 9-1 USB Descriptor Configuration

Descriptors	Default Value	Description
OTPROM Space	1	This field indicates the space left for the OTPROM that can be written (1 or 0). The OTPROM can only be written once and cannot be erased. If value is 0, it means OTPROM has already been written once.
Vendor ID (VID)	067B (hex)	USB unique Vendor ID of Company or Manufacturer. This ID is applied and registered from USB-IF. Refer to this website for applying VID: http://www.usb.org/developers/vendor/
Product ID (PID)	2330 (hex)	USB Product ID assigned by Manufacturer.
Release No. (BCD)	0100 (hex)	This field reports the release number of the USB device chip. This item is not allowed to be modified.
Device Power Mode	Bus Powered (100mA)	This field sets the USB device if bus-powered or self-powered device.
Max Power	100mA	This field sets the USB device maximum power that can be drawn by the device from the USB host. Enter the value here if it is not 100mA or 500mA. Expressed in 2 mA units (i.e., 50 = 100 mA).
USB Selective Suspend	Enable	This field enables/disables the USB Selective Suspend function. When enabled, Windows OS will suspend the device when idle for few seconds (COM port not open).
Manufacturer String	Prolific Technology Inc.	This field contains the product manufacturer string.
Product String	USB to SPI Controller	This field contains the product string.

Serial Number	Enable Unique Serial Number ID	• Disable Serial Number – this option will disable the Serial Number. Operating System will assign a random serial number for the device.
		• Enable Unique Serial Number ID – this default option enables the unique serial number pre-programmed inside the chip.
		• Custom Serial Number – this option allows the customer to set own product serial numbering:
		  ○ Auto SN: allows to add prefix while the numbers auto increment after each write.
		  ○ Fixed SN: this will write the same number.

NOTE: The total string length for the manufacturer + product + serial number string is up to 90 characters.

9.2 GPIO (GPA) Configuration

Also refer to Section 7.3 for the complete GPIO Multi-Function options description.

Table 9-2 GPIO (GPA Group) Configuration

GPIO Function	Default Value	Default I/O	Description
GPA2	GPIO	Input	This field allows setting the pin as a standard GPIO or any of the following function: • RTS (default) • TX_LED • CLK_OUT (also refer to MISC folder) • SUSP_N (also refer to MISC folder) • USB_CFG • GPIO (General Purpose I/O)
GPA3	GPIO	Input	This field allows setting the pin as a standard GPIO or any of the following function: • CTS (default) • VBUS_DET (also refer to MISC folder) • GPIO (General Purpose I/O) • RX_LED • TRX_LED
Enable Open-Drain	Disabled		This field sets the selected I/O pin to open-drain output mode.
Enable-Pull Up	Disabled		This field enables the selected I/O pin weak pull-up. **NOTE: The weak pull-up resistor is pull-up to 3.3V. When enabling pull-up for input pins, the input signal voltage should not be higher than the 3.3V voltage.**
Inverse Polarity	Disabled		This field inverts the selected I/O pin input and output signal polarity.
Output Driving Strength	4mA		This field sets the output driving strength of the selected I/O pin. (4mA up to 8mA @VDDIO=default 3.3V)

10. DC & Temperature Characteristics

10.1 Absolute Maximum Ratings

Table 10-1 Absolute Maximum Ratings

Items	Ratings
Power Supply Voltage – VIN	-0.4 to 6.0 V
Input Voltage of I/O with 5V Tolerance I/O	-0.4 to 6.0 V
Storage Temperature	-40 to 150 °C

Note: Permanent device damage may occur if the absolute maximum ratings are exceeded. These are stress rating only, and functional operation should be restricted to within the conditions. Exposure to absolute maximum rating conditions for extended periods may affect the device's reliability.

10.2 DC Characteristics

10.2.1 Operating Voltage and Suspend Current

Table 10-2a Operating Voltage and Suspend Current

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage Range	VIN	2.8	5	5.5	V
Operating Current(1) (Power Consumption)	I_{DD}	-	9.5	15	mA
Suspend Current	I_{SUS}	-	250	450	μA

Note: (1) – No device connected.

10.2.2 I/O Pins

Table 10-2b I/O Pins

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage (CMOS)					
Low	V_{IL}	--	--	0.4	V
High	V_{IH}	2.3	--	--	V
Output Voltage					
Low	V_{OL}	--	--	0.4	V
High	V_{OH}	2.3	--	--	V

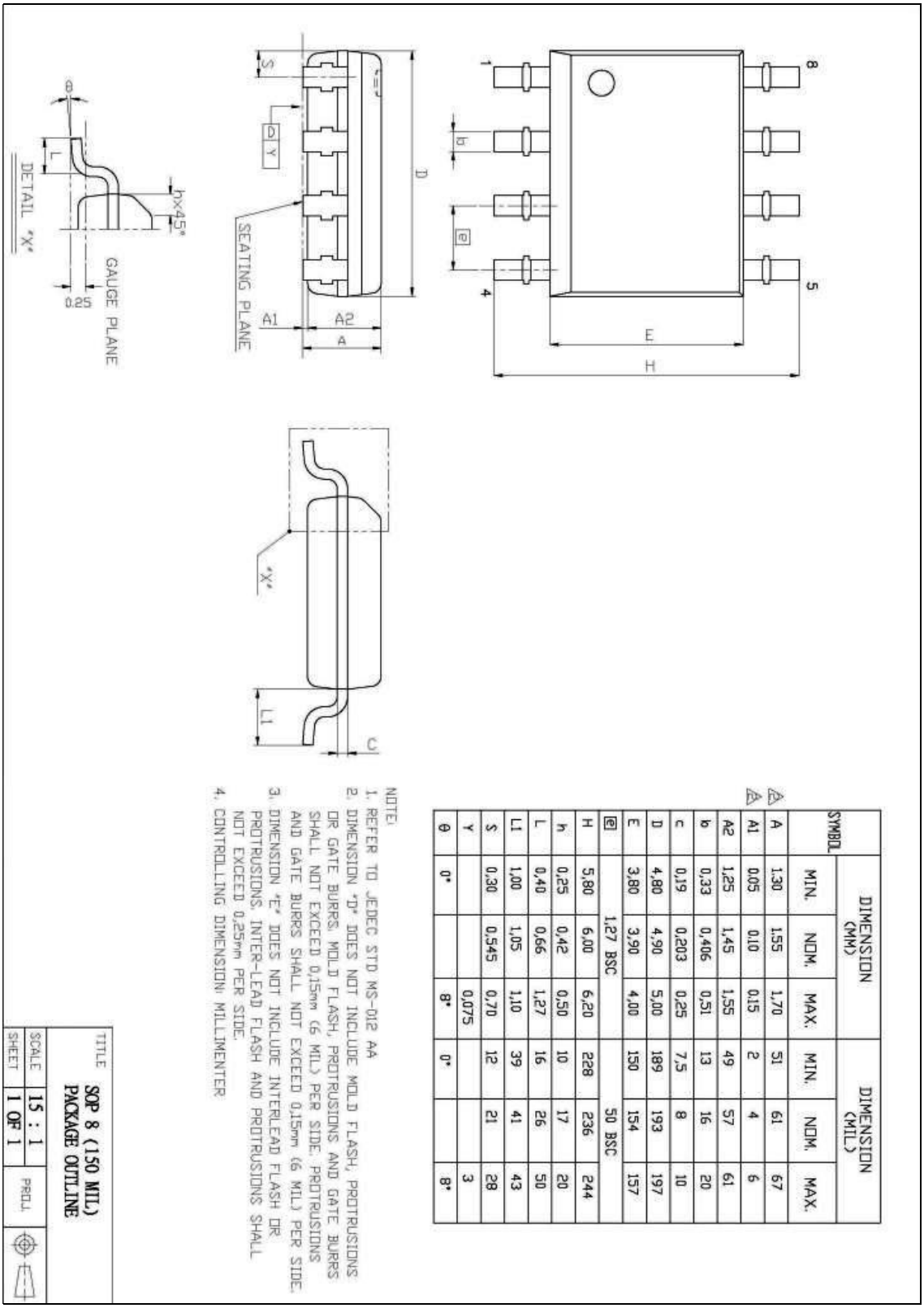
10.4 Temperature Characteristics

Table 10-3 Temperature Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Operating Temperature (ambient)	--	-40	--	85	°C
Junction Operation Temperature	T_J	-40	25	125	°C

11. Outline Diagram

11.1 SOP8 Package



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1,30	1,55	1,70	51	61	67
A1	0,05	0,10	0,15	2	4	6
A2	1,25	1,45	1,55	49	57	61
b	0,33	0,406	0,51	13	16	20
c	0,19	0,203	0,25	7,5	8	10
D	4,80	4,90	5,00	189	193	197
E	3,80	3,90	4,00	150	154	157
e		1,27 BSC			50 BSC	
H	5,80	6,00	6,20	228	236	244
h	0,25	0,42	0,50	10	17	20
L	0,40	0,66	1,27	16	26	50
L1	1,00	1,05	1,10	39	41	43
S	0,30	0,545	0,70	12	21	28
Y			0,075			3
θ	0°		8°	0°		8°

Figure 11-1 PL23B3 Outline Diagram (SOP8)

Disclaimer

All the information in this document is subject to change without prior notice. Prolific Technology Inc. does not make any representations or any warranties (implied or otherwise) regarding the accuracy and completeness of this document and shall in no event be liable for any loss of profit or any other commercial damage, including but not limited to special, incidental, consequential, or other damages.

Trademarks

The Prolific logo is a registered trademark of Prolific Technology Inc. All brand names and product names used in this document are trademarks or registered trademarks of their respective holders.

Copyrights