PL2571 (Chip Rev B) Hi-Speed USB to SATA Bridge Controller

Product Datasheet

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Revision History

Revision	Description	Date
1.3	Section 2.5: Modified System & GPIO Pins Table Description	June 15, 2009
1.2	Added SSOP28 Pin Diagram, Pin Description, and Outline Package Information.	March 27, 2009
1.1	Section 5.2: Update Operating Current Parameters	November 24, 2008
1.0	Formal Release	November 14, 2008

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1.0 Product Overview

1.1 Overview

The PL2571B is a low-power single-chip Hi-Speed USB-to-SATA 1.5Gbps/3Gbps compliant bridge controller that is designed to perform seamless protocol transfer between the USB and SATA interface. The high performance USB interface can connect to any high speed or full speed USB host or USB hub and can instantly be detected as a USB mass storage device. A high performance 8-bit microcontroller is embedded which can be used to support versatile system applications such as one button backup, power control, and others. The PL2571B is implemented according to the USB Bulk-Only Mass Storage Class specification v1.0. The USB mass storage driver is integrated in most OS so no driver installation is needed.

1.2 Features

- Serial ATA Revision 2.5 Specification Compliant
- Embedded SATA PHY and controller
- Universal Serial Bus Specification 2.0 Compliant
- USB Mass Storage Class Bulk-Only Transport Specification Compliant. No driver installation needed in Linux (kernel 2.4.18 or above), Mac OS 9.x or above, and Windows ME or above. Windows 98 requires additional driver installation provided by Prolific. USB mass storage driver for Mac OS 8.6 is provided by Apple in their website.
- Integrated full speed (12Mbps) and high speed (480Mbps) transceiver
- 2K bytes data buffer for downstream and upstream optimized data transfer performance
- High performance embedded 8-bit microcontroller
- Vendor/Product related configuration information can be customized thru external I^2C compatible Serial EEPROM or SPI serial flash.
- Serial EEPROM contents can be updated through USB interface
- Firmware can be upgraded easily through USB interface if larger external Serial EEPROM or Serial Flash is used.
- Multi-function General Purpose IO (GPIO) pins can be defined for USB speed LED, button inputs, and other special functions.
- GPIO pins can be customized by external configuration ROM or through USB interface
- Low power 1.2V core operating voltage
- On-chip 5V to 3.3V,1.2V regulator to supply the power for core circuit
- 5V tolerant inputs, 3.3V output drive
- Single inexpensive 30-MHz crystal for clock source
- Inexpensive LQFP48 (7x7mm) package and SSOP28 package

1.3 Block Diagram

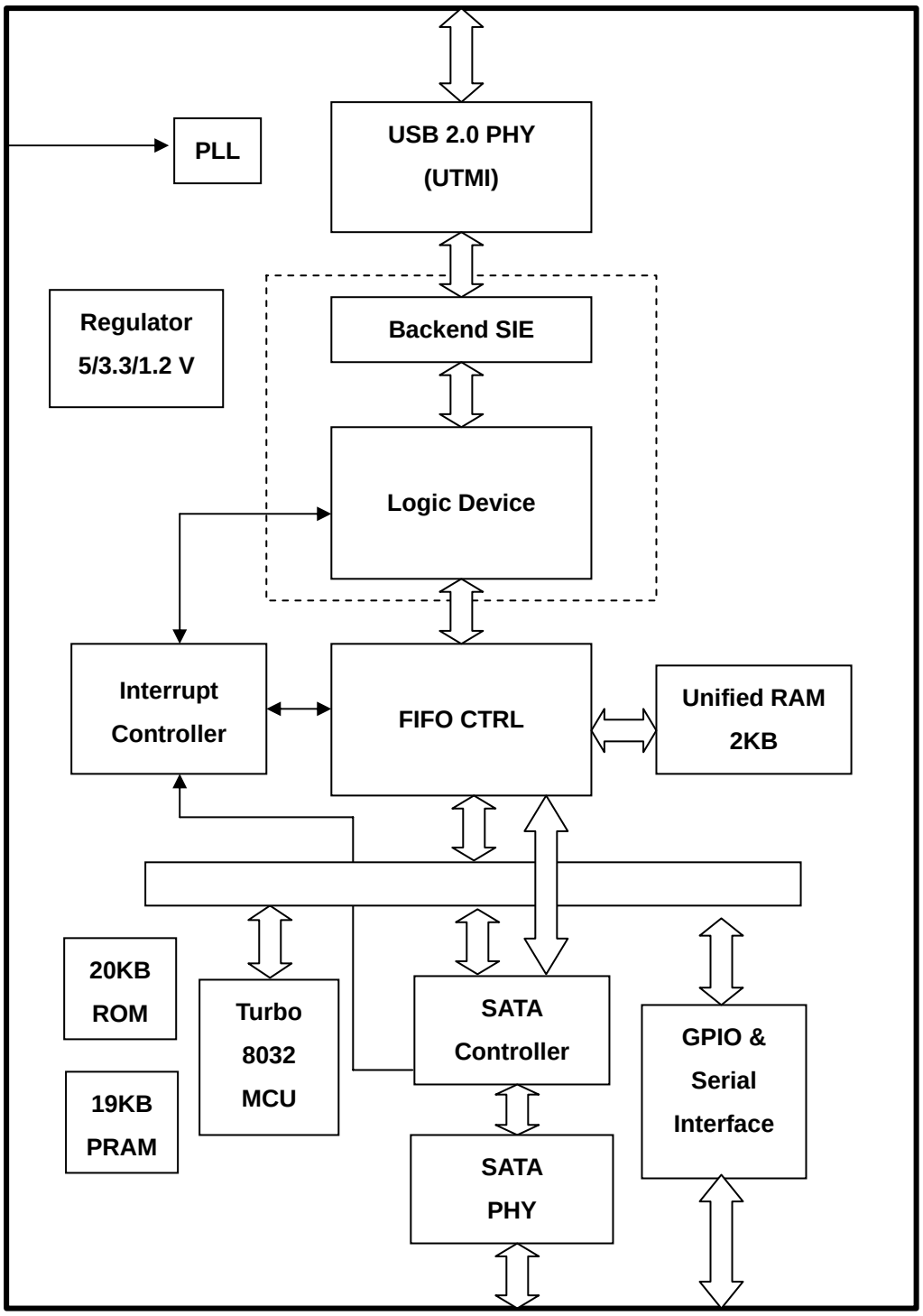


Figure 1-1 Block Diagram of PL2571 (Rev B)

2.0 PIN Assignment & Description

2.1 Pin Assignment for LQFP48 Package

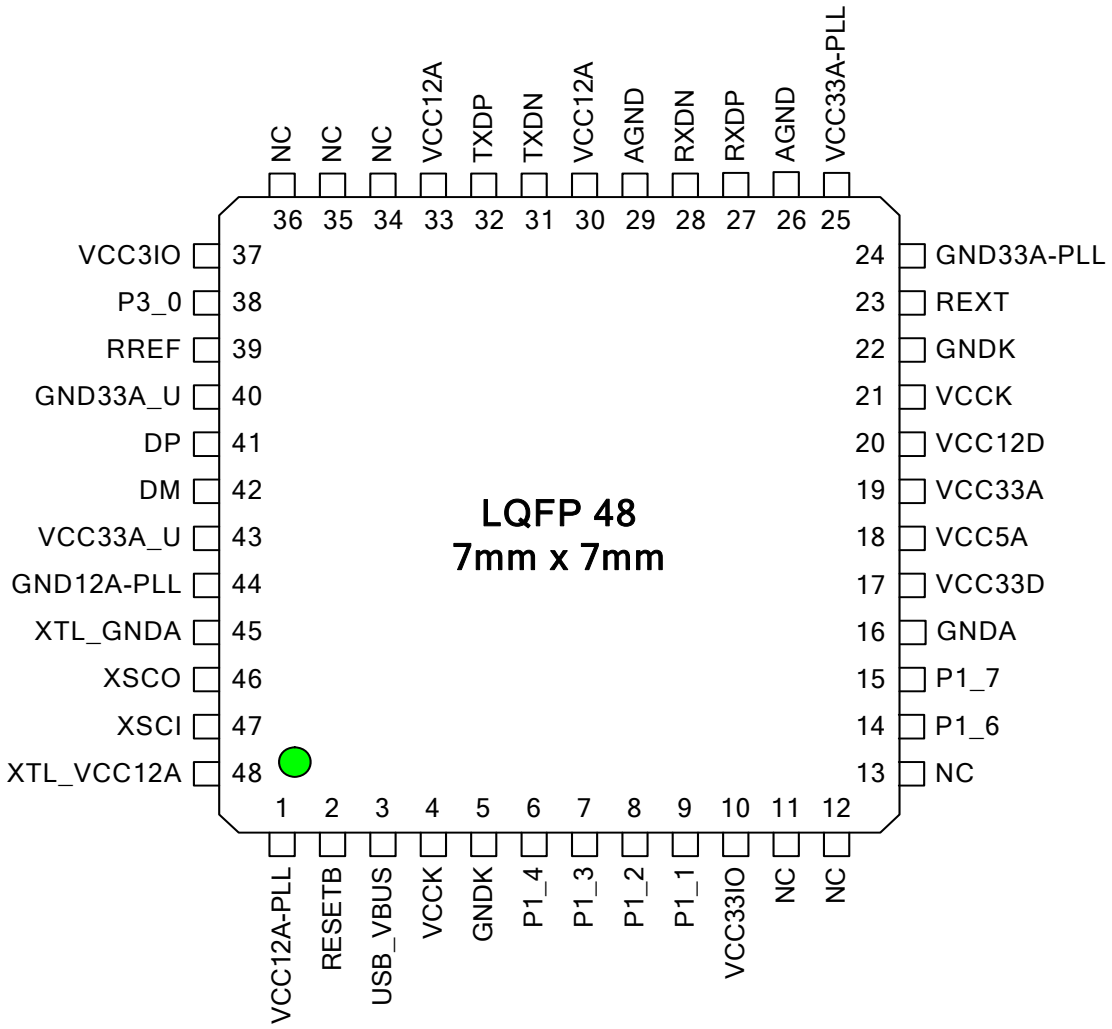


Figure 2-1 Pin Assignment Diagram of PL2571 (Rev B) LQFP48

2.2 Pin Assignment for SSOP28 Package

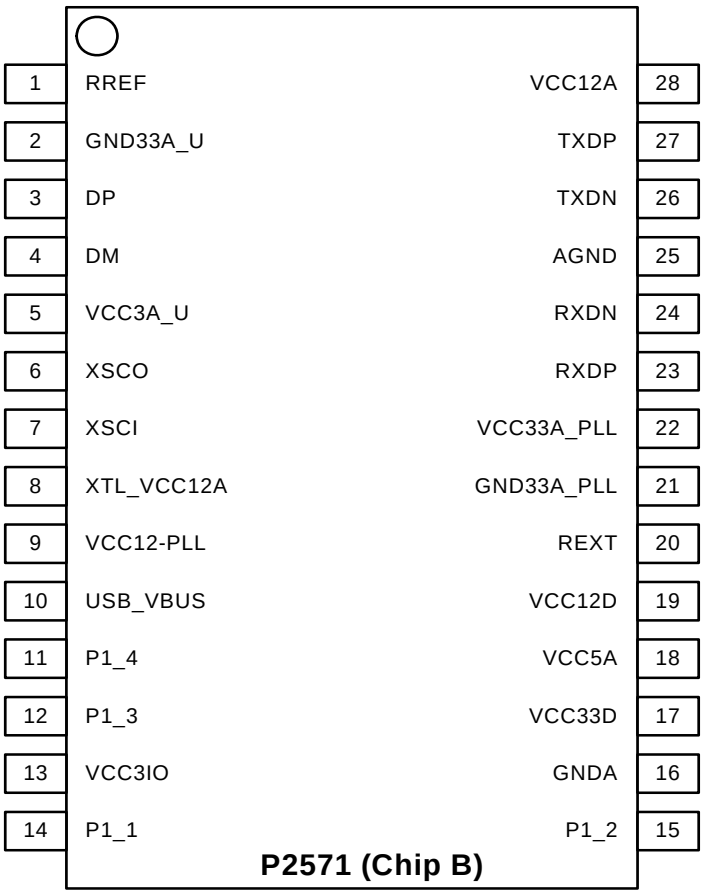


Figure 2-2 Pin Assignment Diagram of PL-2571 (Rev B) SSOP28

2.3 USB2.0 PHY Related Pins

Pin Type Abbreviation:

I: Input	O: Output	B: Bidirectional	A: Analog	P: Power/Ground

Table 2-1 USB2.0 PHY Related Pins

Symbol	Type	LQFP48 Pin No.	SSOP28 Pin No.	Description
RREF	A	39	1	External resistor for bias current generation
DP	B	41	3	High speed D+ signal
DM	B	42	4	High speed D- signal
VCC33A_U	P	43	5	Analog power 3.3V for on-chip USB PHY
GND33A_U	P	40	2	Analog ground for on-chip USB PHY

2.4 SATA PHY Related Pins

Table 2-2 SATA PHY Related Pins

Symbol	Type	LQFP48 Pin No.	SSOP28 Pin No.	Description
TXDP	O	32	27	Transmitter positive output
TXDN	O	31	26	Transmitter negative output
REXT	A	23	20	External resistor for bias current generation
RXDN	I	28	24	Receive negative input
RXDP	I	27	23	Receive positive input
VCC12A	P	33, 30	28	Analog power 1.2V for SATA PHY
AGND	P	26, 29	25	Analog ground for SATA PHY
VCC33A_PLL	P	25	22	Analog power 3.3V for SATA PHY
GND33A_PLL	P	24	21	Analog ground for SATA PHY

2.5 System & GPIO Pins

Table 2-3 System & GPIO Pins

Symbol	Type	LQFP48 Pin No.	SSOP28 Pin No.	Description
VCC5A	I	18	18	Regulator 5V voltage input
VCC33A	P	19	-	Regulator 3.3V power output
VCC33D	P	17	17	Regulator 3.3V power output
VCC12D	P	20	19	Regulator 1.2V power output
GNDA	P	16	16	Regulator analog ground
XTL_VCC12A	P	48	8	Crystal analog power supply
XTL_GNDA	P	45	-	Crystal analog ground
XSCI	I	47	7	Crystal oscillator 30MHz clock input

XSCO	B	46	6	Crystal oscillator 30MHz clock output
VCC12A-PLL	P	1	9	PLL analog power supply
GND12A-PLL	P	44	-	PLL analog ground
VCC33IO	P	10,37	13	PAD power
RESETB	I	2	-	External reset pin. Active low.
USB_VBUS	B	3	10	USB power signal from USB VBUS
P1_1	B	9	14	General Purpose I/O pin ▪ SPI CS: Used as SPI chip select pin.
P1_2	B	8	15	SDA or General Purpose I/O pin ▪ SPI Data or I2C Data: Used as SPI data pin or I2C data pin. ▪ Access LED: Timer mode (2Hz)
P1_3	B	7	12	General purpose I/O pin ▪ SPI CLK or I2C CLK: Used as SPI Clock Pin or I2C Clock Pin.
P1_4	B	6	11	General Purpose I/O pin ▪ Write Protect: When this function is enabled in PL2571 MFG Kit program (Advanced Settings), the chip ROM code will check this pin. If P1_4 is 0, HDD device is not allowed to be written. If P1_4 is 1, HDD device is allowed to be written. ▪ One Button Backup function (SSOP28 Only)
P1_6	B	14	-	General Purpose I/O pin (For LQFP48 Only) ▪ SATA Hot-Plug Enable: If device has no EEPROM, this pin decides whether to enable SATA hot-plug. – P1_6 = 0: Enable – P1_6 = 1: Disable ▪ Suspend Indicator: When this function is enabled in PL2571 MFG Kit program (Advanced Settings), the chip ROM code will control this pin at bus suspend, hot-plug, and bus reset conditions. NOTE: SATA hot-plug and Suspend Indicator are not supported in SSOP28 package.
P1_7	B	15	-	General Purpose I/O pin ▪ One Button Backup function (LQFP48 Only)
P3_0	B	38	-	Reserved
VCCK	P	4, 21	-	1.2V core Power pins
GNDK	P	5, 22	-	Digital ground pins
NC	O	11, 12, 13, 34, 35, 36		No Connection

3.0 USB Port Descriptor for PL2571B

PL2571B supports the following standard USB descriptors:

- Device descriptor
- Configuration descriptor that supports one interface
- String descriptors. Three string descriptors are implemented namely, language ID, Vendor String, and Product String.

3.1 Device Descriptor

Table 3-1 Device Descriptor

Offset	Field	Size	Value	Description
0	bLength	Byte	12h	Size of this descriptor in bytes
1	bDescriptorType	Byte	01h	DEVICE descriptor type
2	bcdUSB	Word	0200h	USB Specification version 2.0
4	bDeviceClass	Byte	00h	Interface Specific
5	bDeviceSubclass	Byte	00h	Interface Specific
6	bDeviceProtocol	Byte	00h	Interface Specific
7	wMaxPacketSize0	Byte	40h	Maximum packet size for endpoint 0 is 64
8	idVendor	Word	067Bh	Vendor ID (1)
10	idProduct	Word	2571h	Product ID for PL2571B (1)
12	bcdDevice	Word	0100h	Device Release 1.0 (1)
14	iManufacturer	Byte	01h	String index 1 describes manufacturer (2)
15	iProduct	Byte	02h	String index 2 describes product (3)
16	iSerialNumber	Byte	03h	String index 3 describes the serial number (4)
17	bNumConfigurations	Byte	01h	One possible configuration

Notes:
(1) – These default values shown here could be modified by external EEPROM;
(2) – The default string is in UNICODE format and could be replaced by the contents of external EEPROM;
(3) – The default string is in UNICODE format and could be replaced by the contents of external EEPROM.
(4) – The default serial number string is “0” in UNICODE format and could be replaced by the contents of external EEPROM.

3.2 Configuration Descriptor

Table 3-2 Configuration Descriptor

Offset	Field	Size	Value	Description
0	bLength	Byte	09h	Size of this descriptor in bytes
1	bDescriptorType	Byte	02h	CONFIGURATION descriptor type
2	bTotalLength	Word	0020h	32 bytes of all INTERFACE & ENDPOINT
4	bNumInterfaces	Byte	01h	The PL2571B has one interface
5	bConfigurationValue	Byte	01h	Value to write to the Device Configuration Register (DCR) to select this configuration.
6	iConfiguration	Byte	00h	No string description for this
7	bmAttributes	Byte	C0h	Configuration characteristics: (5) Self-Powered & No Remote Wakeup
8	MaxPower	Byte	FAh	Maximum power consumption is 500 mA (6)

Note:
(5) (6) – The default value could be replaced by the contents of external EEPROM.

3.3 Interface Descriptors

Table 3-3 Interface Descriptors

Offset	Field	Size	Value	Description
0	bLength	Byte	09h	Size of this descriptor in bytes
1	bDescriptorType	Byte	04h	INTERFACE descriptor type
2	bInterfaceNumber	Byte	00h	Interface 0
3	bAlternateSetting	Byte	00h	Alternate 0
4	bNumEndpoints	Byte	02h	Supports endpoint 0, 1, and 2
5	bInterfaceClass	Byte	08h	MASS STORAGE class (7)
6	iInterfaceSubClass	Byte	06h	SCSI transparent commend set
7	bInterfaceProtocol	Byte	50h	Bulk-Only Transport protocol
8	iInterface	Byte	00h	No String descriptor for this interface

Note:
(7) – This value could be 02h by enabling one bit the contents of external EEPROM.

3.4 Endpoint Descriptors

3.4.1 Hi-Speed mode

Table 3-4 Hi-Speed Bulk Out Endpoint Descriptor (Endpoint 1)

Offset	Field	Size	Value	Description
0	bLength	Byte	07h	Size of this descriptor in bytes
1	bDescriptorType	Byte	05h	ENDPOINT descriptor type
2	bEndpointAddress	Byte	01h	Out Endpoint 1
3	bmAttributes	Byte	02h	BULK Endpoint
4	wMaxPacketSize	Word	0200h	Maximum packet size is 512
6	bInterval	Byte	00h	N/A

Table 3-5 Hi-Speed Bulk In Endpoint Descriptor (Endpoint 2)

Offset	Field	Size	Value	Description
0	bLength	Byte	07h	Size of this descriptor in bytes
1	bDescriptorType	Byte	05h	ENDPOINT descriptor type
2	bEndpointAddress	Byte	82h	In Endpoint 2
3	bmAttributes	Byte	02h	BULK Endpoint
4	wMaxPacketSize	Word	0200h	Maximum packet size is 512
6	bInterval	Byte	00h	N/A

3.4.2 Full-Speed mode

Table 3-6 Full-Speed Bulk Out Endpoint Descriptor (Endpoint 1)

Offset	Field	Size	Value	Description
0	bLength	Byte	07h	Size of this descriptor in bytes
1	bDescriptorType	Byte	05h	ENDPOINT descriptor type
2	bEndpointAddress	Byte	01h	Out Endpoint 1
3	bmAttributes	Byte	02h	BULK Endpoint
4	wMaxPacketSize	Word	0040h	Maximum packet size is 64
6	bInterval	Byte	00h	N/A

Table 3-7 Full-Speed Bulk In Endpoint Descriptor (Endpoint 2)

Offset	Field	Size	Value	Description
0	bLength	Byte	07h	Size of this descriptor in bytes
1	bDescriptorType	Byte	05h	ENDPOINT descriptor type
2	bEndpointAddress	Byte	82h	In Endpoint 2
3	bmAttributes	Byte	02h	BULK Endpoint
4	wMaxPacketSize	Word	0040h	Maximum packet size is 64
6	bInterval	Byte	00h	N/A

3.5 Device_Qualifier Descriptors

Table 3-8 Device Qualifier Descriptors

Offset	Field	Size	Value	Description
0	bLength	Byte	0Ah	Size of this descriptor in bytes
1	bDescriptorType	Byte	06h	DEVICE Qualifier descriptor type
2	bcdUSB	Word	0200h	USB Specification version 2.0
4	bDeviceClass	Byte	00h	Interface Specific
5	bDeviceSubclass	Byte	00h	Interface Specific
6	bDeviceProtocol	Byte	00h	Interface Specific
7	wMaxPacketSize0	Byte	40h	Maximum packet size for endpoint 0 is 64
8	bNumConfigurations	Byte	01h	Number of other-speed configurations
9	bReserved	Byte	00h	Reserved for future use, must be zero

3.6 Other_Speed_Configuration Descriptors

Table 3-9 Other Speed Configuration Descriptors

Offset	Field	Size	Value	Description
0	bLength	Byte	09h	Size of this descriptor in bytes
1	bDescriptorType	Byte	07h	CONFIGURATION descriptor type
2	bTotalLength	Word	0020h	32 bytes of all INTERFACE & ENDPOINT
4	bNumInterfaces	Byte	01h	Number of interface supported (one interface)
5	bConfigurationValue	Byte	01h	Value to write to the Device Configuration Register (DCR) to select this configuration.
6	iConfiguration	Byte	00h	No string description for this
7	bmAttributes	Byte	C0h	Configuration characteristics: Self-Powered & No Remote Wakeup
8	MaxPower	Byte	FAh	Maximum power consumption is 500 mA

4.0 External Configuration ROM

4.1 External Configuration ROM

The PL-2571B uses external serial memory (EEPROM or Flash) to store the Vendor ID, Product ID, Device Release Number in device descriptor, Attributes and Max Power setting in configuration descriptor, Strings of String Descriptor and some chip operation mode configuration. A new version firmware can be stored in this memory when this memory size is large enough. If the external configuration ROM is not present, PL-2571B will use settings in the internal ROM. Two types of serial interface are supported, the one is SPI (Serial Peripheral Interface) and the other is I2C compatible interface. Both interface support master mode only.

The PL2571B allows following possible configurations:

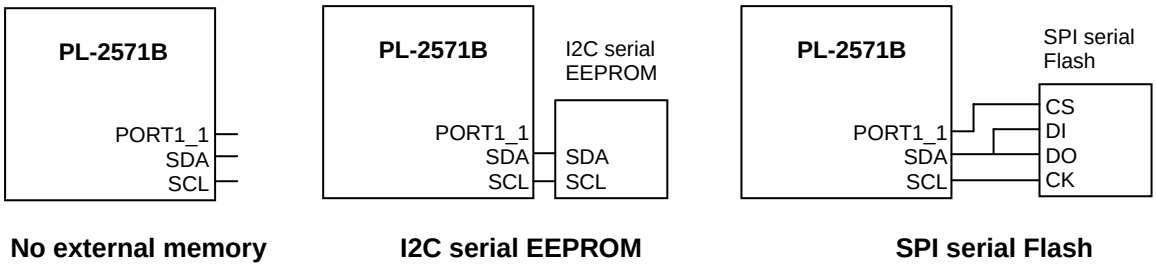


Figure 4-1 External Serial Memory Implementation

- **No external memory:** The chip will use the default configuration in the internal ROM and run the firmware from the internal ROM. The chip will send default Vendor ID, Product ID, chip operation settings, and other default configuration. Product serial number will not be sent.

- **I2C serial EEPROM:** This case uses I2C serial EEPROM to store chip configuration data or configuration data with new firmware. If the I2C serial EEPROM size (like 24C256) is large enough, a new version firmware can be stored therefore new firmware upgrade is possible. If new version firmware is stored in the EEPROM, new firmware will be loaded while system startup.

- **SPI serial Flash:** This is the recommended case. It behaves the same as the I2C serial memory with this chip. But the transfer speed of SPI interface is faster than I2C interface. The device like 25C256 is suitable. The SPI interface is a four-pin interface but this chip uses only three pins to communicate with. Therefore, the DI and DO are shorted or short by a serial 240-ohm resistor is better.

4.2 Data Structure of External Serial Memory Content

The Configuration ROM is organized as follows:

Table 4-1 EEPROM Address and Content

Address	Content	Note
1:0	Check Word – 0x067B (Predefined constant)	
3:2	Vendor ID (idVendor field of Device Descriptor)	
5:4	Product ID (idProduct field of Device Descriptor)	
7:6	Device Release Number (bdcDevice field of Device Descriptor)	
8	Attributes (bmAttributes field of Configuration Descriptor)	
9	Max Power (MaxPower field of Configuration Descriptor)	
10	Chip operation settings	
15:14	Reserved	
249:16	USB String Descriptor Table	
253:250	GPIO Settings	
255:254	Miscellaneous	

From byte 16 to byte 230 are used for USB string descriptors. The String Descriptor table is a linked data structure that holds all string descriptors recognized by this chip in the order of its index. The first entry, String 0, represents the Language ID, as defined by the USB specification. The second entry, String 1, is the Manufacturer Descriptor, as defined by the Device Descriptor. The third and forth entries, String 2 and 3, are the Product Descriptor and Serial Number, respectively, also defined by the Device Descriptor. The user has the option to define String 4, 5, and 6 for their own private use. Each of these String Descriptor Entries is of the following data structure:

Table 4-2 String Descriptor Data Structure

Offset	Field	Size	Value	Note
0	bLength	1	Length of the string plus 2, i.e. (N + 2).	
1	bDescriptorType	1	03h – STRING Descriptor type.	
2	bString	N	UNICODE encoded string.	

The last entry of this table must have a bLength of 0 to indicate the end of this table. A zero-length data will be returned if the host tries to access to the string descriptor beyond the last one.

The following table shows one example of valid EEPROM contents:

Table 4-3 Example of Valid EEPROM Contents

Offset	Content	Note
0:1	Check Word – 0x067B	Constant
2:3	Vendor ID – 0x067B	
4:5	Product ID – 0x2571	
6:7	Device Release Number – 0x0100	
8		
9		
15:10		
16	0x04	String Index 0 (4 Bytes)
17	0x03	
19:18	0x0409	Language ID for English (United States).
20	0x32	String Index 1 (50 Bytes)
21	0x03	
69:22	‘X’, 0x00, ‘X’, 0x00, ‘X’, 0x00, ‘ ‘, 0x00, ‘T’, 0x00, ‘e’, 0x00, ‘c’, 0x00, ‘h’, 0x00, ‘n’, 0x00, ‘o’, 0x00, ‘l’, 0x00, ‘o’, 0x00, ‘g’, 0x00, ‘y’, 0x00, ‘ ‘, 0x00, ‘I’, 0x00, ‘n’, 0x00, ‘c’, 0x00, ‘.’ , 0x00	“XXX Technology Inc.” – manufacturer description. 0x00 is padded for UNICODE.
70	0x34	String Index 2 (52 Bytes)
71	0x03	
121:72	‘M’, 0x00, ‘a’, 0x00, ‘s’, 0x00, ‘s’, 0x00, ‘ ‘, 0x00, ‘S’, 0x00, ‘t’, 0x00, ‘o’, 0x00, ‘r’, 0x00, ‘a‘, 0x00, ‘g’, 0x00, ‘e’, 0x00, ‘ ’, 0x00, ‘D’, 0x00, ‘e’, 0x00, ‘v’, 0x00, ‘i’, 0x00, ‘c’, 0x00, ‘e’, 0x00	“Mass Storage Device” – device description. 0x00 is padded for UNICODE.
122	0x0A	String Index 3 (10 bytes)
123	0x03	
131:124	‘0’, 0x00, ‘1’, 0x00, ‘2’, 0x00, ‘3’, 0x00	“3210” – serial number,
132	0x00	End of String Descriptor Table.

The user could also define other strings, 4 to 6, to hold useful information for the drivers and/or applications, such as software authorization codes, symbolic names, just to name a few. However, the total length of this table must not exceed 256 bytes (include reserved space for chip controlling), the supported maximum size of external configuration ROM.

5.0 DC Characteristics

5.1 Absolute Maximum Ratings

Table 5-1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
VCC3	Power Supply of 3.3V	-0.3 to 4.0	V
V_{IN3}	Input Voltage of 3.3V I/O with 5V Tolerance	-0.3 to 5.8	V
V_{CCK}	Core Power Supply	-0.3 to 1.44	V
I_{IN}	DC input current(5V)	20	mA
I_{OUT}	Output short circuit current(5V)	20	mA
T_{STG}	Storage Temperature	-40 to 150	^{o}C

Note: Permanent device damage may occur if the absolute maximum ratings are exceeded. These are stress rating only, and functional operation should be restricted to within the conditions. Exposure to absolute maximum rating conditions for extended periods may affect the device's reliability.

5.2 Operating Current Parameters

Table 5-2 Operating Current Parameters

SYMBOL	PARAMETER	Conditions	TYP	UNITS
I_{DD}	USB High-Speed Supply Current	Write large files to HDD	70	mA
		VCD Playback using DVD-ROM	68	mA
	USB Full-Speed Supply Current	Write large files to HDD	62	mA
		VCD Playback using DVD-ROM	65	mA
I_{SUS}	Suspend Current		TBD*	mA

TBD: To Be Defined.

5.3 Recommended Operating Conditions

Table 5-3 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CCK}	Core Power Supply (by built-in regulator)	1.08	1.2	1.32	V
VCC3	Power Supply of 3.3V	2.97	3.3	3.63	V
V_{IN3}	Input Voltage of 3.3V I/O with 5V Tolerance	0	3.3	5.25	V
Tj	Junction Operating Temperature	-40	25	125	^{o}C

5.4 DC Characteristics of 3.3V Programmable I/O Cells

Table 5-4 DC Characteristics of 3.3V Programmable I/O Cells

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
Vol	Output low voltage	Iol = 8 mA			0.4	V
Voh	Output high voltage	Ioh = -8 mA	2.4			V
I_{IN}	Input leakage current	No pull-up or pull-down		±1		uA
Ioz	Tri-state output leakage current			±1		uA

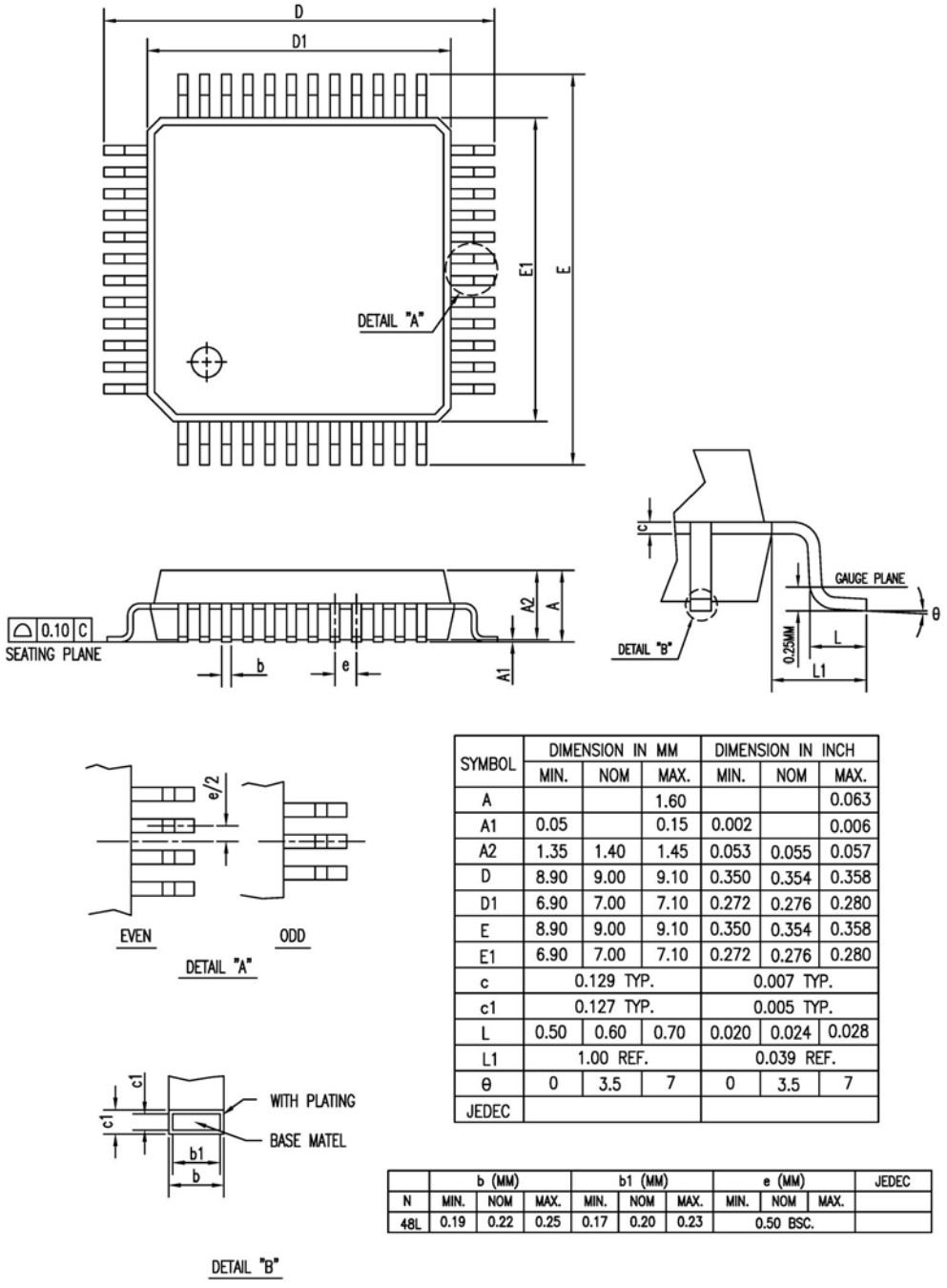
6.0 Ordering Information

Table 6-1 Ordering Information

Part Number	Package Type
PL2571B LQFP48	48-pin LQFP (7x7mm)
PL2571B LQFP48 LF	48-pin LQFP (7x7mm) Lead (Pb) Free
PL2571B SSOP28 LF	28-pin SSOP Lead (Pb) Free

7.0 Outline Diagram

7.1 LQFP48 Package (7x7) Outline Diagram



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	8.90	9.00	9.10	0.350	0.354	0.358
D1	6.90	7.00	7.10	0.272	0.276	0.280
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	6.90	7.00	7.10	0.272	0.276	0.280
c	0.129 TYP.			0.007 TYP.		
c1	0.127 TYP.			0.005 TYP.		
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	1.00 REF.			0.039 REF.		
θ	0	3.5	7	0	3.5	7
JEDEC						

	b (MM)			b1 (MM)			e (MM)			JEDEC
N	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.	
48L	0.19	0.22	0.25	0.17	0.20	0.23		0.50 BSC.		

Figure 7-1 Outline Diagram of PL2571 (Rev B) LQFP48 (7x7mm)

7.2 SSOP28 Package

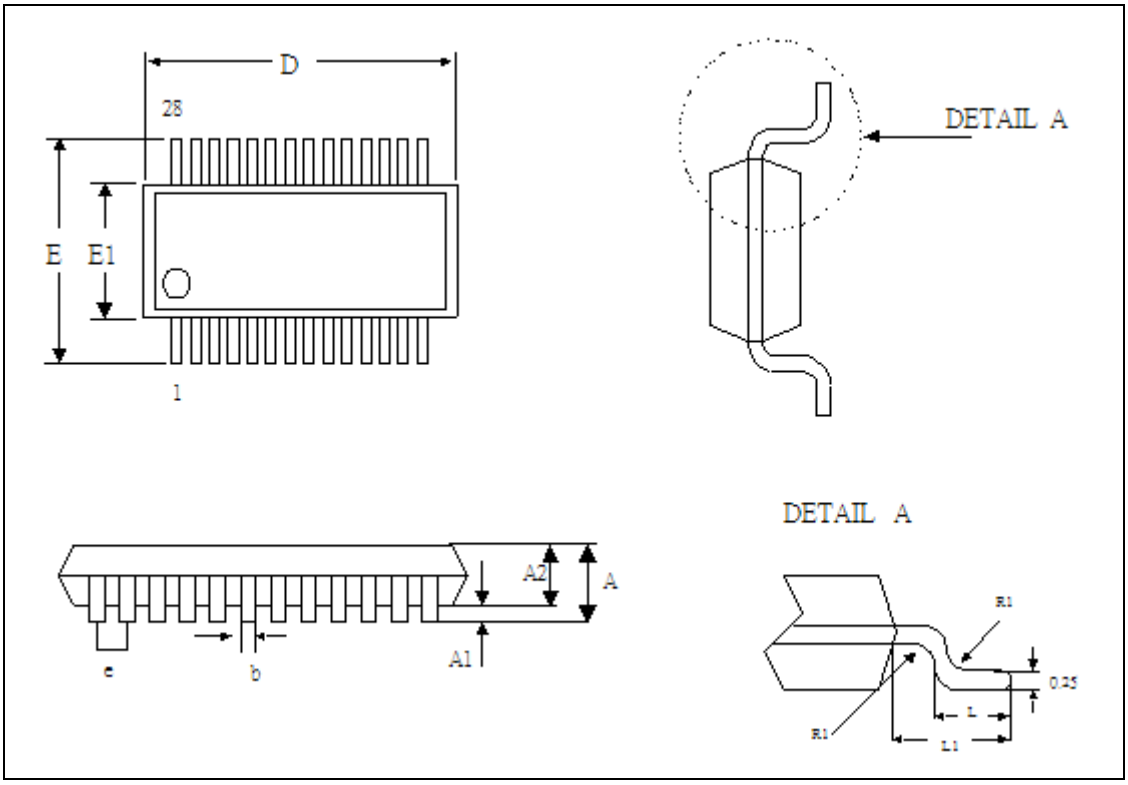


Figure 7-2 Outline Diagram of PL-2571 (Rev B) SSOP28

Table 7-1 SSOP28 Package Dimension

Symbol	Millimeter			Inch		
	Min	Nom	Max	Min	Nom	Max
b	0.22		0.38	0.009		0.015
E	7.40	7.80	8.20	0.291	0.307	0.323
E1	5.00	5.30	5.60	0.197	0.209	0.220
L	0.55	0.75	0.95	0.021	0.030	0.037
R1	0.09			0.004		
D	9.9	10.2	10.5	0.390	0.402	0.413
A			2.0			0.079
e		0.65			0.0256	
L1		1.25			0.050	
A1	0.05			0.020		
A2	1.65	1.75	1.85	0.065	0.069	0.073