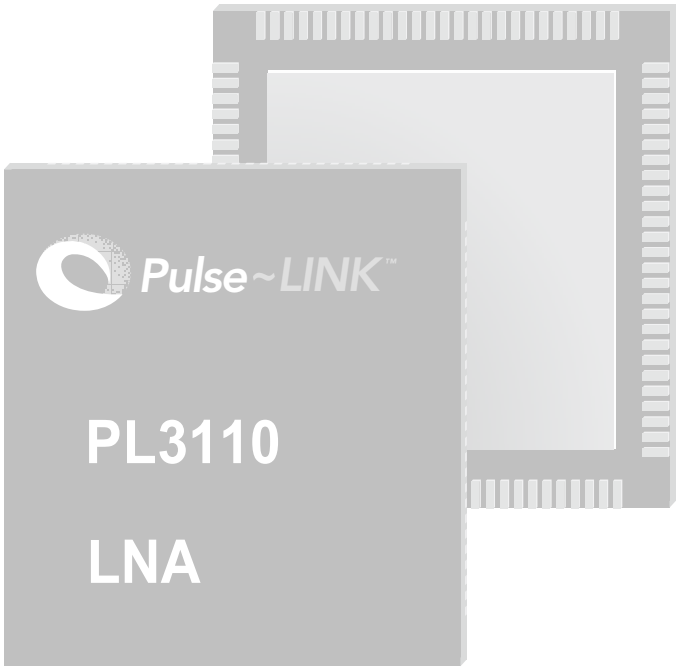
Pulse~LINK®

PL3110

CWave® Ultra Wideband LNA



Datasheet

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PL3110 CWave® Ultra Wideband LNA

PL3110 CWave® Ultra-Wideband Low Noise Amplifier

The PL3110 CWave Ultra-Wideband (UWB) Low-Noise Amplifier (LNA) is an integral part of Pulse~LINK's CWave UWB chipset. The PL3110 LNA is specifically designed for high-speed wireless connectivity solutions. As shown in Figure 1, there are three major blocks encompassing the CWave UWB chipset solution. As depicted, the PL3110 LNA directly interfaces with the PL3120 UWB Transceiver RFIC supporting data rates up to 675 Mbps. The PL3110 UWB LNA operates over a wide frequency range of 3.1GHz to 5.8 GHz.

The PL3110 CWave LNA provides a single receive channel containing a high-performance LNA with large dynamic range and high gain. Control of the LNA operation and gain settings can be performed via a hard-wired interface. The PL3110 LNA is a critical component, making it feasible for Pulse~LINK's CWave system to transmit high data rates wirelessly.

PL3110 UWB LNA Overview

The PL3110 UWB LNA chip consists of a two LNA block low-noise wideband amplifier designed to connect to an UWB antenna system or a coax cable interface. The LNA amplifies an RF receive channel, operating over a wide frequency range from 3.3 - 4.8 GHz optimized at the center frequency of 4 GHz. The PL3110 LNA provides a single-channel receive signal source to the PL3120 Transceiver RFIC.

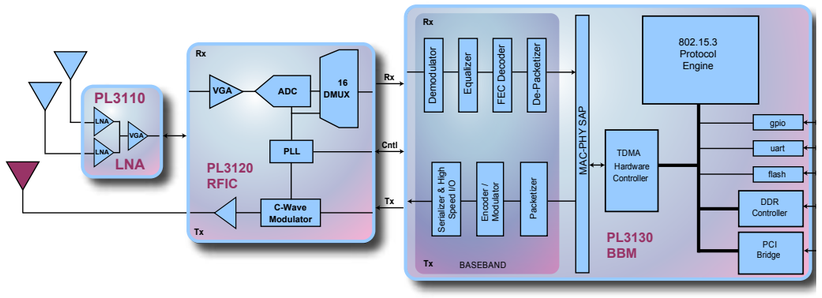

Figure 1: PL3110 Functional Chipset Interfaces

The LNA includes:

- A input variable-gain wideband Low-noise Amplifier (LNA)
- An RF differential output buffer amplifier
- Selection of High-gain or Low-gain mode
- A control interface (to set the modes of operation such as Select Channel A or B gain of LNA, RX enable/disable, and LNA IC On/Off).

Functional Descriptions

As shown in the block diagram of Figure 3, the PL3110 UWB LNA is a basic two-stage receiver Front-End designed specifically for UWB applications. It functions as the initial low-noise gain stage for the PL3120 Transceiver RFIC receiver processing block.

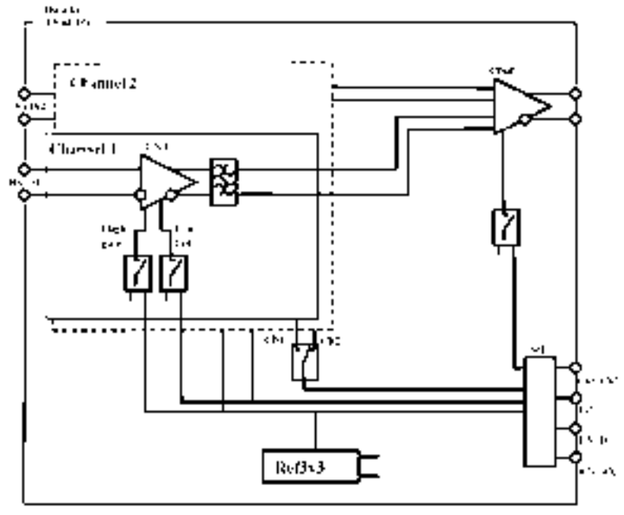

Figure 3: PL3110 LNA Functional Block Diagram

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Ultra-Wideband LNA

The LNA sets the device Noise Figure (NF) at less than 2 dB and the total maximum system gain provided by the LNA in high-gain mode is 24 dB. When the LNA is set in low-gain mode, the total device system gain is typically set at 4 dB.

LNA Inputs

The LNA has differential 100-Ohm inputs. Signals captured by the receive antenna system or coax cable interface are boosted by the LNA prior to filtering through an analog filter, and then passed to the differential output buffer amplifier that provides a second stage of gain.

LNA Gain Control

The LNA gain mode can be configured for either high-gain or low-gain mode and is set by the *(BP)* control lead.

Differential Output Buffer

The LNA output signal stream is buffered by a differential output buffer amplifier stage prior to being sent to the PL3120 Transceiver RFIC. The buffer's differential outputs are also matched to 50 Ohms to drive a coplanar transmission line connected to the PL3120 Transceiver RFIC receiver input.

Integrated Voltage References

On-chip Band-Gap references provide biasing to the internal LNA circuits.

Control Interfaces

Control of the PL3110 UWB LNA is provided via hardwired control leads. These dedicated leads control the high-gain/low-gain mode of the LNA, enable the receive channel and provide for enable/disable control of the PL3110 UWB LNA chip.

Mode Control Hardware Interface

The PL3110 LNA IC is set in the ON (default) or OFF mode by CMOS control lead 20 *(EN_IC)*. Control lead 23 *(BP)* sets the LNA either in a high-gain state (default) or in low-gain mode. Control lead 22 *(EN_RX)* enables/disables the receiver on/offl.

Table 1: LNA Mode Control Hardware Interface

Control Signal	Control Function
EN_IC	LNA IC ON/OFF Mode
EN_RX	Enable/Disable Receive Channel
BP	LNA High-Gain/Low-Gain Mode
Channels 1/2	

Device Connections

This section describes the lead assignments and connection signals for the high-performance PL3110 UWB LNA device.

Pin Configuration

Lead assignments for the PL3110 LNA chip are shown in Figure 4.

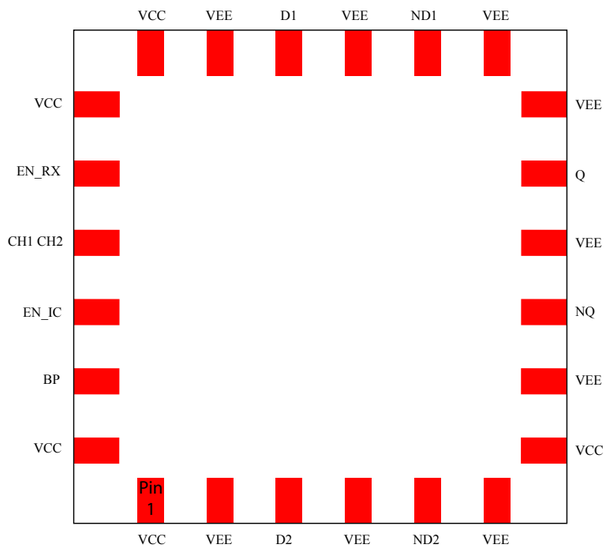

Figure 4: PL3110 LNA Lead Assignments

Pin Description Summary

The following table summarizes the signals names and descriptions for the PL3110 UWB LNA package connections.

Table 2: Signal Names and Lead Assignments

Lead Number	Signal Name	Pad description	Notes
1	VCC	Positive Power supply	Max Ivcc=100mA. Connect a blocking capacitor to GND.
2	VEE	GND termination	Connect to GND
3	D2	Input positive data Channel2	
4	VEE	GND termination	Connect to GND
5	ND2	Input negative data Channel2	
6	VEE	GND termination	Connect to GND

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Lead Number	Signal Name	Pad description	Notes
7	VCC	Positive Power supply. Connect to +3.3V.	Max Ivcc=100mA. Connect a bypass capacitor to GND.
8	VEE	GND termination	Connect to GND
9	NQ	Negative Rx data from output buffer	
10	VEE	GND termination	Connect to GND
11	Q	Positive Rx data from output buffer	
12	VEE	GND termination	Connect to GND
13	VEE	GND termination	Connect to GND
14	ND1	Negative Rx Input data	
15	VEE	GND termination	Connect to GND
16	D1	Positive Rx Input data	
17	VEE	GND termination	Connect to GND
18	VCC	Positive Power supply. Connect to +3.3V.	Max Ivcc=100mA. Connect a bypass capacitor to GND.
19	VCC	Positive Power Supply. Connect to +3.3V.	Max Ivcc=100mA. Connect a bypass capacitor to GND.
20	EN_RX	Enable RX	Enable by default (connected to VCC) For RX disable connect to VEE through 10k resistor.
21	CH1_CH2	Channel 1 or Channel 2 choosing	Channel1 by default (connected to vcc). For choosing of Channel2 connect to vee through 10k resistor
22	EN_IC	Enable IC	LNA ON/OFF mode. ON mode by default (connect to VCC). For OFF mode connect to VEE through 10k resistor
23	BP	High-gain/Low-gain mode select	High gain mode of LNA by default (connect to VCC). For Low-gain mode connect to VEE through 10k resistor.
24	NC	No connection	

Electrical Specifications

Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings

Important: Exceeding these limits may result in malfunction and/or device damage.

Description	Value
Vcc (vcc_a, vcc_d) to GND	4V
RF in (d1, nd1) at 50 Ω source	-2dBm
RF out (q, nq) on 50 Ω load	2 dBm
Managing signals (BP, EN_RX, EN_IC)	3.3V
Operating temperature range	-25˚C to 90˚C
Maximum Junction temperature	125˚C
Max.Power dissipation	330 mW
Storage temperature	-65˚C to 150˚C
Lead Temperature (soldering, 5s)	+260˚C

Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Description	Value
Relative Humidity	95%
Ambient Operating Temperature	0 C to +70 C

DC Characteristics

Table 5: DC Characteristics

Parameter	Condition	Min	Typ	Max	Units
Supply voltage		3.1	3.3	3.5	V
Operating current				72	mA

AC Characteristics

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Table 6: UWB LNA Characteristics

Parameter	Condition	Min	Typ	Max	Units
Operating frequency		3		6	GHz
Gain			25		dB

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Parameter	Condition	Min	Typ	Max	Units
Gain flatness	High gain			3	dB
Gain variation vs temperature (at 4GHz)	High gain		2		dB
Input referred 1dB compression ($P1dB_h$)	High gain	-18			dBm
Input referred 1dB compression ($P1dB_l$)	Low gain	-6			dBm
Noise figure (NF)			<2		dB
Input return loss (S11)			-12		dB
Output return loss (S22)			-12		dB
Power supply rejection ratio (PSRR)		60			dB
Common mode rejection ratio (CMRR)		60			dB
Reverse isolation (2GHz-6GHz)		-43		-62	dB

Typical Operating Characteristics

Typical plots of Noise Figure, Input/Output matching (S11, S22) and Input 1dB compression point for Nominal Corners of the process and temperatures are presented below in Figure 5 and Figure 6.

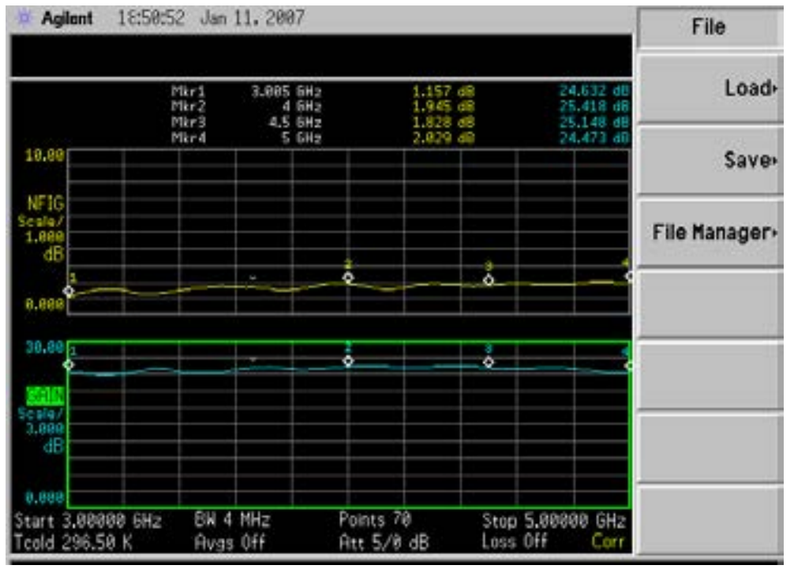

Figure 5: Noise & Gain

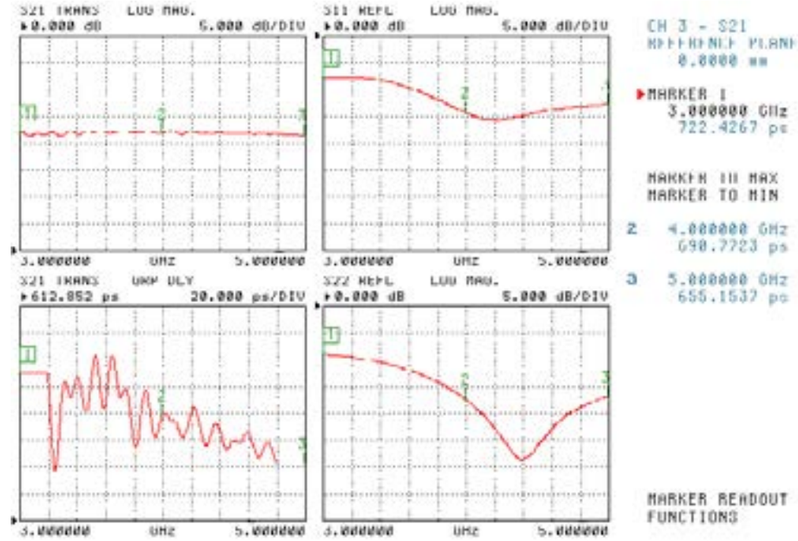

Figure 6: S-Parameter S21, S22 and S11 plots

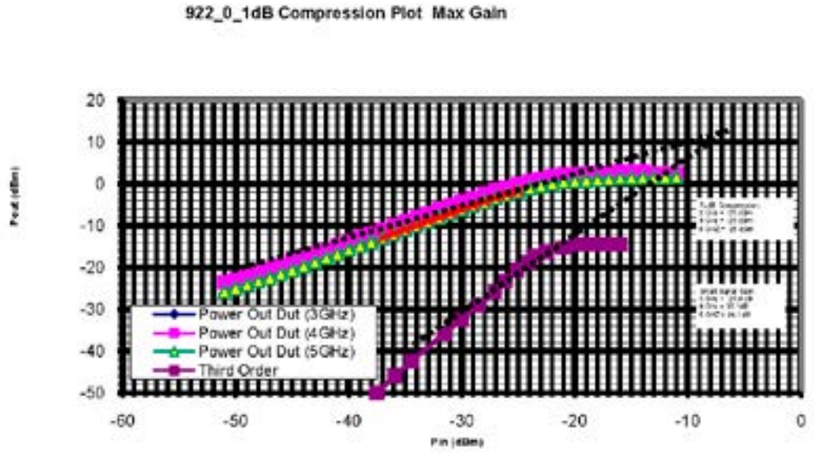

Figure 7: Max Gain Linearity

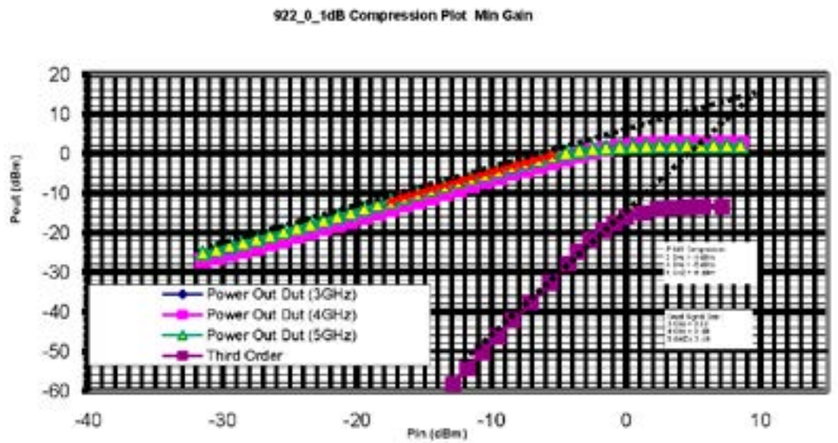

Figure 8: Low Gain Linearity

Mechanical Specifications

The PL3110 LNA 24-pin QFN package specifications are provided in Table 8.

Table 8: PL3110 LNA QFN Package Mechanical Specifications

Area	Dimensions
Compliance	Per JEDEC MO-205
Size	4x4 mm
Connection Leads	24 leads
Lead Pitch	0.50 mm
Nominal Thickness	0.85 mm

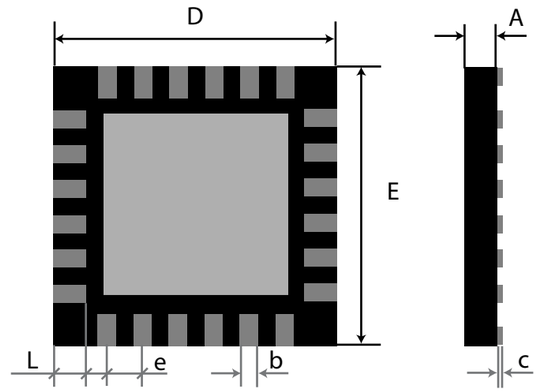

Figure 9: 24-pin QFN Package Dimensions (viewed from bottom)

Table 9: Overall Dimensions

Body Size,mm	Lead Count	Lead Pitch ,mm	Package Thk. mm	Footprint mm	Lead Width mm	L/F Thk. mm
D/E	N	e	A	L	b	c
4/4	24	0.5	0.85	0.4	0.23	0.20

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Acronyms & Abbreviations

ASIC	Application Specific Integrated Circuit
BB	Baseband
DEV	802.15.3 Device
EVK	Evaluation Kit
LNA	Low Noise Amplifier
lsb	Least Significant Bit
LSB	Least Significant Byte
MAC	Media Access Control
msb	Most Significant Bit
MSB	Most Significant Byte
OB	Output Buffer
PHY	Physical Layer
PLL	Phase Lock Loop
PNC	802.15.3 Piconet Coordinator
TDMA	Time Division Multiple Access
UWB	Ultra-Wideband
VGA	Variable Gain Amplifier

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Publication Number

111-00001-01

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