Pulse~LINK®

PL3111

CWave® Ultra Wideband Coax AFE

Datasheet

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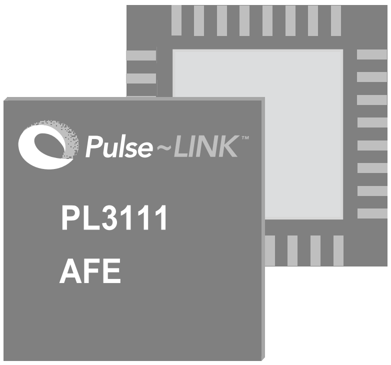

PL3111 CWave® Ultra Wideband Coax AFE

PL3111 CWave® Ultra-Wideband Low Noise Analog Front End Coax Cable Amplifier

The PL3111 CWave Ultra-Wideband (UWB) Analog Front End (AFE) is an integral part of Pulse~LINK's CWave UWB chipset solution for high-speed coax cable connectivity. The PL3111 AFE is specifically designed for high-speed Ethernet-over-coax network solutions, but can also be used on other wired media. As shown in Figure 1, there are three major blocks encompassing the CWave™ UWB chipset solution. As depicted, the PL3111 AFE directly interfaces with the PL3120 UWB Transceiver RFIC supporting data rates up to 675 Mbps. The PL3111 UWB AFE operates over a wide frequency range of 3.1GHz to 5.8 GHz.

The PL3111 UWB AFE provides a single receive channel containing a high-performance LNA with large dynamic range and high gain. LNA operation and gain settings can be controlled through a dedicated control interface, linking the PL3111, PL3120, and the PL3130. The PL3111 AFE is a critical component, making it feasible for Pulse~LINK's CWave system to transmit high data rates over coaxial cable.

PL3111 UWB Coax Cable AFE Overview

The PL3111 UWB AFE chip consists of a two LNA block low-noise wideband amplifier designed to connect to a coax cable interface. The LNA amplifies an RF receive channel, operating over a wide frequency range from 3.3 - 4.8 GHz optimized at the center frequency of 4 GHz. The PL3111 AFE provides a single-channel receive signal source to the PL3120 Transceiver RFIC.

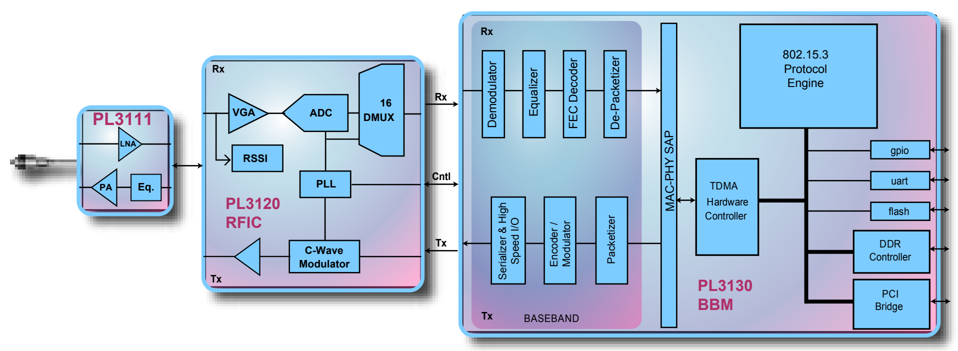

Figure 1: PL3111 Functional Chipset Interfaces

The LNA includes:

- A input variable-gain wideband Low-noise Amplifier (LNA)
- An RF differential output buffer amplifier
- Selection of High-gain or Low-gain mode
- A control interface (to set the modes of operation such as Select Channel A or B gain of LNA, RX enable/disable, and LNA IC On/Off).

Functional Descriptions

As shown in the block diagram of Figure 3, the PL3111 UWB LNA is a basic two-stage receiver Front-End designed specifically for UWB applications. It functions as the initial low-noise gain stage for the PL3120 Transceiver RFIC receiver processing block.

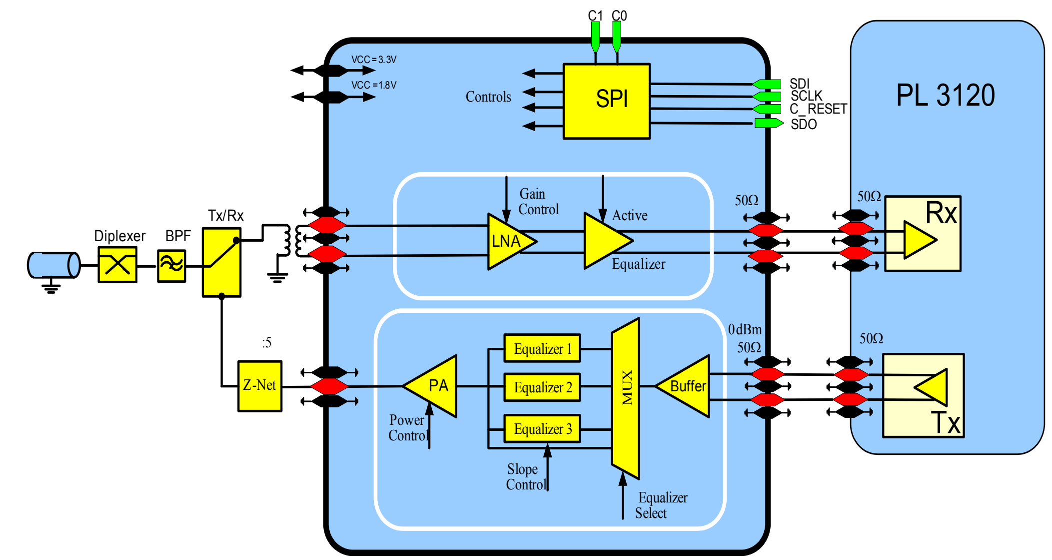

Figure 3: PL3111 LNA Functional Block Diagram

Ultra-Wideband LNA

The LNA sets the device Noise Figure (NF) at less than 2 dB and the total maximum system gain provided by the LNA in high-gain mode is 24 dB. When the LNA is set in low-gain mode, the total device system gain is typically set at 4 dB.

LNA Inputs

The LNA has differential 100-Ohm inputs. Signals captured by the receive antenna system or coax cable interface are boosted by the LNA prior to filtering through an analog filter, and then passed to the differential output buffer amplifier that provides a second stage of gain.

LNA Gain Control

The LNA gain mode can be configured for either high-gain or low-gain mode and is set by the *(BP)* control lead.

Differential Output Buffer

The LNA output signal stream is buffered by a differential output buffer amplifier stage prior to being sent to the PL3120 Transceiver RFIC. The buffer's differential outputs are also matched to 50 Ohms to drive a coplanar transmission line connected to the PL3120 Transceiver RFIC receiver input.

Integrated Voltage References

On-chip Band-Gap references provide biasing to the internal LNA circuits.

Control Interfaces

Control of the PL3111 UWB LNA is provided via hardwired control leads. These dedicated leads control the high-gain/low-gain mode of the LNA, enable the receive channel and provide for enable/disable control of the PL3111 UWB LNA chip.

Mode Control Hardware Interface

The PL3111 LNA IC is set in the ON (default) or OFF mode by CMOS control lead 20 *(EN_IC)*. Control lead 23 *(BP)* sets the LNA either in a high-gain state (default) or in low-gain mode. Control lead 22 *(EN_RX)* enables/disables the receiver on/offl.

Table 1: LNA Mode Control Hardware Interface

Control Signal	Control Function
EN_IC	LNA IC ON/OFF Mode
EN_RX	Enable/Disable Receive Channel
BP	LNA High-Gain/Low-Gain Mode

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Channels 1/2	

Device Connections

This section describes the lead assignments and connection signals for the high-performance PL3111 UWB LNA device.

Pin Configuration

Lead assignments for the PL3111 LNA chip are shown in Figure 4.

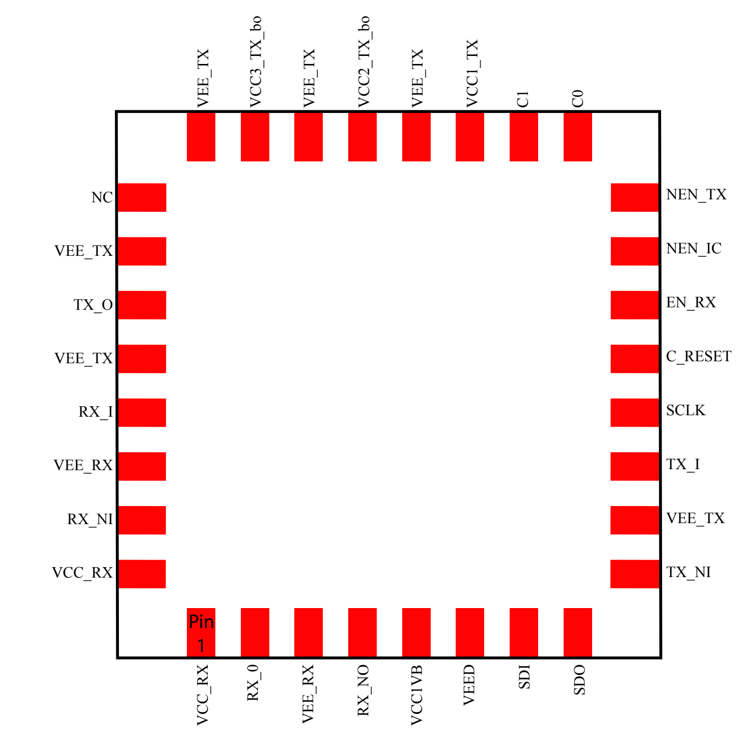

Figure 4: PL3111 LNA Lead Assignments

Pin Description Summary

The following table summarizes the signals names and descriptions for the PL3111 UWB LNA package connections.

Table 2: Signal Names and Lead Assignments

Lead #	Signal Name	Pad description	Notes
1	VCC_RX	Positive 3.3V Power supply	Connect to 3.3V power supply.
2-4	VEE_RX	RX ground	Connect to GND
5	RX_O	Output positive signal RX	
6	VEE_RX	RX ground	Connect to GND

Lead #	Signal Name	Pad description	Notes
7	RX_NO	Output negative RX signal ground	
8	VEE_RX	RX ground	Connect to GND
9	VCC1V8	Positive 1.8V digital power supply for SPI MUX and POR	
10-11	VEE	digital GND	Connect to GND
12	SDI	SPI Serial Data in	
13	VEED	digital GND	Connect to GND
14	VEE_TX	TX ground	Connect to GND
15	SDO	SPI Serial Data out	
16-17	VEE_TX	TX ground	Connect to GND
18	TX_NI	Transmit negative signal RF input	
19	VEE_TX	TX ground	Connect to GND
20	TX_I	Transmit positive signal RF input	
21	VEE_TX	TX ground	Connect to GND
22	SCLK	SPI clock	
23	C_RESET	SPI cycle reset	
24	EN_RX	Enable RX	Connect to 3.3V to enable receiver.
25	VEE_TX	TX ground	Connect to GND
26	NEN_IC	Enable the chip	Enable by default. Disable IC: connect to 3.3V through 10k resistor.
27	VEE_TX	TX ground	Connect to GND
28	NEN_TX	Enable TX	Connect to ground to enable transmitter.
29	CO	First bit for fast switch of slope and gain	Digital signal.
30	C1	Second bit for fast switch of slope and gain	Digital signal
31-33	VEE_TX	TX ground	Connect to GND
34	VCC1_TX	Positive power supply	Vcc=3.3V, bypass capacitor to ground
35-37	VEE_TX	TX ground	Connect to GND

Lead #	Signal Name	Pad description	Notes
38	VCC2_ TX_bo	Positive power supply	2nd stage Vcc=3.3V (r=10 Ohm on chip). Bypass capacitor to ground.
39-40	VEE_TX	TX ground	Connect to GND
41	VCC3_ TX_bo	Positive power supply	3rd stage Vcc=3.3V (r=5 Ohm on chip). Bypass capacitor to ground.
42-45	VEE_TX	TX ground	Connect to GND
46-48	TX_O	Output signal TX	
49-51	VEE_TX	TX ground	Connect to GND
52	VEE_RX	RX ground	Connect to GND
53	RX_I	Input positive RF signal RX	
54	VEE_RX	Negative power supply	Connect to GND
55	RX_NI	Input negarive RF signal RX	
56	VCC_RX	Positive 3.3 Connect to GND power supply	Connect to 3.3V power supply.

Electrical Specifications

Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings

Important: Exceeding these limits may result in malfunction and/or device damage.

Description	Value
Vcc (VCC_RX, , VCC_TX, VCC1_TX, VCC2_TX, VCC3_TX_bo VCC1_TX_bo)to GND	4V
RF in (RX_NI, RX_I, TX_I) at 50 Ω source	2 dBm
RF out (RX_O, RX_NO) on 50 Ω load	5 dBm
Managing signals (NEN_TX, EN_RX, SDO, SDI, SCLK, C_RESET)	4.0V
Operating temperature range	-25˚C to 90˚C
Maximum Junction temperature	125˚C
Max.Power dissipation	1500 mW
Storage temperature	-65˚C to 150˚C
Lead Temperature (soldering, 5s)	+300˚C

Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Description	Value
Relative Humidity	95%
Ambient Operating Temperature	0 C to +70 C

DC Characteristics

Table 5: DC Characteristics

Parameter	Condition	Min	Typ	Max	Units
RX and TX Supply voltage		3.1	3.3	3.6	V
Operating current	Tx -ON,RX-OFF Tx –OFF,Rx-ON Tx -ON,RX-ON Tx -OFF,RX-OFF		350 160 430 20		mA
SPI supply voltage		1.7	1.8	1.9	V

AC Characteristics

Ultra-Wideband LNA

Table 6: UWB LNA Characteristics

Parameter	Condition	Min	Typ	Max	Units
Operating frequency		3		5	GHz
Gain for power amp	see note below table	4		30	dB
Gain for LNA amp	see note below table	4		25	dB
Slope control in TX path	3 to 5 GHz	0		20	dB
Group delay variation on TX path	3 to 5 GHz				dB
Slope control on RX path	3 to 5 GHz	0		20	dB
Group delay variation on RX path	3 to 5 GHz				dB

Parameter	Condition	Min	Typ	Max	Units
Noise figure (3GHz-5GHz)	see note below table	1.5		2.9	dB
Input return loss for TX	3 to 5 GHz	-20		-10	dB
Output return loss for TX	3 to 5 GHz	-8		-7	dB
Input return loss for RX	3 to 5 GHz	-25		-10	dB
Output return loss for RX	3 to 5 GHz	-14		-9	dB
Reverse isolation (2GHz-6GH)	3 to 5 GHz			-56	dB
Input output isolation (RX OFF mode)				-50	dB

Note: Include losses for PC board, connectors, and input/outpout baluns. Baluns have a loss of 1.0 dB at 4GHz.

Typical Operating Characteristics

Typical plots of Noise Figure, Input/Output matching (S11, S22) and Input 1dB compression point for Nominal Corners of the process and temperatures are presented below in Figure 5 and Figure 6.

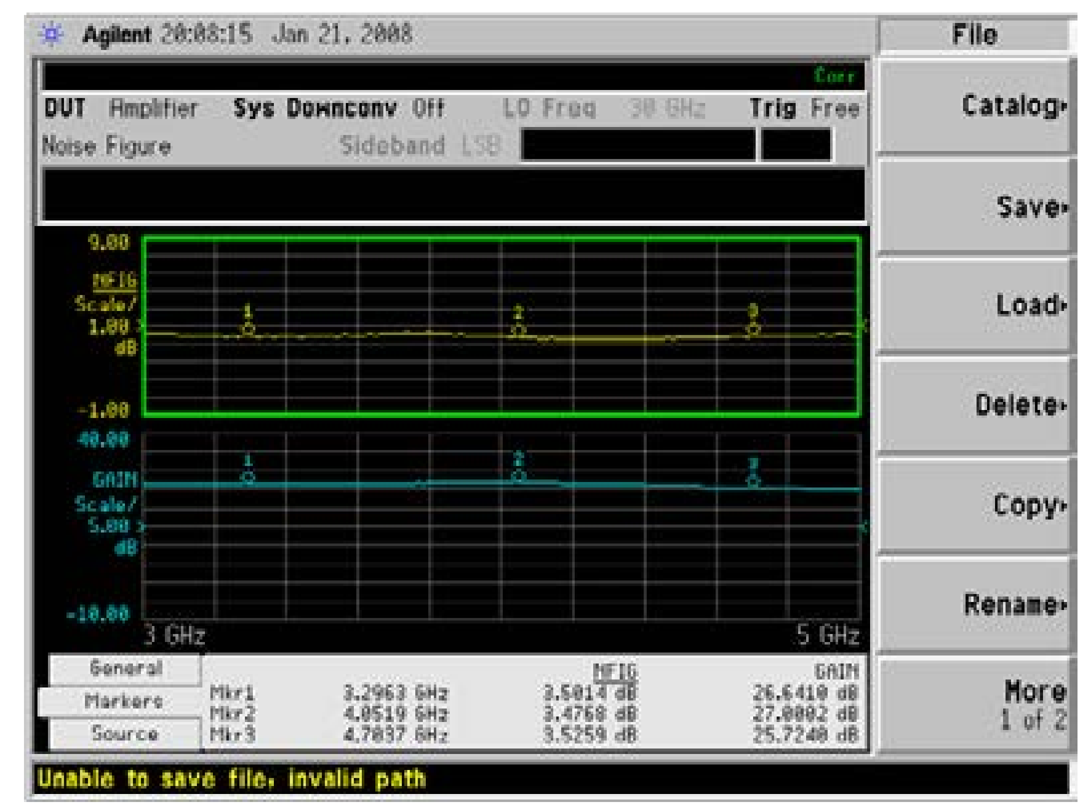

Figure 5: Noise & Gain

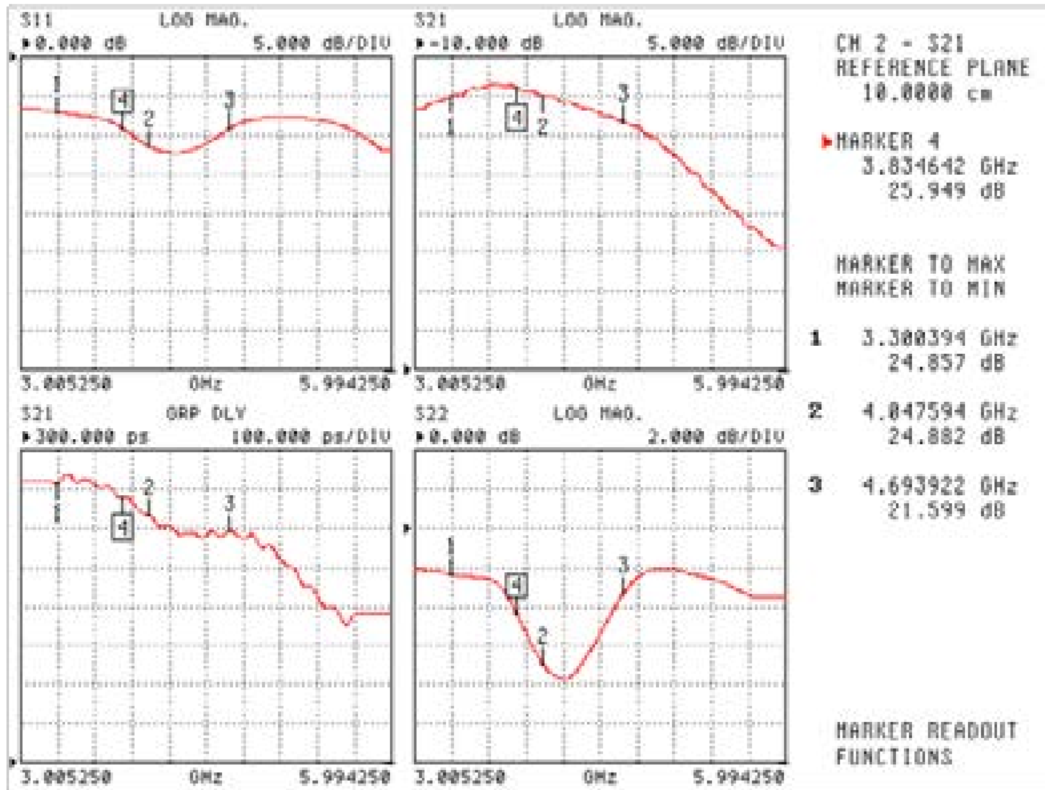

Figure 6: S-Parameter S21, S22 and S11 plots

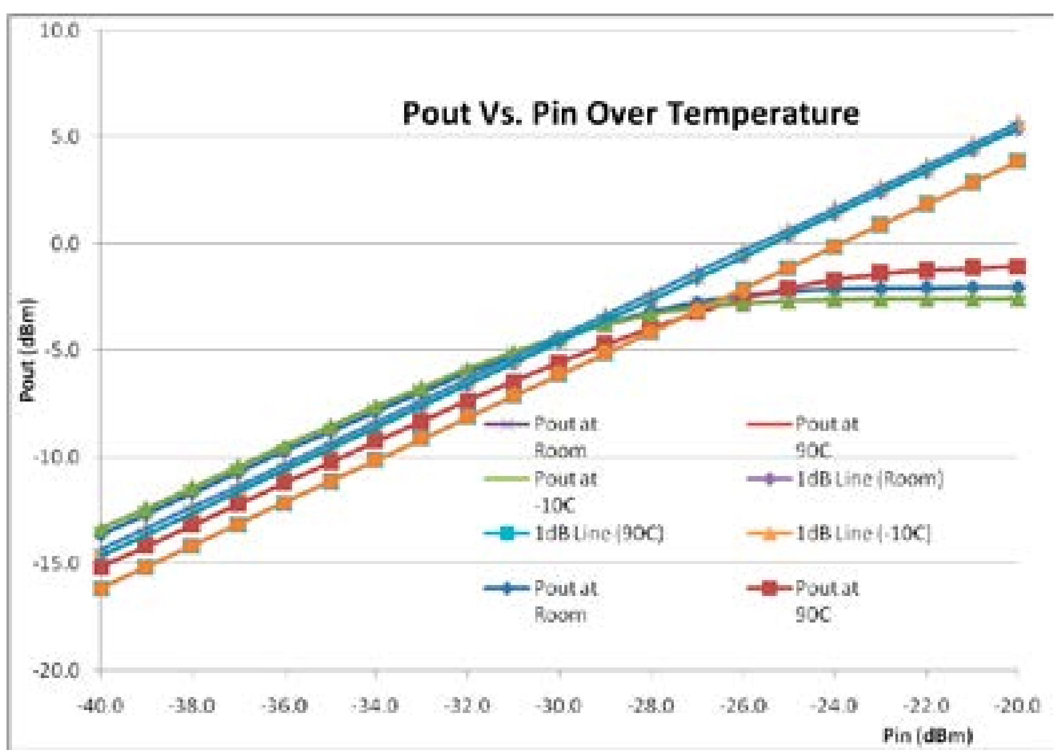

Figure 7: Pout vs. Pin at 4.05GHz and 24dB Gain with Slope Bypassed

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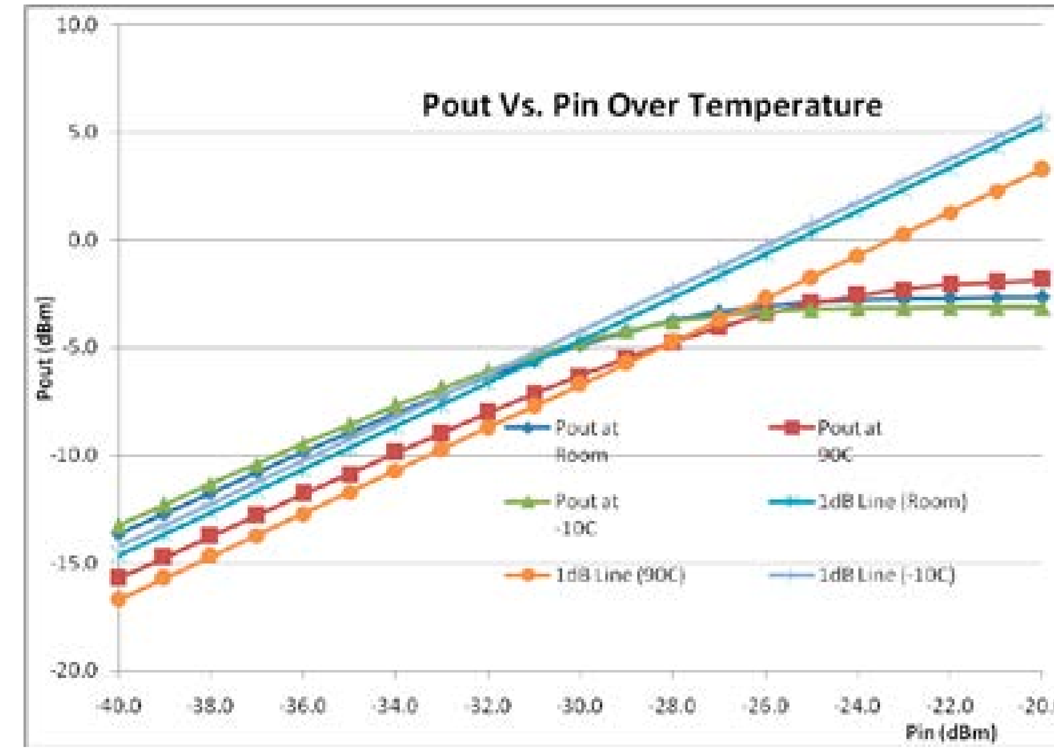

Figure 8: Pout vs. Pin at 4.7GHz and 24dB Gain with Slope Bypassed.

Mechanical Specifications

The PL3111 LNA 24-pin QFN package specifications are provided in Table 8.

Table 8: PL3111 LNA QFN Package Mechanical Specifications

Area	Dimensions
Compliance	Per JEDEC MO-205
Size	4x4 mm
Connection Leads	24 leads
Lead Pitch	0.50 mm
Nominal Thickness	0.85 mm

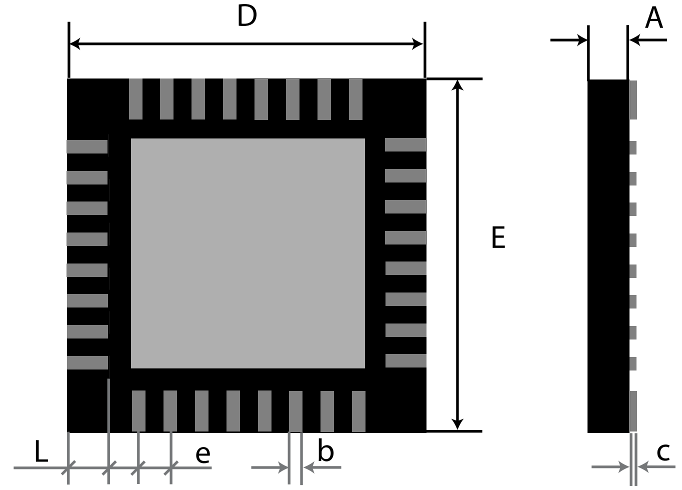

Figure 9: 36-pin QFN Package Dimensions (viewed from bottom)

Table 9: Overall Dimensions

Body Size,mm	Lead Count	Lead Pitch ,mm	Package Thk. mm	Footprint mm	Lead Width mm	L/F Thk. mm
D/E	N	e	A	L	b	c
5/5	32	0.5	0.85	0.4	0.23	0.20

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Acronyms & Abbreviations

ASIC Application Specific Integrated Circuit
BB Baseband
DEV 802.15.3 Device
EVK Evaluation Kit
LNA Low Noise Amplifier
lsb Least Significant Bit
LSB Least Significant Byte
MAC Media Access Control
msb Most Significant Bit
MSB Most Significant Byte
OB Output Buffer
PHY Physical Layer
PLL Phase Lock Loop
PNC 802.15.3 Piconet Coordinator
TDMA Time Division Multiple Access
UWB Ultra-Wideband
VGA Variable Gain Amplifier

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