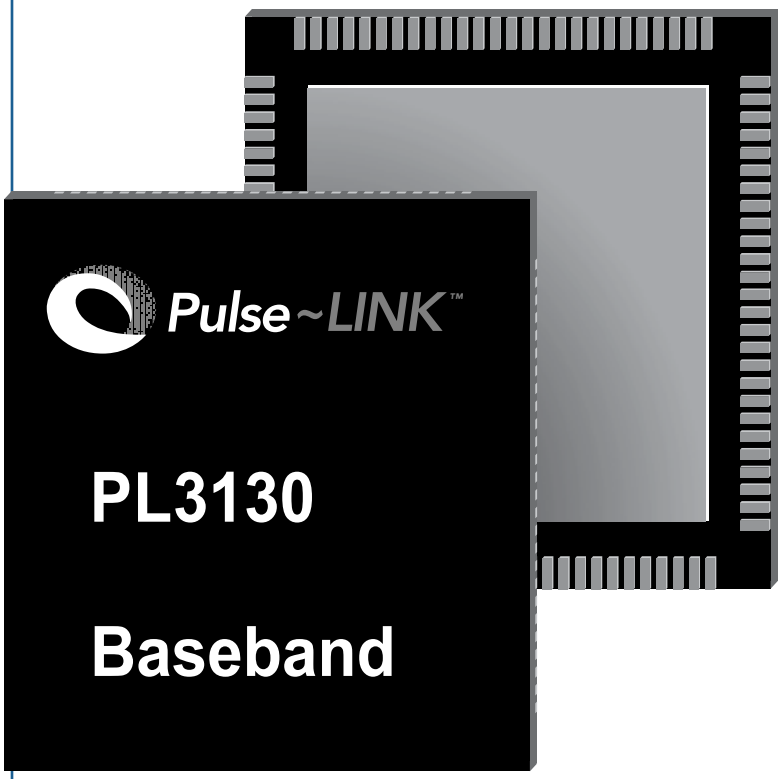
Pulse~LINK®

PL3130

CWave® Ultra Wideband BBM



Datasheet

111-00003-01 [8/13/14]

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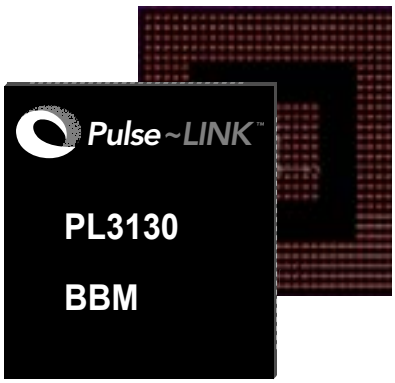

Introduction

The PL3130 CWave® Ultra Wideband Baseband+MAC (BBM) is an integral part of Pulse~LINK's CWave UWB chipset solutions for high-speed coax, wireless and hybrid connectivity. The PL3130 supports data rates up to 675 Mbps and directly interfaces with, and controls, the PL3120 Transceiver RFIC and the PL3110 Low Noise Amplifier (LNA) or the PL3111 Analog Front End(AFE).

The PL3130 CWave Baseband+MAC chip comprises a Media Access Controller (MAC) and a Baseband Physical Layer (BB PHY) encoder/decoder. The basic PL3130 communication and control is performed via a standard 32-bit PCI Bus over which instructions, status, and transport data are transferred. The MAC core consists of an embedded 802.15.3b MAC Protocol Processor (MPP), a TDMA Hardware Controller (THC), a 32-bit PCI Bridge controller (PBC), DDR memory controller (DRC), a serial FLASH memory controller (SFC), and the transport signal and control interfaces for the PL3120 Transceiver RFIC and PL3110 LNA. Internal communication is performed over a multi-layered internal MAC Bus Matrix enabling simultaneous multi-bus transactions to occur, greatly enhancing total system performance. The chipset functional diagram in Figure 1 shows the PL3130 Baseband+MAC as it fits into the high-performance Pulse~LINK CWave® UWB chipset solution.

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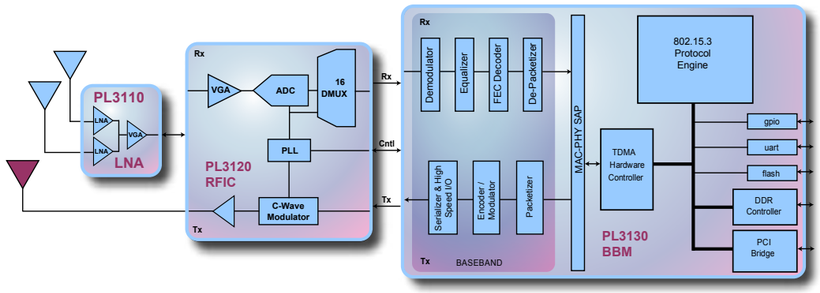

Figure 1: PL3130 Baseband + MAC Functional Chipset Interfaces

Baseband Transmitter & Receiver Signal Interface

The Baseband (BB) transmitter section of the PL3130 adds sync signals, cyclic redundance check (CRC) parity , and forward error correction (FEC) parity bits to the data stream, and scrambles the resultant bit stream to whiten its spectrum. The Baseband receiver detects the syncs and decodes the data stream for the MAC layer. Listed below are some of the main features of the PL3130 Baseband block.

- CWave® UWB modulation and demodulation
- User-selectable transmit data rates of 21, 42, 84, 169, 338, and 675 Mbps
- Automatic adjustment of corresponding receiver data rate
- Advanced Forward Error Correction (FEC)
- Direct interface to the PL3120 Transceiver RFIC.

Media Access Controller – MAC

The MAC portion of the PL3130 implements the wireless personal area network (WPAN) media access control layer as defined in the IEEE 802.15.3b Standard. Though defined as a wireless protocol, the 802.15.3b MAC is also suitable for UWB communication over wired medium such as coax cable. The MAC supports both Device (DEV) and Piconet Coordinator (PNC) capabilities and handles all required MAC functionality. Listed below are some of the main features of the PL3130 MAC block.

- Supports MAC protocol functions such as Piconet Scan, Association, Disassociation, and Channel Time Allocation (CTA)
- Piconet Coordinator (PNC) capable
- Hardware acknowledgement and retransmission
- Supports both asynchronous and isochronous data (with QoS)
- Embedded MAC Protocol Processor (MPP)
- Standard 32-bit PCI Bus for connection to a host device [or a PCI device that emulates the host operation]
- A 16-bit wide DDR266 (type 1) SDRAM interface.
- Serial Flash interface for boot-up and configuration memory

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MAC Associated PCI Drivers

- Windows or Linux PCI drivers
- Ethernet driver type
- Supports UDP/IP and TCP/IP traffic
- Control application utility plcfg used for:
  - Joining and leaving a piconet
  - Creating and terminating streams
  - Collecting and displaying link statistics
- Interacts with the PL3130 IEEE 802.15.3b MAC layer
- Generation of test traffic through utility commands plgive and pltake

Functional Descriptions

Functional Block Diagram

The PL3130 Baseband+MAC chip interfaces an external PCI Bus to the internal MAC Bus Matrix. External DDR memory and external Serial Flash memory are required for data and program storage. The BB interfaces to the MAC through a well-defined Baseband/MAC Interface. In addition to processing the Tx and Rx data streams, the BB also provides control signaling to the PL3120 Transceiver RFIC and the PL3110 LNA. A functional block diagram of the PL3130 Baseband+MAC is provided in Figure 3.

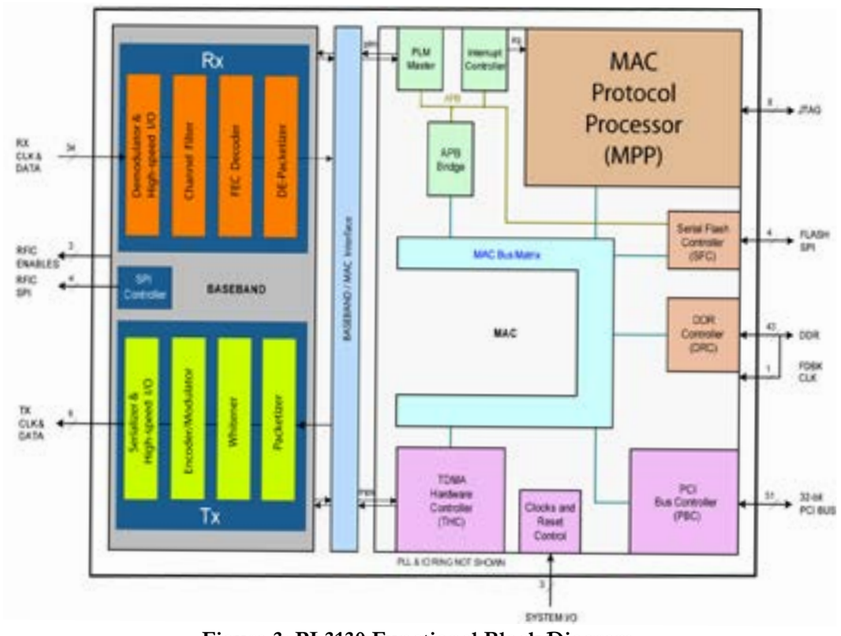

Figure 3: PL3130 Functional Block Diagram

Baseband Physical Layer

The Baseband Physical Layer portion of the PL3130 comprises separate transmitter and receiver sections, and performs communication control of the PL3120 Transceiver RFIC via a Serial Peripheral Interface (SPI) bus. The Baseband transceiver currently supports six operating modes: 21 Mbps, 42 Mbps, 84 Mbps, 169 Mbps, 338 Mbps, and 675 Mbps.

Transmit Data Encoding

The transmit block collects incoming data from the MAC and formats it for transmission over the UWB medium, inserting appropriate synchronization and header control signals into the emerging transport bitstream. The data bits are serialized, packetized, and finally whitened/scrambled. A CRC is appended to the header to facilitate error detection in the receiver.

The transmitter receives data from the TDMA Hardware Controller (THC) and instructions from the Physical Layer Management (PLM) Master via the Baseband/MAC interface. During operation, as the MAC provides header information for the beginning of each data packet, the transmitter parses the operating mode, the total packet length, and request for scrambling.

The transmitter generates and outputs a preamble comprising 80 sequences at 128 chips each (or 40 sequences of 256 chips each), sending these chips two at a time to the RF transmitter. Following the 10,240 chip preamble, the transmitter next spreads each bit of the 128 bit header with a 64-chip Golay sequence, which is then sent to the serializer and on to the RF transmitter. Following the header, the transmitter sends a Protocol Data Unit (PDU) spread by a variable number of data chips. The FEC rate and the length of the packet are determined by the MAC and are set to optimize throughput and minimize Packet Error Rate (PER).

Depending on the data rate, each bit may be spread into 64 data chips (21 Mbps mode), 16 data chips (42 Mbps, which has parity in LDPC mode, and 84 Mbps modes), or 4 data chips (169 Mbps, which has FEC, and 338 Mbps modes). In 675 Mbps mode, two chips represent each data bit, one of which is the bit itself, and the other of which is a parity bit generated using a Low Density Parity Check (LDPC) algorithm. The same rate 1/2 FEC is provided in the 42 and 169 Mbps modes. Each transmitted data packet therefore comprises a 10,240-chip synchronization preamble, a 128-bit control and address header, and the data payload itself, with periodic embedded resynchronization patterns. The header carries information on payload length, data rate, and operating mode. The data payload is also passed through a whitener/scrambler before being spread to minimize spectral spikes and to optimize error correction efficiency.

The transmitter's Low Voltage Differential Signaling (LVDS) interface then provides the digital data to the PL3120 RFIC transceiver chip at an aggregate 1.35 Gbps data rate. To keep the interface clock rates low, the data stream is divided into separate

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odd and even LVDS pairs sent at a half-speed rate of 675 Mbps. The data is latched and retimed within the PL3120 RFIC transceiver, modulated, and then sent over the UWB channel.

Transmit Data Synchronization

During the PDU, the transmitter inserts a series of sequences used for synchronization. These synch fields are special 256-chip Golay sequences that are used by the receiver to maintain clock/data timing recovery even when using a low precision & low cost oscillator. The sync fields are spaced between blocks of 24,576 data chips in the PDU and continue throughout the entire packet. The transmitted frame structure is shown in Figure 4.

Preamble	SFD	Header	GE	Data	GE	Data
9,216 chips	1024 chips	8192 chips	1280 chips	24,576 chips	1280 chips	24,576 chips

Start Frame Delimiter — Golay Extended Sync Fields

Figure 4: Transmit Frame Structure

Receive Data Decoding

The majority of the UWB receiver functionality is handled by the digital Baseband receive circuitry. This simplifies the PL3120 RFIC transceiver design, allowing for greater scalability to achieve higher data rates, and allows for Moore's Law efficiency improvements as device technology shrinks.

The receiver LVDS interface receives sampled digital data from the PL3120 RFIC transceiver chip. The data stream is accompanied by a synchronous clock used to latch the data as well as serving as the primary clock source for the Baseband digital logic. The digital down-converter provides the initial signal demodulation to present full 1.35 Gbps of raw data to the receiver. Any channel filtering and/or error detection therefore has the benefit of higher resolution than that of other receiver architectures.

In decoding the arriving data, the BB receiver basically performs the reverse functions of the transmitter. It down-samples the original data, detects the incoming preambles, decodes the incoming header to determine the data rate mode, and recovers the data. It also derives a CRC from the decoded header and reports any discrepancy between this derived CRC and the one received with the incoming header. Data CRC is performed by the MAC.

RFIC SPI Bus Controller

Four signal lines support the RFIC SPI Protocol defined in this specification:

- O_rfcSpiCycleRst_n (SPI_CYCLE_RESET_LOW) to the RFIC SPI SLAVE SPI_RSET. O_rfcSpiCycleRst_n is normally low, and when low holds the RFIC SPI SLAVE logic in a reset condition and TRI-STATEs the RFIC SPI SLAVE SDO (MISO) output. O_rfcSpiCycleRst_n is driven high during SPI write and

read transactions. O_rfcSpiCycleRst_n has no effect on the RFIC SPI SLAVE's control register outputs.

- O_rfcSpiCK (SPI_CLOCK) to the RFIC SPI SLAVE SCLK input. The frequency of O_rfcSpiCK is 12.5 MHz, and the duty cycle is 50%.
- O_rfcSpiDO (SERIAL DATA OUT) (MOSI) to the RFIC SPI SLAVE SDI (MOSI) input. MOSI=Master Out Slave In.
- I_rfcSpiDI (SERIAL DATA IN) (MISO) from the RFIC SPI SLAVE SDO (MISO) output. MISO=Master In Slave Out.

SPI Slave addressing is implemented in the SPI write and read transaction protocol, or frame structure. As such, there is no SPI chip select signal. The SPI protocol allows for a single SPI Master (PL3130) to talk to multiple Slave ICs within the chipset, where each Slave IC has an SPI Slave interface and may have multiple internal SPI SLAVEs.

There is a control and status register pair associated with each SPI SLAVE. Within this chipset SPI system, all SPI_CYCLE_RESET_LOW lines are connected together, all SPI_CLOCK lines are connected together, all MOSI lines are connected together, and all MISO lines are connected together. Each control and status register pair (SPI SLAVE) must have a unique address. Across the chipset's SPI five bit address space, every control and status register pair must have a unique address. The five bit address field is common to all ICs in the chipset.

The SPI output signals (O_rfcSpiCycleRst_n, O_rfcSpiCK, O_rfcSpiDO) are LVTTL 3.3V logic outputs, and can sink 8mA. The SPI input signal (I_rfcSpiDI) is an LVTTL 3.3V logic input. The RFIC SPI SLAVE SDO (MISO) output is normally in a TRI-STATE condition, and is driven only during SPI read transactions. After the end of a read transaction, the RFIC SPI SLAVE SDO (MISO) output returns to the TRI-STATE condition when O_rfcSpiCycleRst_n is driven low.

An SPI transaction or frame consists of 24 bits for both write and read. There are exactly 24 O_rfcSpiCKs per transaction. O_rfcSpiCK remains low except during SPI transactions. There are 5 address bits, 1 R/W bit, 2 reserved bits, and 16 data bits in each transaction. The R/W bit indicates whether the transaction is a write or a read (R/W=0=write; R/W=1=read). The reserved bits are ignored by the RFIC SPI SLAVE. Write transactions contain 16 data bits sent from the SPI Master to the RFIC SPI SLAVE. Read transactions contain 16 data bits sent from the RFIC SPI SLAVE to the SPI Master. Details of write and read transactions are given in the following sections.

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SPI Write Transaction

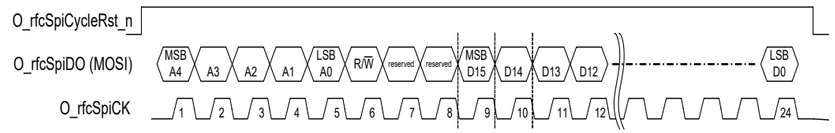

Figure 5. SPI Write Transaction

The SPI write transaction begins when the Master drives O_rfcSpiCycleRst_n high. Then about ½ the O_rfcSpiCK period later, the Master drives the first address bit A4 (MSB) onto O_rfcSpiDO (MOSI). After a setup interval of ½ the O_rfcSpiCK period, the Master issues the first O_rfcSpiCK rising edge. The Slave captures the information on O_rfcSpiDO with the O_rfcSpiCK rising edge. The bit on O_rfcSpiDO remains stable until the falling edge of O_rfcSpiCK, at which time the Master presents the next bit. After the 5 address bits are sent, the R/W bit (0=write) is sent. Then two reserved bits are sent. After the reserved bits, the Master sends the 16 data bits of the write transaction, starting with D15 and ending with D0.

On the rising edge of the 24th O_rfcSpiCK, the SPI Slave whose address matches the SPI transaction address (A4 through A0) will load all 16 bits of the write transaction data into its 16 bit control output register. The Master drives O_rfcSpiCycleRst_n low 1 O_rfcSpiCK period after the rising edge of the 24th O_rfcSpiCK.

SPI Read Transaction

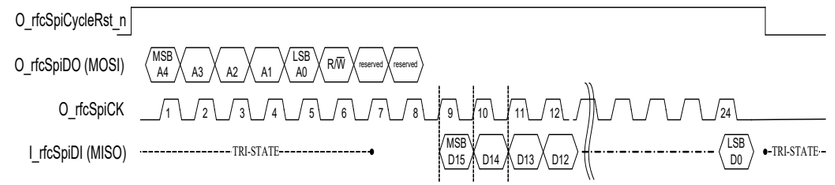

Figure 6. SPI Read Transaction

The SPI read transaction begins like the write transaction when the Master drives O_rfcSpiCycleRst_n high. Then about ½ the O_rfcSpiCK period later, the Master drives the first address bit A4 (MSB) onto O_rfcSpiDO (MOSI). After a setup interval of ½ the O_rfcSpiCK period, the Master issues the first O_rfcSpiCK rising edge. The Slave captures the information on O_rfcSpiDO with the O_rfcSpiCK rising edge. The bit on O_rfcSpiDO remains stable until the falling edge of O_rfcSpiCK, at which time the Master presents the next bit. After the 5 address bits are sent, the R/W bit (1=read) is sent.

On the rising edge of the 7th O_rfcSpiCK, the RFIC SPI SLAVE whose address matches the SPI transaction address (A4 through A0) begins to drive I_rfcSpiDI

[(MISO) RFIC SPI SLAVE SDO output], taking I_rfcSpiDI out of TRI-STATE. Also on the rising edge of the 7th O_rfcSpiCK, the SPI Slave internally captures or registers (not depicted in the figure) the 16 bits of read data that will be sent serially out onto I_rfcSpiDI. Then the Master sends the 2 reserved bits on O_rfcSpiDO. On the rising edge of the 9th O_rfcSpiCK, the addressed SPI Slave drives D15 (MSB of the read data) onto I_rfcSpiDI. The Slave then sends D14 on the 10th rising edge of O_rfcSpiCK, and so forth, finishing with D0 on the 24th rising edge of O_rfcSpiCK.

The Master captures or registers the I_rfcSpiDI read data 1 O_rfcSpiCK period after the Slave launched the data (on the next rising edge of O_rfcSpiCK, or the equivalent time interval). The Master drives O_rfcSpiCycleRst_n low 1.5 O_rfcSpiCK periods after the rising edge of the 24th O_rfcSpiCK, and in response the SPI Slave TRI-STATEs I_rfcSpiDI [(MISO) RFIC SPI SLAVE SDO output].

SPI Transaction Timing

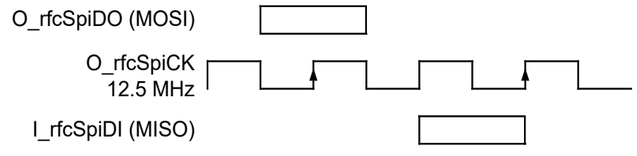

Figure 7. SPI Write and Read Timing

Figure 7 depicts timing for both write and read transactions. On a write transaction (including the address bits, R/W, and reserved bits for both write and read transactions), O_rfcSpiDO (MOSI) is stable approximately ½ O_rfcSpiCK period before, and through to ½ O_rfcSpiCK period after the O_rfcSpiCK rising edge the Slave uses to capture or register the O_rfcSpiDO write data. On a read transaction, I_rfcSpiDI [(MISO) RFIC SPI SLAVE SDO output] is launched by the Slave on an O_rfcSpiCK rising edge and captured or registered by the Master on the next O_rfcSpiCK rising edge. Thus I_rfcSpiDI has 1 O_rfcSpiCK period to become valid before being captured by the Master.

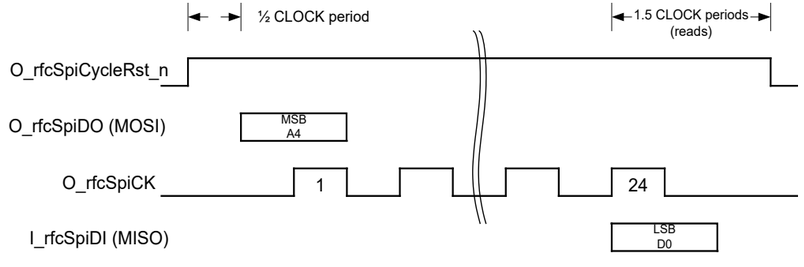

Figure 8. SPI CYCLE_RESET Timing

Figure 8 depicts O_rfcSpiCycleRst_n timing for both write and read transactions. The

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transaction begins when the Master drives O_rfcSpiCycleRst_n high. Then about ½ the O_rfcSpiCK period later, the Master drives the first address bit A4 (MSB) onto O_rfcSpiDO. After a setup interval of ½ the O_rfcSpiCK period, the Master issues the first O_rfcSpiCK rising edge. O_rfcSpiCycleRst_n timing at the end of a write transaction where the Master drives O_rfcSpiCycleRst_n low 1 O_rfcSpiCK period after the rising edge of the 24th O_rfcSpiCK is not depicted above. O_rfcSpiCycleRst_n timing at the end of a read transaction where the Master drives O_rfcSpiCycleRst_n low 1.5 O_rfcSpiCK periods after the rising edge of the 24th O_rfcSpiCK is depicted above.

MAC - Media Access Control Layer

The MAC layer contains the entire hardware protocol functionality for an Ultra-Wideband device. It provides a 32-bit Bus Master interface and 32-bit PCI Initiator interface for high-speed data and command frame transfers between the MAC Protocol Processor (MPP) system memory data buffers and host data buffers across the PCI interface.

The MAC is composed of a MAC Protocol Processor (MPP) and several peripherals interconnected by a multi-layer internal bus matrix. The MAC Bus Matrix enables multiple bus transactions to occur simultaneously to speed up system performance. Only the MPP, the PCI Bus Controller (PBC), and TDMA Hardware Controller (THC) can initiate transactions on the MAC Bus Matrix. The MAC Bus Matrix provides arbitration in the case where more than one master attempts to access the same slave at any one time. Transactions are limited in size so that no master can block out another master's transaction for an extended period. A system address map, as shown in Figure 23 (page 38), describes the address ranges that are used by every master to access each slave. Access of the TDMA Controller and the PCI Bus Controller is limited to the memories (DDR and Serial Flash), and a 'Default Slave' for address error handling.

The MAC hardware intelligently and efficiently moves blocks of information (data and/or control) between the PCI interface and memory and between memory and the BB, to support the transmission and reception of IEEE 802.15.3b defined frames over the UWB medium. Blocks of information are moved in one or more transactions. Transactions are supported in both directions. A "TX transaction" is defined as moving information towards the Baseband/MAC Interface. A "RX transaction" is defined as moving information towards the PCI Bus interface.

MAC Hardware and Interfaces

802.15.3b MAC Protocol Processor (MPP)

The on-chip 802.15.3b MPP works in conjunction with the THC and is specifically designed for optimal data handling performance and implementation. The MPP is based on a 32-bit wide processing architecture and is tightly coupled to the PCI Bus interface and various support block interface controllers.

TDMA Hardware Controller (THC)

The THC is a full-featured TDMA MAC protocol engine designed with multiple options to achieve maximum throughput efficiency and at the same time save power. When the TDMA MAC performs as a PNC, it sends out beacons with a defined interval (typically 10-65 ms). The time between the beacons is called a Superframe (SF) (refer to section 2.4). The PNC will divide the time in the SF between DEVs requesting Channel Time. The resulting time slots are called Channel Time Allocations (CTA). The CTA for an SF is listed in the frame body of the beacon and identifies the destination, source, stream index (handle) and the location (offset from beacon time) and duration of the CTA. A DEV is allowed to transmit only inside the time duration of its allocated CTA.

Reservation of channel time is done through a client-server style Channel Time Manager (CTM). When the application needs a stream with certain QoS parameters, the client side calculates how much channel time it needs per SF, how often it needs to be allocated to maintain acceptable delays, and what minimum time is required to be able to send individual frames. The client CTM has to take into account the extra time needed to fit retransmissions and acknowledgements (ACK) into the payload stream. The time needed per frame is dependent on the PHY rate used and specific PHY related parameters such as the length of the preamble.

The server side of the CTM resides in the PNC. The PNC needs to find the most efficient way to fit all requests for channel time into each SF. It needs to honor the CTA agreements it has made with each DEV while at the same time maintain some level of fairness between DEVs. It can use different kinds of prioritization schemes to decide which CTA takes precedence if the available time for allocation is getting limited.

Once the PNC has decided the CTA layout, it will generate it in every beacon. The CTA layout may look different in different beacons, for instance a low data rate CTA may only be put in every second beacon (or even further apart as required).

The last part of the protocol scheme is the beacon CTA parser. Every DEV has a parser to set up their PHY to perform transmission and reception at the correct times.

The PNC may set up CTA for a DEV even if it hasn't been requested. A typical example of such voluntary CTA is the Management CTA (MCTA). This is a regular CTA dedicated for command and control traffic.

A CTA requested by a DEV for dedicated isochronous traffic to one or more recipients is called a stream. Each stream is allocated by a PNC, mapped to a CTA and assigned a Stream Index. The Stream Index is used for all future manipulation of the stream. Time not assigned to streams is typically used for asynchronous traffic.

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An example of a Superframe is shown in Figure 7. The 802.15.3b protocol format is reviewed in more detail in Section 2.4.

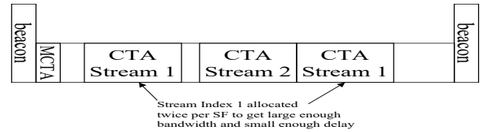

Figure 9: Example of a Superframe

The specifics of the CTM is not defined in the standard, so it is up to the end-user to find the optimal solution for their application. Dynamic Rate Adaptation is an example of functionality a user may want to design into their system. The radio conditions are never constant and are always dynamically changing. Every DEV needs to monitor the effective bandwidth of their streams and request adjustments when needed to fulfill the QoS contract with higher layers.

The THC utilizes a 4 KByte system memory address space for registers. Figure 23 in the Appendix indicates where these registers are located in the MAC system memory map.

PCI Bus Interface

The MAC contains a 32-bit PCI Initiator interface for data buffer transactions and 32-bit PCI Target interface for configuration purposes and to allow the PCI host to start bridge processing on its end. The MAC PCI Bus interface supports a maximum PCI clock of 66MHz. Refer to the PCI Local Bus Specification, Revision 2.3, for details on the PCI interface. The MAC supports mini-PCI Revision 1.0 in addition to PCI.

PCI Bus Controller

The PCI Bus Controller (PBC) interfaces the PCI Bus to the internal MAC Bus Matrix. On the PCI Bus, transactions are not tied in to the TDMA engine but instead queues are established and serviced in a software specified order. Higher priorities can be assigned to individual queues so they can get serviced longer. This is implemented to support high-speed isochronous data transfer over the PCI Bus where some queues require more bandwidth than others. In the PCI Bus Controller, both Rx and Tx queues run simultaneously with a built-in arbiter alternating between Rx and Tx transactions on the PCI Bus interface.

MAC Bus Matrix

The MAC Bus Matrix allows simultaneous concurrent bus transactions between multiple MAC Bus Matrix masters (THC, PCI Bus Controller, MPP-Instruction, and MPP-Data) and slave devices (DDR, SFC, and APB Bridge) connected to the MAC Bus Matrix.

APB Bridge

The Auxiliary Peripheral Bus (APB) Bridge connects the MAC Bus Matrix to the APB bus. The function of this module is to separate low-speed devices, such as the Interrupt Controller and PLM Master, from the high-throughput MAC Bus Matrix.

DDR Memory

There is a single DDR Controller (DRC) provided in the MAC. It provides 4 slave interfaces to an external DDR SDRAM from the MAC. Additionally, it provides a single MAC Bus Matrix interface for programming. The 16-bit wide MAC DDR interface runs at a 133MHz rate and each of the four MAC Bus Matrix masters (THC, PCI Bus Controller, MPP-Instruction, and MPP-Data) has access to the DDR memory.

Serial Flash Controller

The Serial Flash Controller (SFC) provides an SPI interface to external Serial Flash for device boot-up purposes. The SFC utilizes a single slave interface to a 16 MByte MPP system memory address space for data access, and a 4 KByte system memory address space for register accesses. Figure 23 (page 38) indicates where these registers are located in the MAC system memory map.

Interrupt Controller

The Interrupt Controller gathers and prioritizes all interrupts from the MAC peripherals and provides a single, maskable interrupt (nIRQ), to the MPP core. The MAC provides a single, active-low interrupt output to the MPP Interrupt Controller. The MAC's Interrupt Controller module combines and prioritizes interrupts from the MPP, THC, PLM, SFC, DDR, and PCI Bus Controller modules.

The Interrupt Controller utilizes a 4 KByte system memory address space for registers and is physically connected to the APB bus. Figure 23 indicates where these registers are located in the MAC system memory map.

Baseband/MAC Interface

On the Baseband/MAC interface, queues are processed under control of the hardware TDMA engine (THC) designed to support the IEEE 802.15.3b protocol. Information contained in the IEEE 802.15.3b Beacon frame is decoded to identify timeslots relative to the start of the Beacon frame in which the MAC hardware services a particular queue (or queues). A timeslot can be identified as either Rx or Tx and therefore only one direction can be active at any one time. Within a timeslot, blocks of information (both Rx and Tx) are moved under control of the MPP to and from the Baseband/MAC Interface. The MPP sets up descriptors in memory that define the blocks of information to be moved. Hardware state machines within the THC read the descriptors from memory and move the blocks accordingly.

To support separate command streams, asynchronous data, and multiple isochronous data streams, the MPP sets up multiple queues of descriptors. The queues are

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processed by the MAC hardware in a well-defined manner and the THC automatically retries frames as necessary per protocol definition.

Physical Layer Management

The Physical Layer Management (PLM) Master is a MAC APB slave peripheral that is used to read and write registers across the Baseband/MAC Interface for the set up and management of the BB hardware. It provides a simple register interface on the APB slave as described below to generate the PLM Master transactions.

To avoid potentially lengthy latencies on read transactions, both PLM read and write transactions are initiated by write transactions from the APB. The command bit in the plmControl register indicates whether the PLM Master should perform a read or write transaction on the Baseband/MAC interface. The MPP writes the ownByHw bit in the plmControl register to '1' to start a PLM transaction, and hardware clears the ownByHw bit to '0' when the transaction is complete. On a read transaction, the data that is read from the PLM interface will be valid in the plmRdData register when the ownByHw bit is cleared. On a write transaction, the MPP must set up plmWrData with the 32-bit data word to write prior to setting the ownByHw bit to '1'. The PLM Master indicates that the write has completed after the transaction has completed on the Baseband/MAC interface.

The PLM module uses 4 Kbytes of system memory space as indicated in Figure 23 in the Appendix.

THC to Baseband Interface

The Baseband/MAC Interface is the main data and control interface between the THC and the BB Physical Interface. With the exception of reset, it is a completely synchronous interface. Several features of the interface are listed below:

- Single, synchronous clock
- 16-bit data path supports required bit rates
- Simple protocol keeps hardware design complexity to a minimum
- Fully supports 802.15.3b MAC protocol with a CWave® UWB PHY

Buffer Management

The MPP manages buffers throughout the MAC by using descriptors to eliminate any unnecessary copying of data, effectively saving bandwidth. As an example, for a Tx stream, the MPP sets up a queue of receive buffers to accommodate data retrieved from the PCI Bus for a stream. After the PCI Bus Controller has read a block of information from the PCI Bus and moved that block into a buffer from the input queue, the PCI Bus Controller informs the MPP that the buffer has been used. The MPP then moves that buffer to a THC output queue. This is performed by adding the descriptor for that buffer to the end of that stream's THC's Tx queue, therefore no data copy is made. The descriptor is added to the queue only by moving pointers. The THC then sends the data block to the BB through the BB/MAC Interface at the appropriate time. After the frame is sent, the THC marks the

descriptor (and therefore buffer) as being complete, and the MPP can now recycle this buffer onto the end of a receive queue.

CWave® MAC Protocol Structure

Pulse~LINK selected the 802.15.3b MAC as the basis for their CWave® MAC protocol as it was determined to provide the following benefits for a UWB system:

- The best, most reliable support for High-Definition video applications,
- Support for efficient transfer of data files 100's of megabytes in size,
- Performance that scales with increasing CWave® UWB PHY data rates.

Superframe Structure

In any wireless network there are several issues that must be addressed to ensure efficient use of the available wireless bandwidth. The first issue is a means of providing network timing synchronization for each of the wireless network devices. The second issue is support for coordinated access to the RF medium. The third issue is finding a solution to the hidden node problem. The IEEE 802.15.3b MAC protocol addresses each of these issues via the Superframe, which is illustrated in Figure 8.

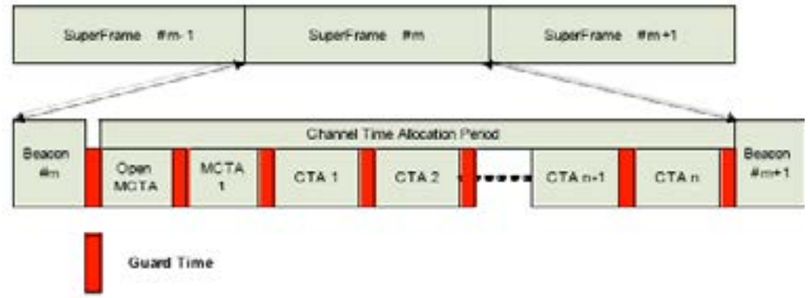

Figure 10: 802.15.3b MAC Protocol Superframe

The Beacon provides the fundamental "heart beat" or synchronization timing reference for the piconet. In addition, the beacon broadcasts piconet management information and assigned channel time allocations to each of the client DEVs. Any device that cannot hear the PNC piconet beacon is not allowed to transmit. Thus the potential hidden node problem in an 802.15.3b piconet is resolved. The Channel Time Allocation Period (CTAP) consists of:

One or more assigned MCTAs that may be used by associated DEVs to send command and control frames to either the PNC or other associated DEVs.

One or more assigned Channel Time Allocations (CTAs) during which time DEVs may transmit/receive asynchronous and/or isochronous data frames.

Guard time intervals between adjacent CTAs. The guard time intervals are used to prevent collisions due to clock drift.

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Frame Formats

In any communications protocol there is a need for a set of building block message types which, when used in combination with other message types, enables the effective exchange of useful information. The 802.15.3b MAC is no different in this regard. The fundamental building blocks of the 15.3b MAC are the beacon, command, data, and ACK frames.

802.15.3b General MAC Frame Format

Figure 9 illustrates the components that are common to each of the 802.15.3b frame types (i.e. beacon, command, data and ACK). Each frame type includes a ten-octet MAC header, an optional MAC frame body Payload followed by a Frame Check.

bits: b23	b22 - b16	b15 - b9	b8 - b0
Reserved	Last fragment number	fragment number	MSDU number

Octets: 4	Ln		1	3	1	1	2	2
FCS	Payload		Stream Index	Fragmentation control	Source DEVID	Destination DEVID	PN ID	Frame Control
MAC Frame Body			802.15.3 MAC Header					

bits: b15 - b14	b13	b12	b11	b10	b9	b8 - b7	b6	b5 - b3	b2 - b0
Reserved	CTA relinqish	Imp-ACK NAK	Imp-ACK NAK	More data	Retry	ACK policy	SEC	Frame type	Protocol version

Figure 11: General 802.15.3b MAC Frame Format

The 10-octet long MAC header is composed of these fields:

- Frame Control
- PNID – piconet ID
- Destination DEVID
- Source DEVID
- Fragmentation control
- Stream index

The Payload may be zero octets long in the case of an Immediate ACK or up to a maxMTU size (64KB) in octets. The FCS field contains a 32-bit CRC. This field is

used to determine if any bit errors due to transmission have occurred in the payload portion of the transmitted frame.

Beacon Frame Format

The 802.15.3b beacon frame is composed of a MAC header followed by the Piconet synchronization parameters field, one or more Information Elements (IE)s in the beacon's frame body payload, and then followed by the FCS. Figure 10 illustrates the components of a beacon frame that could be present during initial startup of a piconet. Note that in this example the mandatory BSID IE is in the first IE position immediately following the Piconet Synchronization Parameters field.

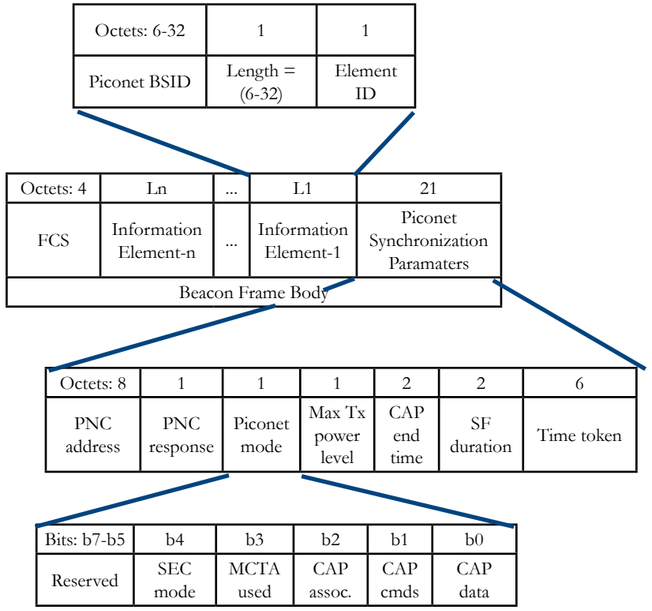

Figure 12: 802.15.3b Beacon Frame Format with BSDI IE

Figure 13 illustrates a beacon in which a Channel Time Allocation (CTA) IE and the mandatory BSID IE are present.

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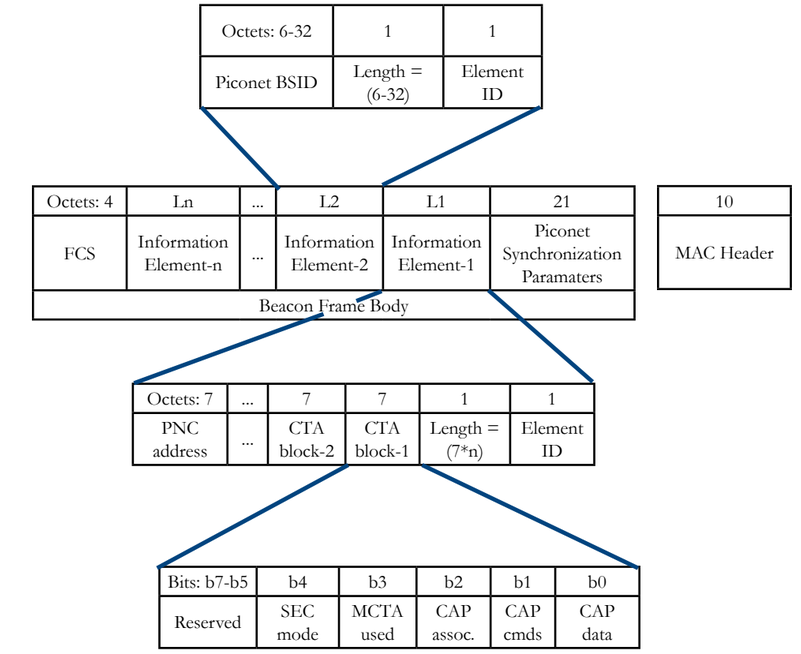

Figure 13: 802.15.3b beacon Frame Format with BSID and CTA IEs

Other essential beacon only information elements are:

- DEV Association IE
- PNC Shutdown IE
- Channel Time Status IE

Command Frame Format

The 802.15.3b command frame illustrated in Figure 14 is the format used by the MAC to transfer command frames to the PHY for transmission over the selected medium. On the receive side it is the format used by the PHY to transfer received command frames to the MAC.

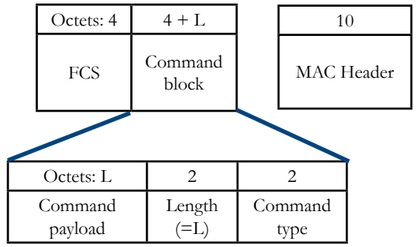

Figure 14: 802.15.3b Command Frame Format

The essential MAC to MAC layer commands are:

- Association request/response
- Disassociation request
- Channel Time request/response
- PNC Handover request/response
- PNC Handover information.

Data Frame Format

The data frame illustrated in Figure 15 is the format used by the MAC to transfer data to the PHY for transmission over the selected medium. On the receive side it is the format used by the PHY to transfer received data to the MAC.

Octets: 4	L	10
FCS	Data payload	MAC Header

Figure 15: 802.15.3b Data Frame Format

ACK Frame Format

The Immediate-ACK frame format is illustrated in Figure 16. The Immediate- ACK frame is used by DEV-B to indicate to DEV-A that the data frame that DEV-A just sent has been successfully received.

10
MAC Header

Figure 16: 802.15.3b ACK Frame Format

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Device Connections

This section describes the connection signals and ball assignments for the PL3130 IC.

I/O Configuration

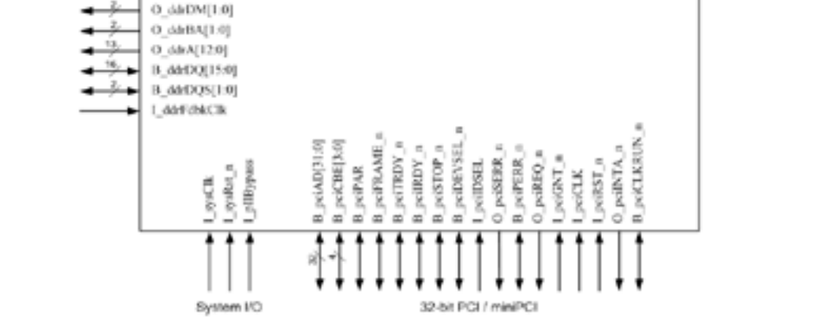

Figure 17: PL3130 Baseband+MAC Signal I/O

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Signal Description Summary

The following tables summarize the PL3130 signal descriptions and ball connections.

Table 1: I/O Designators

Type	Description
I	Input
O	Output
IO	Input/Output
OD	Open Drain
P	Power
G	Ground
DNC	Do Not Connect

Table 2: System I/O

System I/O (3)	Dir.	Type	Description	Ball
I_sysClk	I	LVTTL	25MHz system clock Input to PLL.	W19
I_sysRst_n	I	LVTTL	Active-low, asynchronous reset input must be debounced external to the chip. This signal is identical in function to swRst and resets the entire device except for the pciCore in the PAB module.	AB22
I_pllBypass	I	LVTTL	1 : bypass PLL 0 : normal / engage PLL	Y20

Table 3: PCI I/O

PCI I/O (51)	Dir.	Type	Description	Ball
B_pciAD[0]	IO	PCI	address/data	A10
B_pciAD[1]				H2
B_pciAD[2]				G3
B_pciAD[3]				F1
B_pciAD[4]				F2
B_pciAD[5]				E1
B_pciAD[6]				D1
B_pciAD[7]				E2
B_pciAD[8]				C1
B_pciAD[9]				E3
B_pciAD[10]				D2
B_pciAD[11]				C2
B_pciAD[12]				D3

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PCI I/O (51)	Dir.	Type	Description	Ball
B_pciAD[13]	IO	PCI	address/data	B1
B_pciAD[14]				B2
B_pciAD[15]				A1
B_pciAD[16]				C6
B_pciAD[17]				C7
B_pciAD[18]				B6
B_pciAD[19]				C8
B_pciAD[20]				B7
B_pciAD[21]				B8
B_pciAD[22]				A7
B_pciAD[23]				A8
B_pciAD[24]				B9
B_pciAD[25]				A10
B_pciAD[26]				C10
B_pciAD[27]				C11
B_pciAD[28]				B10
B_pciAD[29]				A11
B_pciAD[30]				B11
B_pciAD[31]				A12
B_pciCBE_n[0]	IO	PCI	command/byte enables	F3
B_pciCBE_n[1]				C3
B_pciCBE_n[2]				A5
B_pciCBE_n[3]				A9
B_pciPAR	IO	PCI	parity	A6
B_pciFRAME_n	IO	PCI	frame	A4
B_pciTRDY_n	IO	PCI	0 : target ready	B4
B_pciIRDY_n	IO	PCI	0 : initiator ready	B5
B_pciSTOP_n	IO	PCI	0 : stop	C4
B_pciDEVSEL_n	IO	PCI	0 : device selected	A2
I_pciIDSEL	I	PCI	initialization device select	C9
O_pciSERR_n	OD	PCI	0 : system error	A3
B_pciPERR_n	IO	PCI	0 : parity error	B3
O_pciREQ_n	O	PCI	0 : PCI bus request	C12
I_pciGNT_n	I	PCI	0 : PCI bus grant	B12
I_pciCLK	I	PCI	1 : 66MHz, 0 : 33MHz PCI Clock	B13
I_pciRST_n	I	PCI	0 : PCI reset	A13
O_pciINTA_n	OD	PCI	0 : interrupt	C13
B_pciCLKRUN_n	I, OD	PCI	0 : clock run	C5

Note: PL3130 does not support the 64-bit PCI extension, nor does it support the optional PCI device signals

LOCK#, SMBCLK, or SMBDAT. M66EN is not used by PL3130. No Mini PCI sideband signals are supported. PL3130 does not support the PME# power management event signal.

Table 4: DDR

DDR (44)	Dir.	Type	Description	Ball
I_ddrFdbkClk	I	SSTL_2	Feedback Clock for Deskew	P1
O_ddrCK_p	O	SSTL_2	Differential Clock (CK +)	R1
O_ddrCK_n	O	SSTL_2	Differential Clock (CK -)	T1
O_ddrCKE	O	SSTL_2	Clock Enable (CKE)	P2
O_ddrCS_n	O	SSTL_2	Chip Select (CS#)	N3
O_ddrRAS_n	O	SSTL_2	Command input (RAS#)	U1
O_ddrCAS_n	O	SSTL_2	Command input (CAS#)	R2
O_ddrWE_n	O	SSTL_2	Command input (WE#)	P3
O_ddrDM[0] O_ddrDM[1]	O	SSTL_2	Data mask (DM), bit 1 is for DQ[15:8]	H1 J3
O_ddrBA[0] O_ddrBA[1]	O	SSTL_2	Bank Address (BA)	H2 G1
O_ddrA[0] O_ddrA[1] O_ddrA[2] O_ddrA[3] O_ddrA[4] O_ddrA[5] O_ddrA[6] O_ddrA[7] O_ddrA[8] O_ddrA[9] O_ddrA[10] O_ddrA[11] O_ddrA[12]	O	SSTL_2	Address (A)	J2 J1 K3 K2 K1 L3 L2 L1 M1 M2 M3 N1 N2
B_ddrDQ[0] B_ddrDQ[1] B_ddrDQ[2] B_ddrDQ[3] B_ddrDQ[4] B_ddrDQ[5] B_ddrDQ[6] B_ddrDQ[7] B_ddrDQ[8] B_ddrDQ[9] B_ddrDQ[10] B_ddrDQ[11] B_ddrDQ[12] B_ddrDQ[13] B_ddrDQ[14] B_ddrDQ[15]	IO	SSTL_2	Data I/O (DQ)	T2 R3 V1 U2 T3 W1 V2 U3 V3 AA1 Y2 AB1 W3 AA2 AB2 Y3

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DDR (44)	Dir.	Type	Description	Ball
B_ddrDQS[0] B_ddrDQS[1]	IO	SSTL_2	Data Strobe (DQS)	Y1 W2

Table 5: SPI Serial Flash

SPI Serial Flash (4)	Dir.	Type	Description	Ball
O_sfcSpiCK	O	LVTTL	SPI Clock	Y21
O_sfcSpiCS_n	O	LVTTL	Active low SPI Chip select	W20
O_sfcSpiDO	O	LVTTL	SPI Data Out to Serial Flash Device	AA22
I_sfcSpiDI	I	LVTTL	SPI Data In from Serial Flash Device	W21

Table 6: JTAG

JTAG (8)	Dir.	Type	Description	Ball
I_jtagArmSel	I	LVTTL	1: selects MPP JTAG, 0: selects Boundary Scan. For normaloperation, pull-up with 4.7K to 3v3.	AA19
I_jtagTCK	I	LVTTL	Test Clock	AA20
I_jtagTDI	I	LVTTL	Test Data Input	Y18
O_jtagTDO	O	LVTTL	Test Data Output	AB19
I_jtagTMS	I	LVTTL	Test Mode Select	AB21
I_jtagTRST_n	I	LVTTL	Test Reset	Y19
O_jtagRTCK	O	LVTTL	Returned Test Clock	AA21
B_jtagSRST_n	IO	LVTTL	JTAG system reset	AB20

Table 7: RFIC Interface

RFIC Interface (43)	Dir.	Type	Description	Ball
I_rfcRxClk_p	I	LVDS	675 MHz diff clock + from RFIC	AA8
I_rfcRxClk_n	I	LVDS	675 MHz diff clock - from RFIC	AB8

RFIC Interface (43)	Dir.	Type	Description	Ball
I_rfcRxData_p[0]	I	LVDS	675 Mbps diff data + from RFIC	Y12
I_rfcRxData_p[1]				AB12
I_rfcRxData_p[2]				AB11
I_rfcRxData_p[3]				Y11
I_rfcRxData_p[4]				AB10
I_rfcRxData_p[5]				W10
I_rfcRxData_p[6]				AB9
I_rfcRxData_p[7]				W9
I_rfcRxData_p[8]				AA7
I_rfcRxData_p[9]				AA6
I_rfcRxData_p[10]				AA5
I_rfcRxData_p[11]				W6
I_rfcRxData_p[12]				AA4
I_rfcRxData_p[13]				W5
I_rfcRxData_p[14]				AA3
I_rfcRxData_p[15]				W4
I_rfcRxData_n[0]	I	LVDS	675 Mbps diff data - from RFIC	W12
I_rfcRxData_n[1]				AA12
I_rfcRxData_n[2]				AA11
I_rfcRxData_n[3]				W11
I_rfcRxData_n[4]				AA10
I_rfcRxData_n[5]				Y10
I_rfcRxData_n[6]				AA9
I_rfcRxData_n[7]				Y9
I_rfcRxData_n[8]				AB7
I_rfcRxData_n[9]				AB6
I_rfcRxData_n[10]				AB5
I_rfcRxData_n[11]				Y6
I_rfcRxData_n[12]				AB4
I_rfcRxData_n[13]				Y5
I_rfcRxData_n[14]				AB3
I_rfcRxData_n[15]				Y4
O_rfcTxClk_p	O	LVDS	675 MHz diff clock + to RFIC	AB13
O_rfcTxClk_n	O	LVDS	675 MHz diff clock - to RFIC	AA13
O_rfcTxData_p[0]	O	LVDS	675 Mbps diff data + to RFIC	AB14
O_rfcTxData_n[0]	O	LVDS	675 Mbps diff data - to RFIC	AA14
O_rfcTxData_p[1]	O	LVDS	675 Mbps diff data + to RFIC	AB15
O_rfcTxData_n[1]	O	LVDS	675 Mbps diff data - to RFIC	AA15
O_rfcEnIC_n	O	LVTTL	Active low RFIC chip enable	W13
O_rfcEnRx	O	LVTTL	Active high receive enable	AB16
O_rfcEnTx_n	O	LVTTL	Active low transmit enable	AA16

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Table 8: Coax AFE Interface

Coax AFE (3)	Dir.	Type	Description	Ball
B_TEST[8]	IO	LVTTL	COAX_AFE_CTRL0	N22
B_TEST[9]	IO	LVTTL	COAX_AFE_CTRL1	M20
B_TEST[10]	IO	LVTTL	COAX_AFE_CTRL2	M21

Table 9 VCXO Interface

VCXO Interface (1)	Dir.	Type	Description	Ball
B_TEST[63]	IO	LVTTL	VCXO PWM	A14

Table 10: RFIC SPI Interface

RF SPI Interface (4)	Dir.	Type	Description	Ball
I_rfcSpiDI MISO	I	LVTTL	From RFIC SPI data output	Y16
O_rfcSpiDO MOSI	O	LVTTL	To RFIC SPI data input	AA17
O_rfcSpiCK	O	LVTTL	To RFIC SPI clock input	AB18
O_rfcSpiCycleRst_n	O	LVTTL	To RFIC SPI cycle reset input	AB17

Table 11: Test

Test (5)	Dir.	Type	Description	Ball
I_testMode[0]	I	LVTTL	Pullup to VDD_33	R19
I_testMode[1]	I	LVTTL	Connect to GND	U22
I_testMode[2]	I	LVTTL	Connect to GND	U21
B_testPLMClk	IO	LVTTL	Do not connect	T21
B_testMPSClk	IO	LVTTL	Do not connect	T22

Table 12: UART

UART (2)	Dir.	Type	Description	Ball
I_urtSin	I	LVTTL	Serial in	Y17
I_urtSout	O	LVTTL	Serial out	AA18

Table 13: GPIO

GPIO	Dir.	Type	Description	Ball
B_regGPIO[0]	IO	LVTTL	Coax_AFE_PRESENT_N	V20
B_regGPIO[1]	IO	LVTTL	1394_SYNC	Y22
B_regGPIO[2]	IO	LVTTL	LED/miniPCI_YELP_12	W22
B_regGPIO[3]	IO	LVTTL	LED/miniPCI_GRNP_11	V21

GPIO	Dir.	Type	Description	Ball
B_regGPIO[4]	IO	LVTTL	miniPCI_LNA_GAIN	T19
B_regGPIO[5]	IO	LVTTL	miniPCI_LNA_CH12	U20
B_regGPIO[6]	IO	LVTTL	Coax_AFE_RX_GAIN	V22
B_regGPIO[7]	IO	LVTTL	Coax_AFE_RX_CTRL	T20

Table 14: Reserved

Reserved (60)	Ball
Reserved I/Os	R20, R21, R22, P20, P21, P22, N20, N21, M22, L22, L21, K22, L20, K21, J22, J21, K20, H22, G22, H21, J20, F22, G21, H20, E22, F21, G20, E21, F20, D22, C22, D21, E20, C21, D20, B22, A22, B21, C20, D19, A21, B20, A20, C19, A19, B19, C18, B18, A18, C17, B17, A17, C16, B16, A16, C15, B15, A15, C14, B14

Table 15: Power and Ground

Power Supply	Dir.	Type	Description	Ball
VDD		P	1.2V core power	H10, H12, H14, H8, J15, K8, L15, M8, N15, R13, R15, R9
VDD_125		P	1.25V DDR SSTL2 reference	L8, P8
VDD_25L		P	2.5V LVDS IO power	W7, W8, W14
VDD_25S		P	2.5V DDR SSTL2 IO power	L4, N4, R4, U4
VDD_33		P	3.3V IO power	D5, D7, D9, D11, D13, D15, D17, E4, F19, G4, H19, J4, K19, M19, P19, V19, W17
VREF_12		P	1.2V LVDS output reference	R11

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Power Supply	Dir.	Type	Description	Ball
VSS		G	ground	D10, D12, D14, D16, D18, D4, D6, D8, E19, F4, G19, H11, H13, H15, H4, H9, J10, J11, J12, J13, J14, J19, J8, J9, K10, K11, K12, K13, K14, K15, K4, K9, L10, L11, L12, L13, L14, L19, L9, M10, M11, M12, M13, M14, M15, M4, M9, N10, N11, N12, N13, N14, N19, N8, N9, P10, P11, P12, P13, P14, P15, P4, P9, R10, R12, R14, R8, T4, U19, V4, W18, Y13, Y14, Y15, Y7, Y8
VDD_33A		P	3.3V Analog PLL power	W15
VSSA		G	Analog PLL ground	W16

Electrical Specifications

Absolute Maximum Ratings

Table 16: Absolute Maximum Ratings

Description	Value
Ambient Storage Temp	-65 to +150 C
Input Voltage	-0.3V to VDD + 0.3V

Recommended Operating Conditions

Table 17: Recommended Operating Conditions

Description	Value
Relative Humidity	< 95%
Ambient Operating Temperature	0 C to +70 C

DC Characteristics

Table 18: DC Operating Characteristics

Symbol	Parameter	Min	Typ	Max	Units
Power Supplies					
VDD	Supply voltage	1.14	1.2	1.26	V
	Operating current		1000		mA
	Quiescent current		25		mA
VDD_125	Supply voltage	1.19	1.25	1.31	V
	Operating current		13		mA
	Quiescent current		0		mA
VDD_25S	Supply voltage	2.375	2.5	2.625	V
	Operating current		100		mA
	Quiescent current		25		mA
VDD_25L	Supply voltage	2.375	2.5	2.625	V
	Operating current		60		mA
	Quiescent current		60		mA
VDD_33	Supply voltage	3.14	3.3	3.47	V
	Operating current		200		mA
	Quiescent current		2		mA
VDD_33A	Supply voltage	3.14	3.3	3.47	V
	Operating current		7		mA
	Quiescent current		0		mA
VREF_12	Supply voltage	1.14	1.2	1.26	V
	Operating current		5		mA
	Quiescent current		5		mA
PCI inputs					
VIH	Input high level	0.5* VDD_33		VDD_33	V
VIL	Input low level	-0.3		0.3* VDD_33	V
IIH	Input high current			+/-25	uA
IIL	Input low current			+/-25	uA
PCI outputs					

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Symbol	Parameter	Min	Typ	Max	Units
VOH	Output high voltage	0.9* VDD_33			V
VOL	Output low voltage			0.1* VDD_33	V
LVTTL inputs					
VIH	Input high level	2.0		VDD_33 +0.5	V
VIL	Input low level	-0.3		0.8	V
IIH	Input high current			+/-1	uA
IIL	Input low current			+/-1	uA
LVTTL outputs					
VOH	Output high voltage	VDD_33 -0.2			V
VOH	Output high voltage	VDD_33 -0.5			V
VOL	Output low voltage			0.2	V
VOL	Output low voltage		0.2	0.4	V
IOZH	High impedance output current			+/- 1	uA
IOZL	High impedance output current			+/- 1	uA
SSTL_2 inputs					
VIH (DC)	Input high level	SstlVref +0.15		sstlV+0.3	V
VIL (DC)	Input low level	-0.3		sstlVref-0.15	V
IIH	Input high current			+/-1	uA
IIL	Input low current			+/-1	uA
SSTL_2 outputs					
VOH (DC)	Output high voltage	1.74			V
VOL (DC)	Output high voltage			0.56	V
IOH (DC)	Output low voltage	-8.1			mA
IOL (DC)	Output low voltage	8.1			mA
IOZH	High impedance output current			+/- 1	uA
IOZL	High Impedance output current			+/- 1	uA
LVDS inputs					
VIN_LVDS	Input single-ended voltage	10		2400	mV

Symbol	Parameter	Min	Typ	Max	Units
VDIN_LVDS	Input differential voltage range	100		1200	mV
LVDS outputs					
VDOUT_LVDS	Output differential voltage	200	330	450	mV
VOH_LVDS	Output voltage high			1.5	V
VOL_LVDS	Output voltage low	0.9			V
VOCM_LVDS	Output common mode	1.125	1.2	1.275	V

AC Electrical Characteristics – I/O Pins

Table 19: AC Electrical Characteristics – I/O Pins

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SSTL_2 inputs						
VIH (AC)	Input high level		sstlVref +0.31			V
VIL (AC)	Input low level				sstlVref 0.31	V
SSTL_2 outputs						
VOH (AC)	Output high voltage	vc = Min sstlV = Min RS = 25 Ohms RT = 50 Ohms VTT = sstlV*0.5	Vtt +0.608			V
VOL (AC)	Output high voltage	vc = Min sstlV = Min RS = 25 Ohms RT = 50 Ohms VTT = sstlV*0.5			Vtt-0.608	V

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Control & Support Interface Timing Characteristics

As previously shown in the PL3130 functional interface diagram in Figure 1, there are data, control and support interfaces to the Baseband and MAC blocks. Each of these interfaces have specific data format and timing requirements associated with them as detailed in the following sections.

PCI Bus Timing

The following tables provide the parameters for the 33MHz and 66MHz PCI system clocks and signal timing.

Table 20: PCI Clock Timing

		66 MHz		33 MHz		
Symbol	Parameter	Min	Max	Min	Max	Units
tcyc	CLK Cycle Time	15	30	30	-	ns
thigh	CLK High Time	6		11		ns
tlow	CLK Low Time	6		11		ns
tslew	CLK Slew Rate	1	4	1	4	V/ns

Table 21: 66 MHz and 33 MHz Signal Timing Parameters

		66 MHz		33 MHz		
Symbol	Parameter	Min	Max	Min	Max	Units
tval	CLK to Signal Valid Delay bused signals	2	6	2	11	ns
tval(ptp)	CLK to Signal Valid Delay point to point signals	2	6	2	12	ns
ton	Float to Active Delay	2		2		ns
toff	Active to Float Delay		14		28	ns
tsu	Input Setup Time to CLK bused signals	4		7		ns
tsu(ptp)	Input Setup Time to CLK point to point signals	5		10,12		ns
th	Input Hold Time from CLK	0		0		ns
trst	Reset Active Time after power stable	1		1		ms

		66 MHz		33 MHz		
Symbol	Parameter	Min	Max	Min	Max	Units
trst-clk	Reset Active Time after CLK stable	100		100		µs
trst-off	Reset Active to output float delay		40		40	ns
trhfa	RST# high to first Configuration access	225		225		clocks
trhff	RST# high to first FRAME# assertion	5		5		clocks

DDR Interface Timing

The following tables define the characteristics for DDR266 memory devices.

Table 22: DDR Timing

0°C ≤ TA ≤ 70 °C; VDDQ = +2.5 V ±0.2 V; VDD_25S = +2.5 V ±0.2 V

AC Characteristics		DDR266		
Parameter	Symbol	Min	Max	Units
CK high-level width	tCH	0.45	0.55	ns
CK low-level width	tCL	0.45	0.55	ns
DQ and DM input hold time	tDH	0.5		ns
DQ and DM input setup time	tDS	0.5		ns
DQS-DQ Skew (for DQS and associated DQ signals)	tDQSQ		+0.5	ns
DQ/DQS output hold time from DQS	tQH	tHPtQHS		ns

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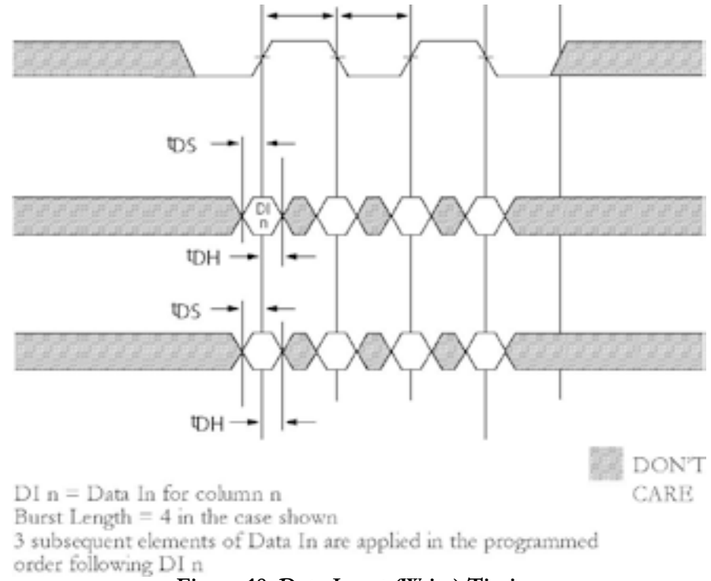

Figure 18: Data Input (Write) Timing

RFIC SPI Timing

Refer to Figure 7, SPI Write and Read timing.

Table 23: Baseband SPI Timing

Constraints relative to rising edge of O_RfcSpiCK (at 12.5MHz) are:

Signal	Parameter	Min	Max	Notes
O_rfcSpiDO	Output Valid		44.6 ns	after O_rfcSpiCK rising edge
O_rfcSpiDO	Output Hold Time	35.4 ns		after O_rfcSpiCK rising edge
I_rfcSpiDO	Input Setup	14.2 ns		before O_rfcSpiCK rising edge
O_rfcSpiCK	Period	80 ns	80 ns	

RX Input Data Timing

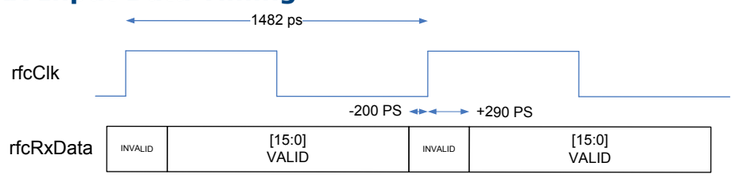

Figure 19: Rx Clock & Data Timing

TX Output Data Timing

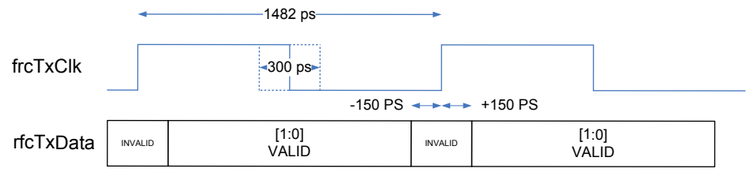

Figure 20: Tx Clock & Data Timing

Serial Flash Interface Timing

The Serial Flash Controller within the MAC provides the following features:

- The ability to access up to 16 Mbytes of serial flash memory
- Ability to boot the embedded processor and to store system information such as PCI Subsystem Vendor ID
- The ability to erase portions of or entire serial flash memory contents
- Control of any configuration settings of the serial flash
- Generation of read/write requests to an SPI-compatible serial flash
- A programmable clock frequency for SPI clock (1/2 to 1/16th MAC Bus Matrix clock)
- Data output on falling clock edge of SPI clock to meet setup and hold time requirements.

Table 24: Serial Flash Interface Timing

Signal	Parameter	Min	Max	Units	Notes
I_sfcSpiDI	Setup	8		ns	
I_sfcSpiDI	Hold	0		ns	
O_sfcSpiCK	Period	20		ns	
O_sfcSpiCS_n	Output Delay	0	1	ns	
O_sfcSpiDO	Output Delay	0	1	ns	

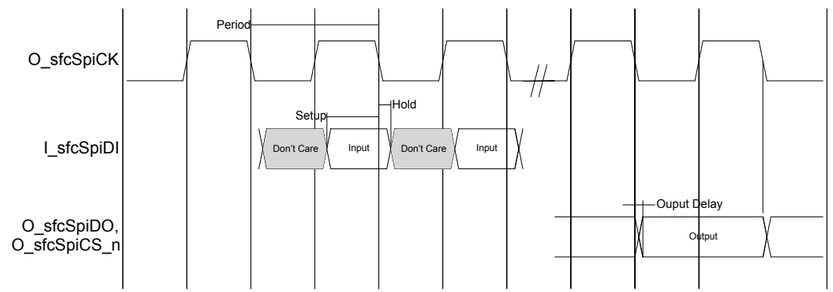

Figure 21: Serial Flash SPI Timing

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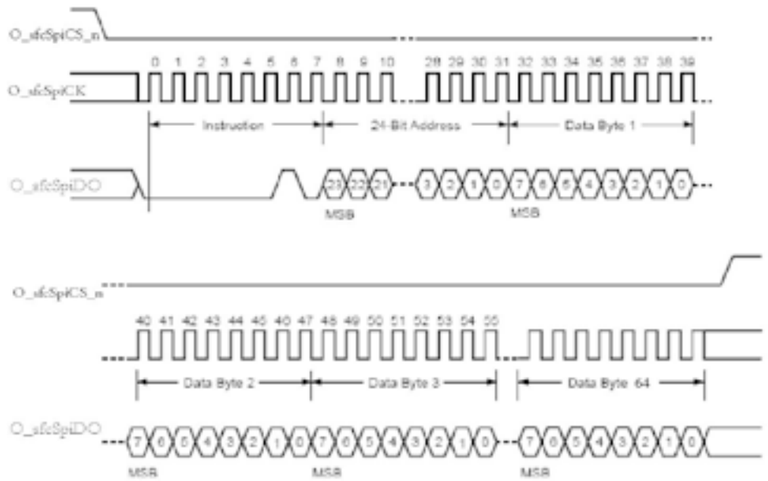

Figure 22: Fast Write Instruction Sequence

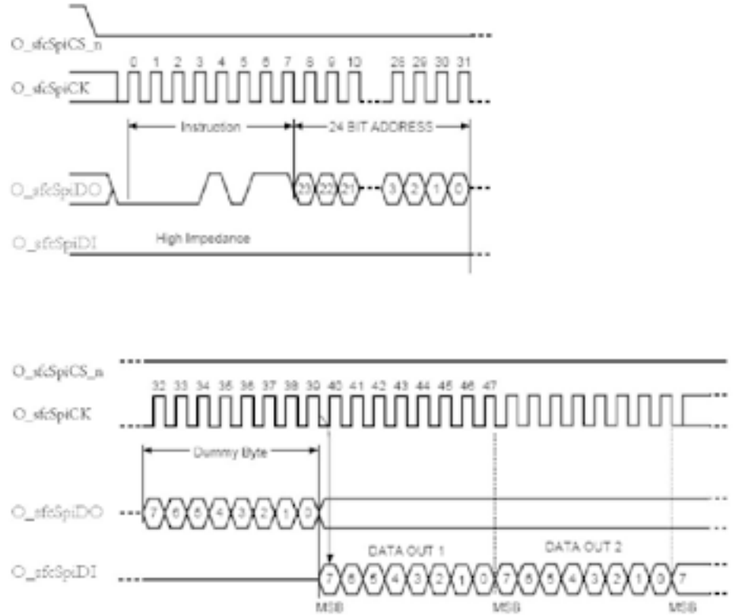

Figure 23: Fast Read Sequence

Mechanical Specifications

Table 26: BGA Package Mechanical Specifications

Area	Dimensions
Compliance	Per JEDEC MO-192
Size	23 x 23 mm
Connection Points	352 Balls
Ball Pitch	1.0 mm BSC
Nominal Thickness	1.76 mm

Package Thermal

Θ_{ja} supplied by the manufacturer.
FBGA23x23: 28 deg.C/W

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SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.58	1.76	1.94	.062	.069	.076
A1	0.40	0.50	0.60	.016	.020	.024
A2	0.51	0.56	0.61	.020	.022	.024
A3	0.67	0.70	0.73	.026	.028	.029
b	0.50	0.60	0.70	.020	.024	.028
D	22.90	23.00	23.10	.902	.906	.909
D1		21.00 BSC			.827 BSC	
E	22.90	23.00	23.10	.902	.906	.909
E1		21.00 BSC			.827 BSC	
e		1.00 BSC			.039 BSC	
f	0.90	1.00	1.10	.035	.039	.043

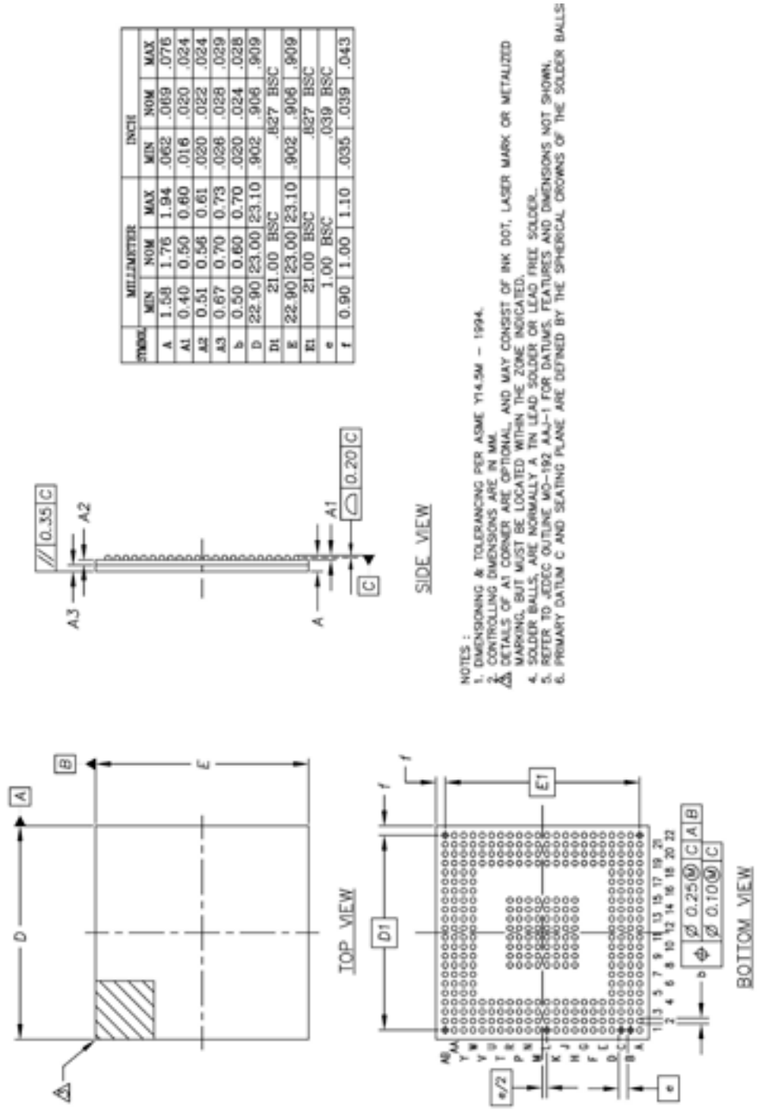

Figure 24: BGA Package Dimensions

APPENDIX

Address Map

Figure 24 shows the system address map for the PL3130 MAC

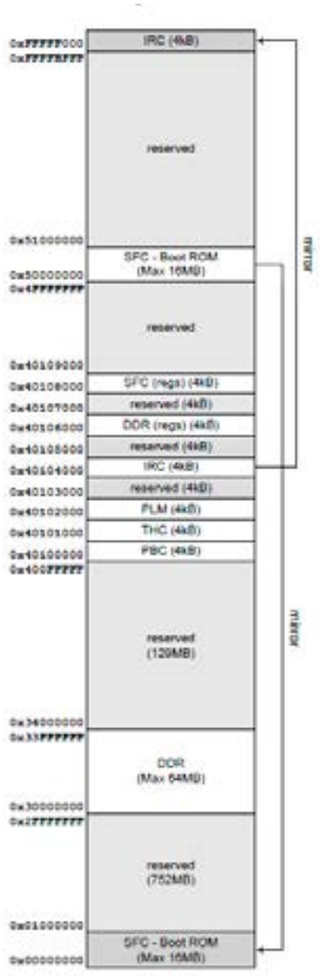

Figure 25 MAC Address Map

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Acronyms & Abbreviations

AFE	Analog Front End
APB	Auxiliary Peripheral Bus
ASIC	Application Specific Integrated Circuit
BB	Baseband
CRC	Cyclic Redundancy Check
CTA	Channel Time Allocation
CTM	Channel Time Manager
DDR	Double-Data-Rate SDRAM
DEV	802.15.3 Device
DRC	DDR Controller
EVK	Evaluation Kit
FCS	Frame Check Sequence
FEC	Forward Error Correction
HCS	Header Check Sequence
IP	Internet Protocol
IRC	Interrupt Controller
JTAG	Joint Test Action Group
LDPC	Low Parity Density Check
LNA	Low Noise Amplifier
lsb	Least Significant Bit
LSB	Least Significant Byte
MAC	Media Access Control
MISO	Master In Slave Out
MOSI	Master Out Slave In
MPP	MAC Protocol Processor
msb	Most Significant Bit
MSB	Most Significant Byte
PDU	Protocol Data Unit
PHY	Physical Layer
plcfg	MAC Control Application Utility
PLM	Physical Layer Management
PBC	PCI Bus Controller
PNC	802.15.3 Piconet Coordinator
QoS	Quality of Service
SFC	Serial FLASH Controller
SPI	Serial Peripheral Interface
TCP	Transmission Control Protocol
TDMA	Time Division Multiple Access
THC	TDMA Hardware Controller
UDP	User Datagram Protocol
UWB	Ultra-Wideband

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