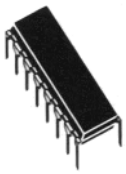
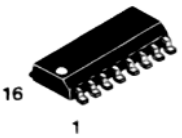
PULSE-WIDTH-MODULATION CONTROL CIRCUITS

- Complete PWM Power Control Circuitry
- Uncommitted Outputs for 200-mA Sink or Source Current
- Output Control Selects Single-Ended or Push-Pull Operation
- Internal Circuitry Prohibits Double Pulse at Either Output
- Variable Dead Time Provides Control Over Total Range
- Internal Regulator Provides a Stable 5-V Reference Supply With 5% Tolerance
- Circuit Architecture Allows Easy Synchronization

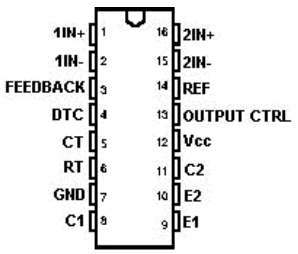
PLASTIC PACKAGE DIP-16



PLASTIC PACKAGE SO-16



PIN CONNECTIONS



(TOP VIEW)

Description

The PL494 incorporates on a single monolithic chip all the functions required in the construction of a pulse-width-modulation control circuit.
Designed primarily for power supply control, this device offers the systems engineer the flexibility to tailor the power supply control circuitry to a specific application.

The PL494 contains two error amplifiers, an on-chip adjustable oscillator, a dead-time control (DTC) comparator , a pulse-steering control flip-flop, a 5-V, 5%-precision regulator, and output-control circuits.

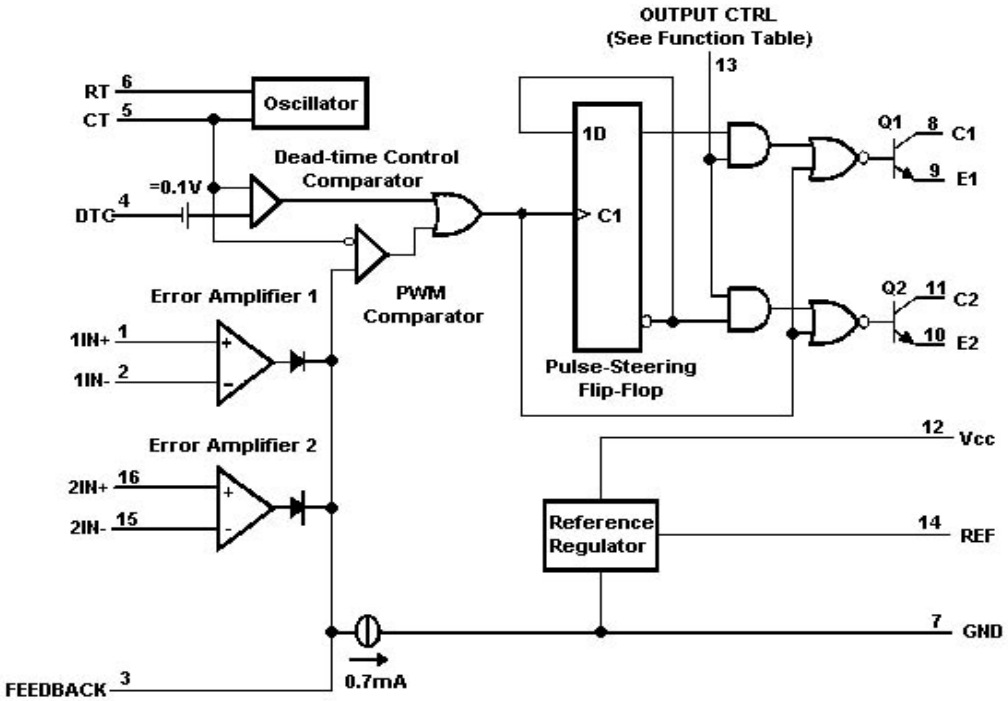
The error amplifiers exhibit a common-mode voltage range from –0.3V to Vcc –2V.
The dead-time control comparator has a fixed offset that provides approximately 5% dead time. The on-chip oscillator may be bypassed by terminating RT to the reference output and providing a sawtooth input to CT, or it may drive the common circuits in synchronous multiple-rail power supplies.

FUNCTION TABLE

INPUT TO OUTPUT CTRL	OUTPUT FUNCTION
V_I=GND	Single-ended or parallel output
V_I=V_{ref}	Normal push-pull operation

Description (continued)
The uncommitted output transistors provide either common-emitter or emitter-follower output capability. The PL494 provides for push-pull or single-ended output operation, which may be selected through the output-control function. The architecture of this device prohibits the possibility of either output being pulsed twice during push-pull operation.
The PL494CN is characterized for operation from 0°C to 70°C.

Functional block diagram



Absolute maximum rations over operating free-air temperature range (unless otherwise noted)*

	PL494CN	UNIT
Supply voltage, Vcc (see Note 1)	41	V
Amplifier input voltage, V_I	- 0.3 to + 42	V
Collector output voltage, V_0	41	V
Collector output current, I_0	250	mA
Power Dissipation T_A □ 45 □	1	W
Operating free-air temperature range, T_A	0 to 70	□
Storage temperature range, T_{stg}	- 55 to + 125	□

*Stresses beyond those listed under “absolute maximum rations” may cause permanent damage to the device. These are stress rations only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 1: All voltage values, except differential voltages, are with respect to the network ground terminal.

Recommended operating conditions

	PL494CN		UNIT
	MIN	MAX	
Supply voltage, Vcc	7	40	V
Amplifier input voltage, V_I	-0.3	Vcc -2.0	V
Collector output voltage, V_0		40	V
Collector output current, (each transistor)		200	mA
Current into feedback terminal		0.3	mA
Oscillator frequency, f_{OSC}	1	300	kHz
Timing capacitor, C_T	0.47	10000	nF
Timing resistor, R_T	1.8	500	kΩ
Operating free-air temperature, T_A	0	70	°C

Electrical characteristics over recommended operating free-air temperature range, Vcc=15V, f=10kHz (unless otherwise noted)

Reference section

PARAMETER	TEST CONDITIONS*	PL494CN			UNIT
		MIN	TVP**	MAX	
Output voltage (REF)	I_O=1mA	4.75	5	5.25	V
Input regulation	V_{CC}=7V to 40V		2	25	mV
Output regulation	I_O=1mA to 10mA		1	15	mV
Output voltage change with temperature	ΔT_A=MIN to MAX		2	10	mV/V
Short-circuit output current***	REF= 0V		25		mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
**All typical values except for parameter changes with temperature are at T_A=25°C.
***Duration of the short circuit should not exceed one second.

Oscillator section, C_T=0.01 mkF, R_T=12kΩ

PARAMETER	TEST CONDITIONS*	PL494CN			UNIT
		MIN	TVP**	MAX	
Frequency			10		kHz
Standard deviation of frequency	All values of Vcc, CT, RT,and T_A constant		100		Hz/kHz
Frequency change with voltage	Vcc=7V to 40V, TA=25°C		1		Hz/kHz
Frequency change with temperature***	ΔT_A=MIN to MAX			10	Hz/kHz

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
**All typical values except for parameter changes with temperature are at T_A=25°C.
***Temperature coefficient of timing capacitor and timing resistor not taken into account.

Error amplifier section

PARAMETER	TEST CONDITIONS	PL494CN			UNIT
		MIN	TYP*	MAX	
Input offset voltage	V_O (FEEDBACK) = 2.5V		2	10	mV
Input offset current	V_O (FEEDBACK) = 2.5V		25 250		nA
Input bias current	V_O (FEEDBACK) = 2.5V		0.2 1		mkA
Common-mode input voltage range	V_{CC} = 7V to 40V	-0.3 to V_{CC} –2			V
Open-loop voltage amplification	ΔV_O=3V, R_L=2kΩ, V_O=0.5V to 3.5V	70	95		dB
Unity-gain bandwidth	V_O=0.5V to 3.5V, R_L=2kΩ		800		kHz
Common-mode rejection ratio	ΔV_O = 40V, T_A=25°C	65	80		dB
Output sink current (FEEDBACK)	V_{ID}=-15mV to –5V, V(FEEDBACK)=0.7V	0.3	0.7		mA
Output source current (FEEDBACK)	V_{ID}=15mV to 5V, V(FEEDBACK)=3.5V	-2			mA

*All typical values except for temperature coefficient are at T_A=25°C

electrical characteristics over recommended operating free-air temperature range, V_{CC}=15V, f = 10kHz (unless otherwise noted)

Output section

PARAMETER		TEST CONDITIONS	PL494CN MIN	TYP*	MAX	UNIT
Corrector off-state current		V_{CE}=40V ,V_{CC}=40V		2	100	mkA
Emitter off-state current		V_{CC}=V_C=40V , V_E = 0			-100	mkA
Collector emitter saturation voltage	Common emitter	V_E=0, I_C =200mA		1.1	1.3	V
	Emitter follower	$V_{0\ (C1orC2)}$=15V,I_E=-200mA		1.5	2.5	
Output control input current		V_I=V_{ref}			3.5	mA

*All typical values except for temperature coefficient are at T_A=25°C

dead-time control section

PARAMETER	TEST CONDITIONS	PL494CN MIN	TYP*	MAX	UNIT
Input bias current (DEAD-TIME CTRL)	V_I =0 to 5.25V		-2	-10	nA
Maximum duty cycle, each output	V_I (DEAD-TIME CTRL) = 0, C_T=0.1mkF, R_T=12kΩ		45%		
Input threshold voltage (DEAD-TIME CTRL)	Zero duty cycle		3	3.3	V
	Maximum duty cycle	0°			

On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
*All typical values except for temperature coefficient are at T_A=25°C.

PWM comparator section

PARAMETER	TEST CONDITIONS	PL494CN MIN	TYP*	MAX	UNIT
Input threshold voltage (FEEDBACK)	Zero duty cycle		4	4.5	V
Input sink current (FEEDBACK)	V(FEEDBACK) = 0.7V	0.3	0.7		mA

*All typical values except for temperature coefficient are at T_A=25°C.

Total Device

PARAMETER	TEST CONDITIONS		PL494CN MIN	TYP*	MAX	UNIT
Standby supply current	R_T = V_{ref} All other inputs and outputs open	V_{CC} = 15V		6	10	mA
		V_{CC} = 40V		9	15	
Average supply current	V_I (DEAD-TIME CTRL) = 2V			7.5		mA

*All typical values except for temperature coefficient are at T_A=25°C.

electrical characteristics over recommended operating free-air temperature range, V_{CC}=15V, f-10kHz (unless otherwise noted) (continued)

Switching characteristics, T_A=25°C

PARAMETER	PL494CN MIN	TYP*	MAX	UNIT
Rise time		100	200	ns
Fall time		25	100	ns
Rise time		100	200	ns
Fall time		40	100	ns

*All typical values except for temperature coefficient are at T_A=25°C.

Figure 1. Representative Block Diagram

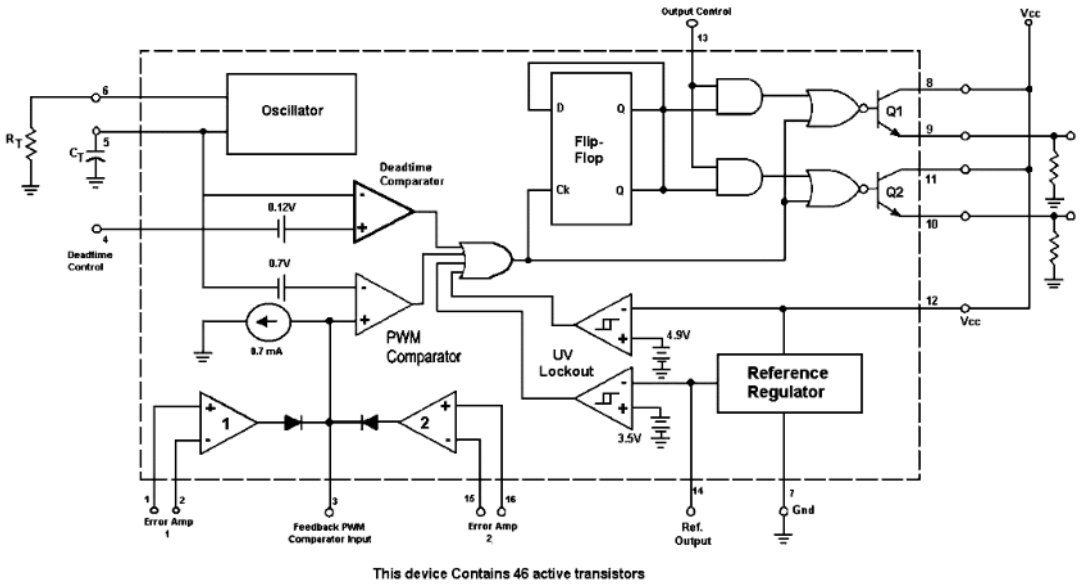
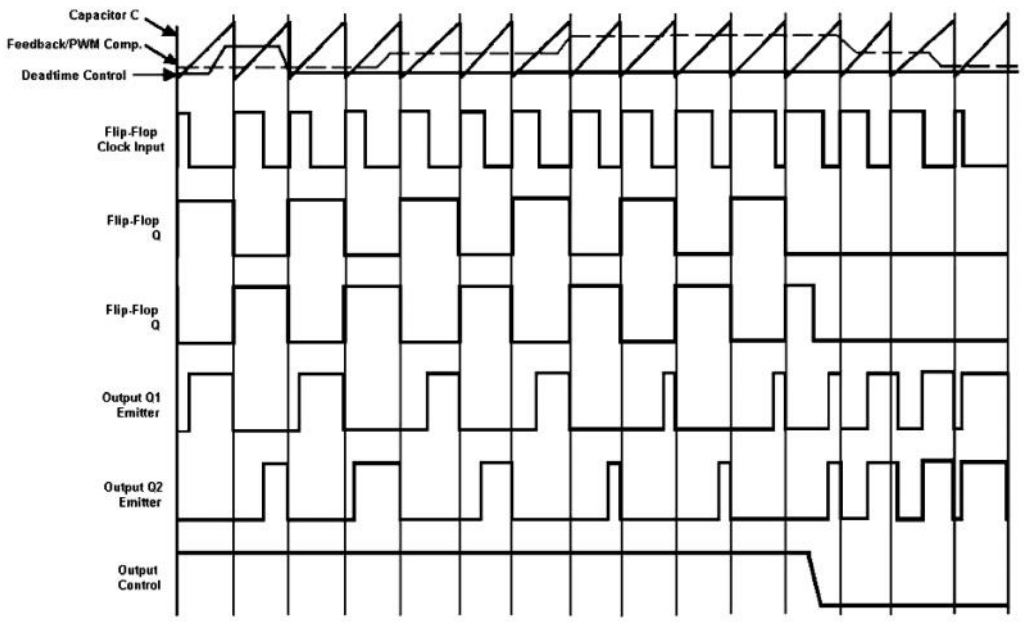


Figure 2. Timing Diagram



APPLICATIONS INFORMATION

Description

The PL494CN is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure1.) An internal-linear sawtooth oscillator is frequency-programmable by two external components. R_T and C_T. The Approximate oscillator frequency is determined by:

$$f_{osc} \approx \frac{1.1}{R_T \cdot C_T}$$

For more information refer to Figure 3.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The NOR gates, which drive output transistors Q1and Q2, are enabled only when the flip-flop clock-input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the Timing Diagram shown in Figure2.)

The Control signals are external inputs that can be fed into the deadtime control, the error amplifier inputs, or the feedback input. The deadtime control comparator has an effective 120 mV input offset which limits the minimum output deadtime to approximately the first 4% of the sawtooth-cycle time. This would result in a maximum duty cycle on a given output of 96% with the output control grounded, and 48% with it connected to the reference line. Additional deadtime may be imposed on the output by setting the deadtime-control input to a fixed voltage, ranging between 0 V to 3.3 V.

Functional Table

Input/Output Controls	Output Function	$\frac{f_{out}}{f_{osc}}$ =
Grounded	Single-ended PWM @ Q1 and Q2	1.0
@ Vref	Push-pull Operation	0.5

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the deadtime control input, down to zero, as the voltage at the feedback pin varies from 0.5 V to 3.5 V. Both error amplifiers have a common mode input range from -0.3 V to (Vcc - 2V), and may be used to sense power-supply output voltage and current. The error-amplifier outputs are active high and are ORed together at the noninverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

When capacitor C_T is discharged, a positive pulse is generated on the output of the deadtime comparator, which clocks the pulse-steering flip-flop and inhibits the output transistor, Q1 and Q2. With the output-control connected to the reference line, the pulse-steering flip-flop directs the modulated pulses to each of the two output transistors equal to half that of the oscillator. Output drive can also be taken from Q1 or Q2, when sinle-ended operation with a maximum on-time of less than 50% is required. This is desirable when the output transformer has a ringback winding with a catch diode used for snubbing. When higher operation, Q1 and Q2 may be connected in parallel, and the output-mode pin must be tied to ground to disable the flip-flop. The output frequency will now be equal to that of the oscillator.

The PL494CN has an internal 5.0 V reference capable of sourcing up to 10 mA of load current for external bias circuits. The reference has an internal accuracy of ±5.0% with a typical thermal drift of less than 50 mV over an operating temperature range of 0°to 70□.

Figure 3. Oscillator Frequency versus Timing Resistance

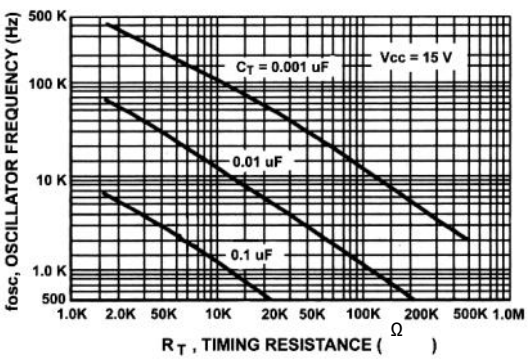


Figure 4. Open Loop Voltage Gain and Phase versus Frequency

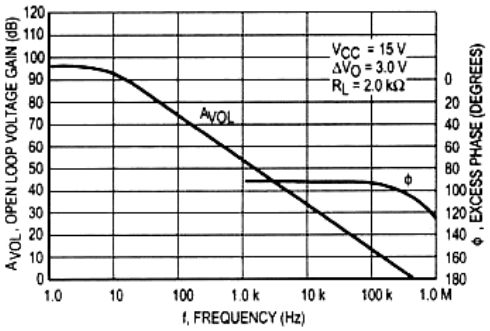


Figure 5. Percent Deadtime versus Oscillator Frequency

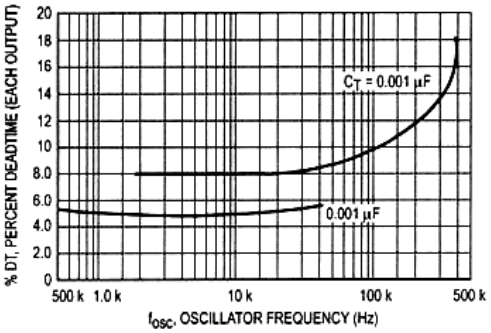


Figure 6. Percent Duty Cycle versus Deadtime Control Voltage

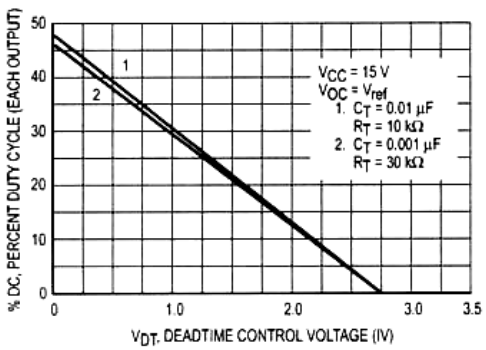


Figure 7. Emitter-Follower Configuration Output Saturation Voltage versus Emitter Current

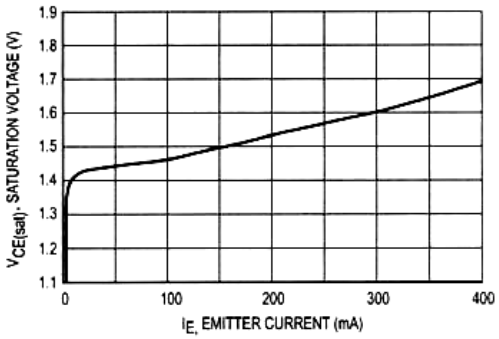


Figure 8. Common-Emitter Configuration Output Saturation Voltage versus Collector Current

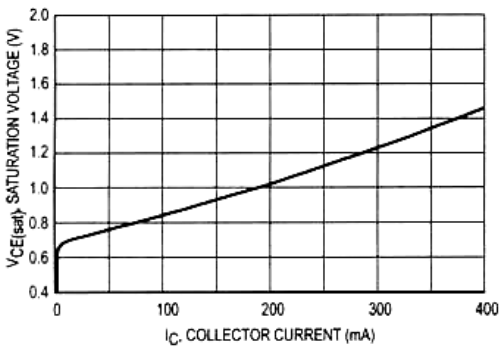


Figure 9. Standby Supply Current versus Supply Voltage

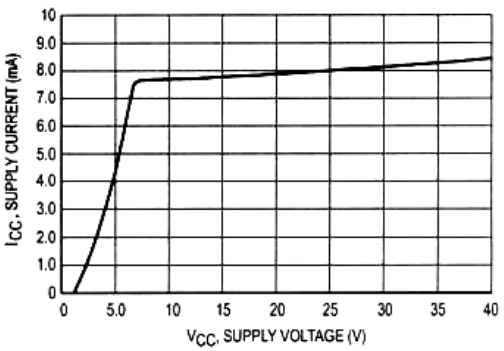


Figure 10. Error–Amplifier Characteristics

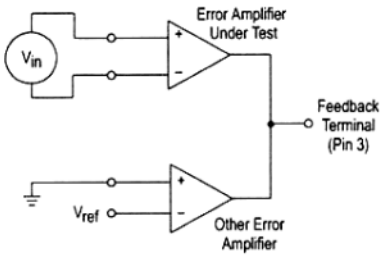


Figure 11. Deadtime and Feedback Control Circuit

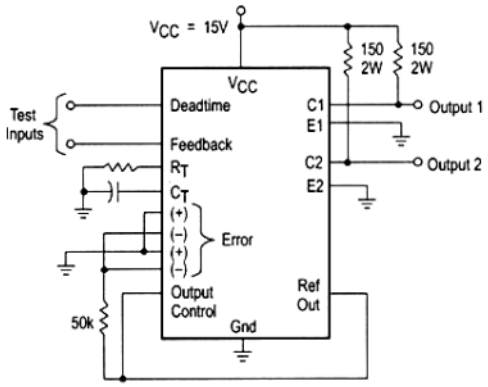


Figure 12. Common–Emitter Configuration Test Circuit and Waveform

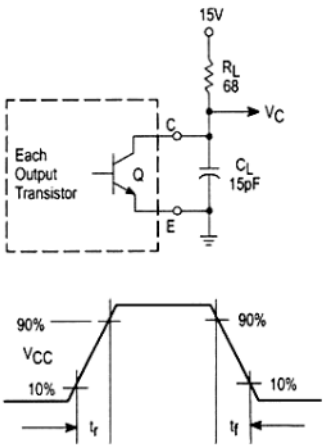


Figure 13. Emitter–Follower Configuration Test Circuit and Waveform

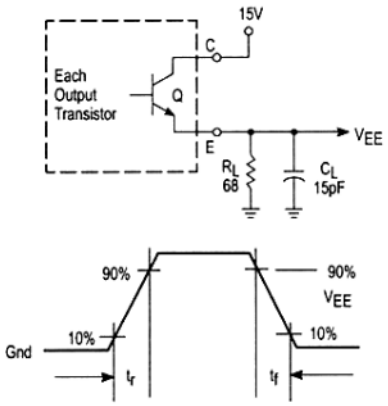
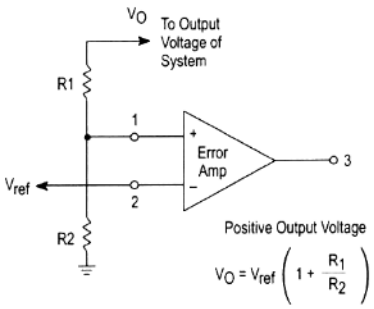


Figure 14. Error–Amplifier Sensing Techniques



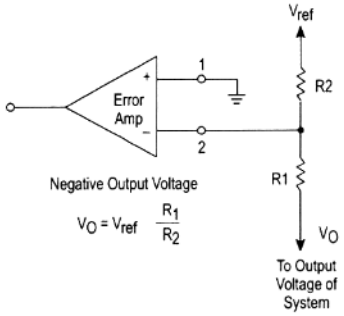
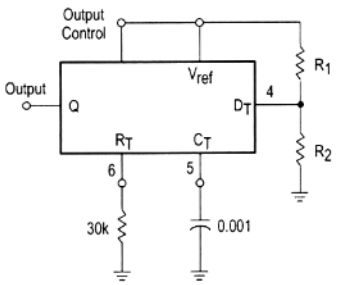


Figure 15. Deadtime Control Circuit



Max. % on Time, each output = $45 - \left(\frac{80}{1 + \frac{R1}{R2}} \right)$

Figure 16. Soft–Start Circuit

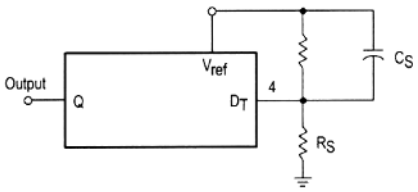
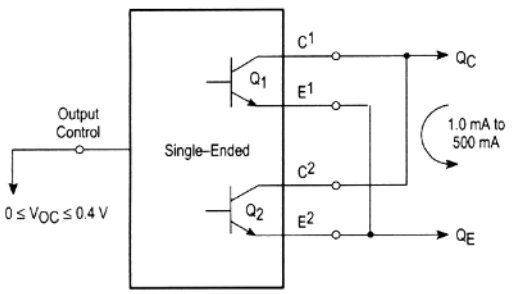


Figure 17. Output Connections for Single–Ended and Push–Pull Configurations



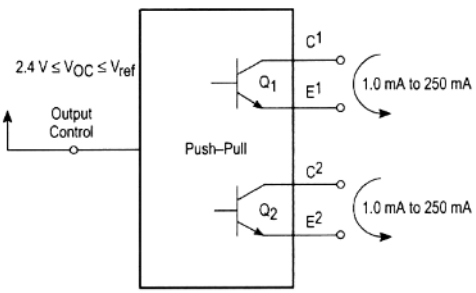


Figure 18. Slaving Two or More Control Circuits

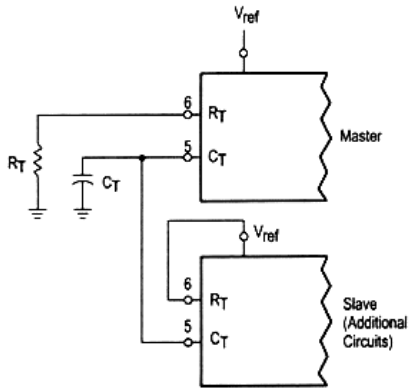


Figure 19. Operation with V_{in} > 40 V Using External Zener

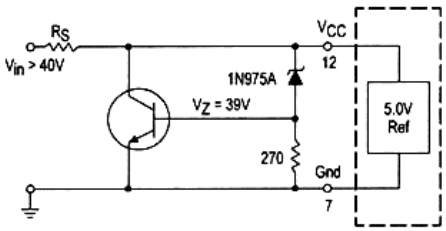
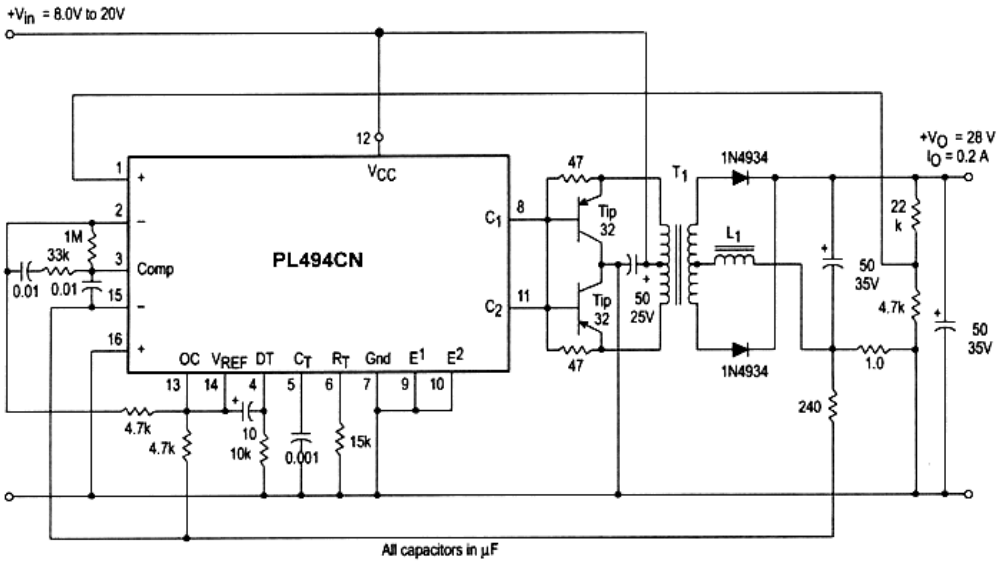


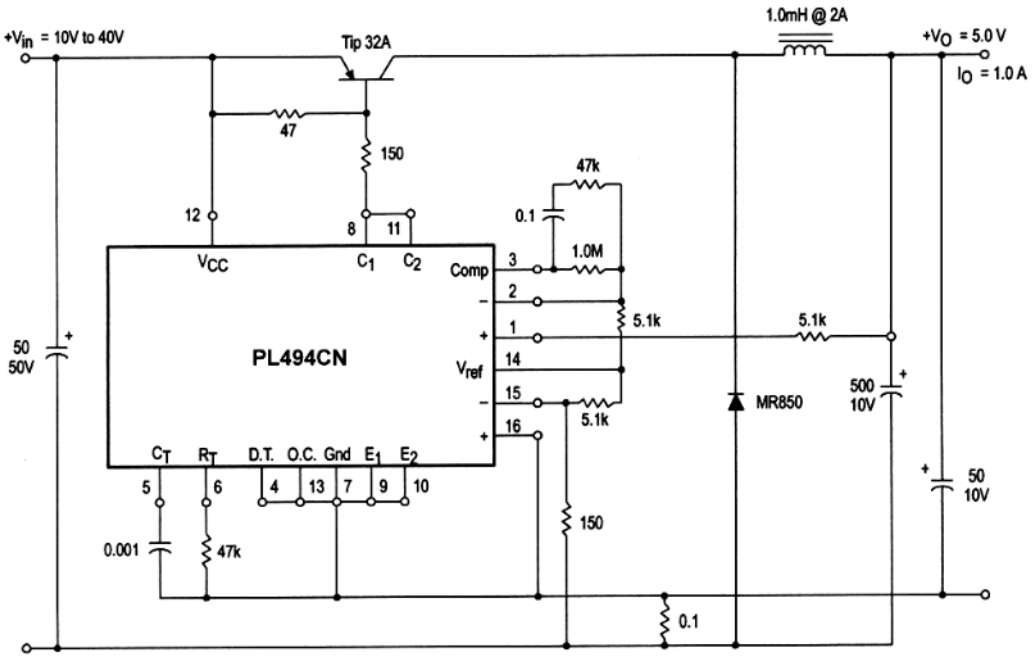
Figure 20. Pulse Width Modulated Push–Pull Converter



Test	Conditions	Results
Line Regulation	V_{in} = 10 V to 40 V	14 mV 0.28%
Load Regulation	V_{in} = 28 V, I_O = 1.0 mA to 1.0 A	3.0 mV 0.06%
Output Ripple	V_{in} = 28 V, I_O = 1.0 A	65 mV pp P.A.R.D.
Short Circuit Current	V_{in} = 28 V, R_L = 0.1 Ω	1.6 A
Efficiency	V_{in} = 28 V, I_O = 1.0 A	71%

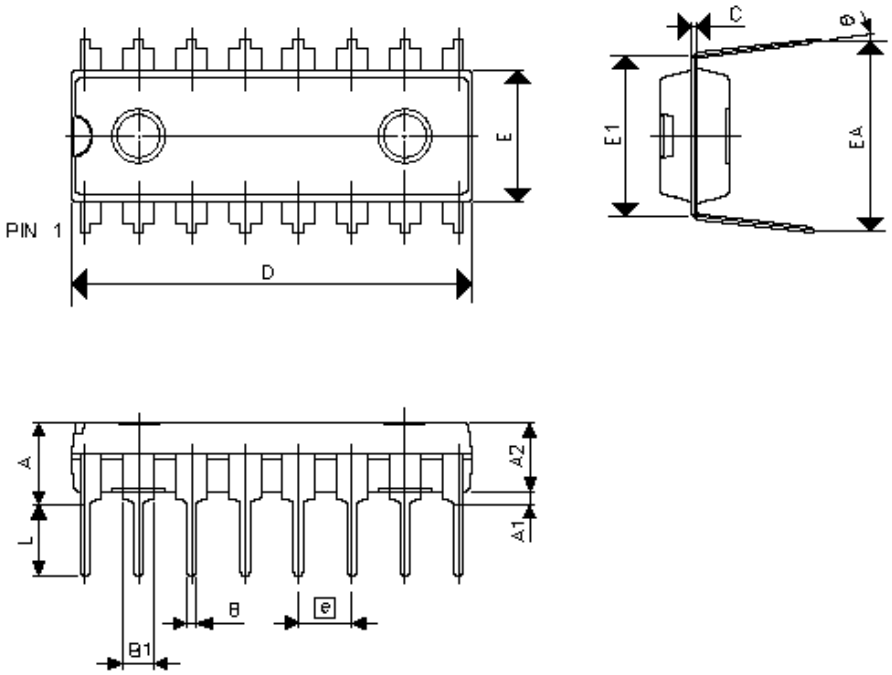
L1 – 3.5 mH @ 0.3 A
T1 – Primary: 20T C.T. #28 AWG
Secondary: 12OT C.T. #36 AWG
Core: Ferroxcube 1408P–L00–3CB

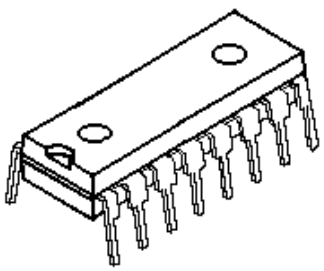
Figure 21. Pulse Width Modulated Step-Down Converter



Test	Conditions	Results
Line Regulation	Vin = 8.0V to 40V	3.0mV 0.01%
Load Regulation	Vin = 12.6V, Io = 0.2 mA to 200 mA	5.0mV 0.02%
Output Ripple	Vin = 12.6V, Io = 200 mA	40mVpp P.A.R.D.
Short Circuit Current	Vin = 12.6V, R_L = 0.1Ω	250mA
Efficiency	Vin = 12.6V, Io = 200 mA	72%

DIP-16P Dimension



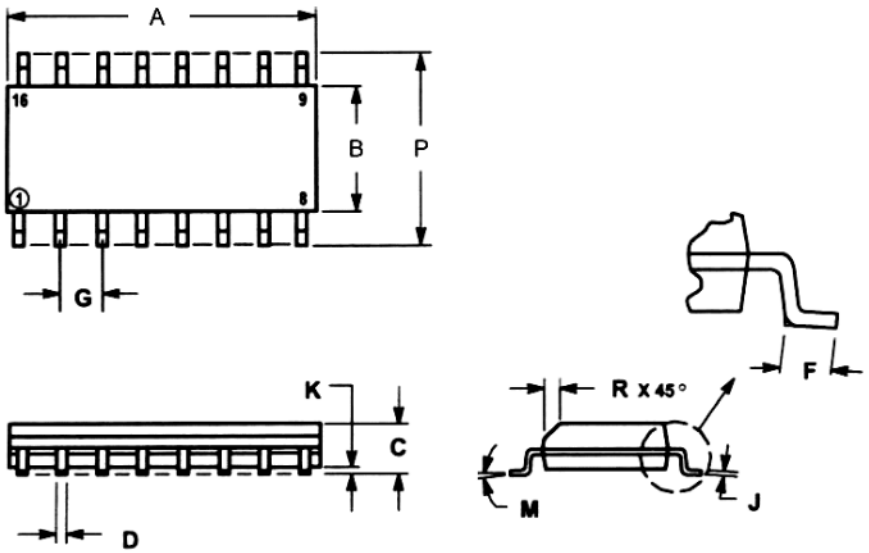


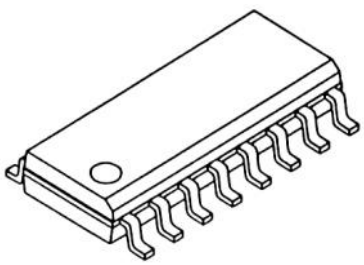
SYMBOL	DIMENSION IN INCH	DIMENSION IN MM
A	0.170 MAX.	4.318 MAX.
A1	0.015 MIN	0.381 MIN.
A2	0.130±0.005	3.302±0.127
B	0.018 TYP.	0.457 TYP.
B1	0.060 TYP.	1.524 TYP.
C	0.010 NOM.	0.254 NOM.
D	0.752±0.005	19.101±0.127
E	0.252±0.005	6.401±0.127
E1	0.300±0.010	7.62±0.254
EA	0.355±0.020	9.017±0.508
e	0.100 TYP.	2.540 TYP.
L	0.130±0.010	3.302±0.254
θ	0°~15°	0°~15°

NOTE :

1. DIMEMSION D & E DOES NOT INCLUDE FLASH.

SOP-16 Dimension





DIM	MILLIMETERS
A	9.90 ± 0.10
B	3.90 ± 0.09
C	1.60 ± 0.13
D	0.400 (REF.)
F	0.700 ± 0.20
G	1.27 (BSC.)
J	0.250
K	0.160 ± 0.08
M	0° ~ 5°
P	5.99 ± 0.20
R	0.375