# PL602-30

## 750kHz – 800MHz Low Phase Noise XO (for 12 to 25MHz Crystals)

### FEATURES

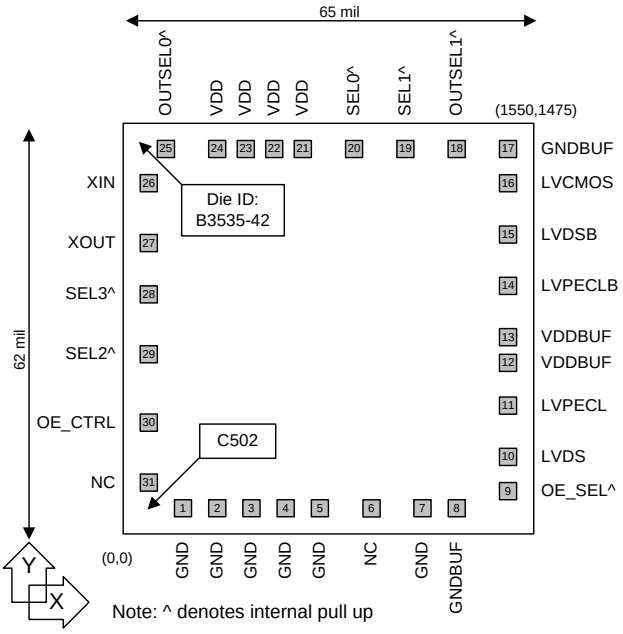
- 750kHz to 800MHz output range.
- Low phase noise output
  - -127dBc/Hz for 155.52MHz @ 10kHz offset
  - -115dBc/Hz for 622.08MHz @ 10kHz offset
- Selectable LVCMOS, LVPECL or LVDS output.
- Selectable High Drive or Standard Drive LVCMOS.
- 12MHz to 25MHz crystal input.
- No external load capacitor or varicap required.
- Output Enable selector.
- 3.3V operation.
- Available in Die form (65 mil x 62 mil).

### DESCRIPTION

The PL602-30 is a monolithic low jitter and low phase noise XO IC with LVCMOS, LVDS and LVPECL output capabilities, covering the 750kHz to 800MHz output range using a low cost 12MHz to 25MHz crystal.

This one IC can be used to produce a XO with output frequencies ranging from $F_{XIN}$ / 16 to $F_{XIN}$ x 32 thanks to the four frequency selector pads. This makes the PL602-30 ideal as a universal die for applications ranging from ADSL to SONET.

### DIE CONFIGURATION




### OUTPUT SELECTION AND ENABLE

| OUTSEL1 (Pad #18) | OUTSEL0 (Pad #25) | Selected Output |
|---|---|---|
| 0 | 0 | High Drive LVCMOS |
| 0 | 1 | Standard Drive LVCMOS |
| 1 | 0 | LVPECL |
| 1 | 1 | LVDS |

| OE_SELECT (Pad #9) | OE_CTRL (Pad #30) | State |
|---|---|---|
| 0 | 0 (Default) | Output enabled |
| | 1 | Tri-state |
| 1 (Default) | 0 | Tri-state |
| | 1 (Default) | Output enabled |

Pad #9: Bond to GND to set to "0", bond to VDD to set to "1"

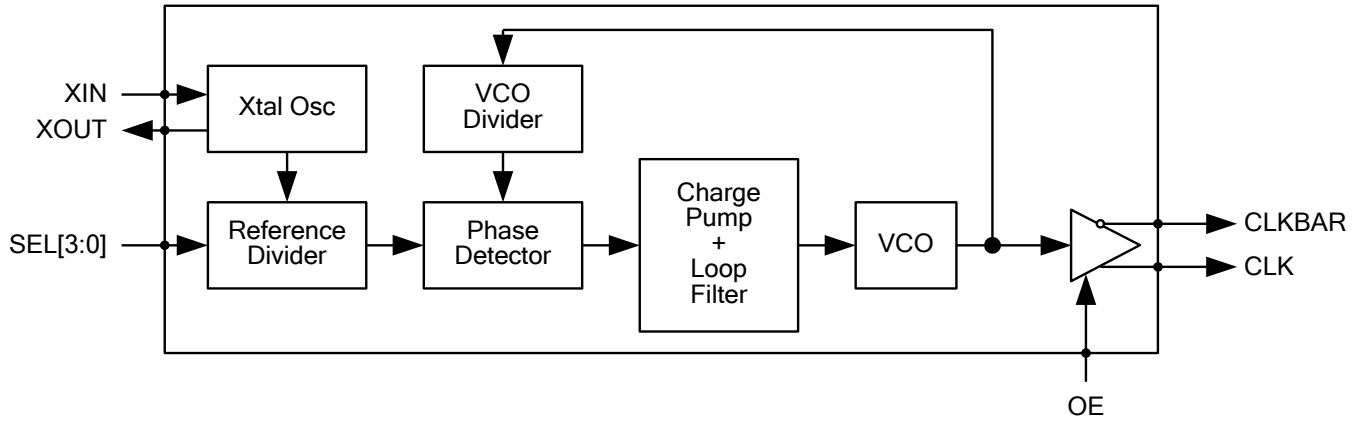
Pad #30: Logical states defined by PECL levels if OE_SELECT is "0"
Logical states defined by CMOS levels if OE_SELECT is "1"

### DIE SPECIFICATIONS

| Name | Value |
|---|---|
| Size | 62 x 65 mil |
| Reverse side | GND |
| Pad dimensions | 80 micron x 80 micron |
| Thickness | 8 mil |

## 750kHz – 800MHz Low Phase Noise XO (for 12 to 25MHz Crystals)

### BLOCK DIAGRAM




### FREQUENCY SELECTION TABLE

| SEL3 (Pad #28) | SEL2 (Pad #29) | SEL1 (Pad #19) | SEL0 (Pad #20) | Selected Multiplier |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Reserved |
| 0 | 0 | 0 | 1 | Reserved |
| 0 | 0 | 1 | 0 | Reserved |
| 0 | 0 | 1 | 1 | Fin x 32 |
| 0 | 1 | 0 | 0 | Reserved |
| 0 | 1 | 0 | 1 | Reserved |
| 0 | 1 | 1 | 0 | Fin / 8 |
| 0 | 1 | 1 | 1 | Fin x 2 |
| 1 | 0 | 0 | 0 | Reserved |
| 1 | 0 | 0 | 1 | Fin / 2 |
| 1 | 0 | 1 | 0 | Fin / 16 |
| 1 | 0 | 1 | 1 | Fin x 4 |
| 1 | 1 | 0 | 0 | Fin / 4 |
| 1 | 1 | 0 | 1 | Fin x 8 |
| 1 | 1 | 1 | 0 | Fin x 16 |
| 1 | 1 | 1 | 1 | No multiplication |

All pads have internal pull-ups (default value is 1). Bond to GND to set to 0.

# 750kHz – 800MHz Low Phase Noise XO (for 12 to 25MHz Crystals)

## ELECTRICAL SPECIFICATIONS

### 1. Absolute Maximum Ratings

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | 4.6 | V |
| Input Voltage, dc | $V_I$ | -0.5 | $V_{DD}$+0.5 | V |
| Output Voltage, dc | $V_O$ | -0.5 | $V_{DD}$+0.5 | V |
| Storage Temperature | $T_S$ | -65 | 150 | °C |
| Ambient Operating Temperature* | $T_A$ | -40 | 85 | °C |
| Junction Temperature | $T_J$ | | 125 | °C |
| Lead Temperature (soldering, 10s) | | | 260 | °C |
| ESD Protection, Human Body Model | | 2.5 | | kV |

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

### 2. Crystal Specifications

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| Crystal Resonator Frequency | $F_{XIN}$ | Parallel Fundamental Mode | 12 | | 25 | MHz |
| Crystal Loading Rating | $C_{L\ (xtal)}$ | | | 20 | | pF |
| Recommended ESR | $R_E$ | AT cut | | | 30 | Ω |

### 3. General Electrical Specifications

| PARAMETERS | SYMBOL | CONDITIONS | | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|---|
| Supply Current, Dynamic (with loaded outputs, 15pF) | $I_{DD}$ | LVPECL/ LVDS/ LVCMOS | Fout<24MHz | | | 60/28/15 | mA |
| | | | 24MHz<Fout<96MHz | | | 65/45/30 | |
| | | | 96MHz<Fout<700MHz | | | 100/80/40 | |
| Operating Voltage | $V_{DD}$ | | | 2.97 | | 3.63 | V |
| Output Clock Duty Cycle | | @ 50% $V_{DD}$ (LVCMOS)<br>@ 1.25V (LVDS)<br>@ $V_{DD}$ – 1.3V (LVPECL) | | 45 | 50 | 55 | % |

## 4. Jitter Specifications

| PARAMETERS | CONDITIONS | FREQUENCY | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| Period Jitter, RMS | With capacitive decoupling between $V_{DD}$ and GND. Over 10,000 cycles. | 155.52MHz | | 4.3 | | ps |
| | | 622.08MHz | | 5.0 | | |
| Period Jitter, Peak-to-Peak | With capacitive decoupling between $V_{DD}$ and GND. Over 10,000 cycles. | 155.52MHz | | 35 | | ps |
| | | 622.08MHz | | 45 | | |
| Integrated Jitter, RMS | Integrated 12 kHz to 20 MHz | 155.52MHz | | 2.4 | | ps |
| | | 622.08MHz | | 2.5 | | |

## 5. Phase Noise Specifications

| PARAMETERS | FREQUENCY | @10Hz | @100Hz | @1kHz | @10kHz | @100kHz | UNITS |
|---|---|---|---|---|---|---|---|
| Phase Noise, relative to carrier (typical) | 155.52MHz | -63 | -93 | -117 | -126 | -123 | dBc/Hz |
| | 622.08MHz | -52 | -83 | -105 | -113 | -110 | |

## 6. LVCMOS Electrical Characteristics

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| Output Drive Current (Standard Drive) | $I_{OH}$ | $V_{OH}$= $V_{DD}$-0.4V, $V_{DD}$=3.3V | 6 | | | mA |
| | $I_{OL}$ | $V_{OL}$ = 0.4V, $V_{DD}$ = 3.3V | 6 | | | mA |
| Output Drive Current (High Drive) | $I_{OH}$ | $V_{OH}$= $V_{DD}$-0.4V, $V_{DD}$=3.3V | 18 | | | mA |
| | $I_{OL}$ | $V_{OL}$ = 0.4V, $V_{DD}$ = 3.3V | 18 | | | mA |
| Output Clock Rise/Fall Time (Standard Drive) | | 0.3V ~ 3.0V with 15 pF load | | 2.4 | | ns |
| Output Clock Rise/Fall Time (High Drive) | | 0.3V ~ 3.0V with 15 pF load | | 1.2 | | |

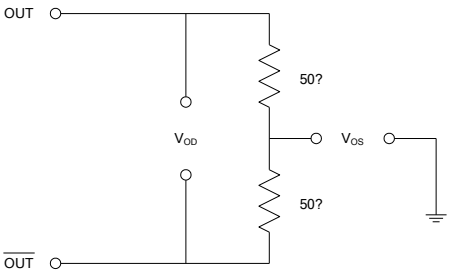
## 7. LVDS Electrical Characteristics

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| Output Differential Voltage | $V_{OD}$ | $R_L$ = 100 Ω (see figure) | 247 | 355 | 454 | mV |
| $V_{DD}$ Magnitude Change | $\Delta V_{OD}$ | | -50 | | 50 | mV |
| Output High Voltage | $V_{OH}$ | | | 1.4 | 1.6 | V |
| Output Low Voltage | $V_{OL}$ | | 0.9 | 1.1 | | V |
| Offset Voltage | $V_{OS}$ | | 1.125 | 1.2 | 1.375 | V |
| Offset Magnitude Change | $\Delta V_{OS}$ | | 0 | 3 | 25 | mV |
| Power-Off Leakage | $I_{OXD}$ | $V_{out}$ = $V_{DD}$ or GND<br>$V_{DD}$ = 0V | | ±1 | ±10 | uA |
| Output Short Circuit Current | $I_{OSD}$ | | | -5.7 | -8 | mA |

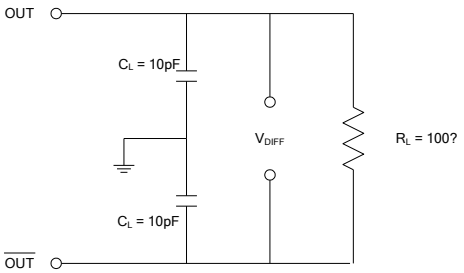
## 8. LVDS Switching Characteristics

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| Differential Clock Rise Time | $t_r$ | $R_L$ = 100 Ω<br>$C_L$ = 10 pF<br>(see figure) | | 0.7 | 1.0 | ns |
| Differential Clock Fall Time | $t_f$ | | | 0.7 | 1.0 | ns |

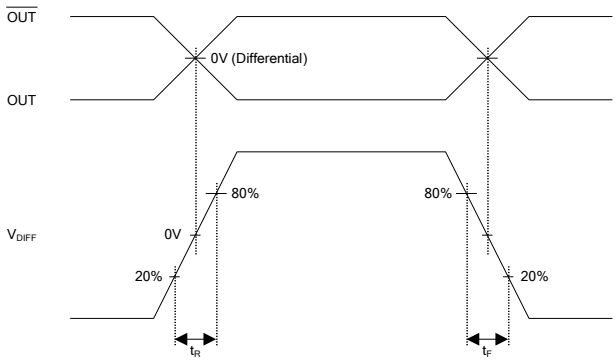
LVDS Levels Test Circuit




LVDS Switching Test Circuit




LVDS Transistion Time Waveform



# 750kHz – 800MHz Low Phase Noise XO (for 12 to 25MHz Crystals)

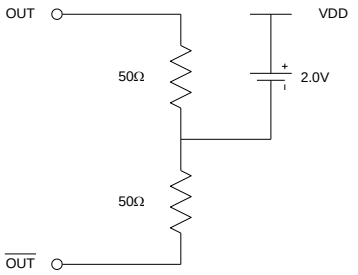
## 9. LVPECL Electrical Characteristics

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | MAX. | UNITS |
|---|---|---|---|---|---|
| Output High Voltage | $V_{OH}$ | $R_L$ = 50 Ω to ($V_{DD}$ – 2V) (see figure) | $V_{DD}$ – 1.025 | | V |
| Output Low Voltage | $V_{OL}$ | | | $V_{DD}$ – 1.620 | V |

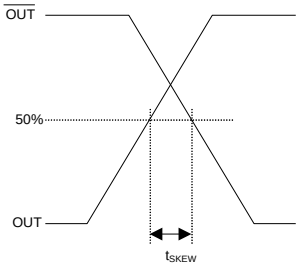
## 10. LVPECL Switching Characteristics

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| Clock Rise Time | $t_r$ | @20/80% - LVPECL | | 0.6 | 1.5 | ns |
| Clock Fall Time | $t_f$ | @80/20% - LVPECL | | 0.5 | 1.5 | ns |

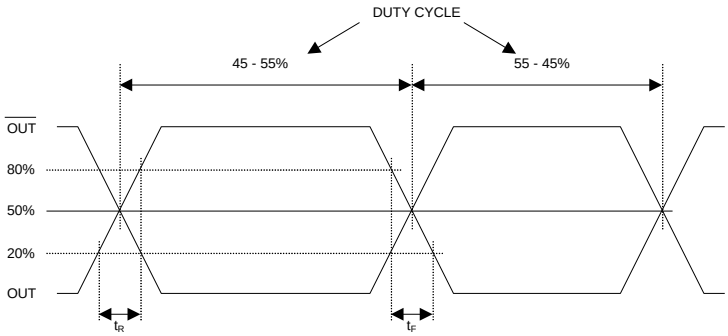
LVPECL Levels Test Circuit




LVPECL Output Skew




LVPECL Transistion Time Waveform



## 750kHz – 800MHz Low Phase Noise XO (for 12 to 25MHz Crystals)

### PAD ASSIGNMENT

| Pad # | Name | X (µm) | Y (µm) | Description |
|---|---|---|---|---|
| 1 | GND | 248 | 109 | Ground. |
| 2 | GND | 361 | 109 | Ground. |
| 3 | GND | 473 | 109 | Ground. |
| 4 | GND | 587 | 109 | Ground. |
| 5 | GND | 702 | 109 | Ground. |
| 6 | NC | 874 | 109 | No connection. |
| 7 | GND | 1042 | 109 | Ground. |
| 8 | GNDBUF | 1171 | 109 | Ground, buffer circuitry. |
| 9 | OE_SELECT | 1400 | 125 | Used to select between LVPECL or LVCMOS logic states for OE. Internal pull up. |
| 10 | LVDS | 1400 | 259 | LVDS output. |
| 11 | LVPECL | 1400 | 476 | LVPECL output. |
| 12 | VDDBUF | 1400 | 616 | 3.3V power supply, buffer circuitry. |
| 13 | VDDBUF | 1400 | 716 | 3.3V power supply, buffer circuitry. |
| 14 | LVPECLB | 1400 | 871 | Complementary LVPECL output. |
| 15 | LVDSB | 1400 | 1089 | Complementary LVDS output. |
| 16 | LVCMOS | 1400 | 1227 | LVCMOS output. |
| 17 | GNDBUF | 1389 | 1365 | Ground, buffer circuitry. |
| 18 | OUTSEL1 | 1232 | 1365 | Used to select LVCMOS, LVPECL or LVDS output type. Internal pull up. |
| 19 | SEL1 | 1042 | 1365 | Used to select multiplication factor. Internal pull up. |
| 20 | SEL0 | 854 | 1365 | Used to select multiplication factor. Internal pull up. |
| 21 | VDD | 659 | 1365 | 3.3V power supply. |
| 22 | VDD | 559 | 1365 | 3.3V power supply. |
| 23 | VDD | 459 | 1365 | 3.3V power supply. |
| 24 | VDD | 358 | 1365 | 3.3V power supply. |
| 25 | OUTSEL0 | 194 | 1365 | Used to select LVCMOS, LVPECL or LVDS output type. Internal pull up. |
| 26 | XIN | 109 | 1223 | Crystal input. See crystal specification page 3. |
| 27 | XOUT | 109 | 1017 | Crystal output. See crystal specification page 3. |
| 28 | SEL3 | 109 | 858 | Used to select multiplication factor. Internal pull up. |
| 29 | SEL2 | 109 | 646 | Used to select multiplication factor. Internal pull up. |
| 30 | OE_CTRL | 109 | 397 | Used to enable/disable the output(s). See Output Selection and Enable table on page 1. |
| 31 | NC | 109 | 181 | No connection |

# 750kHz – 800MHz Low Phase Noise XO (for 12 to 25MHz Crystals)

***For part ordering, please contact our Sales Department:***

2180 Fortune Drive, San Jose, CA 95131, USA
Tel: (408) 944-0800 Fax: (408) 474-1000

***PART NUMBER***

The order number for this device is a combination of the following:
Part Number, Package Type and Operating Temperature Range

**PL602-30 X X**

**Part Number**

**Package Type**
D=Die
W=Wafer

**Temperature**
C=Commercial (0°C to 70°C)

| Part Number/Order Number | Marking | Package Option |
|---|---|---|
| PL602-30DC | N/A | Die (Waffle Pack |
| PL602-30WC | N/A | Wafer |