PL611S-02

1.8V-3.3V PicoPLL, World's Smallest Programmable Clock

Features

- Lowest-Power, Smallest Programmable PLL
- Very Low Jitter and Phase Noise
- Output Frequency up to:
  - 110 MHz @ 1.8V Operation
  - 166 MHz @ 2.5V Operation
  - 200 MHz @ 3.3V Operation
- Input Frequency:
  - Fundamental Crystal: 10 MHz to 50 MHz
  - Reference Clock: 1 MHz to 200 MHz
- Accepts >0.1V Reference Signal Input Voltage
- One I/O Pin can be Configured as Output Enable (OE), Frequency Switching (FSEL), Power Down (PDB) Input, or CLK1 Output.
- <10 µA Current Consumption with PDB Active.
- Single 1.8V to 3.3V, ±10% Power Supply
- Operating Temperature Range from –40°C to +85°C
- Available in 6-pin DFN and SOT-23 GREEN/RoHS Compliant Packages

General Description

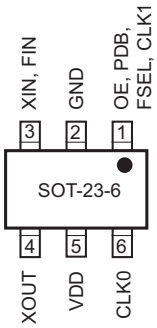
The PL611s-02 is a low-power, small form factor, high performance OTP-base programmable frequency synthesizer and a part in the PicoPLL Factory Programmable Quick Turn Clocks family.

Designed to fit in a small DFN or SOT-23 package for a broad range of applications, the PL611s-02 offers the best phase noise and jitter performance, and power consumption of its rivals. In addition, one programmable I/O pin can be configured as Output Enable (OE), Frequency Switching (F_{SEL}), Power Down (PDB) input, or CLK1 (F_{OUT}, F_{REF}, $F_{REF}/2$) output. The power down feature of PL611s-02, when activated, allows the IC to consume less than 10 µA of power, while its programming flexibility allows generating any output, up to 200 MHz using a low-cost crystal or reference input.

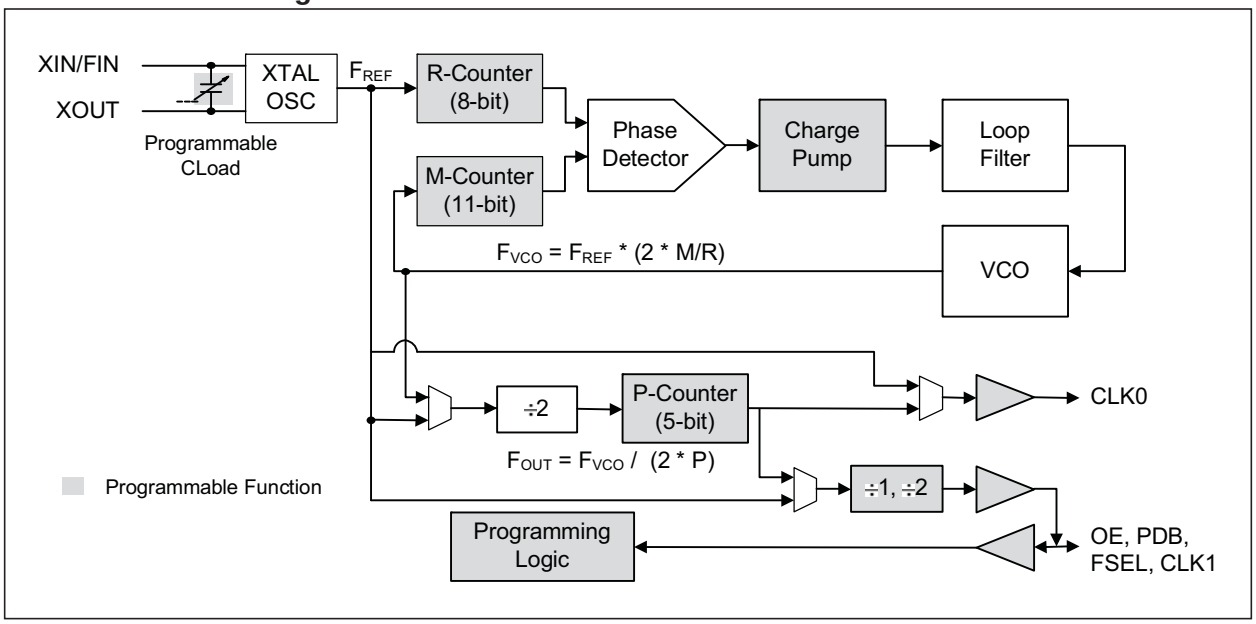
Package Types

PL611s-02
DFN
2.0x1.3
Top View

PL611s-02
SOT-23
3.0x3.0
Top View



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage Range, V_{DD} ..... –0.5V to +7.0V
Input Voltage Range, V_{IN} ..... –0.5V to V_{DD} +0.5V
Output Voltage, V_{OUT} ..... –0.5V to V_{DD} +0.5V
Data Retention @ 85°C ..... 10 Years

† **Notice:** Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

TABLE 1-1: DC SPECIFICATIONS

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Current, Dynamic	I_{DD}	—	6.0	—	mA	V_{DD} = 3.3V, 30 MHz, Load = 15 pF
		—	3.9	—		V_{DD} = 2.5V, 30 MHz, Load = 15 pF
		—	2.1	—		V_{DD} = 1.8V, 30 MHz, load = 15 pF
PLL Off: Supply Current, Dynamic	I_{DD}	—	2.0	—	mA	V_{DD} = 3.3V, 30 MHz, Load = 15 pF
		—	1.6	—		V_{DD} = 2.5V, 30 MHz, Load = 15 pF
		—	0.8	—		V_{DD} = 1.8V, 30 MHz, Load = 15 pF
Supply Current, Disabled State	I_{DD}	—	—	<10	µA	When PDB=0
Operating Voltage	V_{DD}	1.62	—	3.63	V	—
Power Supply Ramp	t_{PU}	0.05	—	100	ms	Time for V_{DD} to reach 90% V_{DD}. Power ramp must be monotonic.
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = +4 mA Standard Drive
Output High Voltage	V_{OH}	V_{DD} –0.4	—	—	V	I_{OH} = –4 mA Standard Drive
Output Current, Low Drive	I_{OSD}	4	—	—	mA	V_{OL} = 0.4V, V_{OH} = 2.4V
Output Current, Standard Drive	I_{OSD}	8	—	—	mA	V_{OL} = 0.4V, V_{OH} = 2.4V
Output Current, High Drive	I_{OHD}	16	—	—	mA	V_{OL} = 0.4V, V_{OH} = 2.4V

TABLE 1-2: AC SPECIFICATIONS

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Crystal Input Frequency (X_{IN})		10	—	50	MHz	Fundamental Crystal
Input (F_{IN}) Frequency		1	—	200	MHz	@ V_{DD} = 3.3V
		1	—	166		@ V_{DD} = 2.5V
		1	—	110		@ V_{DD} = 1.8V
Input (F_{IN}) Signal Amplitude		0.9	—	V_{DD}	V_{PP}	Internally AC coupled (High Frequency)
Input (F_{IN}) Signal Amplitude		0.1	—	V_{DD}	V_{PP}	Internally AC coupled (Low Frequency) 3.3V<50 MHz, 2.5V<40 MHz, 1.8V<15 MHz
Output Frequency		—	—	200	MHz	@ V_{DD} = 3.3V
		—	—	166		@ V_{DD} = 2.5V
		—	—	110		@ V_{DD} = 1.8V
Settling Time		—	—	2	ms	At power-up (after V_{DD} increases over 1.62V)

TABLE 1-2: AC SPECIFICATIONS (CONTINUED)

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Enable Time		—	—	10	ns	OE Function; T_A =25°C, 15 pF Load. Add one clock period to this measurement for a usable clock output.
		—	—	2	ms	PDB Function; T_A =25°C, 15 pF Load
V_{DD} Sensitivity		–2	—	2	ppm	Frequency vs. V_{DD} ±10%
Output Rise Time		—	1.2	1.7	ns	15 pF Load, 10/90% V_{DD}, High Drive, 3.3V
Output Fall Time		—	1.2	1.7	ns	15 pF Load, 90/10% V_{DD}, High Drive, 3.3V
Duty Cycle		45	50	55	%	@2.5V and 3.3V over entire frequency range, $V_{DD}/2$
		45	50	55		@1.8V, ≤ 75 MHz F_{OUT}, $V_{DD}/2$
		40	—	60		@1.8V, 75 MHz < F_{OUT} ≤ 110 MHz
Period Jitter, Pk-to-Pk (Note 1) (10,000 samples measured)		—	70	—	ps	With capacitive decoupling between V_{DD} and GND

Note 1: Jitter performance depends on the programming parameters.

TABLE 1-3: CRYSTAL SPECIFICATIONS

Parameters		Symbol	Min	Typ	Max	Units
Fundamental Crystal Resonator Frequency		F_{XIN}	10	—	50	MHz
Crystal Loading Rating (The IC can be programmed for any value in this range)		$C_{L\ (xtal)}$	8	—	12	pF
Maximum Sustainable Drive Level		—	—	—	100	µW
Operating Drive Level		—	—	30	—	µW
Metal Can Crystal	Shunt Capacitance	C0	—	—	5.5	pF
	ESR Max	ESR	—	—	50	Ω
Small SMD Crystal	Shunt Capacitance	C0	—	—	2.5	pF
	ESR Max	ESR	—	—	80	Ω

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature Range	T_S	–65	—	150	°C	—
Soldering Temperature	T_S	—	—	260	°C	Green Package
Ambient Operating Temperature Range	T_A	–40	—	85	°C	—

Note 1: Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Name	Pin Assignment		Type	Description
	SOT-23	DFN		
OE, PDB, FSEL, CLK1	1	2	I/O	This programmable I/O pin can be configured as an Output Enable (OE) input, Power Down input (PDB), On-the-Fly Frequency Switching Selector (FSEL), or CLK1 clock output This pin has an internal 60 kΩ pull up resistor for OE, PDB, and FSEL.
				State / **OE** / **PDB** / **FSEL**
				0 / Tri-State CLK / Power Down Mode / Bank 1
				1 (default) / Normal Mode / Normal Mode / Bank 2
GND	2	3	P	GND connection
XIN, FIN	3	1	I	Crystal or Reference Clock input pin
XOUT	4	6	O	Crystal Output pin. Do Not Connect (DNC) when F_{IN} is present.
VDD	5	5	P	V_{DD} connection
CLK0	6	4	O	Programmable Clock Output

TABLE 2-2: KEY PROGRAMMING PARAMETERS

CLK[0:1] Output Frequency	Output Drive Strength	Programmable Input/Output
$F_{OUT} = F_{REF} \times M / (R \times P)$ Where: M = 11 bit R = 8 bit P = 5 bit CLK0 = F_{OUT}, F_{REF} or $F_{REF}/(2\times P)$ CLK1 = F_{REF}, $F_{REF}/2$, CLK0 or CLK0/2	Three optional drive strengths to choose from: • Low: 4 mA • Std: 8 mA (default) • High: 16 mA	One output pin can be configured as: • OE - input • PDB - input • FSEL - input • CLK1 - output

3.0 FUNCTIONAL DESCRIPTION

PL611s-02 is a highly featured, very flexible, advanced programmable PLL design for high performance, low-power, small form-factor applications. The PL611s-02 accepts a fundamental input crystal of 10 MHz to 50 MHz or reference clock input of 1 MHz to 200 MHz and is capable of producing two outputs up to 200 MHz. This flexible design allows the PL611s-02 to deliver any PLL generated frequency, F_{REF} (Crystal or REF_CLK) frequency or $F_{REF}/(2\times P)$ to CLK0 and/or CLK1. The following content explains some of the design features of the PL611s-02.

3.1 PLL Programming

The PLL in the PL611s-02 is fully programmable. The PLL is equipped with an 8-bit input frequency divider (R-Counter), and an 11-bit VCO frequency feedback loop divider (M-Counter). The output of the PLL is transferred to a 5-bit post VCO divider (P-Counter). The output frequency is determined by the following formula:

EQUATION 3-1:

$$F_{OUT} = \frac{F_{REF} \times M}{R \times P}$$

3.2 Clock Output (CLK0)

CLK0 is the main clock output. The output of CLK0 can be configured as the PLL output ($F_{VCO}/(2\times P)$), F_{REF} (Crystal or REF_CLK) output, or $F_{REF}/(2\times P)$ output. The output drive level can be programmed to Low Drive (4 mA), Standard Drive (8 mA) or High Drive (16 mA). The maximum output frequency is determined by the Power Supply Voltage; 200 MHz at 3.3V, 166 MHz at 2.5V and 110 MHz at 1.8V.

3.3 Clock Output (CLK1)

The CLK1 feature allows the PL611s-02 to have an additional clock output programmed to one of the following:

- F_{REF} - Reference (Crystal or REF_CLK) Frequency
- F_{REF} / 2
- CLK0
- CLK0 / 2

3.4 Maximum VCO Frequency

For the best performance, we recommend to use the highest VCO frequency allowed at the power supply voltage where the PL611s-02 will be used. It is actually the maximum VCO frequency that determines the maximum output frequency. When a PL611s-02 is programmed for use at a certain power supply voltage, it is safe to use that part at higher voltages also because at higher voltages the maximum VCO frequency is also higher. The other way around, using the part at a lower voltage than what it was originally configured for, is not safe.

3.5 Output Enable (OE)

The Output Enable feature allows the user to enable and disable the clock output(s) by toggling the OE pin. The OE pin incorporates a 60 kΩ pull up resistor giving a default condition of logic “1”.

3.6 Power-Down Control (PDB)

The Power Down (PDB) feature allows the user to put the PL611s-02 into “Sleep Mode”. When activated (logic ‘0’), PDB disables the PLL, the oscillator circuitry, counters, and all other active circuitry. In Power Down mode the IC consumes <10 µA of power. The PDB pin incorporates a 60 kΩ pull up resistor giving a default condition of logic “1”.

3.7 Frequency Select (FSEL)

The Frequency Select (FSEL) feature allows the PL611s-02 to switch between two pre-programmed outputs allowing the device “On the Fly” frequency switching. The FSEL pin incorporates a 60 kΩ pull up resistor giving a default condition of logic “1”.

4.0 LAYOUT RECOMMENDATIONS

The following guidelines are to assist you with a performance optimized PCB design.

4.1 Signal Integrity and Termination Considerations

- Keep traces short!
- Trace = Inductor. With a capacitive load this equals ringing
- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).
- Design long traces (greater than one inch) as striplines or microstrips with defined impedance.
- Match trace at one side to avoid reflections bouncing back and forth.

4.2 Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the V_{DD} pin(s) to limit noise from the power supply
- Multiple V_{DD} pins should be decoupled separately for best performance.
- Addition of a ferrite bead in series with V_{DD} can help prevent noise from other board sources
- Value of decoupling capacitor is frequency dependent. Typical values to use are 0.1 µF for designs using frequencies < 50 MHz and 0.01 µF for designs using frequencies > 50 MHz.

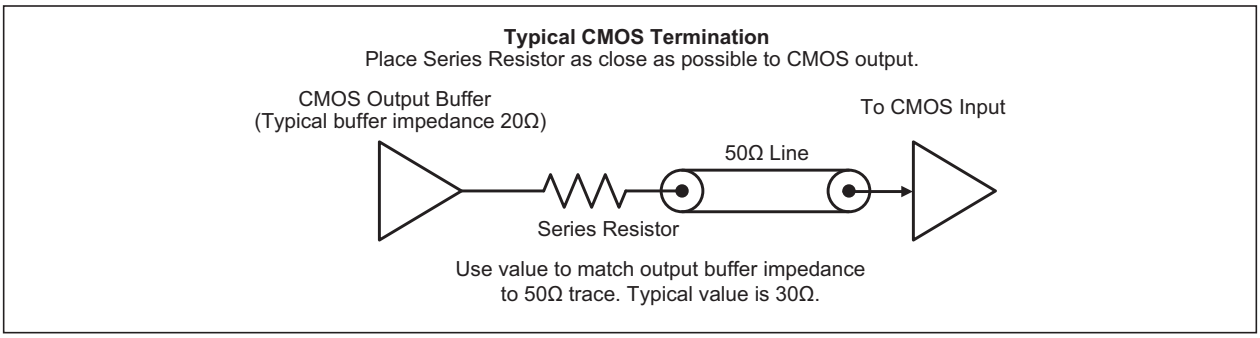


FIGURE 4-1: *Typical CMOS Termination.*

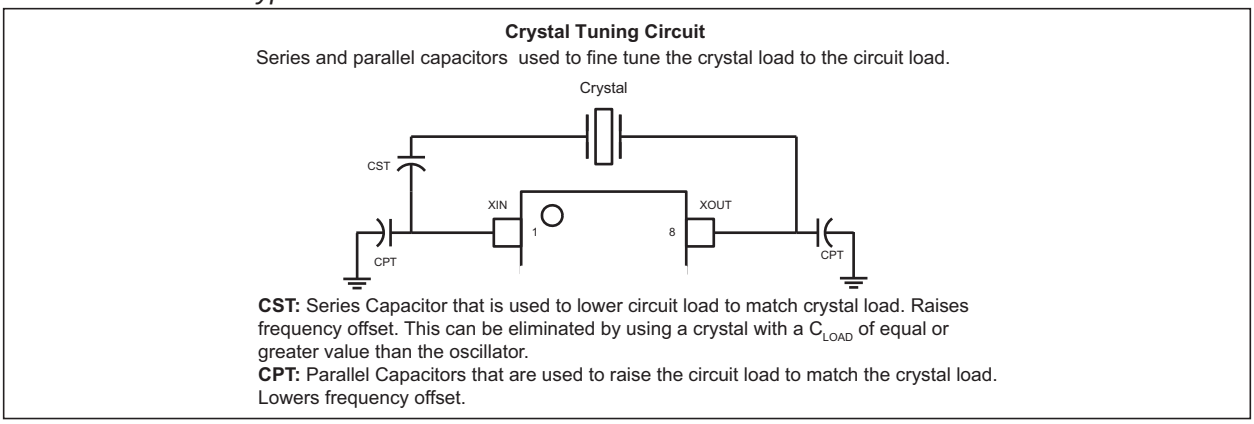
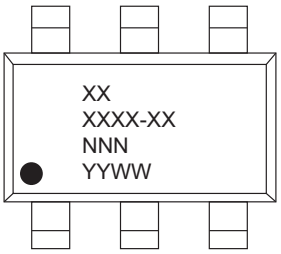
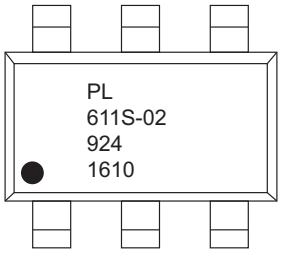


FIGURE 4-2: *Crystal Tuning Circuit.*

5.0 PACKAGING INFORMATION

5.1 Package Marking Information



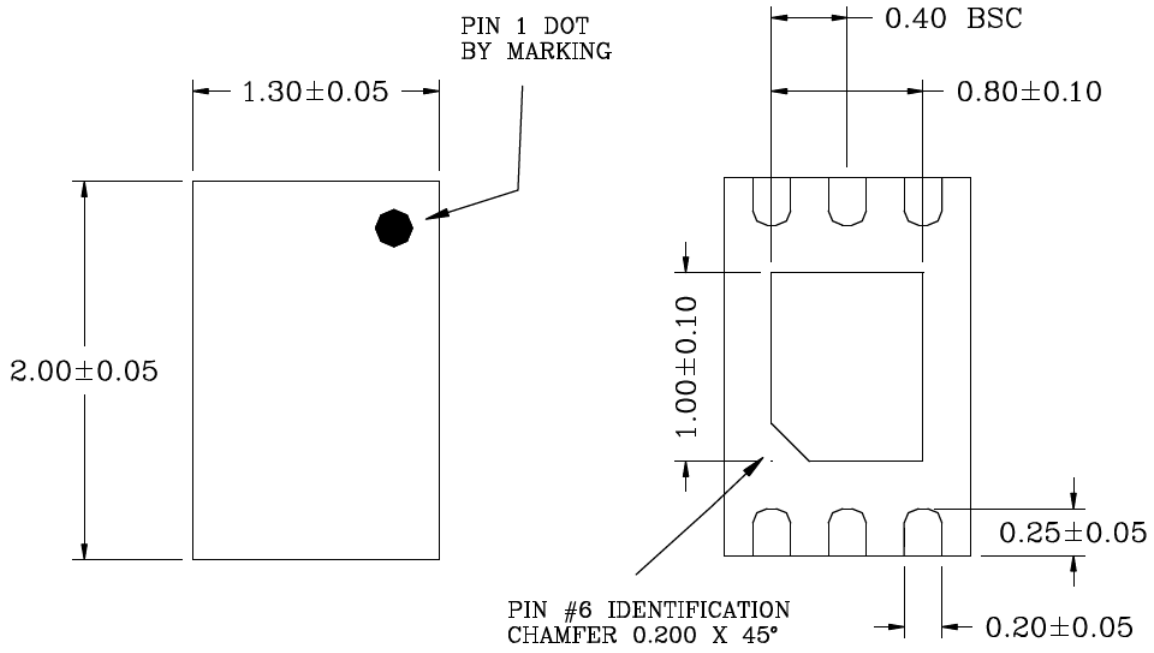


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

6-LEAD TDFN 2.0 MM × 1.3 MM PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

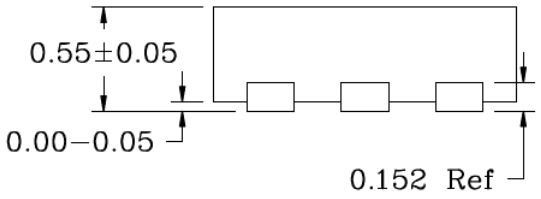
TITLE
6 LEAD TDFN 2.0x1.3 mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	TDFN2013-6LD-PL-1	**UNIT**	MM
Lead Frame	NiPdAu	**Lead Finish**	NiPdAu



TOP VIEW
NOTE: 1, 2

BOTTOM VIEW
NOTE: 1, 2



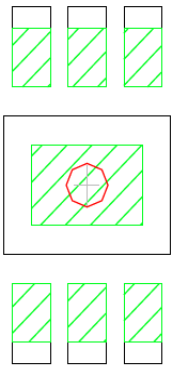
SIDE VIEW
NOTE: 1, 2

NOTES
1. MAX PACKAGE WARPAGE IS 0.05mm.
2. MAX ALLOWABLE BURR IS 0.076mmm IN ALL DIRECTIONS.
3. PIN #1 IS ON TOP WILL BE LASER MARKED.
4. UNIT IN mm.
5. SHADED AREA IS SOLDER STENCIL OPENING.
6. RECOMMENDED VIA SIZE IS 0.30-0.35mm.

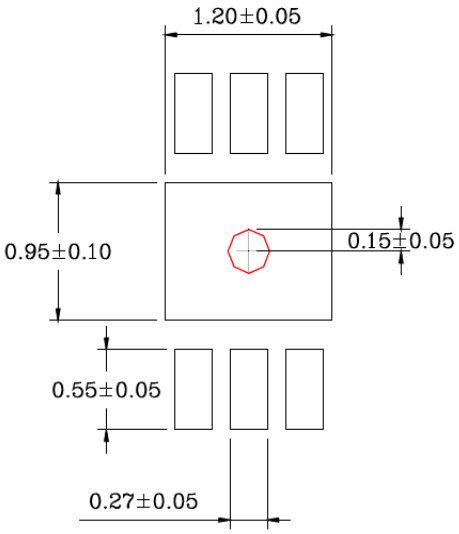
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

POD-Land Pattern TDFN2013-6LD-PL-1

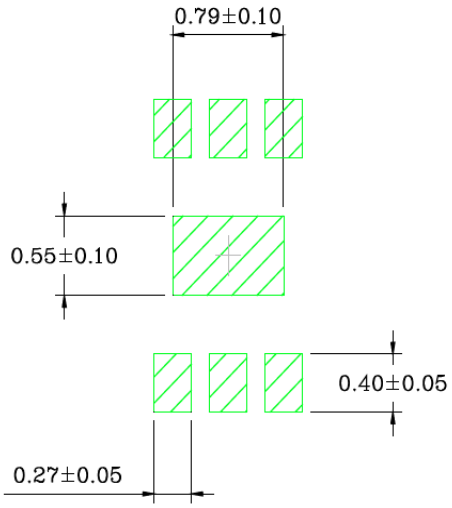
RECOMMENDED LAND PATTERN



STACKED-UP
NOTE: 4, 5, 6



EXPOSED METAL TRACE
NOTE: 4, 6



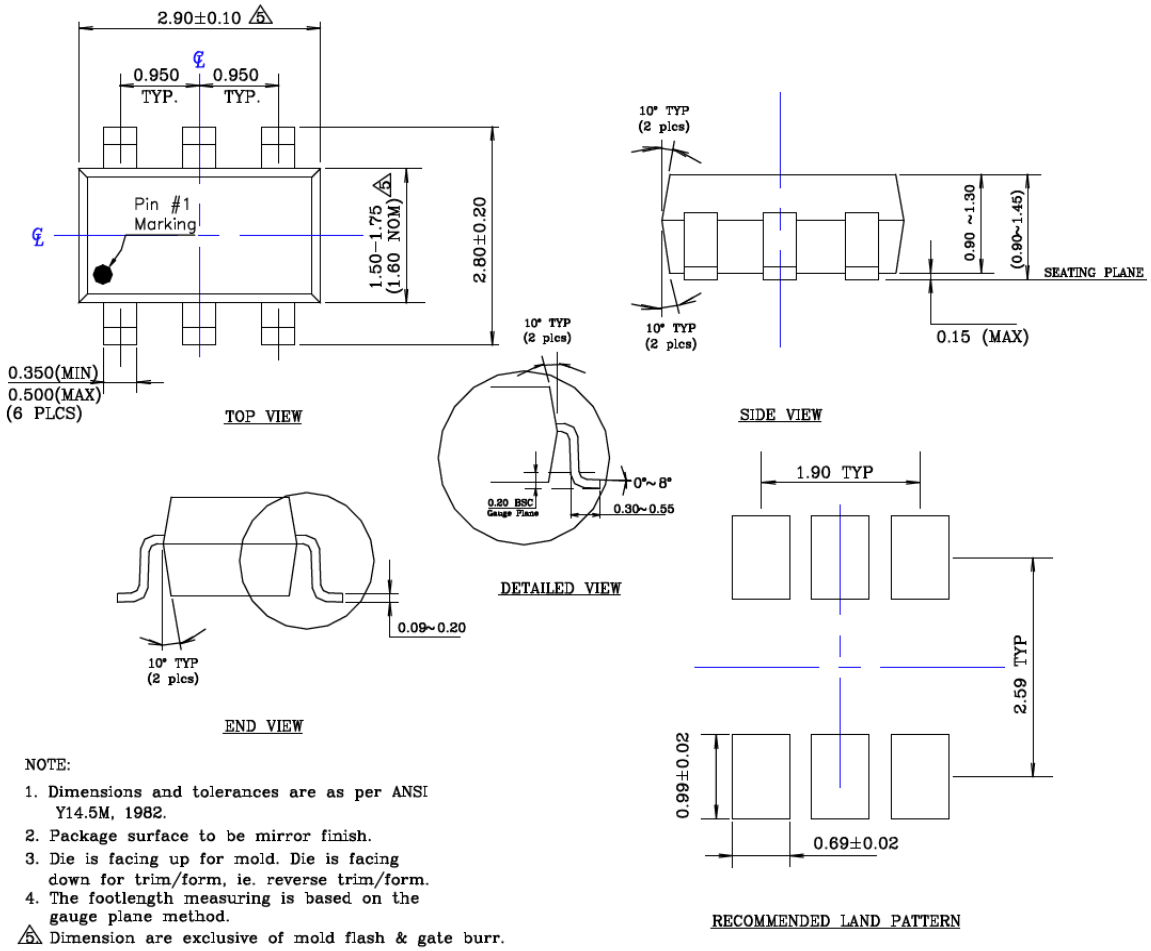
SOLDER STENCIL OPENING
NOTE: 4, 5

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

6-LEAD SOT-23 PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

TITLE
6 LEAD SOT23 PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	SOT23-6LD-PL-1	UNIT	MM



NOTE:

1. Dimensions and tolerances are as per ANSI Y14.5M, 1982.
2. Package surface to be mirror finish.
3. Die is facing up for mold. Die is facing down for trim/form, ie. reverse trim/form.
4. The footlength measuring is based on the gauge plane method.

⚠5 Dimension are exclusive of mold flash & gate burr.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

APPENDIX A: REVISION HISTORY

Revision A (November 2016)

- Converted Micrel document PL611s-02 to Microchip data sheet DS20005670A
- Minor grammatical and text changes throughout document.
- Remove TM trademark from “PicoPLL” in title and throughout document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	–	XXX	X	X	–	XX
Device		ID Code	Package Type	Temperature		Media Type

Device:	PL611s-02:		1.8V-3.3V PicoPLL, World's Smallest Programmable Clock
ID Code	XXX	=	Unique 3-digit code assigned at programming time
Package Type:	G	=	DFN-6 Lead
	T	=	SOT23-6 Lead
Temperature:	C	=	Commercial (0°C to +70°C)
	I	=	Industrial (–40°C to +85°C)
Media Type:	Blank	=	Tube
	TR	=	Tape & Reel

Examples:

a) PL611s-02-XXXGC-TR: 1.8V-3.3V PicoPLL™ Clock, Unique 3-digit programming code, DFN-6 Lead, Commercial Temperature, Tape & Reel

b) PL611s-02-XXXTC-TR: 1.8V-3.3V PicoPLL™ Clock, Unique 3-digit programming code, SOT23-6 Lead, Commercial Temperature, Tape and Reel

c) PL611s-02-XXXGI: 1.8V-3.3V PicoPLL™ Clock, Unique 3-digit programming code, DFN-6 Lead, Industrial Temperature, Tube

d) PL611s-02-XXXGI-TR: 1.8V-3.3V PicoPLL™ Clock, Unique 3-digit programming code, DFN-6 Lead, Industrial Temperature, Tape & Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
═ ISO/TS 16949 ═

Trademarks

ISBN: 978-1-5224-1079-9

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon

Hong Kong
Tel: 852-2943-5100
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115
Fax: 86-571-8792-8116

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-3326-8000
Fax: 86-21-3326-8021

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

ASIA/PACIFIC

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-3019-1500

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880- 3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

France - Saint Cloud
Tel: 33-1-30-60-70-00

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-67-3636

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7289-7561

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820