1.8V-3.3V PicoPLL™ 32K Programmable Clock

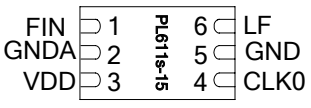
FEATURES

- Advanced Programmable PLL design for low-frequency (KHz) input applications.
- OTP selectable AC/DC Ref. Coupling.
- Accepts <1.0V reference signal input voltage
- Very low Jitter and Phase Noise (30-70ps Pk-Pk typical)
- Output frequency up to
  - 133MHz @ 1.8V operation
  - 166MHz @ 2.5V operation
  - 200MHz @ 3.3V operation
- Offered in Tiny **GREEN**/RoHS compliant packages
  - 6-pin DFN (2.0mmx1.3mmx0.6mm)
  - 6-pin SC70 (2.3mmx2.25mmx1.0mm)
  - 6-pin SOT23 (3.0mmx3.0mmx1.35mm)
- Input Frequency: 10KHz – 200MHz
- Single 1.8V, 2.5V, or 3.3V ± 10% power supply
- Operating temperature range from 0°C to 70°C

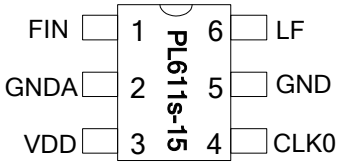
DESCRIPTION

The PL611s-15 is a low-cost general purpose frequency synthesizer and a member of PhaseLink's PicoPLL™ Factory Programmable 'Quick Turn Clock (QTC)' family. Designed to fit in a small SOT23, SC70, or DFN package for high performance applications, the PL611s-15 accepts low frequency (>10KHz) Reference input and generates up to 200MHz output with the best phase noise, jitter performance, and power consumption for handheld devices and notebook applications. Cascading PL611s-15 with other PicoPLL ICs could result in producing all required system clocks with specific savings in board space, power consumption, and cost.

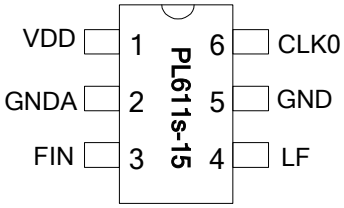
PACKAGE PIN ASSIGNMENT



DFN-6L
(2.0mmx1.3mmx0.6mm)

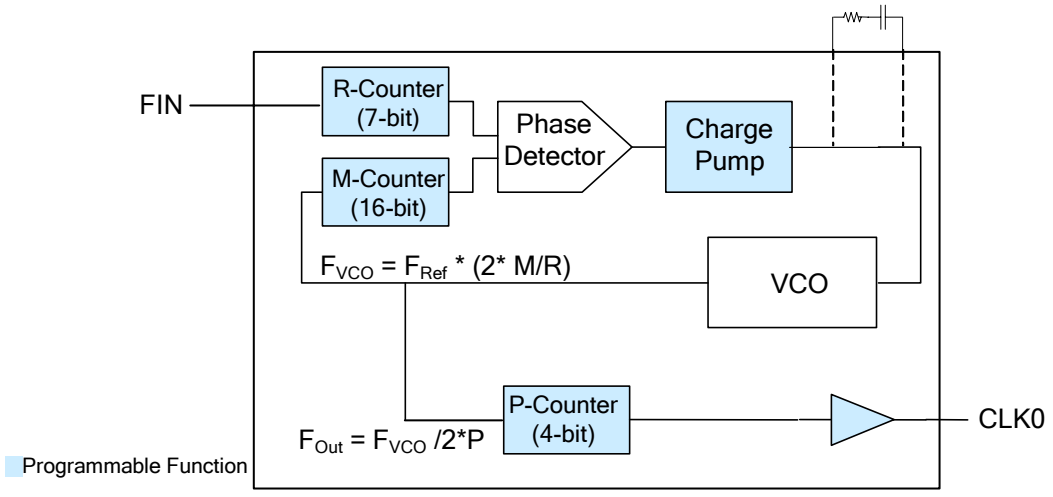


SC70-6L
(2.3mmx2.25mmx1.0mm)



SOT23-6L
(3.0mmx3.0mmx1.35mm)

BLOCK DIAGRAM



1.8V-3.3V PicoPLL™ 32K Programmable Clock

PACKAGE PIN ASSIGNMENT

Name	Pin #			Type	Description
	SOT	SC70	DFN		
VDD	1	3	3	P	VDD connection.
GNDA	2	2	2	P	Ground connection for Analog Circuitry.
FIN	3	1	1	I	Reference input pin.
LF	4	6	6	I	Loop Filter input pin.
GND	5	5	5	P	GND connection
CLK0	6	4	4	O	Programmable Clock Output

GUIDELINES FOR EXTERNAL COMPONENT SELECTION

For the optimum performance, accurate external loop filter components must be selected. A general guideline for selecting these components based on the input frequency is shown in the below table. Please contact PhaseLink for more accurate component selections.

Input frequency	Capacitor Value	Resistor Value
3MHz ~ 200MHz	4.7nF	2.2KΩ
300KHz ~ 10MHz	4.7nF	6.8KΩ
30KHz ~ 1.0MHz	4.7nF	22KΩ
10KHz ~ 100KHz	47nF	22KΩ

APPLICATION RECOMMENDATIONS FOR PL611s-15

PL611s-15 can accept a reference input >10KHz and produce a clock output in the MHz range, as shown in the diagram '1', below. However, to save costs in consumer product system designs and for greater area optimization, it is possible to use the XOUT of the RTC crystal (32.768KHz) as the reference input to the PL611s-15, as shown in diagram '2', below.

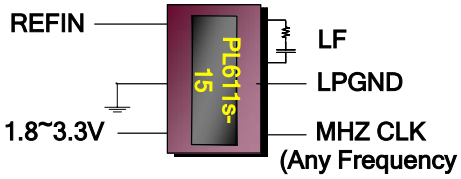


Diagram '1'

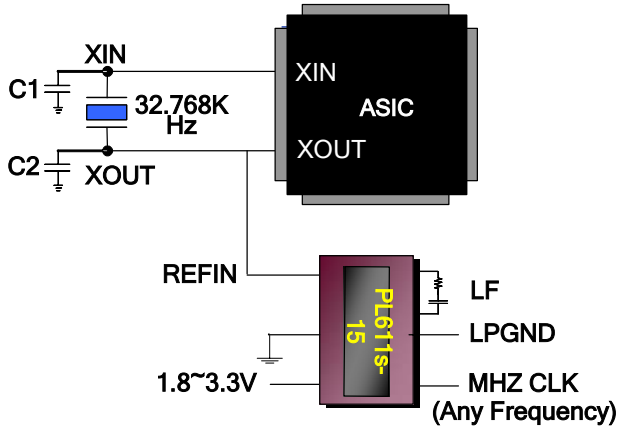


Diagram '2'

Note: An AC Coupling Cap may be required if RTC Clock amplitude is too small.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V_{DD}	-0.5	4.6	V
Input Voltage Range	V_I	-0.5	V_{DD}+0.5	V
Output Voltage Range	V_O	-0.5	V_{DD}+0.5	V
Data Retention @ 85°C		10		Year
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature		-40	85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

AC SPECIFICATIONS

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Frequency (FIN)	Reference Clock Input	10KHz		200	MHz
Output Frequency	@ Vdd=3.3V	2.5		200	MHz
Output Frequency	@ Vdd=2.5V	2.5		166	MHz
Output Frequency	@ Vdd=1.8V	2.5		133	MHz
Settling Time	At power-up (after VDD increases over 1.62V)			2	ms
Input (FIN) Signal Amplitude	Internally AC coupled	0.9		VDD	Vpp
Output Rise Time	15pF Load, 10/90%VDD, High Drive, 3.3V		1	1.2	ns
Output Fall Time	15pF Load, 90/10%VDD, High Drive, 3.3V		1	1.2	ns
Duty Cycle	VDD/2	45	50	55	%

* Note: Jitter performance depends on the programming parameters.

DC SPECIFICATIONS

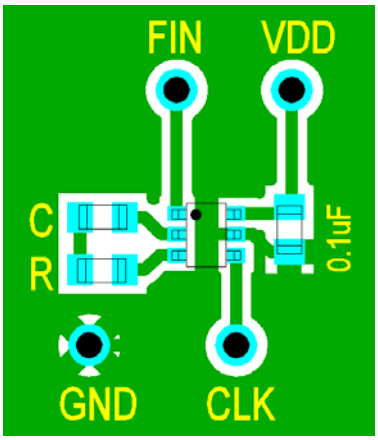
PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic, with Loaded CMOS Outputs	I_{DD}	@Vdd=3.3V,30MHz, load=15pF		6.0		mA
Supply Current, Dynamic, with Loaded CMOS Outputs	I_{DD}	@Vdd=2.5V,30MHz, load=15pF		3.9		mA
Supply Current, Dynamic with Loaded CMOS Outputs	I_{DD}	@Vdd=1.8V,30MHz, load=5pF		2.1*		mA
Operating Voltage	V_{DD}		1.62	3.3	3.63	V
Output Low Voltage	V_{OL}	I_{OL} = +4mA Standard Drive			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4mA Standard Drive	V_{DD} – 0.4			V
Output Current, Low drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V			4	mA
Output Current, Standard drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V			8	mA
Output Current, High drive	I_{OHD}	V_{OL} = 0.4V, V_{OH} = 2.4V			16	mA
Short-circuit Current	I_S			±50		mA

* Note: Please see PL611s-16 datasheet if lower power is required.

PCB LAYOUT CONSIDERATIONS FOR PERFORMANCE OPTIMIZATION

The following guidelines are to assist you with a performance optimized PCB design:

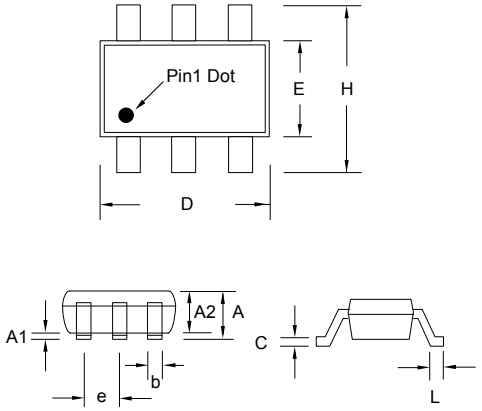
- Keep all the PCB traces to PL611s-15 as short as possible, as well as keeping all other traces as far away from it as possible.
- When a reference input clock is generated from a crystal (see diagram above), place the PL611s-15 'FIN' as close as possible to the 'Xout' crystal pin. This will reduce the cross-talk between the reference input and the other signals.
- Place the Loop Filter (LF) components as close to the package pin of PL611s-15 as possible.
- Place a 0.01µF~0.1µF decoupling capacitor between VDD and GND, on the component side of the PCB, close to the VDD pin. It is not recommended to place this component on the backside of the PCB. Going through vias will reduce the signal integrity, causing additional jitter and phase noise.
- It is highly recommended to keep the VDD and GND traces as short as possible.
- When connecting long traces (> 1 inch) to a CMOS output, it is important to design the traces as a transmission line or 'stripline', to avoid reflections or ringing. In this case, the CMOS output needs to be matched to the trace impedance. Usually 'striplines' are designed for 50Ω impedance and CMOS outputs usually have lower than 50Ω impedance so matching can be achieved by adding a resistor in series with the CMOS output pin to the 'stripline' trace.
- Please contact PhaseLink for the application note on how to design outputs driving long traces or the Gerber files for the PL611s-15 layout.



PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

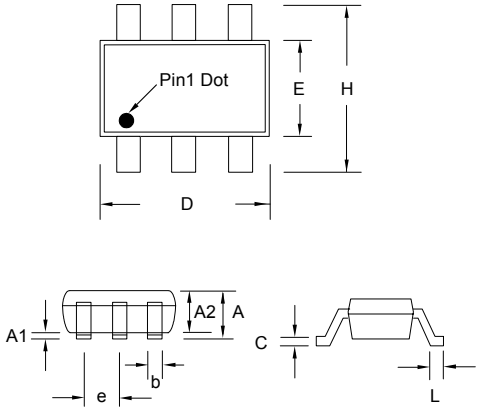
SOT23-6 L

Symbol	Dimension in MM	
	Min.	Max.
A	1.05	1.35
A1	0.05	0.15
A2	1.00	1.20
b	0.30	0.50
c	0.08	0.20
D	2.80	3.00
E	1.50	1.70
H	2.60	3.0
L	0.35	0.55
e	0.95 BSC	



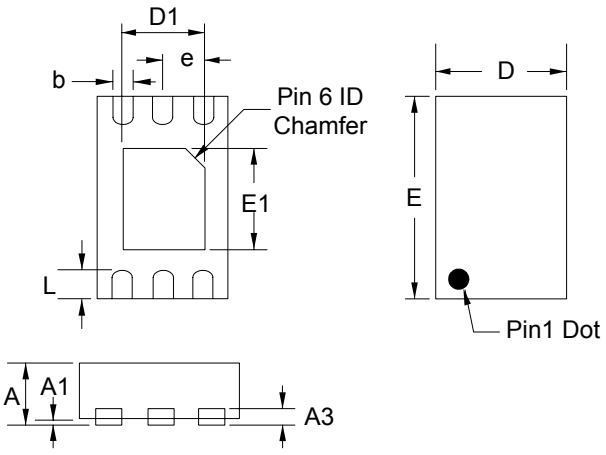
SC70-6L

Symbol	Dimension in MM	
	Min.	Max.
A	0.80	1.00
A1	0.00	0.09
A2	0.80	0.91
b	0.15	0.30
c	0.08	0.25
D	1.85	2.25
E	1.15	1.35
H	2.00	2.30
L	0.21	0.41
e	0.65BSC	



DFN-6L

Symbol	Dimension in MM	
	Min.	Max.
A	0.50	0.60
A1	0.00	0.05
A3	0.152	0.152
b	0.15	0.25
e	0.40BSC	
D	1.25	1.35
E	1.95	2.05
D1	0.75	0.85
E1	0.95	1.05
L	0.20	0.30

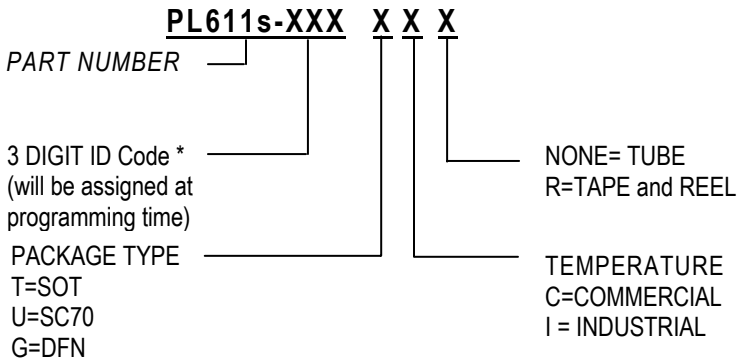


ORDERING INFORMATION (GREEN PACKAGE COMPLIANT)

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range



Part Number	Order Number	Marking†	Package Option
PL611s-XXX	PL611s-15-XXXGC-R	15XXX	6-Pin SC70 (Tape and Reel)
PL611s-XXX	PL611s-15-XXXUC-R	15XXX	6-Pin SC70 (Tape and Reel)
PL611s-XXX	PL611s-15-XXXTC-R	15XXX	6-Pin SOT-23 (Tape and Reel)

† Note: 'XXX' designates marking identifier that could be independent of the part number.