30V, 3.1A Monolithic USB Charger with QC 2.0 and Port Controller

1 Features

- 3.1A continuous output current capability
- 6.5V to 30V wide operating input range with input Over Voltage Protection
- Integrated 36V, 75mΩ high side and 36V, 57mΩ low side power MOSFET switches
- Up to 95% efficiency
- CV/CC Mode control (Constant voltage and constant current). Cycle-by-Cycle Current Limiting
- Certified QC2.0 compatible port controller
- Automatic USB charger Identification, Support Apple® Devices fast charging. (Apple® 2.4A mode). Support Samsung® Devices fast charging. Support BC1.2 & YD/T 1591-2009 charging spec
- Configurable Line Drop Compensation with resistor
- Configurable Charging Current Limit with resistor
- Internal Soft-Start limits the inrush current at turn-on
- Internal compensation to save external components
- Stable with Low ESR Ceramic Output Capacitors
- Fixed 100KHz Switching Frequency
- Input Under-Voltage Lockout.
- Input over-voltage protection to protect device from working in high voltage and high current condition
- Output Over-Voltage Protection
- Output short protection with both high side current limit and low side current limit to protect the device in hard short
- Over-Temperature Protection
- Thermally Enhanced ESOP-8 Package

2 Applications

- Quick Charge Car charger
- Portable charging device
- General purpose USB charger

3 Description

PL6320 is a monolithic USB charger with certified Qualcomm® QC2.0 interface and USB charging port controller, which can automatically detect Apple® Devices, Samsung Devices and general BC1.2 & YD/T 1591-2009 devices.

PL6320 integrates a high efficiency synchronous step-down switching regulator, which includes a 36V, 75mΩ high side and a 36V, 57mΩ low side MOSFETs to provide 3.1A continuous load current over 6.5V to 30V wide operating input voltage. Peak current mode control provides fast transient responses and cycle-by-cycle current limiting. PL6320 has configurable line drop compensation, configurable charging current limit. CC/CV mode control provides a smooth transition between constant current charging and constant voltage charging stages. Built-in soft-start prevents inrush current at power-up.

PL6320 provides a total solution for quick charge USB charging in a small ESOP8 package, which make it a best fit at narrow space applications. PL6320 is a perfect choice for single port or dual-port fast-charge car chargers.

4 Typical Application Schematic

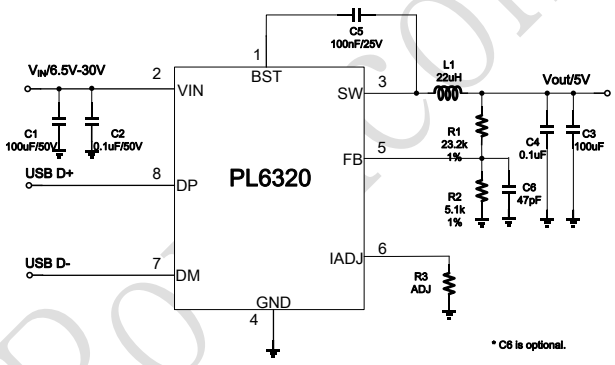


Fig. 1 Schematic

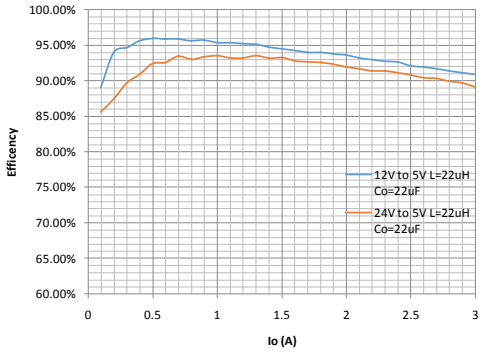
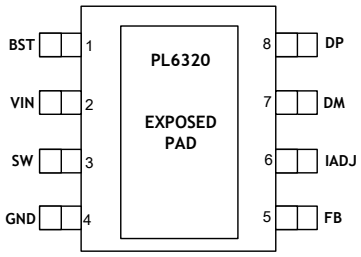


Fig. 2 Efficiency curve

5 Pin Configuration and Functions

ESOP-8 Package (Top View)



Pin-Functions

Pin		Description
Number	Name	
1	BST	Boot-Strap pin. Connect a 0.1μF or greater capacitor between SW and BST to power the high side gate driver. Minimize BST and SW loop to reduce EMI.
2	VIN	Power Input. Vin supplies the power to the IC. Supply Vin with a 6.5V to 30V power source. Bypass Vin to GND with a large capacitor and at least another 0.1uF ceramic capacitor to eliminate noise on the input to the IC. Put the capacitors, especially 0.1uF ceramic capacitor as close as possible to VIN and GND pins. Minimize 0.1uF capacitor, VIN pin, GND pin loop to reduce EMI and voltage spike on high side power device.
3	SW	Power Switching pin. Connect this pin to the switching node of inductor.
4	GND	Ground
5	FB	Feedback Input. FB senses the output voltage. Connect FB with a resistor divider connected between the output and ground. FB is a sensitive node. Keep FB away from SW and BST pin. It is better to connect a 47pF capacitor on FB pin to filter out possible coupling from other noisy node such as SW, BST, and VIN. Try to keep IADJ pin away from FB as well.
6	IADJ	Connect a resistor between IADJ and GND to configure load current limit and line drop compensation.
7	DM	USB D- pin.
8	DP	USB D+ pin

6 Device Marking Information

Part Number	Order Information	Package	Package Qty	Top Marking
PL6320	**PL6320IES08**	**ESOP-8**	**2500**	**6320 RAABB**

PL6320: Part Number
RAABB: Lot Number. R: Year; AABB: Manufacturing Code

7 Specifications

7.1 Absolute Maximum Ratings(Note1)

	PARAMETER	MIN	MAX	Unit
Input Voltages	V_{IN} to GND	-0.3	36	V
	V_{DP} to GND	-0.3	6	
	V_{DM} to GND	-0.3	6	
	V_{FB} to GND	-0.3	6	
Output Voltages	V_{IADJ} to GND	-0.3	6	V
	V_{BST} to V_{SW}	-0.3	6	
	V_{SW} to GND	-1	V_{IN}+ 0.3	

7.2 Handling Ratings

PARAMETER	DEFINITION		MIN	MAX	UNIT
T_{ST}	Storage Temperature Range		-65	150	°C
T_J	Junction Temperature			+150	°C
T_L	Lead Temperature			+260	°C
V_{ESD}	HBM Human body model	DP, DM		7	kV
		All other pins		2	
	CDM Charger device model			500	V

7.3 Recommended Operating Conditions (Note 2)

	PARAMETER	MIN	MAX	Unit
Input Voltages	V_{IN} to GND	6.5	30	V
	DP	-0.3	5	
	DM	-0.3	5	
	FB	-0.3	5	
Output Voltages	V_{OUT}	0.5	V_{IN}*D_{max}	V
Output Current	I_{OUT}	0	3.1	A
Temperature	Operating junction temperature range, T_J	-40	+125	°C

7.4 Thermal Information (Note 3)

Symbol	Description	ESOP-8	Unit
θ_{JA}	Junction to ambient thermal resistance	56	°C/W
θ_{JC}	Junction to case thermal resistance	45	

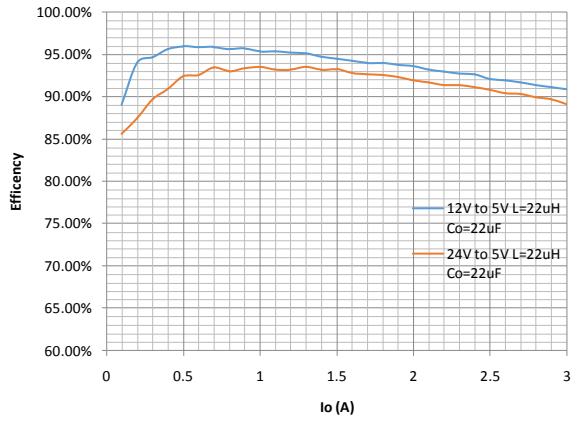
Notes:
1) Exceeding these ratings may damage the device.
2) The device function is not guaranteed outside of the recommended operating conditions.
3) Measured on approximately 1" square of 1 oz copper.

7.5 Electrical Characteristics (Typical at Vin = 12V, T_J=25°C, unless otherwise noted.)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
BUCK CONVERTER						
MOSFET						
$R_{DS(ON)\_H}$	High-Side Switch On-Resistance	I_{OUT} = 1A, V_{OUT} = 3.3V		75		mΩ
$R_{DS(ON)\_L}$	Low-Side Switch On-Resistance	I_{OUT} = 1A, V_{OUT} = 3.3V		57		mΩ
SUPPLY VOLTAGE (VIN)						
V_{UVLO_up}	Minimum input voltage for startup				6.5	V
V_{UVLO_down}				6.0		V
V_{UVLO_hys}				0.3		V
$I_{Q\text{-}NONSW}$	Operating quiescent current	V_{FB} =1.3V, DP, DM are floating		1		mA
CONTROL LOOP						
F_{oscb}	Buck oscillator frequency			100		kHz
V_{FB}	Feedback Voltage	QC 2.0 DP=3.3V, DM=0.6V		1.65		V
		QC 2.0 DP=DM=0.6V		2.20		
		Other conditions	0.89	0.90	0.92	
V_{FB_OVP}	Feedback Over-voltage Threshold			1.1* V_{FB}		V
D_{max}	Maximum Duty Cycle(Note 4)			95		%
T_{on}	Minimum On Time(Note 4)			200		ns
PROTECTION						
I_{ocl_hs}	Upper Switch Current Limit	Minimum Duty Cycle		5.5		A
I_{ocl_ls}	Lower Switch Current Limit	From Source to Drain		4.5		A
V_{inovp}	Input Over voltage protection			33		V
T_{ss}	Soft-Start Period			0.8		ms
Th_{sd}	Thermal Shutdown(Note 4)			155		°C
Th_{sdhys}	Thermal Shutdown Hysteresis(Note 4)			15		°C
T_{hicup}	Hicup period (Note 4)			3.5		ms
D_{hiccup}	Hicup duty cycle (Note 4)			20		%
USB INTERFACE CONTROLLER						
Apple® Mode						
V_{dp_app}	DP output voltage in Apple® mode			2.7		V
V_{dm_app}	DM output voltage in Apple® mode			2.7		V
R_{dp_app}	DP output impedance in Apple® mode			30		kΩ
R_{dm_app}	DM output impedance in Apple® mode			30		kΩ
Samsung Mode						
V_{dp_sam}	DP output voltage in Samsung mode			1.2		V
V_{dm_sam}	DM output voltage in Samsung mode			1.2		V
R_{dp_sam}	DP output impedance in Samsung mode			105		kΩ
R_{dm_sam}	DM output impedance in Samsung mode			105		kΩ
BC1.2 Mode						
R_{bc1p2}	DP to DM short resistance in DCP mode			30		Ω
QC 2.0 Mode						
$T_{dphighf}$	DP high glitch filter time.			1300		ms
$T_{newvdeg}$	New voltage request filter(Note 4)			40		ms
R_{leak}	Leakage resistor on DP(Note 4)			400		kΩ
R_{pd}	Pull down resistor on DM(Note 4)			20		kΩ

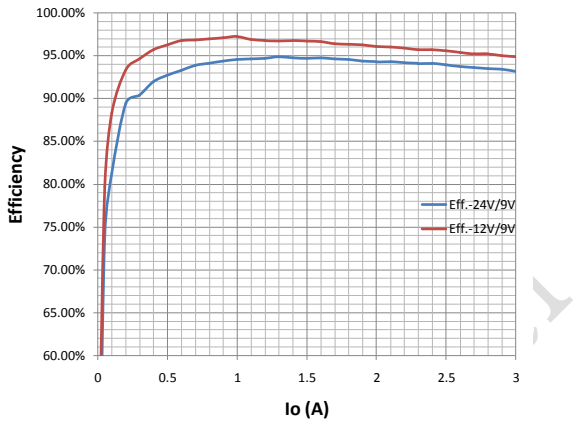
Note: 4) Guaranteed by design, not tested in production.

8 Typical Characteristics



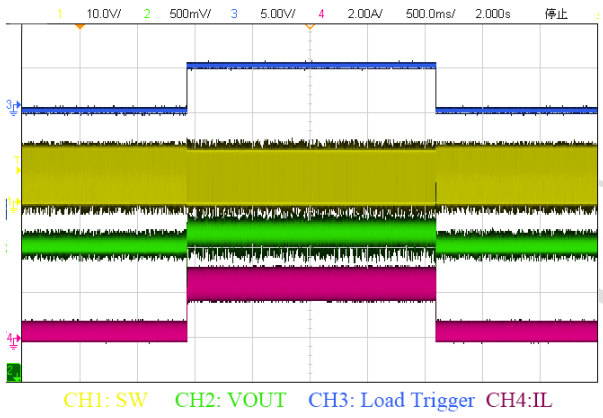
Vin = 12/24V, Vout = 5V

Fig. 3 Efficiency



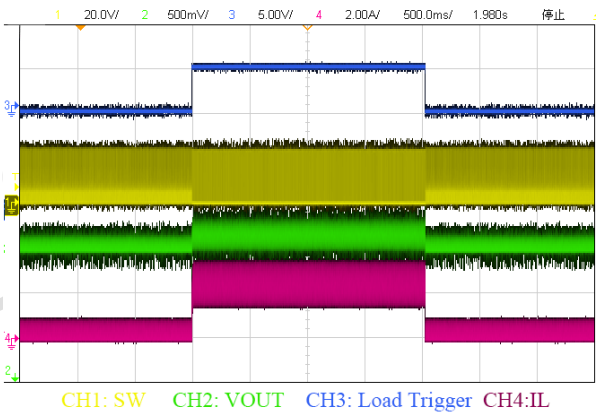
Vin = 12/24V, Vout = 9V

Fig. 4 Efficiency



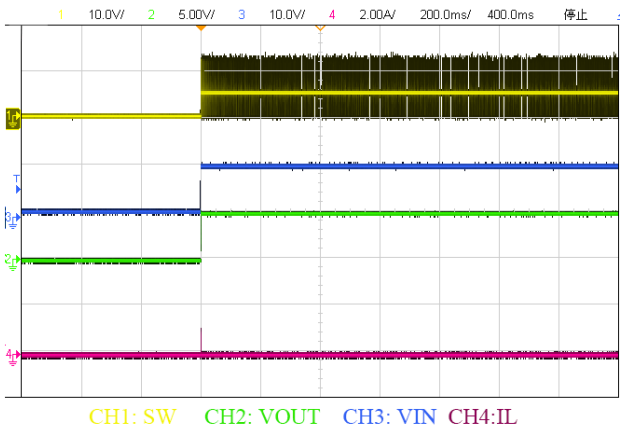
Vin = 12V, Vout = 5V

Fig. 5 Load transient 0.25A to 2.5A



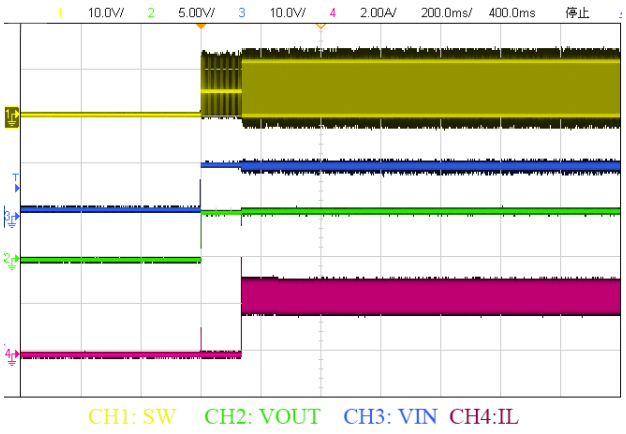
Vin = 24V, Vout = 5V

Fig. 6 Load transient 0.25A to 2.5A



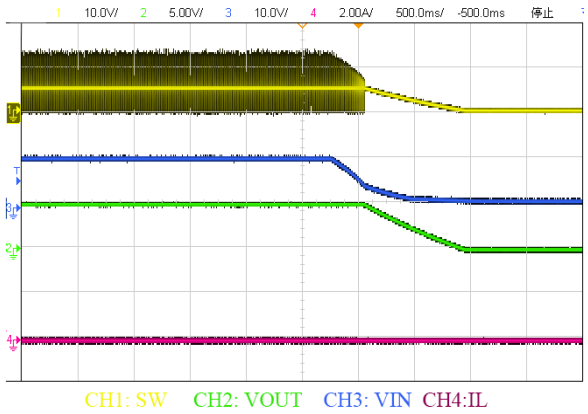
Vin = 12V, Vout = 5V

Fig. 7 Startup waveform, Iout = 0A



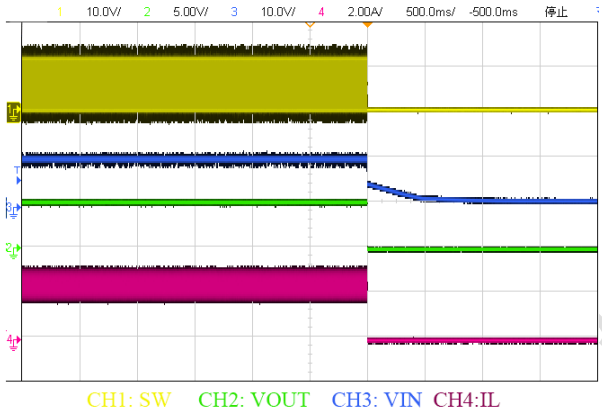
Vin = 12V, Vout = 5V

Fig. 8 Startup waveform, Iout = 3A



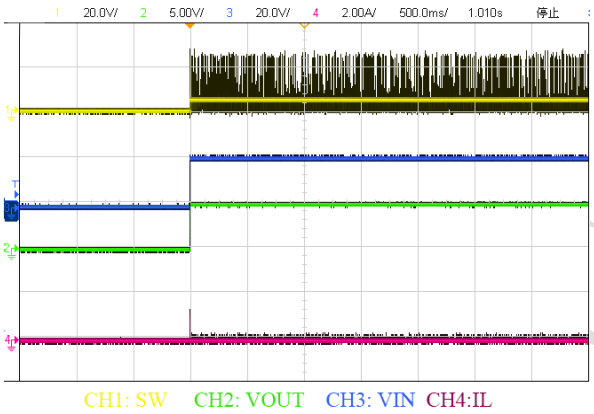
Vin = 12V, Vout = 5V

Fig. 9 Shutdown waveform, Iout = 0A



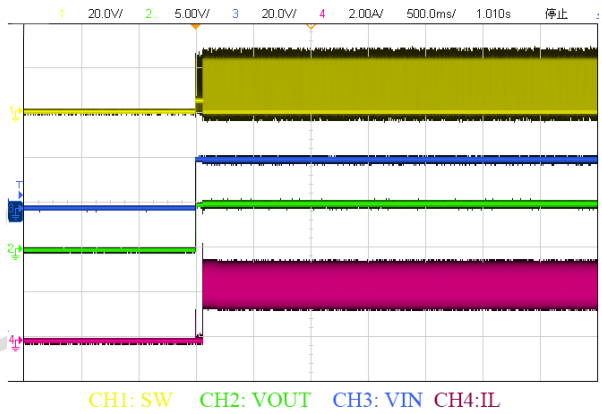
Vin = 12V, Vout = 5V

Fig. 10 Shutdown waveform, Iout = 2.5A



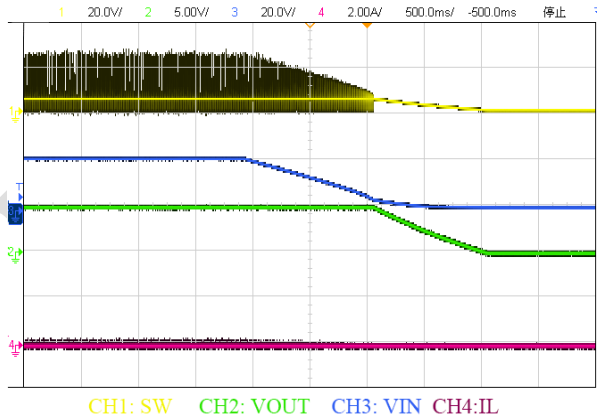
Vin = 24V, Vout = 5V

Fig. 11 Startup waveform, Iout = 0A



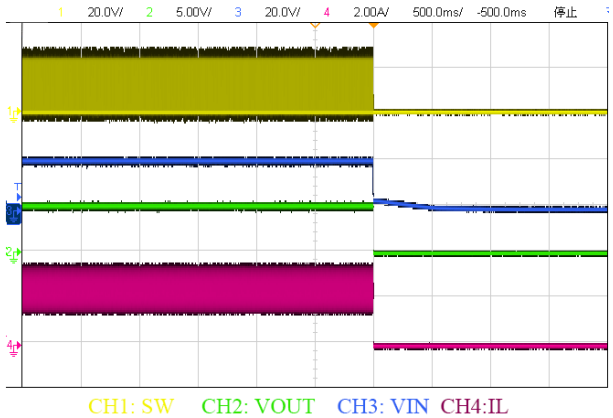
Vin = 24V, Vout = 5V

Fig. 12 Startup waveform, Iout = 2.5A



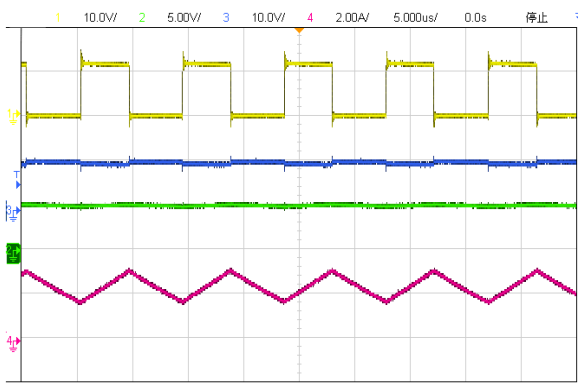
Vin = 24V, Vout = 5V

Fig. 13 Shut down waveform, Iout = 0A



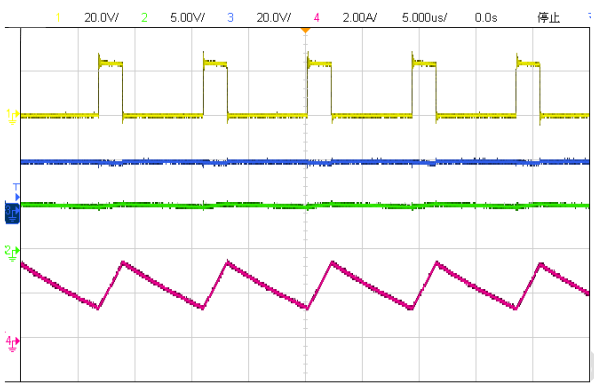
Vin = 24V, Vout = 5V

Fig. 14 Shutdown waveform, Iout = 2.5A



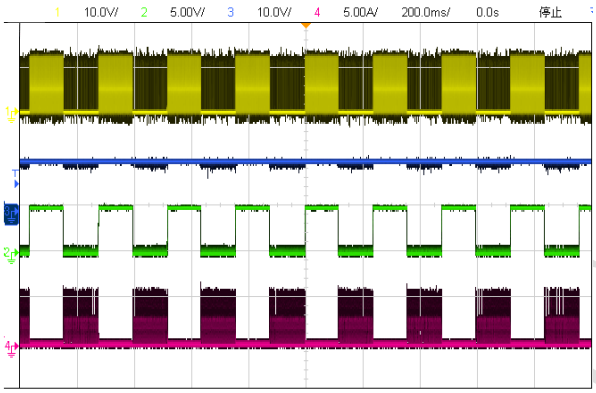
Vin = 12V, Vout = 5V

Fig. 15 Steady State, Iout = 2.5A



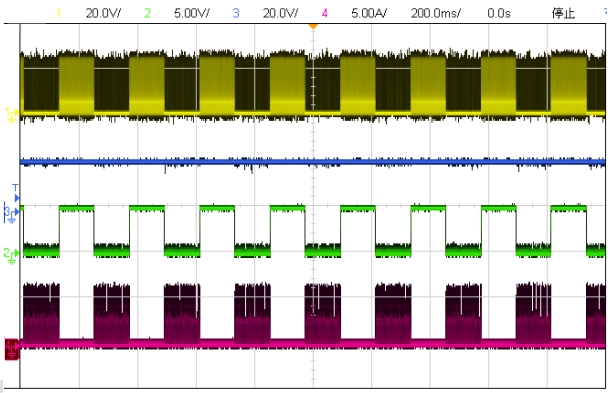
Vin = 24V, Vout = 5V

Fig. 16 Steady State, Iout = 2.5A



Vin = 12V, Vout = 5V

Fig. 17 Short Circuit waveform



Vin = 24V, Vout = 5V

Fig. 18 Short Circuit waveform

9 Detailed Description

9.1 Overview

PL6320 is an easy to use synchronous step-down DC-DC converter that operates from 6.5V to 30V supply voltage. It is capable of delivering up to 3.1A continuous load current with high efficiency and thermal performance in a very small solution size.

PL6320 employs fixed frequency peak current mode control to regulate the output voltage. The device is internally compensated, which reduces design time, and requires fewer external components. The switching frequency is fixed at 100 kHz to minimize inductor size and improve EMI performance.

PL6320 also integrates a USB interface controller to identify different portable devices including Apple mode, Samsung mode, BC1.2 mode and QC2.0 mode. The output voltage can be adjusted to 5V, 9V and 12V based on different control protocol. For safety consideration, PL6320 also integrates input over voltage protection and output over voltage protection. This feature helps customers to design car charger easily.

9.2 Functional Block Diagram

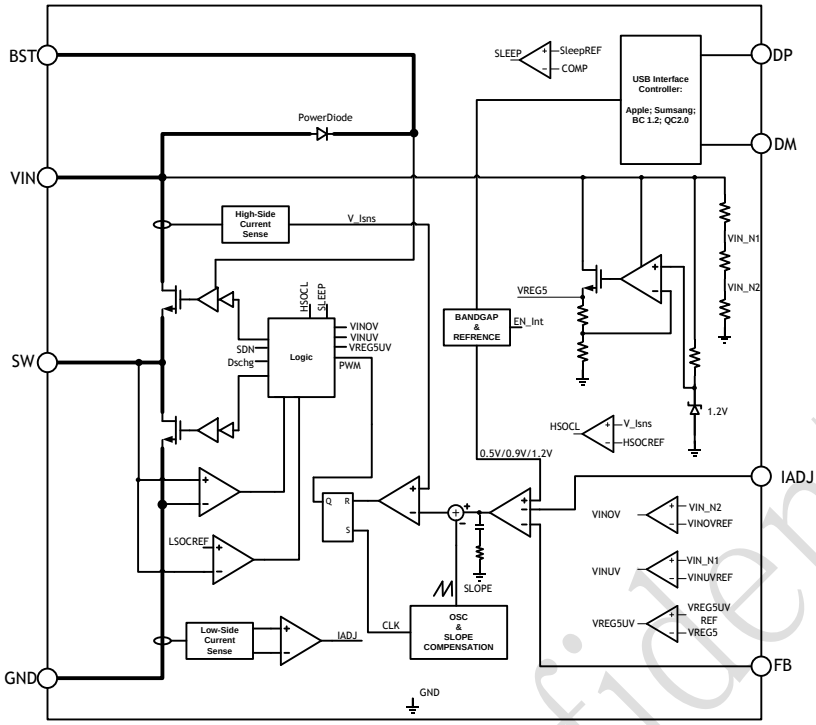


Fig.19 PL6320 Diagram

9.3 Peak Current Mode Control

PL6320 employs a fixed 100 kHz frequency peak current mode control. The output voltage is sensed by an external feedback resistor string on FB pin and fed to an internal error amplifier. The output of error amplifier will compare with high side current sense signal by an internal PWM comparator. When the second signal is higher than the first one, the PWM comparator will generate a turn-off signal to turn off high side switch. The output voltage of error amplifier will increase or decrease proportionally with the output load current. PL6320 has a cycle-by-cycle peak current limit feature inside to help maintain load current in a safe region.

9.4 CC/CV control mode and average load current limiting

PL6320 has a CC/CV control mode. The load current is sensed and averaged. When average load current is high enough, constant-current loop will be dominant and limit the average load current to a value configured by resistor on IADJ pin. For decided average load current limit I_{load}, the resistor R_3 can be roughly calculated as equation (1):

$$R_3 = \frac{1.125}{\frac{I_{load}}{24.7} - 0.016} \quad k\Omega \qquad (1)$$

R_3 is the programming resistor on IADJ pin. The typical range is 5k-50k.

The load current limit is different if the output voltage is programmed to different voltage level by DP and DM. The rough ratio for 5V, 9V and 12V current limit is 3 : 2.5 : 2 to keep output power at a constant level. Comparing with competitor's parts, PL6320 will keep the output power at a rough constant level to keep the part from sending out too much power when output voltage is programmed to 12V. For example, if output voltage is 5V, the current limit is set to 3.6A, the output power will be 18W. If the same current limit is kept for 12V, the output power will be 43.2W, which will generate potential safety issue!

9.5 Line drop compensation

When USB charging cable line is long and resistance is high, there will be some significant voltage drop on the cable. Portable device will see much lower input voltage. If the voltage across the load input terminals is too low, it will affect the charge time for the load. It is recommended to adjust the output voltage of charger to compensate this voltage drop. PL6320 has a configurable line drop compensation. The line drop compensation value can be programmed by the top sensing resistor R_1 in Fig 1. The value can be roughly calculated as equation (2):

$$V_{lineDrop} = \frac{I_{load} * G_{ls} * R_3 * R_1}{100k} \qquad (2)$$

I_{load} is the load current. G_{ls} is the load current sense gain from load current to sourcing current on IADJ pin, G_{ls} Is roughly

48u/1A. R_3 is the programming resistor on IADJ pin. R_1 is the top output sensing resistor.

9.6 Sleep Operation for light load efficiency

PL6320 has an internal feature to help improving light load efficiency. When output current is low, PL6320 will go into sleep mode to save power.

9.7 Quick Charge 2.0 interface

PL6320 integrated a USB interface controller to provide fast charging for portable device which is compatible with QC 2.0 fast charging protocol. The port controller is officially certified.

At power-up, PL6320 will set the reference voltage to 0.9V. PL6320 USB interface will detect DP and DM voltage from portable device and identify the correct portable device type. After correct portable device type is identified, DP and DM will be released from being shorted and allow portable device to identify HVDCP charging port. After HVDCP protocol is established, portable device can use DP and DM signal to change the internal reference of PL6320.

The voltage reference generation system produces a precise voltage reference over temperature to change the regulated FB voltage according to DP and DM signals from portable device when HVDCP protocol is established. Table 1 shows the DP, DM voltage from portable devices and reference voltages generated.

Portable Device		PL6320
DP	**DM**	**Vref**
0.6V	GND	0.9V(Default)
0.6V	0.6V	2.2V
3.3V	0.6V	1.65V

Customer can use external resistor divider to program the required output voltage according to QC 2.0 class A spec, which will be 5V, 9V and 12V.

9.8 Setting Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. The 1% resistance accuracy of this resistor divider is preferred. The output voltage value is set as equation (3) below:

$$V_{out}=V_{ref}\times\frac{R_1+R_2}{R_2} \quad (3)$$

V_{ref} is the internal reference voltage of PL6320, which will be 0.9V, 1.65V or 2.2V according to DP, DM signal voltages.

9.9 Error Amplifier

The error amplifier compares the FB voltage against the internal reference (V_{ref}) and outputs a current proportional to the difference between these two signals. This output current charges or discharges the internal compensation network to generate the error amplifier output voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control-loop design.

9.10 Slope Compensation

In order to avoid sub-harmonic oscillation at high duty cycle, PL6320 adds a slope compensation ramp to the sensed signal of current flowing through high side switch.

9.11 Bootstrap Voltage provided by internal LDO

PL6320 has an internal LDO to provide energy consumed by high side switch. At BST pin, PL6320 needs a small ceramic capacitor like 100nF between BST and SW pin to provide gate-drive voltage for high side switch. The bootstrap capacitor is charged when high side is off. In Continuous-Current-Mode, the bootstrap capacitor will be charged when low side is on. The bootstrap capacitor voltage will be maintained at about 5.3V. When IC works under sleep mode, what value the bootstrap capacitor is charged depends on the difference of Vin and output voltage. However, when the voltage on the bootstrap capacitor is below bootstrap voltage refresh threshold, PL6320 will force low side on to charge bootstrap capacitor. Connecting an external diode from the output of regulator to the BST pin will also work and increase the efficiency of the regulator when output is high enough.

9.12 Internal Soft-Start

PL6320 has a built-in soft-start to control the ramp up speed of output voltage and limit the input current surge during IC start-up. The soft-start time is set to be about 0.8ms.

9.13 Over-Current Protection and Hiccup

PL6320 has cycle-by-cycle peak current limit for both high side and low side switch. When high side switch current is higher than high side current limit, high side switch will be turned off. PL6320 will not turn on high side switch again until low side switch current is lower than low side switch current limit. PL6320 has a CC/CV control structure. When load current is smaller than load current limit programmed by resistor on IADJ pin, CV (constant voltage) loop is dominant. FB voltage will be regulated to internal reference point. When load current is close to load current limit point, CC (constant current) loop will be dominant and regulate load current to be constant by lower down output voltage. After soft start end , if VOUT<1.25V or VFB<0.3V, PL6320 will go into hiccup mode to limit average load current. PL6320 will exit hiccup mode once the over current condition is removed.

9.14 Thermal Shutdown

The internal thermal-shutdown circuitry forces the device to stop switching if the junction temperature exceeds 155°C typically. When the junction temperature drops below 140°C, IC will start to work again.

10 Application and Implementation

10.1 Inductor selection

An inductor is required to supply constant current to the load while being driven by the switched input voltage. A larger value inductor will result in less current ripple and lower output voltage ripple. However, the larger value inductor will have larger physical size, higher DC resistance, and/or lower saturation current. A good rule to calculate the inductance is to allow the peak-to-peak ripple current in the inductor to be approximately 25% of the maximum load current. At the same time, it is needed to make sure that the peak inductor current is below the inductor saturation current.

The inductance value can be calculated by:

$$L=\frac{V_{OUT}}{f_s\times\Delta I_L}\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_S is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum peak current. The peak inductor current can be calculated by:

$$I_{L\_P}=I_{load}+\frac{V_{OUT}}{2\times f_s\times L}\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

Where I_{load} is the load current.

The choice of inductor material mainly depends on the price vs. size requirements and EMI constraints.

10.2 Optional Schottky Diode

During the transition between the high-side switch and low-side switch, the body diode of the low-side power MOSFET conducts the inductor current. The forward voltage of this body diode is high. An optional Schottky diode may be paralleled with low side MOSFET to improve overall efficiency. Table 2 lists example Schottky diodes and their Manufacturers.

Table 2 – Diode Selection Guide

Part Number	Voltage/Current Rating	Vendor
SS25FA	50V/2A	Fairchild
B240A	40V/2A	Vishay

10.3 Input capacitors selection

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the converter. It is recommend to use low ESR capacitors to optimize the performance. Ceramic capacitor is preferred, but tantalum or low-ESR electrolytic capacitors may also meet the requirements. It is better to choose X5R or X7R dielectrics when using ceramic capacitors.

Since the input capacitor (C_{IN}) absorbs the input switching current, a good ripple current rating is required for the capacitor. The RMS current in the input capacitor can be estimated by:

$$I_{CIN}=I_{load}\times\sqrt{\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)} \quad (6)$$

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, where:

$$I_{CIN} = \frac{I_{load}}{2} \quad (7)$$

For simplification, choose the input capacitor whose RMS current rating is greater than half of the maximum load current.

When electrolytic or tantalum capacitors are used, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When ceramic capacitors are used, make sure that they have enough capacitance to maintain voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{load}}{f_s \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

C_{IN} is the input capacitance.

10.4 Output capacitors selection

The output capacitor (C_{OUT}) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended.

Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_s \times C_{OUT}}\right) \quad (9)$$

Where L is the inductor value, R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor and C_{OUT} is the output capacitance value. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly determined by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

The characteristics of the output capacitor also affect the stability of the regulator. PL6320 is optimized for a wide range of capacitance and ESR values.

10.5 External bootstrap diode

It is recommended that an external bootstrap diode could be added when the system has a 5V fixed input or the power supply generates a 5V output. This helps improve the efficiency of the regulator. The bootstrap diode can be a low cost one such as IN4148 or BAT54.

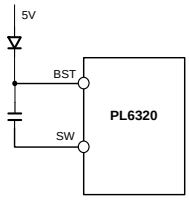


Fig. 20 External Bootstrap Diode

This diode is also recommended for high duty cycle operation (when (V_{OUT} / V_{IN}) > 65%) and high output voltage (V_{OUT}>12V) applications.

11 PCB Layout

11.1 Guideline

PCB layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion efficiency, thermal performance, and minimized EMI.

1. The feedback network, resistor R_1 and R_2, should be kept close to FB pin. V_{out} sense path should stay away from noisy nodes, such as SW, BST and IADJ signals, and preferably through a layer on the other side of shielding layer.

2. The input bypass capacitor C_1 and C_2 must be placed as close as possible to the V_{IN} pin and ground. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin and PAD. It is a good practice to place a ceramic cap near the V_{IN} pin to reduce the high frequency injection current.
3. The inductor L should be placed close to the SW pin to reduce magnetic and electrostatic noise.
4. The output capacitor, C_{OUT} should be placed close to the junction of L and the diode D. The L, D, and C_{OUT} trace should be as short as possible to reduce conducted and radiated noise and increase overall efficiency.
5. The ground connection for C_1, C_2 and C_3, C_4 should be as small as possible and connect to system ground plane at only one spot (preferably at the C_{OUT} ground point) to minimize injecting noise into system ground plane.
6. DP, DM trace should be placed as far from the inductor and noisy power traces as possible.
7. Place current sense resistor R_3 as close as possible to the chip and stay away from noisy nodes such as SW, BST and IADJ.
8. Keep FB away from IADJ node since IADJ may have switching noise at heavy load.

11.2 Example

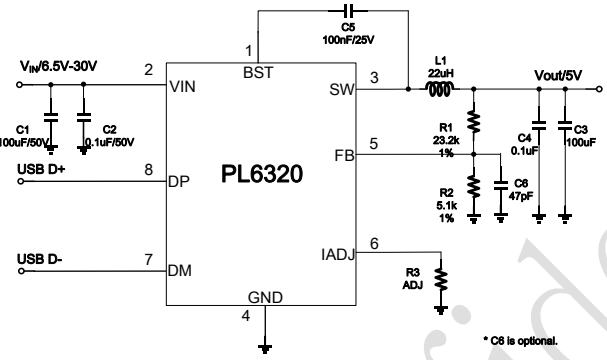


Fig. 21 Schematic

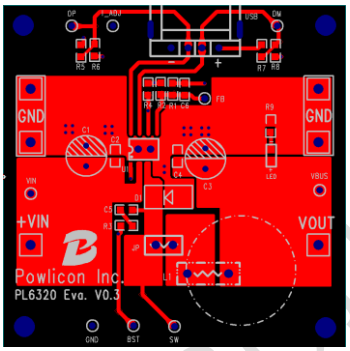


Fig. 22 Top layer layout

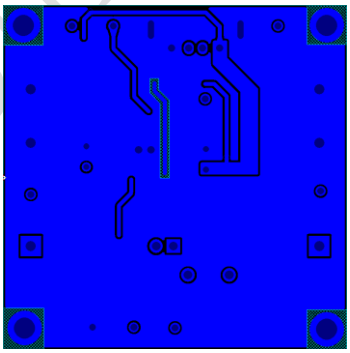
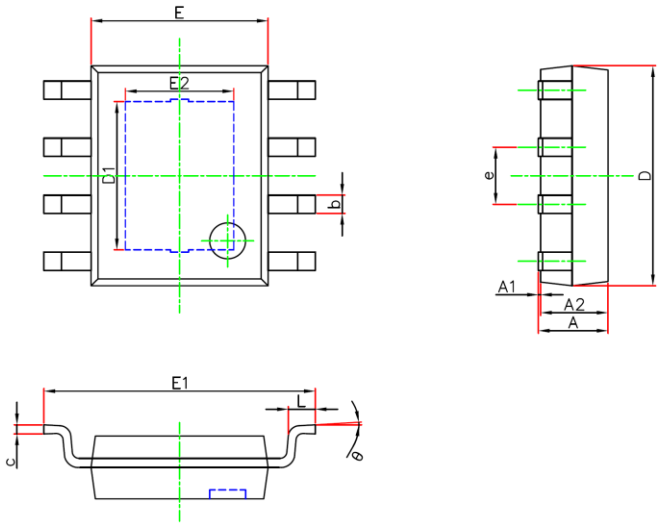


Fig. 23 Bottom layer layout

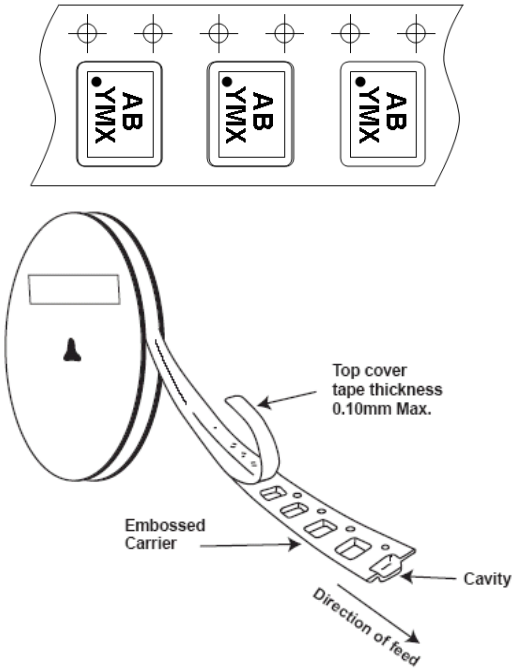
12 Packaging Information

SOP8/PP(95×130) PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

13 Taping Orientation



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