PL671-00

PicoEMI™ Programmable Spread Spectrum Clock

FEATURES

- Advanced programmable Spread Spectrum clock generator with 16 modulation steps to choose from
- Programmable SST Modulation Magnitude:
  - o Center Spread: ±0.125% to ±2.0% in ±0.125% steps
  - o Down Spread: -0.25% to -4.0% in 0.25% steps
- Input Frequency Range:
  - o Fundamental Crystal: 10MHz to 40MHz
- Output Frequency Range:
  - o 1MHz to 200MHz @ 3.3V operation
  - o 1MHz to 166MHz @ 2.5V operation
- Programmable Output Drive (4mA, 8mA, 16mA)
- Low Cycle to Cycle jitter, 100pS
- Single 2.5V to 3.3V, ± 10% power supply
- Available in Die form

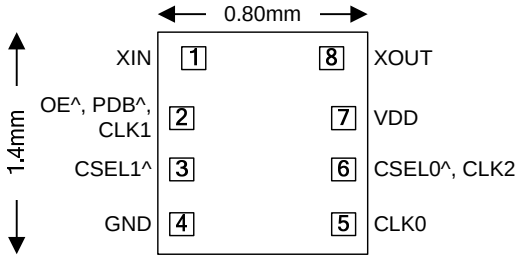
DESCRIPTION

The PL671-00 is an advanced programmable Spread Spectrum clock generator (PSSCG), and a member of PhaseLink's PicoPLL Programmable Clock family.

The PL671-00 clock outputs can be programmed up to 200MHz (3.3V) or 166MHz (2.5V), and has 16 modulation magnitudes (±0.125 to ±2.0% or -0.25 to -4.0%) to choose from for use in Center or Down Spread modulation applications. In addition, 2 configuration pins can be programmed to allow cycling the device through 4 pre-programmed states*. The option of being able to turn 'ON/OFF' the Spread Spectrum modulation allows for completing a design with PL671-00 and having the assurance of turning 'ON' the EMI modulation if EMI becomes an issue*. The PL671-00's spread spectrum modulation greatly reduces the fundamental and harmonic frequencies' peak magnitude, reducing the system level electromagnetic radiation by as much as 20dB.

*Note: Requires 6-pad package

PAD CONFIGURATION

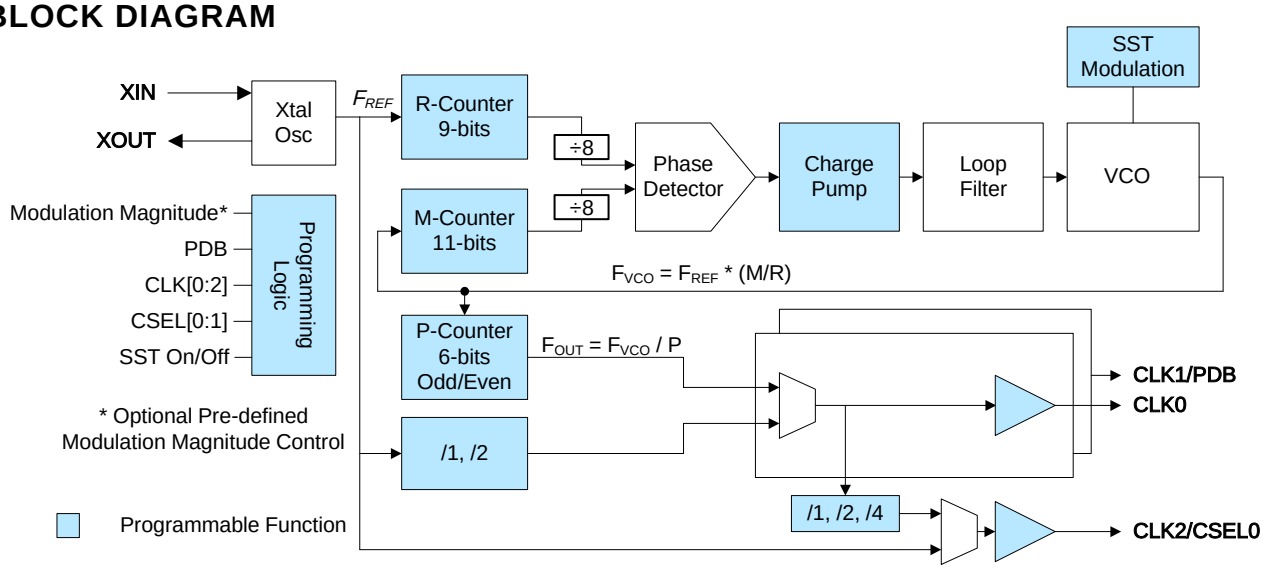


Note: ^ denotes internal pull up resistor

DIE SPECIFICATION

Parameter	Value
Chip size	1.40mm x 0.80mm
Chip thickness	150 to 250µm
PAD size	90µm x 90 µm
Chip base	GND level

BLOCK DIAGRAM



PAD ASSIGNMENT AND DESCRIPTION

<table>
<tr><th rowspan="2">Name</th><th colspan="3">Pad Assignment*</th><th rowspan="2">Type</th><th rowspan="2">Description</th></tr>
<tr><th>Pad #</th><th>X (µm)</th><th>Y (µm)</th></tr>
<tr><td>XIN</td><td>1</td><td>124</td><td>1286</td><td>I</td><td>Crystal input pad.</td></tr>
<tr><td>OE, PDB, CLK1</td><td>2</td><td>87</td><td>930</td><td>I/O</td><td>This pin can be programmed to function as OE (input), PDB (input) or CLK1 (output).
Output Enable (OE) input. Enables and disables the clock output buffer. Internal pull up resistor.
Power Down (PDB) input. Turns off the oscillator, PLL and the output when pulled to logic “0”. Internal pull up resistor.
<table>
<tr><th>Pin State</th><th>OE</th><th>PDB</th></tr>
<tr><td>0</td><td>Disable CLK</td><td>Power Down Mode</td></tr>
<tr><td>1 (default)</td><td>Normal mode</td><td>Normal mode</td></tr>
</table>
Clock1 (CLK1) output. This optional clock can be set to F_{REF}, $F_{REF}/2$ or F_{OUT} (Programmable PLL output).</td></tr>
<tr><td>CSEL1</td><td>3</td><td>87</td><td>628</td><td>I</td><td>Optional programming of CSEL0 & CSEL1 input pins allow switching between ‘4’ pre-defined configurations. Internal pull up resistor.</td></tr>
<tr><td>GND</td><td>4</td><td>87</td><td>275</td><td>P</td><td>GND connection</td></tr>
<tr><td>CLK0</td><td>5</td><td>714</td><td>380</td><td>O</td><td>Programmable Clock Output</td></tr>
<tr><td>CSEL0, CLK2</td><td>6</td><td>714</td><td>677</td><td>I</td><td>This pin can be programmed to function as CSEL0 (input) or CLK2 (output).
CSEL0 input. Optional programming of CSEL0 & CSEL1 input pins allow switching between ‘4’ pre-defined configurations. Internal pull up resistor.
CLK2 output. This optional clock can be set to F_{REF}, CLK0, CLK0/2 or CLK0/4.</td></tr>
<tr><td>VDD</td><td>7</td><td>714</td><td>916</td><td>P</td><td>VDD connection</td></tr>
<tr><td>XOUT</td><td>8</td><td>677</td><td>1286</td><td>O</td><td>Crystal output pad. See Crystal Specifications on page 6.</td></tr>
</table>

* Note: The X/Y coordinates indicate pad centers referenced from the lower left corner of the die.

PicoEMI™ Programmable Spread Spectrum Clock

KEY PROGRAMMING PARAMETERS

CLK[0:2] Output Frequency	SST Modulation Magnitude (Spread Percentage)	Programmable Input/Output	Output Drive Strength
$F_{OUT} = F_{REF} * M / (R * P)$ where M =11 bit R = 9 bit P = 6 bit • CLK0= F_{REF}, $F_{REF}/2$ or F_{VCO}/P* • CLK1= F_{REF}, $F_{REF}/2$ or F_{VCO}/P* • CLK2= F_{REF}, CLK0, CLK0/2 or CLK0/4 * 'P' is a 6-bit Odd/Even divider.	16 programmable modulation magnitudes to choose from: • Center Spread: ±0.125% to ±2.0% in ±0.125% steps • Down Spread: -0.25% to -4.0% in 0.25% steps • SST On/Off Control.	Programmable I/O's include: • PDB – input • Optional CSEL0, CSEL1 (Pre-defined configurations) – input • SST On/Off control – input • CLK[0:2] - output	Three optional drive strengths to choose from: •Low: 4mA •Std: 8mA (default) •High: 16mA

FUNCTIONAL DESCRIPTION

PL671-00 is a highly featured, very flexible, advanced programmable PLL design for high performance, low-power Spread Spectrum modulation applications. The PL671-00 accepts a fundamental input crystal of 10MHz to 40MHz or a reference clock input of 1MHz to 200MHz and is capable of producing three SST modulated outputs up to 200MHz. This flexible design allows the PL671-00 to deliver any PLL generated frequency, FREF (Crystal or Ref Clk) frequency or FREF /2 to CLK0, CLK1 and/or CLK2. Alternate configuration using CSEL0 & CSEL1 allows the device to choose from up to 4 different pre-defined settings providing a range of spread settings, drive levels and outputs to choose from. Some of the design features of the PL671-00 are mentioned below.

PLL Programming

The PLL in the PL671-00 is fully programmable. The PLL is equipped with a 9-bit input frequency divider (R-Counter), and an 11-bit VCO frequency feedback loop divider (M-Counter). The output of the PLL is transferred to a 6-bit post VCO Odd/Even divider (P-Counter). The output frequency is determined by the following formula [$F_{OUT} = (F_{REF} * M)/(R*P)$.

Modulation Magnitude and Type

The PL671-00 provides the following programmable capabilities for Modulation Type and Modulation Magnitude (Spread Percentage):

Modulation Type	Modulation Magnitude	Programming Steps
Center Spread	±0.125% thru ±2.00%	±0.125%
Down Spread	-0.25% thru -4.00%	0.25%

Modulation Rate

The PL671-00 modulation rate is defined as FREF (Crystal Frequency) divided by 8 times the R-counter, i.e. Modulation Rate = (F_{REF} / 8R). The rate can be changed by choosing alternate R-Counter settings.

Clock Outputs (CLK[0:2])

CLK0 is the main clock output. The PL671-00 can also be programmed with additional clock outputs CLK1 and CLK2. The outputs of CLK[0:2] can be configured as described below:

- CLK0= FREF, FREF/2 or FVCO/P*
- CLK1= FREF, FREF/2 or FVCO/P*
- CLK2= FREF, CLK0, CLK0/2 or CLK0/4

Where

FREF - Reference (Crystal) Frequency
$F_{OUT} = F_{REF} * M / (R * P)$

The output drive level of each output can be independently programmed to Low Drive (4mA), Standard Drive (8mA) or High Drive (16mA). The output frequency can be programmed up to 200MHz at 3.3V (166MHz at 2.5V).

Output Enable Control (OE)

When activated (logic '0'), OE disables the clock output buffer putting it into a Hi-Z state. The PDB input incorporates a pull up resistor giving a default condition of logic "1".

Power-Down Control (PDB)

When activated (logic '0'), PDB 'Disables the PLL, the oscillator circuitry, counters, and all other active circuitry. In Power Down mode the IC consumes <10µA of power. The PDB input incorporates a pull up resistor giving a default condition of logic "1".

Configuration Selectors (CSEL[0:1])

The PL671-00 has the capability to be programmed with 4 distinct configurations and to toggle "On the Fly" between these configurations using the selector pads CSEL0 and CSEL1. CSEL0 and CSEL1 both incorporate a pull up resistor giving a default condition of logic "1".

When the CSEL0/CLK2 pin is programmed to be CLK2, CSEL0 is set to a default of Logic 1. This means that two programmable configurations are available to be selected "On the Fly" using CSEL1.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN	MAX	UNITS
Supply Voltage Range	V_{DD}	-0.5	7	V
Input Voltage Range	V_I	-0.5	V_{DD}+0.5	V
Output Voltage Range	V_O	-0.5	V_{DD}+0.5	V
Data Retention @ 85°C		10		Year
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*		-40	85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

AC SPECIFICATIONS

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Crystal Input Frequency(XIN)	Fundamental Crystal	10		40	MHz
Output Frequency	@ V_{DD} =3.3V	1		200	MHz
	@ V_{DD} =2.5V			166	
Settling Time	At power-up (after V_{DD} increases over 2.25V)			2	ms
Output Enable Time	OE Function; Ta=25º C, 15pF Load. Add one clock period to this measurement for a usable output.			10	ns
	PDB Function; Ta=25º C, 15pF Load			2	ms
Output Rise Time	15pF Load, 10/90% V_{DD}, Standard Drive		2.0	3.0	ns
	15pF Load, 10/90% V_{DD}, High Drive		1.2	1.7	
Output Fall Time	15pF Load, 90/10% V_{DD}, Standard Drive		1.7	2.5	ns
	15pF Load, 90/10% V_{DD}, High Drive		1.2	1.7	

AC SPECIFICATIONS (Continued)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Duty Cycle	At V_{DD} /2	45	50	55	%
Cycle to Cycle Jitter*	$T_{CYC-CYC}$ Over output frequency range @ 3.3V			100	ps

* Note: Jitter performance depends on the programming parameters.

DC SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current, Dynamic, with Loaded Outputs	I_{DD}	27MHz, 3.3V, load=15pF, (PDB=1)			15	mA
		PDB=0			10	µA
Operating Voltage	V_{DD}		2.25		3.63	V
Power Supply Ramp	t_{PU}	Time for V_{DD} to reach 90% V_{DD}. Power ramp must be monotonic.			100	ms
Output Low Voltage	V_{OL}	I_{OL} = +4mA (Std Drive)			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4mA (Std Drive)	V_{DD} - 0.4			V
Output Current, Low Drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V	4			mA
Output Current, Std Drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V	8			mA
Output Current, High Drive	I_{OHD}	V_{OL} = 0.4V, V_{OH} = 2.4V	16			mA

CRYSTAL SPECIFICATIONS

PARAMETERS		SYMBOL	MIN	TYP	MAX	UNITS
Fundamental Crystal Resonator Frequency		F_{XIN}	10		40	MHz
Crystal Loading Rating		$C_{L\ (xtal)}$		14		pF
Maximum Sustainable Drive Level					100	µW
Operating Drive Level				30		µW
High C0	Shunt Capacitance	C0			5.5	pF
	ESR Max	ESR			50	Ω
Low C0	Shunt Capacitance	C0			2.5	pF
	ESR Max	ESR			80	Ω

ORDERING INFORMATION

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER
The ordering number for this device is a combination of the following:
Part number, Package type and Operating temperature range

PL671-00 X C

Part Number

Package Type
D=Die
W=Wafer

Temperature
C=Commercial (0°C to 70°C)

Part / Order Number	Marking	Package Option
PL671-00DC	PL671-00DC	Die (Waffle pack)
PL671-00WC	PL671-00WC	Wafer