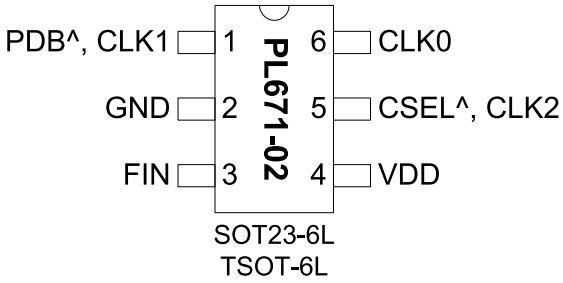
PL671-02

PicoEMI™ Spread Spectrum Clock Generator

FEATURES

- Advanced programmable PLL with Spread Spectrum
- Reference Clock input
  - o 1MHz to 200MHz
- Output Frequency
  - o ≤200MHz
- Two programmable I/O pins
  - o PDB for Power Down function
  - o CSEL for Configuration Select
  - o CLK1/CLK2 additional clock outputs
- Programmable Output Drive
- Low Cycle to Cycle jitter
- Single 2.5V or 3.3V ± 10% power supply
- Available in 6-pin SOT23 or Thin SOT (TSOT) GREEN/RoHS compliant packaging.

PIN CONFIGURATION



SOT23-6L
TSOT-6L

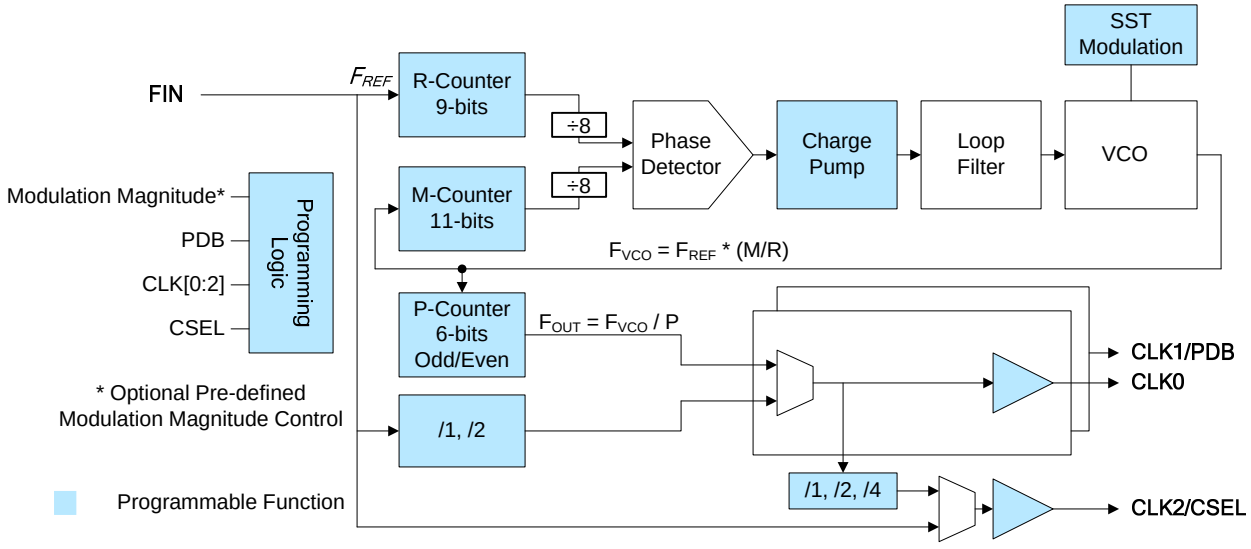
Note: ^ Denotes 60kΩ Pull-up resistor

DESCRIPTION

The PL671-02 is an advanced Spread Spectrum clock generator (SSCG), and a member of PhaseLink's PicoPLL™ Programmable Clock family.

The PL671-02 offers up to three 200MHz outputs, and allows for programming the modulation type (Center or Down Spread) as well as 16 modulation magnitudes (±0.125% to ±2.0% or -0.25% to -4.0%). In addition, the CSEL pin can be used to toggle the device between 2 pre-programmed configurations. The option of being able to turn 'ON/OFF' the Spread Spectrum modulation allows for completing a design with PL671-02 and having the assurance of turning 'ON' the EMI modulation, if EMI becomes an issue. The PL671-02's frequency modulation greatly reduces the fundamental and harmonic frequencies' peak magnitude, therefore reducing the system level Electro Magnetic Interference (EMI), by as much as 20dB

BLOCK DIAGRAM



KEY PROGRAMMING PARAMETERS

CLK[0:2] Output Frequency	SST Modulation Magnitude (Spread Percentage)	Programmable Input/Output	Output Drive Strength
$F_{OUT} = F_{REF} * M / (R * P)$ where M =11 bit R = 9 bit P = 6 bit • CLK0= F_{REF}, $F_{REF}/2$ or F_{VCO}/P* • CLK1= F_{REF}, $F_{REF}/2$ or F_{VCO}/P* • CLK2= F_{REF}, CLK0, CLK0/2 or CLK0/4 * 'P' is a 6-bit Odd/Even divider.	16 programmable modulation magnitudes to choose from: • Center Spread: ±0.125% to ±2.0% in ±0.125% steps • Down Spread: -0.25% to -4.0% in 0.25% steps • SST On/Off Control.	Programmable I/O's include: • PDB – input • CSEL Configuration Selection - input • CLK[0:2] - output	Three optional drive strengths to choose from: •Low: 4mA •Std: 8mA (default) •High: 16mA

PACKAGE PIN ASSIGNMENT

Name	(T)SOT23-6L Pin #	Type	Description
FIN	3	I	Reference input pin (27MHz)
PDB, CLK1	1	B	This pin can be programmed as PDB (input) or CLK1 (output). Power Down (PDB) input. This pin has an internal 60KΩ pull up resistor and turns off the oscillator and the output when pulled to logic "0". **PDB Logic / Osc / PLL / Output** 0 / Off / Off / Hi Z (Default) 1 / Normal Operation (Default) Clock1 (CLK1) output. This optional clock can be set to F_{REF}, $F_{REF}/2$ or F_{OUT} (Programmable PLL output).
CSEL, CLK2	5	I	This pin can be programmed as CSEL (input) or CLK2 (output). CSEL input. Selector pin used to toggle between two pre-programmed configurations. CLK2 output. This optional clock can be set to F_{REF}, CLK0, CLK0/2 or CLK0/4.
GND	2	P	GND connection
VDD	4	P	VDD connection
CLK0	6	O	Programmable Clock Output

FUNCTIONAL DESCRIPTION

PL671-02 is a highly featured, very flexible, advanced programmable PLL design for high performance, low-power Spread Spectrum modulation applications. The PL671-02 accepts a reference clock input of 1MHz to 200MHz and is capable of producing three SST modulated outputs up to 200MHz. This flexible design allows the PL671-02 to deliver any PLL generated frequency, FREF (Ref Clk) frequency or FREF /2 to CLK0, CLK1 and/or CLK2. Alternate programming using CSEL allows the device to choose from 2 different pre-programmed settings providing a range of spread settings and outputs to choose from. Some of the design features of the PL671-02 are mentioned below.

PLL Programming

The PLL in the PL671-02 is fully programmable. The PLL is equipped with an 8-bit input frequency divider (R-Counter), and an 11-bit VCO frequency feedback loop divider (M-Counter). The output of the PLL is transferred to a 6-bit post VCO Odd/Even divider (P-Counter). The output frequency is determined by the following formula [FOUT = (FREF * M)/(R*P).

Modulation Magnitude and Type

The PL671-02 provides the following programmable capabilities for Modulation Type and Modulation Magnitude (Spread Percentage):

Modulation Type	Modulation Magnitude	Programming Steps
Center Spread	±0.125% thru ±2.00%	±0.125%
Down Spread	-0.25% thru -4.00%	0.25%

Modulation Rate

The PL671-02 modulation rate is defined as FREF (Ref Clk Frequency) divided by 8 times the R-counter, i.e. Modulation Rate = (F_{REF} / 8R). The rate can be changed by choosing alternate R-Counter settings.

Clock Outputs (CLK[0:2])

CLK0 is the main clock output. The PL671-02 can also be programmed with additional clock outputs CLK1 and CLK2. The outputs of CLK[0:2] can be configured as described below:

- CLK0= FREF, FREF/2 or FVCO/P*
- CLK1= FREF, FREF/2 or FVCO/P*
- CLK2= FREF, CLK0, CLK0/2 or CLK0/4

Where

FREF - Reference (Ref Clk) Frequency
FOUT = FREF * M / (R * P)

The output drive level of each output can be independently programmed to Low Drive (4mA), Standard Drive (8mA) or High Drive (16mA). The output frequency can be programmed up to 200MHz at 3.3V (166MHz at 2.5V).

Power-Down Control (PDB)

When activated (logic '0'), PDB 'Disables the PLL, the oscillator circuitry, counters, and all other active circuitry. In Power Down mode the IC consumes <10µA of power. The PDB input incorporates a 60kΩ pull up resistor giving a default condition of logic "1".

Configuration Select (CSEL)

The PL671-02 has the capability to be programmed with 2 distinct configurations and to toggle "On the Fly" between these configurations using the selector pin CSEL. CSEL incorporates a 60kΩ pull up resistor giving a default condition of logic "1".

LAYOUT RECOMMENDATIONS

The following guidelines are to assist you with a performance optimized PCB design:

Signal Integrity and Termination Considerations

- Keep traces short!

- Trace = Inductor. With a capacitive load this equals ringing!

- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).

- Design long traces (> 1 inch) as “striplines” or “microstrips” with defined impedance.

- Match trace at one side to avoid reflections bouncing back and forth.

Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the VDD pin(s) to limit noise from the power supply

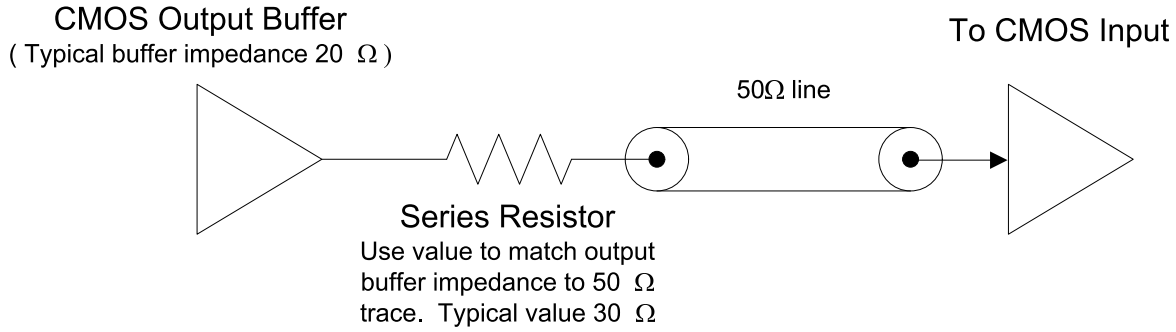
- Multiple VDD pins should be decoupled separately for best performance.

- Addition of a ferrite bead in series with VDD can help prevent noise from other board sources

- Value of decoupling capacitor is frequency dependant. Typical values to use are 0.1μF for designs using frequencies < 50MHz and 0.01μF for designs using frequencies > 50MHz.

Typical CMOS termination

Place Series Resistor as close as possible to CMOS output



ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN	MAX	UNITS
Supply Voltage Range	V_{DD}	-0.5	4.6	V
Input Voltage Range	V_I	-0.5	V_{DD}+0.5	V
Output Voltage Range	V_O	-0.5	V_{DD}+0.5	V
Soldering Temperature (Green package)			260	°C
Data Retention @ 85°C		10		Year
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*		-40	85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

AC SPECIFICATIONS

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Input (FIN) Frequency	@ V_{DD} =3.3V	1		200	MHz
	@ V_{DD} =2.5V			166	
Input (FIN) Signal Amplitude	Internally AC coupled (High Frequency)	0.9		V_{DD}	Vpp
Input (FIN) Signal Amplitude	Internally AC coupled (Low Frequency) 3.3V ≤50MHz, 2.5V ≤40MHz	0.1		V_{DD}	Vpp
Output Frequency	@ V_{DD} =3.3V			200	MHz
	@ V_{DD} =2.5V			166	
Settling Time	At power-up (after V_{DD} increases over 2.25V)			2	ms
Output Enable Time	PDB Function; Ta=25° C, 15pF Load			2	ms
Output Rise Time	15pF Load, 10/90% V_{DD}, Standard Drive		2.0	3.0	ns
	15pF Load, 10/90% V_{DD}, High Drive		1.2	1.7	
Output Fall Time	15pF Load, 90/10% V_{DD}, Standard Drive		1.7	2.5	ns
	15pF Load, 90/10% V_{DD}, High Drive		1.2	1.7	
Duty Cycle	At V_{DD} /2	45	50	55	%
Cycle to Cycle Jitter*	$T_{CYC-CYC}$ Over output frequency range @ 3.3V			100	ps

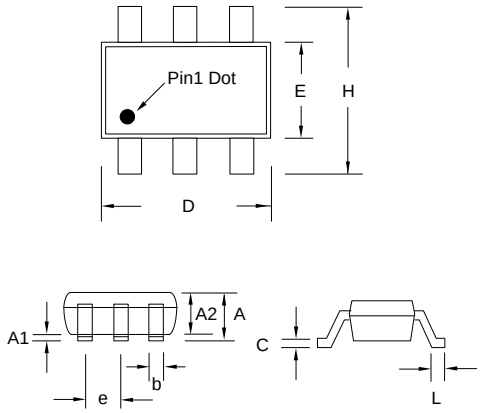
DC SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic, with Loaded Outputs	I_{DD}	At 27MHz, 3.3V, load=15pF, (PDB=1)			15	mA
		PDB=0			10	µA
Operating Voltage	V_{DD}		2.25		3.63	V
Power Supply Ramp	t_{PU}	Time for V_{DD} to reach 90% V_{DD}. Power ramp must be monotonic.			100	ms
Output Low Voltage	V_{OL}	I_{OL} = +4mA (Std. Drive)			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4mA (Std. Drive)	V_{DD} – 0.4			V
Output Current, Low Drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V	4			mA
Output Current, Standard Drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V	8			mA
Output Current, High Drive	I_{OHD}	V_{OL} = 0.4V, V_{OH} = 2.4V	16			mA

PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

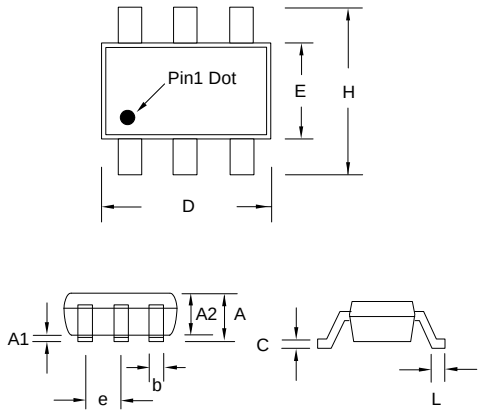
SOT23-6L

Symbol	Dimension in MM	
	Min.	Max.
A	1.05	1.35
A1	0.05	0.15
A2	1.00	1.20
b	0.30	0.50
c	0.08	0.20
D	2.80	3.00
E	1.50	1.70
H	2.60	3.00
L	0.35	0.55
e	0.95 BSC	



TSOT-6L

Symbol	Dimension in MM	
	Min.	Max.
A		1.00
A1	0.00	0.10
A2	0.84	0.90
b	0.30	0.50
c	0.127 w/o plating	
D	2.90 BSC	
E	1.60 BSC	
H	2.80 BSC	
L	0.30	0.50
e	0.95 TYP	



ORDERING INFORMATION (GREEN PACKAGE COMPLIANT)

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: +1 510 492-0990 • Fax: +1 510 492-0991

PART NUMBER
The order number for this device is a combination of the following:
Part Number, Package Type and Operating Temperature Range

PL671-02-xxx T C - R

- Part Number
- 3 Digit ID Code*
- Package Type
  - R = TSOT-6L
  - T = SOT23-6L
- Temperature Range
  - C = Commercial (0°C to 70°C)
- Shipping Option
  - R = Tape & Reel
  - None = Tube

* PhaseLink will assign a unique 3-digit ID code for each approved programmed part number.

Part/Order Number	Marking	Package Option
PL671-02-xxxRC-R	F2xxx	6-Pin TSOT (Tape and Reel)
PL671-02-xxxTC-R	F2xxx	6-Pin SOT23 (Tape and Reel)

Solder reflow profile available at www.phaselink.com/QA/solderingGreen.pdf