36V,2.4A Monolithic Step-Down Switching Regulator with CC/CV control

1 Features

- 2.4A continuous output current capability
- 6.5V to 36V wide operating input range with 33V input Over Voltage Protection
- Integrated 36V, 108mΩ high side and 36V, 102mΩ low side power MOSFET switches
- Up to 95% efficiency
- Internally fixed 3A constant current control
- Programmable Soft-Start limits the inrush current at turn-on
- Stable with Low ESR Ceramic Output Capacitors
- Fixed 100KHz Switching Frequency
- Input Under-Voltage Lockout. Output Over-Voltage Protection
- Over-Temperature Protection
- Thermally Enhanced ESOP-8 Package

2 Applications

- USB car charger
- Portable charging device
- General purpose DC-DC conversion

3 Description

The PL8325B is a monolithic 36V, 2.4A step-down switching regulator with CC/CV control loop. PL8325B integrates a high efficiency synchronous step-down switching regulator, which includes a 36V 108mΩ high side and a 36V, 102mΩ low side MOSFETs to provide 2.4A continuous load current over a 6.5V to 36V wide operating input voltage. Peak current mode control provides fast transient responses and cycle-by-cycle current limiting. Programmable soft-start prevents inrush current at power-up. The supply current drops below 1μA in shutdown mode.

4 Typical Application Schematic & Efficiency

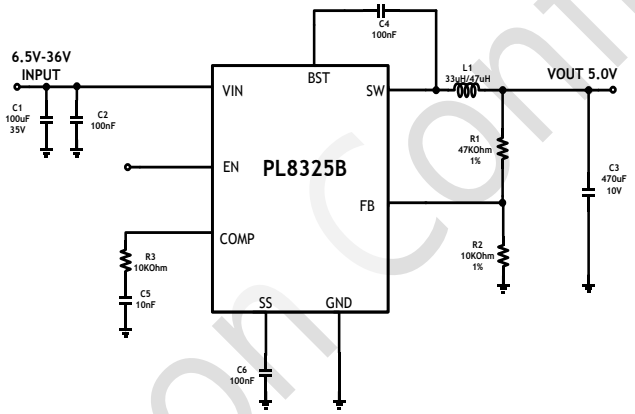


Fig. 1 Schematic

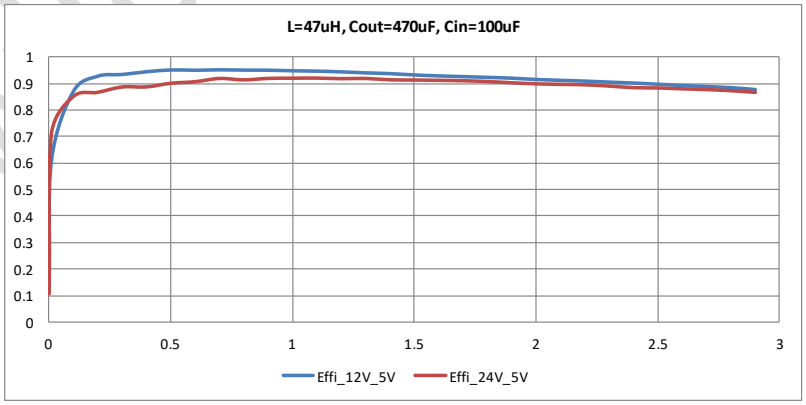
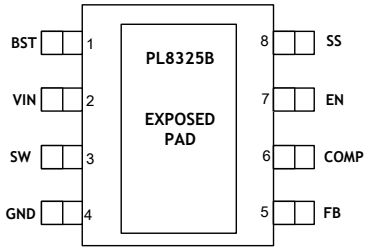


Fig. 2 Efficiency curve

5 Pin Configuration and Functions

ESOP-8 Package (Top View)



Pin-Functions

Pin		Description
Number	Name	
1	BST	Boot-Strap pin. Connect a 0.1μF or greater capacitor between SW and BST to power the high side gate driver.
2	VIN	Power Input. VIN supplies the power to the IC. Supply VIN with a 6.5V to 36V power source. Bypass VIN to GND with a large capacitor and at least another 0.1uF ceramic capacitor to eliminate noise on the input to the IC. Put the capacitors close to VIN and GND pins.
3	SW	Power Switching pin. Connect this pin to the switching node of inductor.
4	GND	Ground
5	FB	Feedback Input. FB senses the output voltage. Connect FB with a resistor divider connected between the output and ground. FB is a sensitive node. Keep FB away from SW and BST pin.
6	COMP	Connect compensation network to make the converter work stably.
7	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator; low to turn it off. EN is pulled to VIN internally by a large resistor.
8	SS	Soft-start adjustment. Connect a cap to program soft-start time.
9	EPAD	EPAD is connected to GND internally. EPAD must be connected to GND on PCB board to get full power.

6 Device Marking Information

Part Number	Order Information	Package	Package Qty	Top Marking
PL8325B	**PL8325BIES08**	**ESOP-8**	**4000**	**8325B RAAYMD**

PL8325B: Part Number
RAAYMD: RAA:Lot Number；YMD: Package Date

7 Specifications

7.1 Absolute Maximum Ratings(Note1)

	PARAMETER	MIN	MAX	Unit
Input Voltages	VIN to GND	-0.3	36	V
	SS to GND	-0.3	6	
	EN to GND	-0.3	6	
	FB to GND	-0.3	6	
Output Voltages	COMP to GND	-0.3	6	V
	BST to SW	-0.3	6	
	SW to GND	-1	VIN+ 0.3	

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
T_{ST}	Storage Temperature Range	-65	150	°C
T_J	Junction Temperature		+150	°C
T_L	Lead Temperature		+260	°C
V_{ESD}	HBM Human body model		2	kV
	MM model		400	V

7.3 Recommended Operating Conditions (Note 2)

	PARAMETER	MIN	MAX	Unit
Input Voltages	VIN to GND	6.5	30	V
	FB to GND	-0.3	6	
	EN to GND	-0.3	6	V
Output Voltages	V_{OUT}	0.5	V_{IN}*D_{max}	V
Output Current	I_{OUT}	0	2.4	A
Temperature	Operating junction temperature range, T_J	-40	+125	°C

7.4 Thermal Information (Note 3)

Symbol	Description	ESOP-8	Unit
θ_{JA}	Junction to ambient thermal resistance	56	°C/W
θ_{JC}	Junction to case thermal resistance	45	

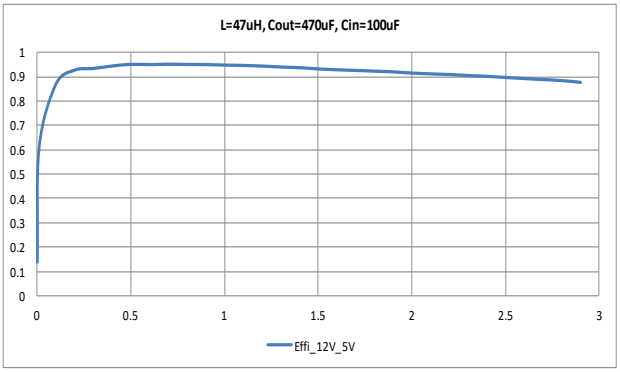
Notes:
1) Exceeding these ratings may damage the device.
2) The device function is not guaranteed outside of the recommended operating conditions.
3) Measured on approximately 1" square of 1 oz copper.

7.5 Electrical Characteristics (Typical at VIN = 12V, T_J=25°C, unless otherwise noted.)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
BUCK CONVERTER						
MOSFET						
I_{leak_sw}	High-Side Switch Leakage Current	V_{EN} = 0V, V_{SW} = 0V		0	10	μA
$R_{DS(ON)\_H}$	High-Side Switch On-Resistance	I_{OUT} = 1A, V_{OUT} = 5V		108		mΩ
$R_{DS(ON)\_L}$	Low-Side Switch On-Resistance	I_{OUT} = 1A, V_{OUT} = 5V		102		mΩ
SUPPLY VOLTAGE (VIN)						
V_{UVLO_up}	Minimum input voltage for startup			6.375		V
V_{UVLO_down}				6.0		V
V_{UVLO_hys}				0.375		V
$I_{Q-NONSW}$	Operating quiescent current	V_{FB} =1V		1		mA
I_{Q-SW}	Quiescent Supply Current	V_{FB} =0.9V I_{OUT} = 0A V_{OUT} = 5V		1.5		mA
CONTROL LOOP						
F_{oscb}	Buck oscillator frequency			100		kHz
V_{FB}	Feedback Voltage	6.5V ≤ VIN ≤ 36V		0.9		V
V_{FB_OVP}	Feedback Over-voltage Threshold			1		V
D_{max}	Maximum Duty Cycle (Note 4)			96		%
T_{on}	Minimum On Time (Note 4)			100		ns
PROTECTION						
I_{ocl_hs}	Upper Switch Current Limit	Minimum Duty Cycle		4.5		A
I_{ocl_ls}	Lower Switch Current Limit	From Drain to Source		2.7		A
V_{inovp}	Input Over voltage protection			33		V
T_{ss}	Soft-Start Period			0.5		ms
Th_{sd}	Thermal Shutdown (Note 4)			155		°C
Th_{sdhys}	Thermal Shutdown Hysteresis (Note 4)			30		°C
V_{IH}	EN High Voltage		1.2			V
V_{IL}	EN Low Voltage				1	V
I_{EN}	EN Input Current			2.6		uA
I_{chg_ss}	Soft-Start Charge Current			4		uA
$V_{boot,refresh}$	Bootstrap refresh voltage			3.4		V
I_{cmp_src}	Comp Source Current	V_{FB} = 1.0 V		60		uA
I_{cmp_snk}	Comp Sink Current	V_{FB} = 0.8 V		60		uA
G_{m_PS}	COMP to current sense transconductance (Note 4)			5		A/V

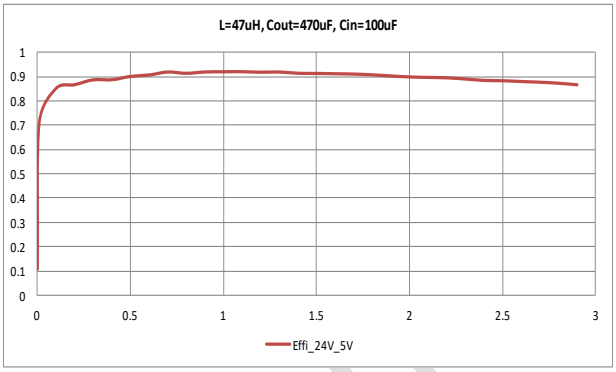
Note:
4) Guaranteed by design, not tested in production
.

8 Typical Characteristics



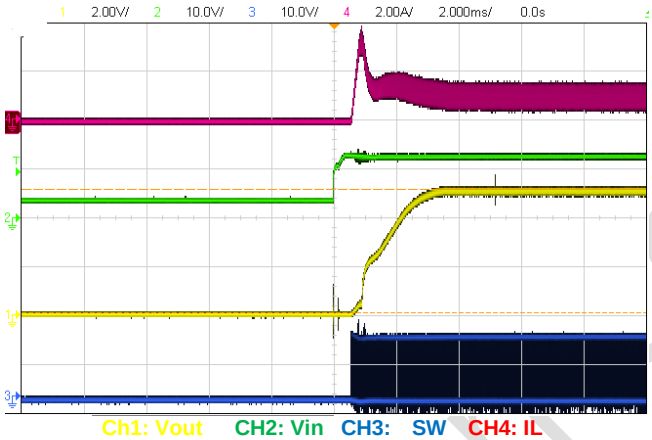
Vin = 12V, Vout = 5V

Fig. 3 Efficiency



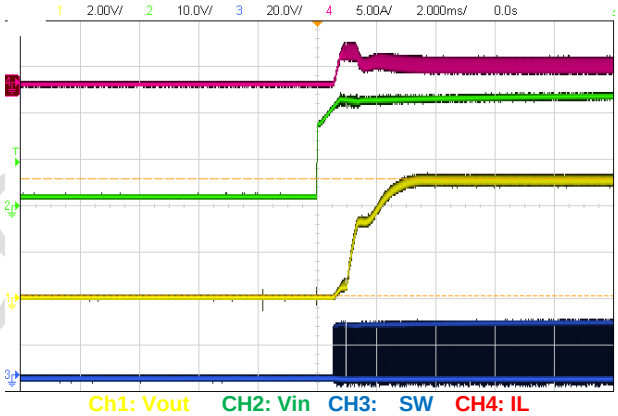
Vin = 24V, Vout = 5V

Fig. 4 Efficiency



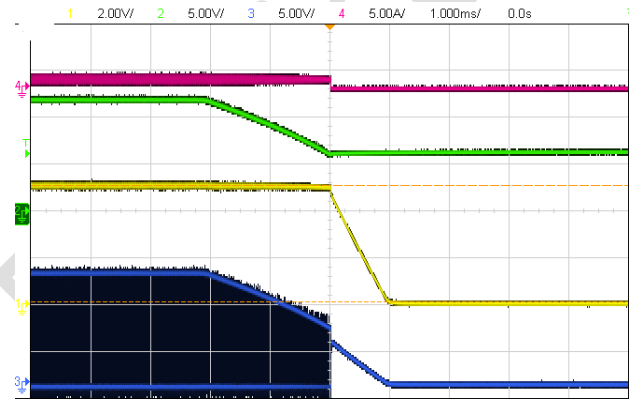
Vin = 12V, Vout = 5V, Iout=1A

Fig. 5 Power Up Waveform



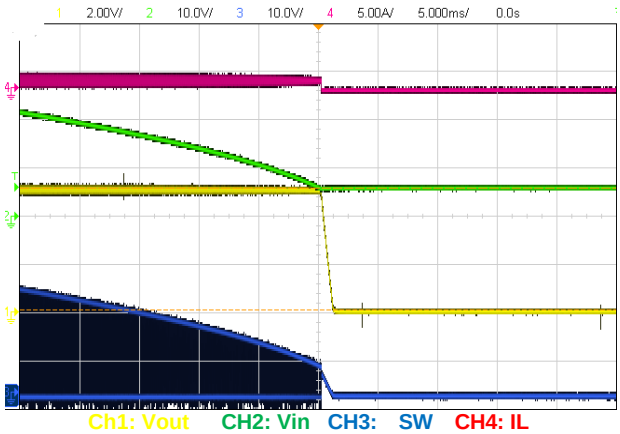
Vin = 24V, Vout = 5V, Iout=2A

Fig. 6 Power Up Waveform



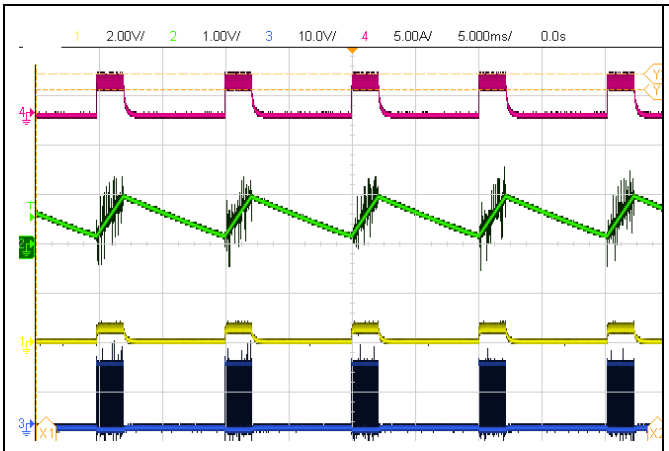
Vin = 12V, Vout = 5V, Iout=1A

Fig. 7 Power Down Waveform



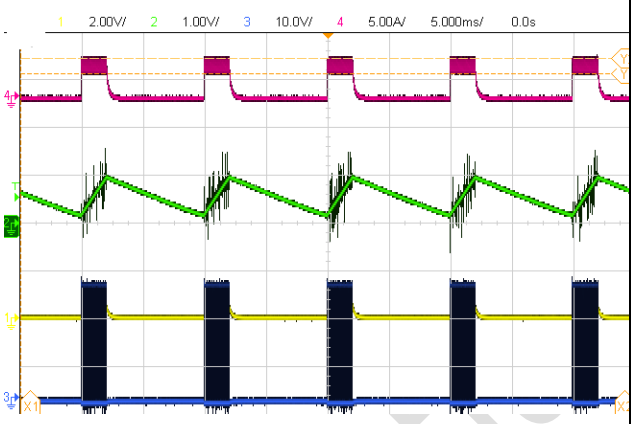
Vin = 24V, Vout = 5V, Iout=1A

Fig. 8 Power Down Waveform



Ch1: Vout CH2: SS CH3: SW CH4: IL

Fig. 9 12V Vin Short Protection Waveform



Ch1: Vout CH2: SS CH3: SW CH4: IL

Fig. 10 24V Vin Short Protection Waveform

9 Detailed Description

9.1 Overview

PL8325B is a single channel, constant frequency, current mode step-down switching regulator for 36V, 2.4A application. It regulates 6.5V to 36V down to an output voltage as low as 0.9V, and supplies up to 2.4A of load current.

PL8325B uses current-mode control to regulate the output voltage. Output voltage is measured at FB by a resistive voltage divider and amplified by the internal error amplifier. The voltage at COMP pin is compared to high-side switch current measured internally to control the output voltage.

The converter uses internal N-channel MOSFET switches to step-down the input voltage to the regulated output voltage. Since the high-side MOSFET requires a gate voltage greater than the input voltage, a boost capacitor is connected between SW and BST, charged by internal boost regulator during the period when low-side MOSFET is on.

When FB voltage exceeds 0.99V , the over-voltage comparator will generate a signal to shut down High-side MOSFET to prevent FB voltage running away.

The PL8325B device has a fixed 100KHZ switching frequency. The device adjusts the soft-start time with the SS pin.

9.2 Functional Block Diagram

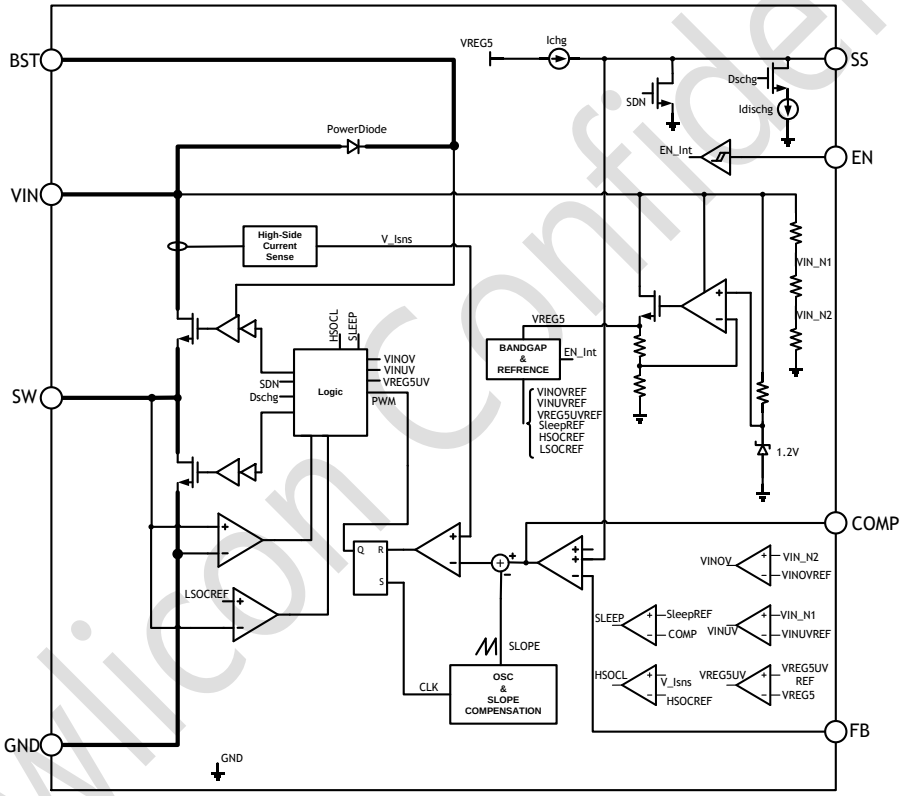


Fig.11 PL8325B Diagram

9.3 Peak Current Mode Control

PL8325B employs a fixed 100kHz frequency, peak current mode control. The output voltage is sensed by an external feedback resistor string on FB pin to an internal error amplifier. The output of error amplifier will compare with the sensed signal of current flowing through high side switch by internal PWM comparator. PWM comparator will generate a turn-off signal to high side driver, which will turn off high side switch. PL8325B has a cycle-by-cycle peak current limit feature inside to help maintain load current in a safe region.

9.4 Sleep Mode for Light Load Efficiency

PL8325B will disable both high side and low side power switches to improve light load efficiency when COMP voltage is less than a threshold. With this work mode, PL8325B will reach a very high efficiency under light load condition.

9.5 Voltage Reference

The voltage reference system produces a precise 0.9V voltage reference over temperature supported by PL8325B.

9.6 Setting Output Voltage

The output voltage is set by a resistor divider from the output node to FB pin. 1% accuracy resistor is preferred for this divider. The output voltage value is set as equation 1.

$$V_{out}=V_{ref}\times\frac{R_1+R_2}{R_2} \quad (1)$$

Vref is the internal reference voltage of PL8325B, 0.9V.

9.7 Setting Enable Threshold

PL8325B has an internal comparator on EN pin. When system needs a higher VIN UVLO threshold, a resistor divider can be used as shown in Figure 12 below.

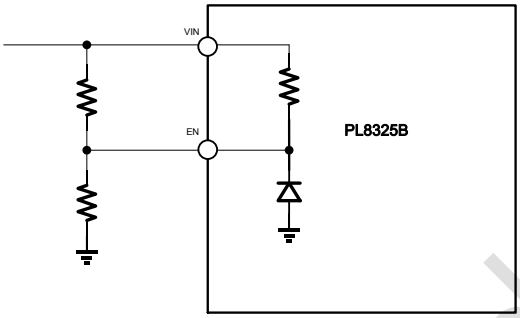


Fig.12 Adjustable VIN Under voltage Lockout

9.8 Soft-Start and Hiccup

PL8325B needs a capacitor at SS pin to support soft-start function. The soft-start time can be programmed by external capacitor on SS pin. PL8325B also uses SS pin to configure hiccup rest time. When the output voltage is lower than 0.4V and high side peak current reaches current limit threshold, the PL8325B will stop working and discharge SS capacitor using 1uA current.

9.9 Thermal Shutdown

The internal thermal-shutdown circuitry forces the device to stop switching if the junction temperature exceeds 155°C typically. When the junction temperature drops below 125°C typically, IC will start to work again.

10 Application and Implementation

10.1 Inductor selection

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher DC resistance, and/or lower saturation current. A good rule for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be approximately 25% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit.

The inductance value can be calculated by:

$$L=\frac{V_{OUT}}{f_s\times\Delta I_L}\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (2)$$

Where VOUT is the output voltage, VIN is the input voltage, f_s is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated by:

$$I_{L\_P}=I_{load}+\frac{V_{OUT}}{2\times f_s\times L}\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (3)$$

Where I_{load} is the load current.

The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI constraints.

10.2 Optional schottky diode

During the transition between high-side switch and low-side switch, the body diode of the low-side power MOSFET conducts the inductor current. The forward voltage of this body diode is high. An optional schottky diode may be paralleled between the SW pin and GND pin to improve overall efficiency.

10.3 Input capacitors selection

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice. Choose X5R or X7R dielectrics when using ceramic capacitors.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{CIN}=I_{load}\times\sqrt{\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs at $V_{IN} = 2\times V_{OUT}$, where:

$$I_{CIN}=\frac{I_{load}}{2} \quad (5)$$

For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1µF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN}=\frac{I_{load}}{f_s\times C_{IN}}\times\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

Where C_{IN} is the input capacitance value.

10.4 Output capacitors selection

The output capacitor (C_{OUT}) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended.

Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_s \times C_{OUT}}\right) \quad (7)$$

Where L is the inductor value, R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor and C_{OUT} is the output capacitance value. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (9)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The PL8325B can be optimized for a wide range of capacitance and ESR values.

10.5 External bootstrap diode

It is recommended that an external bootstrap diode be added when the system has a 5V fixed input or the power supply generates a 5V output. This helps improve the efficiency of the regulator. The bootstrap diode can be a low cost one such as IN4148 or BAT54.

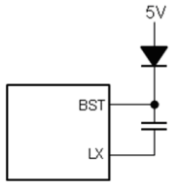


Fig. 13 External Boostrap Diode

This diode is also recommended for high duty cycle operation (when (V_{OUT} / V_{IN}) > 65%).

11 PCB Layout

11.1 Guideline

PCB layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion efficiency, thermal performance, and minimized EMI.

1. The feedback network, resistor R_1 and R_2, should be kept close to FB pin. V_{out} sense path should stay away from noisy nodes, such as SW and BST signals and preferably through a layer on the other side of shielding layer.
2. The input bypass capacitor C_1 and C_2 must be placed as close as possible to the V_{IN} pin and ground. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin and PAD. It is a good practice to place a ceramic cap near the V_{IN} pin to reduce the high frequency injection current.
3. The inductor L should be placed close to the SW pin to reduce magnetic and electrostatic noise.
4. The output capacitor, C_{OUT} should be placed close to the junction of L and the diode D. The L, D, and C_{OUT} trace should be as short as possible to reduce conducted and radiated noise and increase overall efficiency.
5. PL8325B and inductor L1 are generally two hottest components in the system. It is better to place them evenly on PCB board.

11.2 Example

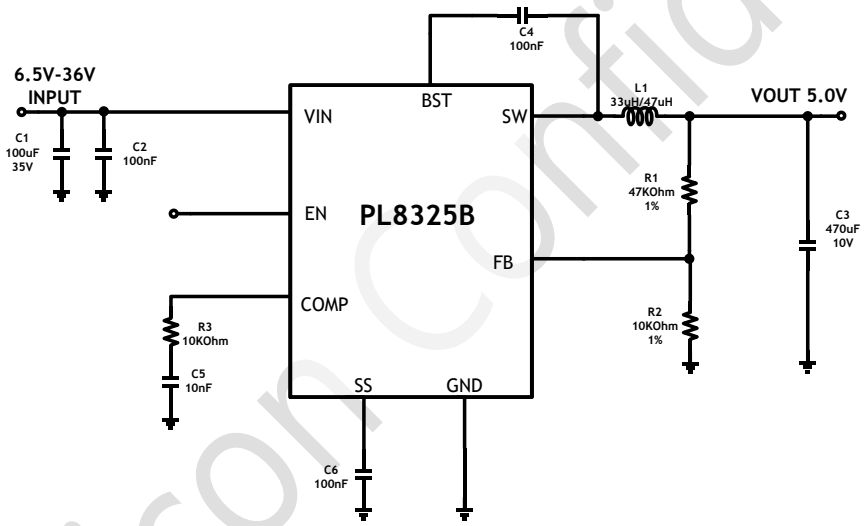


Fig. 14 Schematic

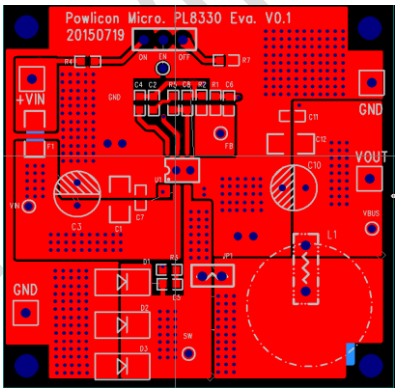


Fig. 15 Top layer layout

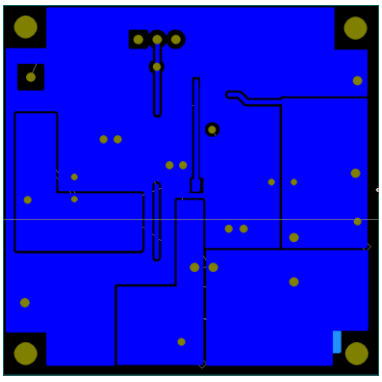
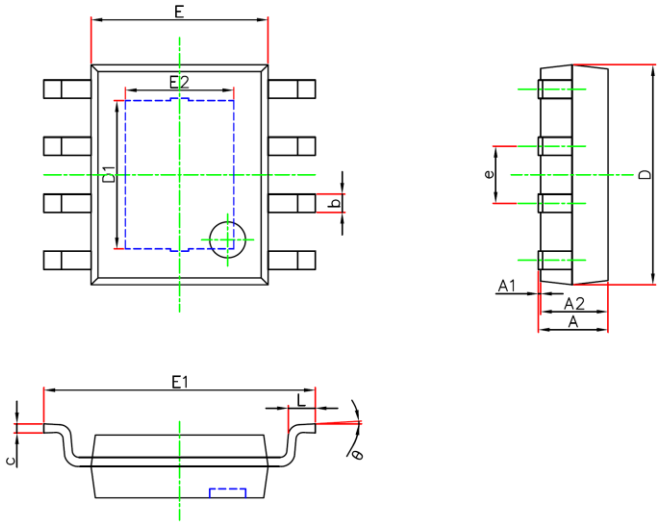


Fig. 16 Bottom layer layout

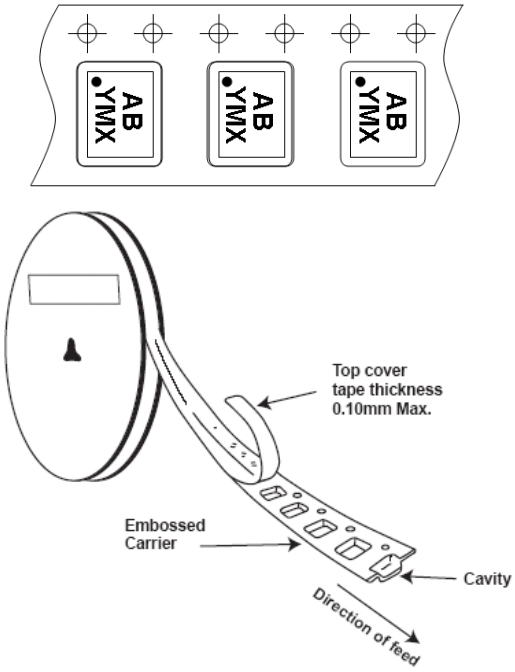
12 Packaging Information

SOP8/PP(95×130) PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

13 Taping Orientation



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