Single Phase, Multifunction Metering IC with Multiple Anti-Tampering Features

Product Data Sheet PL8331

Features

- Wide supply voltage range: 2.4V to 3.6V
- Ultra-low power consumption
  - Normal mode:
    Total: 2.2mA @ 3V
  - Sleep Mode: 3uA
  - RTC only: 1.1uA
- Multi mode power saving function
- Internal switch between regulated and battery inputs
- Compatible with CTs, resistive shunts and Rogowski Coil sensors
- Wake-up from standby mode in less than 5us
- Operation temperature range: -40°C to +80°C
- 64-LQFP(7x7) package

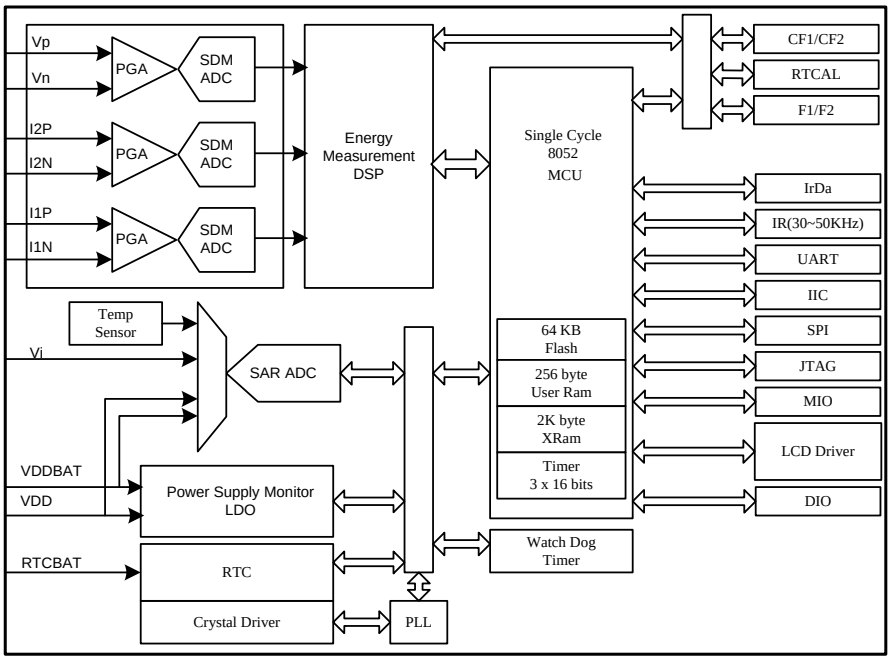
General Description

The PL8331 series of ultra-low power mixed-signal processors consist of several devices featuring different sets of peripherals targeted for energy meter applications. They integrate analog front end and fixed function DSP solution with an enhanced 8052 MCU core, RTC and LCD driver in a single part. The measurement core includes active, reactive, apparent energy calculations, voltage, current RMS, and frequency measurements. This information can be used as energy billing and any necessary application. Also included are a built-in 16-bit timer, LCD segment drive capability and hardware multiplier.

The PL8331 integrates three PGAs with gain settings from 1x to 32x. Three 24-bit sigma-deltas A/D converters guarantee precision in captured data and enough needed resolution.

The microprocessor functionality includes a single-cycle 8052 core, a real-time clock, UART, and an SPI, I2C and JTAG interface. It reduces the program memory size requirement and makes it easy to integrate complicated designs. The programming is very easy and supports multiple ways (SPI or JTAG). No external voltage is needed for programming.

Block Diagram



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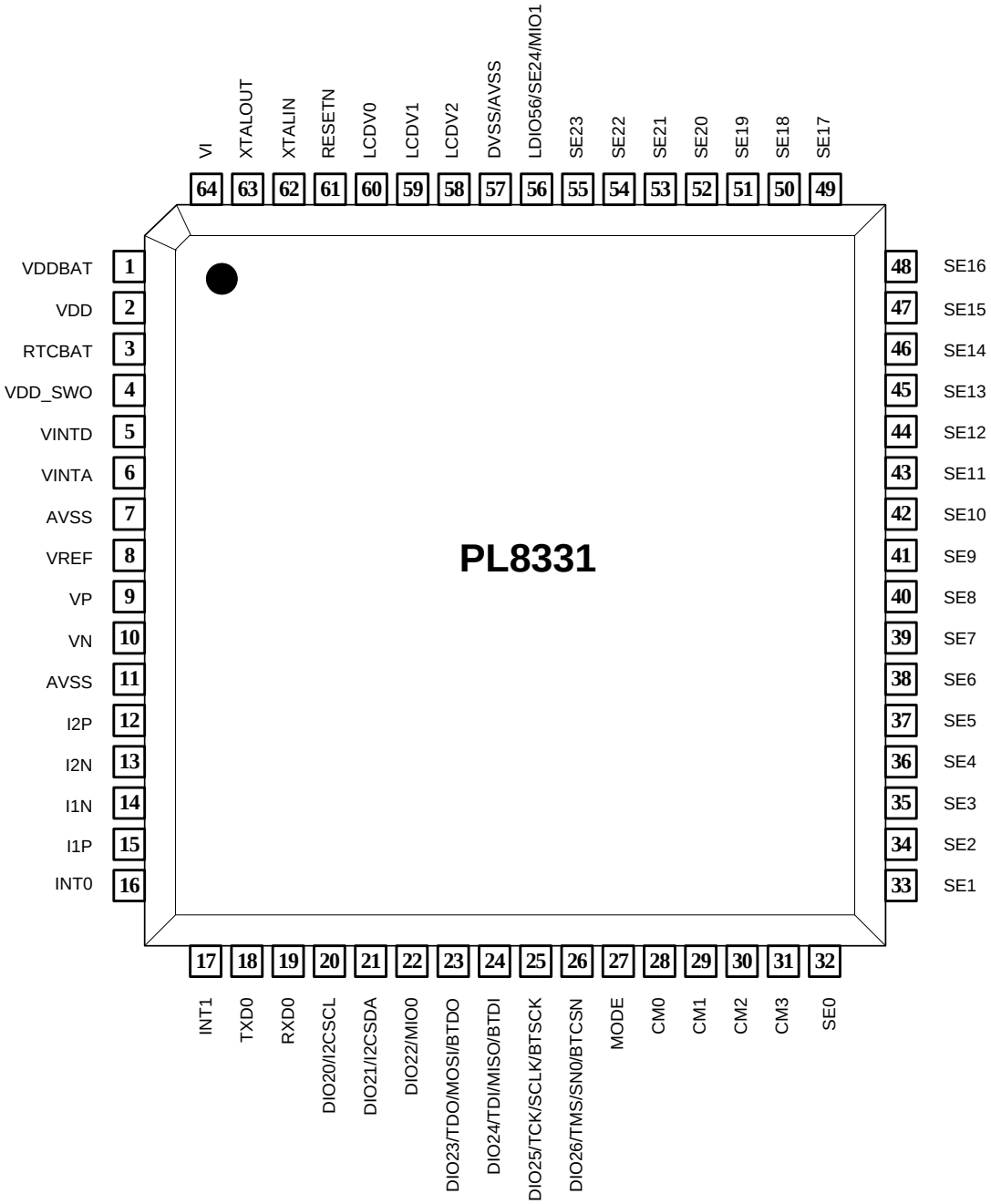
Pin Diagram



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1. Features

GENERAL FEATURES

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ADC FEATURES

- Three second-order, 24-bit, delta-sigma Analog-to-Digital Converters
- Three differential input PGA front ADC (Gain=1,2,4,8,16,24,32)

ENERGY MEASUREMENT FEATURES

- Exceeds IEC62053 / ANSI C12.20 standards
  - 0.1% accuracy in 2000:1 current range
- Line voltage and frequency measurements
- Phase compensation (±5°)
- High frequency outputs proportional to active, reactive, apparent power (AP) or to Irms
- 40~70Hz line frequency range with the same calibration

MICROPROCESSOR FEATURES

- 8052-based core
- Single-cycle 8MIPS (Peak)
- 32.768 kHz external crystal with built in PLL
- Accurate RTC for time-of-use functions
- H/W watchdog timer (WDT)
- External interrupt sources
- SPI / I2C interface for EEPROM
- IrDa/UART/IR I/F for AMR
- Flash security
- 16-Bit timer
- Wake-up from I/O, temperature change, or UART
- 64kB flash memory, 2kB SRAM
- Supply voltage supervisor/monitor with built in SAR ADC
- Serial on board programming/debugging

LCD FEATURES

- Up to 4x25 segment

2. General Descriptions

2.1 Function Block Diagram

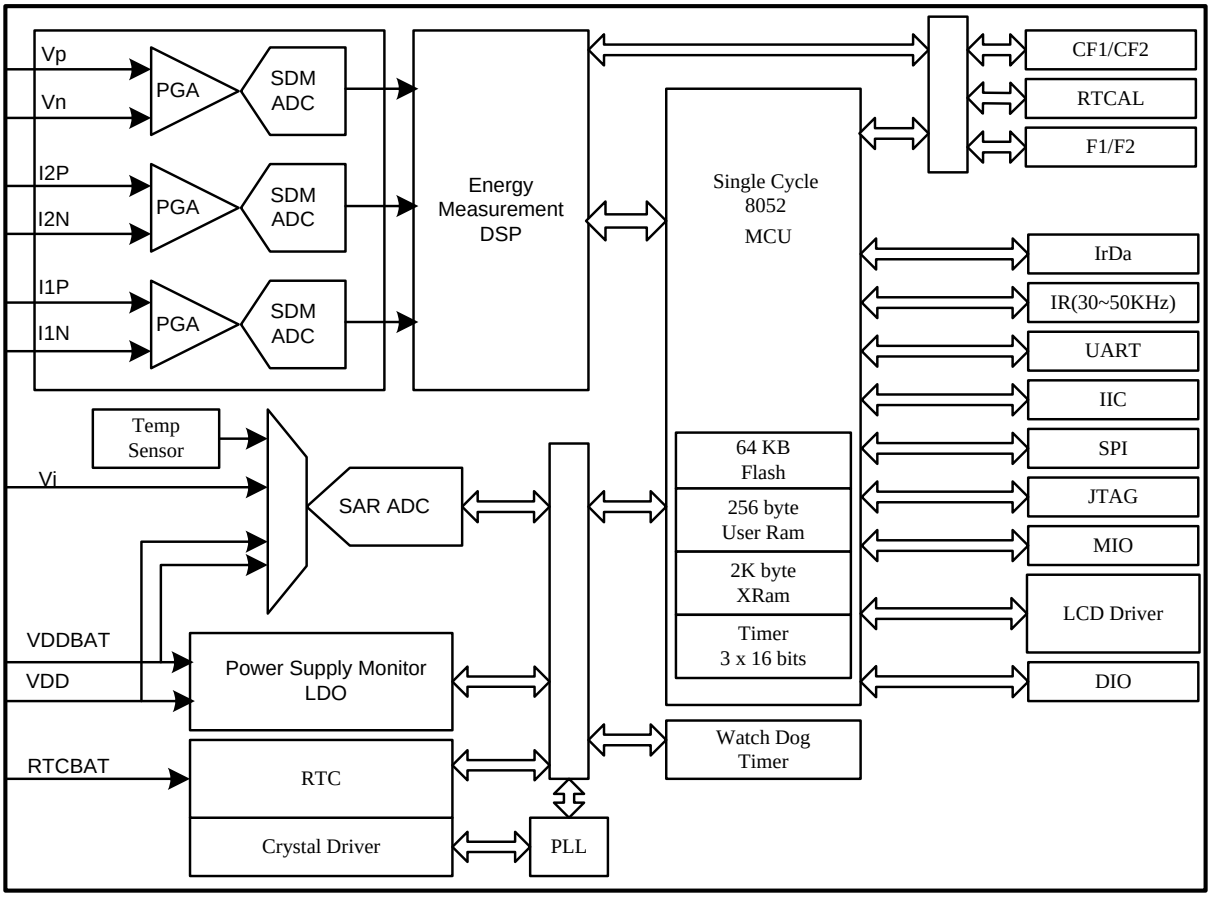


Figure 2-1：Function Block Diagram

2.2 Detail features Description

The PL8331 series of ultra-low power mixed-signal processors consist of several devices featuring different sets of peripherals targeted for energy meter applications. They integrate analog front end and fixed function DSP solution with an enhanced 8052 MCU core, RTC and LCD driver in a single part. The measurement core includes active, reactive, apparent energy calculations, voltage, current RMS, and frequency measurements. This information can be used as energy billing and any necessary application. Also included are a built-in 16-bit timer, LCD segment drive capability, and hardware multiplier.

The PL8331 integrates three PGAs with gain settings from 1x to 32x. Three 24-bit sigma-deltas A/D converters guarantee precision in captured data and enough needed resolution.

The microprocessor functionality includes a single-cycle 8052 core, a real-time clock, UART, an SPI, I2C and JTAG interface. It reduces the program memory size requirement and makes it easy to integrate complicated designs. The programming is very easy and supports multiple ways (SPI or JTAG) without the need of external voltage.

3. Ping Diagram & Pin Descriptions

3.1 Pin Diagram

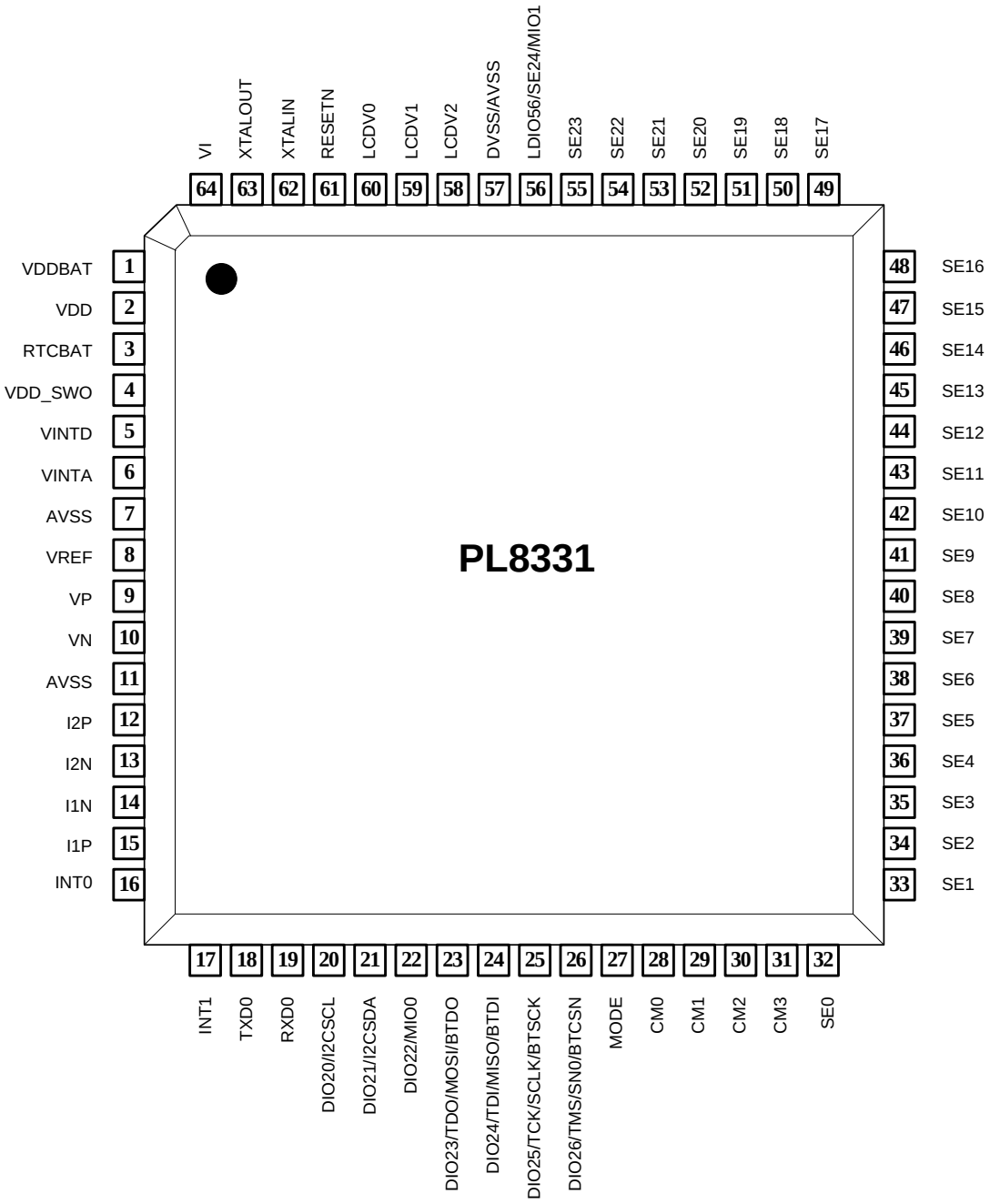


Figure 3-1：64 Pin(7x7) Diagram

3.2 Pin Descriptions

Pin	Symbol	Description
1	VDDBAT	Power supply input from battery with 2.4V to 3.6V range
2	VDD	3V to 3.6V power supply input. This pin should be decoupled with a 10uF capacitor in parallel with a ceramic 100nF capacitor.
3	RTCBAT	Power supply input from battery with 1.8V to 3.6V range
4	VDDSWO	This pin should be decoupled with a 10uF capacitor in parallel with a ceramic 100nF capacitor.
5	VINTD	This pin provides on-chip digital LDO. It should be decoupled with a ceramic 100nF capacitor.
6	VINTA	This pin provides on-chip analog LDO. It should be decoupled with a ceramic 100nF capacitor.
7	AVSS	This pin provides the ground reference for the analog circuitry.
8	VREF	On-chip reference input/output pin. The reference value is 1.2V and should be decoupled with a ceramic 100nF capacitor.
9	VP	Analog Inputs for voltage channel. The maximum differential level is ±500mV
10	VN	Analog Inputs for voltage channel. The maximum differential level is ±500mV
11	AVSS	This pin provides the ground reference for the analog circuitry
12	I2P	Analog Inputs for current channel. The maximum differential level is ±500mV
13	I2N	Analog Inputs for current channel. The maximum differential level is ±500mV
14	I1N	Analog Inputs for current channel. The maximum differential level is ±500mV
15	I1P	Analog Inputs for current channel. The maximum differential level is ±500mV
16	DIO16/INT0	General-Purpose digital I/O External interrupt input 0
17	DIO17/INT1/P1.0	General-Purpose digital I/O External interrupt input 0 / Port P1.0
18	DIO18/ TXD0/P1.1	General-Purpose digital I/O Transmitter Data output port 0(Asynchronous) / Port P1.1
19	DIO19/ RXD0/P1.2	General-Purpose digital I/O Receiver Data input port 0(Asynchronous) /Port P1.2
20	DIO20 I2CSCL	General-Purpose digital I/O Clock pin for I^2C
21	DIO21 I2CSDA	General-Purpose digital I/O Data pin for I^2C
22	DIO22 MIO0	General-Purpose digital I/O PWM/CF/IRCF/RTCAL
23	DIO23	General-Purpose digital I/O

	TDO/MOSI/BTDO	JTAG TDO/SPI MOSI/SPI Flash Card programming mode data output
24	DIO24 TDI/MISO/BTDI	General-Purpose digital I/O JTAG TDI/SPI MISO/ SPI Flash Card programming mode data input
25	DIO25 TCLK/SCLK/BTSCK	General-Purpose digital I/O JTAG TCLK/SPI SCLK/ SPI Flash Card programming mode clock output
26	DIO26 TMS/SN0/BTCSN	General-Purpose digital I/O JTAG TMS/SPI CSN/ SPI Flash Card programming mode CS output
27	MODE	0 : SPI Flash Card programming mode 1 : Normal mode with JTAG port enable
28	CM0	Common output 0 are used for LCD backplanes
29	CM1	Common output 1 are used for LCD backplanes
30	CM2	Common output 2 are used for LCD backplanes
31	CM3	Common output 3 are used for LCD backplanes
32	SE0	LCD segment output 0
33	SE1	LCD segment output 1
34	SE2	LCD segment output 2
35	SE3	LCD segment output 3
36	SE4	LCD segment output 4
37	SE5	LCD segment output 5
38	SE6	LCD segment output 6
39	SE7	LCD segment output 7
40	SE8	LCD segment output 8
41	SE9	LCD segment output 9
42	SE10	LCD segment output 10
43	SE11	LCD segment output 11
44	SE12	LCD segment output 12
45	SE13	LCD segment output 13
46	SE14	LCD segment output 14
47	SE15	LCD segment output 15
48	SE16	LCD segment output 16
49	SE17	LCD segment output 17
50	SE18	LCD segment output 18
51	SE19	LCD segment output 19
52	SE20	LCD segment output 20
53	SE21	LCD segment output 21
54	SE22	LCD segment output 22

55	SE23	LCD segment output 23
56	LDIO56 SE24/MIO1	General-Purpose digital I/O LCD segment output 24/ PWM/CF/IRCF/RTCAL
57	DVSS/AVSS	This pin provides the ground reference for the analog circuitry.
58	LCDV2	Output port for LCD levels. Refer to LCD charge pump section.
59	LCDV	Output port for LCD levels. Refer to LCD charge pump section.
60	LCDV0	Output port for LCD levels. Refer to LCD charge pump section.
61	RESETN	Reset input, active Low
62	XTALIN	Input port for crystal oscillator. Standard or watch crystals can be connected.
63	XTALOUT	Output port of crystal oscillator
64	VI	SAR ADC analog input pin for DC to 1kHz signal

Table 3-1：Pin Descriptions

4. Electrical Characteristics

(All parameters apply at VDD = 3.3 V ± 5%, AGND = DGND = 0 V, Internal Reference, XTAL=32.768 KHz, TA = 25°C)

Parameter	Specifications	Unit	Comments
ACCURACY			Voltage channel with full-scale
Active Energy Measurement Error	0.1	% Reading	signal (±500 mV), 25°C, over a
Phase Error Between Channels			dynamic range of 2000 to 1
PF = 0.8 Capacitive	±0.05	Degrees(°)	
PF = 0.5 Inductive	±0.05	Degrees(°)	
Active Energy Measurement			
Bandwidth	8	KHz	
Reactive Energy Measurement Error	0.5	% Reading	25°C, over a dynamic range of
Vrms Measurement Error	0.5	% Reading	2000 to 1
Vrms Measurement Bandwidth	4	KHz	
Irms Measurement Error	0.5	% Reading	
Irms Measurement Bandwidth	4	KHz	
AC Power Supply Rejection			
Output Frequency Variation (CF)	0.01	% Reading type	
DC Power Supply Rejection			
Output Frequency Variation (CF)	0.01	% Reading type	
ANALOG INPUTS			
Maximum Signal Levels	±0.5	V peak	
		differential	
Input Impedance (DC)	400	kΩ	
Bandwidth (–3 dB)	14	kHz type	
ADC Offset Error	±10	mV max	
Gain Error	±1	% Ideal type	
REFERENCE INPUT			
REFIN/OUT Input Voltage Range	1.2	V	
CLKIN			
Input Clock Frequency	32.768	KHz	
PLL	4	MHz	Note : Selected by internal register
FAULT DETECTION			
Detection Threshold	6.25	%	Adjustable
Input Swap Threshold	6.25	%	Adjustable
Accuracy Fault Mode Operation	0.1	%	
Fault Detection Delay	3	Seconds	

Swap Delay	3	Seconds	
Internal ADCS (Σ-Δ & SAR)			
Power Supply Operation Range	2.4 ~ 3.6	V	
No Mission Codes	18	Bits	
SAR ADC Conversion Rate	500µ	Seconds	
SAR Resolution	10	Bits	
VI Analog Input Maximum Levels	VDD	V	
BATTERY SWITCH OVER			
VDD to VDDBAT Threshold	2.75	V	Typical
VDD to VDDBAT Delay	10	ns	
	30	ms	Active SAR ADC by sensed VI
VDDBAT to VDD Threshold	2.75	V	
VDDBAT to VDD Delay	30	ms	
POWER SUPPLY			
V_{DD}	2.4	V	Min
	3.6	V	Max
VDDBAT	3.6	V	Max
	2.4	V	Min
RTCBAT	3.6	V	Max
	1.8	V	Min
I_{DD}			
Normal Mode	2.2	mA	VDD=3.0V
ADC+Vref	0.3	mA	1 channel
Digital + I/O	0.8	mA	
Sleep Mode	1.1	uA	RTC only / RTCBAT=3.0V
FLASH MEMORY			
Endurance	10,000	Cycles	
Data Retention	20	Years	
CRYSTAL OSCILLATOR			
Frequency	32.768	KHz	
Power On Reset (POR)			
VDD POR			
Detection Threshold	2.7	V	
POR active time out period	30	ms	
VDDSWO POR			
Detection Threshold	2	V	

POR active time out period	15	ms	
VINTD POR			
Detection Threshold	2.1	V	
POR active time out period	15	ms	

Table 4-1：Electrical Characteristics

4.1 Absolute Maximum Rating

TA = 25°C, unless otherwise noted.

Parameter	**Rating**
VDD to DGND	−0.3 V to +3.6 V
VDDBAT to DGND	−0.3 V to +3.6 V
RTCBAT to DGND	−0.3 V to +3.6 V
Input LCD Voltage to AGND, LCDVA, LCDVB, LCDVC[1]	−0.3 V to VDDSWO + 0.3 V
Analog Input Voltage to AGND, VP, VN, IP/IPA, IPB, and IN	−1 V to +1 V
Digital Input Voltage to DGND	−0.3 V to VSWOUT + 0.3 V
Digital Output Voltage to DGND	−0.3 V to VSWOUT + 0.3 V
Operating Temperature Range (Industrial)	−40°C to +80°C
Storage Temperature Range	−65°C to +150°C
64-Lead LQFP, Power Dissipation	
Lead Temperature (Soldering, 30 sec)	300°C

Table 4-2：Absolute Maximum Rating

[1] When used with external resistor divider.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for worst-case condition, that is, a device soldered in a circuit board for surface-mount packages.

Package Type	**θJA θ**	**JC**	**Unit**
64-Lead LQFP	60	20.5	°C/W

Table 4-3：Thermal Resistance

ESD CAUTION	
	**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy [SD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

5. Power Management

5.1 Power Supply Architecture

PL8331 has 3 power supply inputs, VDD, VDDBAT and RTCBAT. VDD require a single 3.3V power supply for full operation. A battery backup with maximum 3.6V can be connected to the VDDBAT input.

Internally, PL8331 connects VDD and VDDBAT to VDDSWO which is used to drive power for internal circuitry. The VDDSWO output pin reflects the voltage at the internal power supply. This pin can also be used to power a limited of peripheral components like EEPROM, hall sensor, etc.

The LDOA and LDOD are on-chip linear regulators and powered by VDDSWO. LDOA is for analog block and LDOD is for digital block. The output voltage can be adjusted for saving power consumption.

PL8331 provides automatic battery switchover between VDD and VDDBAT based on the voltage level detected at VDD. The VBAT_SWITCH flag will be updated when battery switchover occurs and when the VDD power supply is restored.

RTCBAT power is for RTC circuit and 32768Hz crystal driver only.

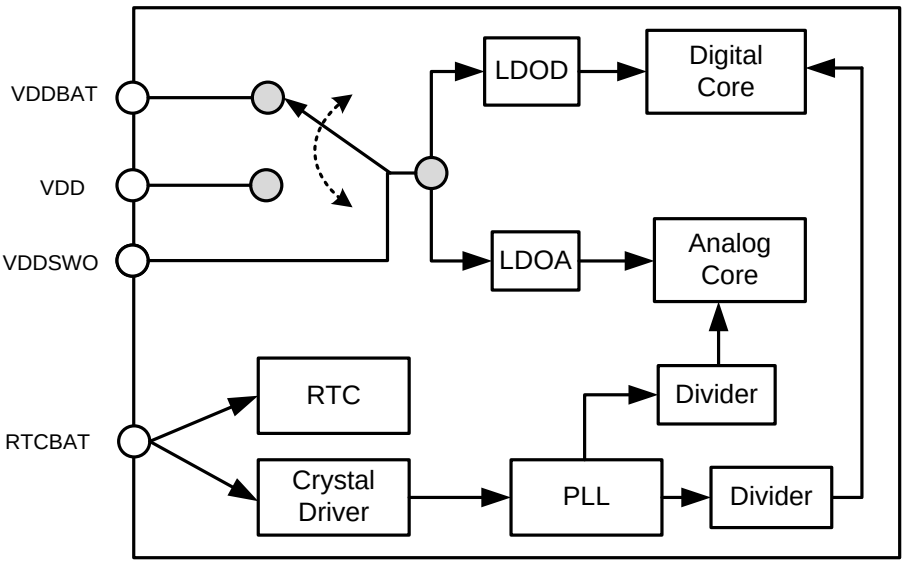


Figure 5-1：Power Supply Architecture

In an energy meter application, VDD(3.3V) is typically generated from the ac line voltage and regulated to 3.3V by a voltage regulator. A 3.3V battery can be connected to VDDBAT and RTCBAT. RTCBAT only supply power for internal hardware calendar and crystal driver.

5.2 Battery Switchover

VDD to VDDBAT

When VDD voltage < 2.75V, VDDSWO switches from VDD to VDDBAT.

VDDBAT to VDD

When VDD voltage > 2.75V, VDDSWO switches back to VDD.

5.3 Power Operation Modes

5.3.1 Normal Mode

VDDSWO is connected to VDD. All of the analog circuitry and digital circuitry are powered by LDOA and LDOD. The default PLL clock frequency established during a power-on reset is 4.096MHz

5.3.2 Battery Mode

VDDSWO is connected to VDDBAT. In this operation mode, MCU and digital blocks are enabled by default, while the ADCs are disabled.

5.3.3 Sleep Mode

This is a very low power consumption mode for use in battery operation. VDDSWO is connected to VDDBAT and all of the digital and analog circuitry powered through LDOA, LDOD regulators are disabled, including the MCU core. Some peripherals are active. The active blocks detect events to wake up. The LCD circuitry can be kept active to show necessary information during sleep mode.

PL8331 provides some scratch pads RAM that are maintained during this mode. These RAM can be used to save data from Normal or Battery mode with entering sleep mode.

PWRHV Control Registers - Indirect Accessing				
Address: PWRHVINDEX(FEh) / Data: PWRHVDATA(FFh)				
SFR-FEh	**SFR-FFh**	**Bits**	**Description**	
20h	**SCRATCH0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCRATCH0[7:0]	7:0	General Purpose register	
21h	**SCRATCH1**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCRATCH1[7:0]	7:0	General Purpose register	
22h	**SCRATCH2**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCRATCH2[7:0]	7:0	General Purpose register	
23h	**SCRATCH3**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCRATCH3[7:0]	7:0	General Purpose register	
24h	**SCRATCH20**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCRATCH20[7:0]	7:0	General Purpose register	
25h	**SCRATCH21**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCRATCH21[7:0]	7:0	General Purpose register	
26h	**SCRATCH22**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCRATCH22[7:0]	7:0	General Purpose register	
27h	**SCRATCH23**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCRATCH23[7:0]	7:0	General Purpose register	
28h	**SCRATCH30**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCRATCH30[7:0]	7:0	General Purpose register	
29h	**SCRATCH31**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCRATCH31[7:0]	7:0	General Purpose register	
2Ah	**SCRATCH32**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCRATCH32[7:0]	7:0	General Purpose register	
2Bh	**SCRATCH33**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCRATCH33[7:0]	7:0	General Purpose register	

Table 5-1：PWRHV Control Registers

5.4 Wakeup Events

In sleep mode, PL8331 can be triggered by the following events:

- Power Restore

  When VDD > 2.75V, VDDSWO will switch from VDDBAT to VDD, and the power operation mode switches to normal mode. This event is maskable.

- RESETN pin

  When RESETN goes low, the power operation mode switches to battery mode. This event is maskable.

- RTC midnight

  When RTC midnight event occurs, the power operation mode switches to battery mode. This event is maskable.

- DIOx pin

  When DIOx goes low or falling edge occurs, the power operation mode switches to battery mode.

- RXn pin

  When a RXn rising or falling edge occurs, the power operation mode switches to battery mode.

- RTC alarm

  When RTC alarm occurs, the power operation mode switches to battery mode.

5.5 Transitioning Between Operation Modes

The operating mode is determined by the power supply connected to VDDSWO. Following describes events that change the operating mode.

5.5.1 Normal Mode to Battery Mode

If VDD < 2.75V, it will enable battery switchover events, and VDDSWO switches to VDDBAT. The ADCs will be disabled automatically by default. To reduce power consumption, the user code can initiate a transition to sleep mode.

Entering Sleep Mode

To reduce power consumption when VDDSWO is connected to VDDBAT, user code can initiate sleep mode by setting registers to shut down the MCU core.

5.5.2 Sleep Mode to Battery Mode

MCU may need to wake up from sleep mode to service wake-up events, and can return to sleep mode by setting registers to shut down the MCU core. Firmware can check VBAT_SWITCH flag to identify if this event happened, then execute wake up events service routine.

5.5.3 Sleep Mode to Normal Mode

If VDD > 2.75V, it will enable battery switchover events, and VDDSWO switches to VDD. When this switch occurs, the MCU code can initiate normal operating mode by identifying VBAT_SWITCH flag.

5.5.4 Battery Mode to Normal Mode

If VDD > 2.75V before MCU enters sleep mode, the operating mode switches to normal mode. When this switch occurs, the code execution continues normally. A software reset can be performed to start from the beginning.

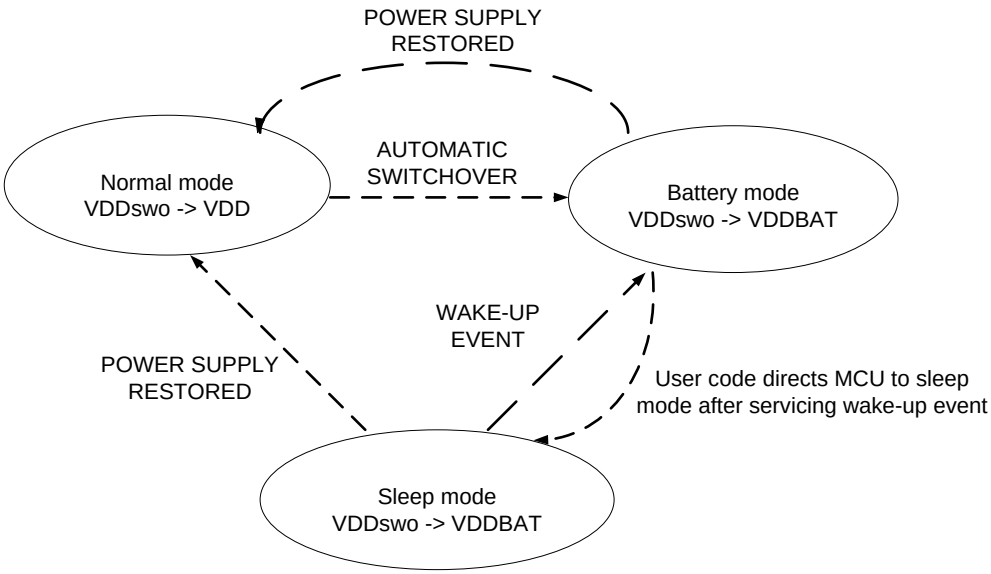


Figure 5-2：Transitioning Between Operation Modes State Machine

5.6 Power Supply Indication Flag

VBAT_SWITCH=1 WDDSWO power by VDDBAT pin.

VBAT_SWITCH=0 WDDSWO power by VDD pin.

PWRHV Control Registers - Indirect Accessing				
Address: PWRHVINDEX(FEh) / Data: PWRHVDATA(FFh)				
SFR-FEh	**SFR-FFh**	**Bits**	**Description**	
83h	**ANAPWR_CTL3**	**7:0**	**Default : 0x00**	**Access : RO**
	VBAT_SWITCH	2	1 = VDDSWO power source is from VDDBAT	

Table 5-2：Power Supply Indication Flag

The VBAT_SWITCH bit indicates what VDDSWO is connected to. This bit can be used to control program flow. Because code execution always starts at the power-on reset vector, this bit can be tested to determine which power supply is being used and branch to normal code execution or to wake up event code execution.

5.7 SDM ADCs Power Control

In metering application, ADC channel may not be used in some conditions like neutral missing. Or application may only need 1voltage/1current input, hence PL8331 provides power down control for saving current consumption. PLL and Vref also can be powered down in sleep mode to save battery power.

PWRLV Control Registers - Indirect Accessing				
Address: PWRLVINDEX(CEh) / Data: PWRLVDATA(CFh)				
SFR-CEh	**SFR-CFh**	**Bits**	**Description**	
2Eh	**ANA_PD0**	**7:0**	**Default : 0xFE**	**Access : R/W**
		7	I2 ADC power down → 1: power down	
		6:1	I1 ADC power down → 1: power down	
		0	Vref power down → 1: power down	
2Fh	**ANA_PD1**	**7:0**	**Default : 0xFF**	**Access : R/W**
		7:5	V ADC power down → 1: power down	
		4:0	I2 ADC power down → 1: power down	
30h	**ANA_PD2**	**7:0**	**Default : 0x07**	**Access : R/W**
		2:0	V ADC power down → 1: power down	
31h	**ANA_CTL13**	**7:0**	**Default : 0x01**	**Access : R/W**
		3	PLL power down 1: power down	

Table 5-3：ADCs Power Control Registers

6. MCU Core Architecture

The PL8331 has one 8052 MCU core – a fast single-chip configurable 8-bit microcontroller which executes ASM51 instruction set. This MCU is equipped with peripherals functionally compatible with peripherals of standard 8052. The peripherals are accessed by MCU with SFR (special function register) accession. The SFR (special function register) space is mapped into the upper 128 bytes of internal data memory space and is accessed by direct addressing only. It provides an interface between the CPU and all on-chip peripherals.

The structure of the blocks consists of：

TIMER0 – provides a flexible 16-bit timer/counter with control and status register.

TIMER1 – provides a flexible 16-bit timer/counter with control and status register.

TIMER2 – contains the 16-bit Timer-2 with Compare-Unit (4 compare modules), control and status register.

The MCU manipulates operands in three memory spaces; these are the 256-bytes internal data memory (RAM), the 2k-bytes external data memory (embedded external-RAM), and the 64k-bytes internal program memory (FLASH ROM).

6.1 8052 REGISTERS

The most widely used registers are A (accumulator), B, R0, R1, R2, R2, R3, R4, R5, R6, R7, PC (program counter), SP, PSW, and DPTR (data pointer).

6.1.1 Accumulator

The instruction uses the accumulator as both source and destination for calculations, logic operations and moves.

6.1.2 B register

The B register is used by the multiply and divide instructions, MUL AB and DIV AB, to hold one of the operands.

6.1.3 R0 ~ R7 registers

The registers R0 ~ R7 are implemented by Register-Bank. There are total 4 Register-Banks among MCU. These registers are convenient for temporary storage of mathematical operands. The four register banks are located in the first 32 bytes of Internal Data Memory RAM. The RS0 and RS1 bits in the program status word SFR (PSW, 0xD0) decide which bank is active.

6.1.4 Program Counter

The program counter points to the address of the next instruction to be executed. The program counter in the 8051 is 16 bits wide. The MCU wake up at memory address 0000 when it is powered up or system reset.

6.1.5 Stack Point Register

The 8-bit Stack Pointer is an internal SFR used to address the On-chip Memory (IRAM) when operating as a software stack. The Stack Pointer points to the last used location of the stack. When MCU is powered up, the SP contains the value 07.

6.1.6 PSW (program status word) Register

The PSW register is referred to as flag register. Only 6 bits of it are used by MCU and defined as CY (carry), AC (auxiliary carry), RS1, RS0 (Register Bank Select), OV (overflow), and P (parity).

6.1.7 DPTR (data pointer register)

Data pointers accelerate data blocks moving. Data Pointer Register (DPTR) is a 16-bit register that is used to address external memory or peripherals.

There are 2 data pointers in MCU. Only one of them can be active at a given moment and it is selected using the “dpsel” register. The active Data Pointer Register can be accessed as SFRs: DPH, DPL.

6.2 Memory Overview

The PL8331 has four memory spaces, program memory, internal data memory, embedded external data memory and SFR (Special Function Register).

6.2.1 Program Memory

The program memory address space comprises of an internal 64k-byte memory space. The embedded Flash can be erased/programmed by SPI-interface/UART download operation.

6.2.2 Internal Data Memory

The internal 256-bytes data memory is divided into two parts: 0 to 127 RAM and 128 to 255 RAM. They can be addressed as below:

- RAM 0 to 127 can be addressed directly and indirectly as in the 80C51. Address pointers are R0 and R1 of the selected register bank.

- RAM 128 to 255 can only be addressed indirectly. Address pointers are R0 and R1 of the selected register bank.

6.2.3 Embedded External Data Memory

The embedded external Data Memory has 2k-bytes RAM space. It is indirectly addressable locations 0 to 2047 by the MOVX instructions. Address pointers are R0 and R1 of the selected register bank and DPTR.

6.2.4 SFRs

Through direct addressing at address location 128-255, SFRs control the most parts of peripherals like traditional 8052, the memory spaces must be addressed by separated address mode. The chart below shows the methods.

6.3 Addressing Mode

The MCU supports eight addressing modes.

- Register Addressing
- Direct Addressing
- Indirect Addressing
- Immediate Addressing
- Indirect Addressing with Displacement
- Relative Addressing
- Page Addressing
- Extended Addressing

6.4 Instruction Set

The MCU instructions are binary code compatible and perform the same functions as industry standard 8052.

The tables below give a summary of the instruction cycles.

Mnemonic	Description	Code	Bytes	Cycles
Arithmetic operations				
ADD A,Rn	Add register to accumulator	0x28-0x2F	1	2
ADD A,direct	Add directly addressed data to accumulator	0x25	2	3
ADD A,@Ri	Add indirectly addressed data to accumulator	0x26-0x27	1	4
ADD A,#data	Add immediate data to accumulator	0x24	2	2
ADDC A,Rn	Add register to accumulator with carry	0x38-0x3F	1	2
ADDC A,direct	Add directly addressed data to accumulator with carry	0x35	2	3
ADDC A,@Ri	Add indirectly addressed data to accumulator with carry	0x36-0x37	1	4
ADDC A,#data	Add immediate data to accumulator with carry	0x34	2	2
SUBB A,Rn	Subtract register from accumulator with borrow	0x98-0x9F	1	2
SUBB A,direct	Subtract directly addressed data from accumulator with borrow	0x95	2	2
SUBB A,@Ri	Subtract indirectly addressed data from accumulator with borrow	0x96-0x97	1	4
SUBB A,#data	Subtract immediate data from accumulator with borrow	0x94	2	2
INC A	Increment accumulator	0x04	1	1
INC Rn	Increment register	0x08-0x0F	1	3
INC direct	Increment directly addressed location	0x05	2	4
INC @Ri	Increment indirectly addressed location	0x06-0x07	1	5
INC DPTR	Increment data pointer	0xA3	1	1
DEC A	Decrement accumulator	0x14	1	1
DEC Rn	Decrement register	0x18-0x1F	1	3
DEC direct	Decrement directly addressed location	0x15	2	4
DEC @Ri	Decrement indirectly addressed location	0x16-0x17	1	5
MUL AB	Multiply A and B	0xA4	1	4
DIV	Divide A by B	0x84	1	4
DA A	Decimally adjust accumulator	0xD4	1	1
Logic operations				
ANL A,Rn	AND register to accumulator	0x58-0x5F	1	2
ANL A,direct	AND directly addressed data to accumulator	0x55	2	3

Mnemonic	Description	Code	Bytes	Cycles
ANL A,@Ri	AND indirectly addressed data to accumulator	0x56-0x57	1	4
ANL A,#data	AND immediate data to accumulator	0x54	2	2
ANL direct,A	AND accumulator to directly addressed location	0x52	2	4
ANL direct,#data	AND immediate data to directly addressed location	0x53	3	4
ORL A,Rn	OR register to accumulator	0x48-0x4F	1	2
ORL A,direct	OR directly addressed data to accumulator	0x45	2	3
ORL A,@Ri	OR indirectly addressed data to accumulator	0x46-0x47	1	4
ORL A,#data	OR immediate data to accumulator	0x44	2	2
ORL direct,A	OR accumulator to directly addressed location	0x42	2	4
ORL direct,#data	OR immediate data to directly addressed location	0x43	3	4
XRL A,Rn	Exclusive OR register to accumulator	0x68-0x6F	1	2
XRL A,direct	Exclusive OR directly addressed data to accumulator	0x65	2	3
XRL A,@Ri	Exclusive OR indirectly addressed data to accumulator	0x66-0x67	1	4
XRL A,#data	Exclusive OR immediate data to accumulator	0x64	2	2
XRL direct,A	Exclusive OR accumulator to directly addressed location	0x62	2	4
XRL direct,#data	Exclusive OR immediate data to directly addressed location	0x63	3	4
CLR A	Clear accumulator	0xE4	1	1
CPL A	Complement accumulator	0xF4	1	1
RL A	Rotate accumulator left	0x23	1	1
RLC A	Rotate accumulator left through carry	0x33	1	1
RR A	Rotate accumulator right	0x03	1	1
RRC A	Rotate accumulator right through carry	0x13	1	1
SWAP A	Swap nibbles within the accumulator	0xC4	1	1
Data transfer operations				
MOV A,Rn	Move register to accumulator	0xE8-0xEF	1	1
MOV A,direct	Move directly addressed data to accumulator	0xE5	2	3
MOV A,@Ri	Move indirectly addressed data to accumulator	0xE6-0xE7	1	4
MOV A,#data	Move immediate data to accumulator	0x74	2	2
MOV Rn,A	Move accumulator to register	0xF8-0xFF	1	1
MOV Rn,direct	Move directly addressed data to register	0xA8-0xAF	2	4
MOV Rn,#data	Move immediate data to register	0x78-0x7F	2	2

Mnemonic	Description	Code	Bytes	Cycles
MOV direct,A	Move accumulator to direct	0xF5	2	2
MOV direct,Rn	Move register to direct	0x88-0x8F	2	3
MOV direct1,direct2	Move directly addressed data to directly addressed location	0x85	3	4
MOV direct,@Ri	Move indirectly addressed data to directly addressed location	0x86-0x87	2	5
MOV direct,#data	Move immediate data to directly addressed location	0x75	3	3
MOV @Ri,A	Move accumulator to indirectly addressed location	0xF6-0xF7	1	3
MOV @Ri,direct	Move directly addressed data to indirectly addressed location	0xA6-0xA7	2	4
MOV @Ri,#data	Move immediate data to in directly addressed location	0x76-0x77	2	3
MOV DPTR,#data16	Load data pointer with a 16-bit immediate	0x90	3	3
MOVC A,@A+DPTR	Load accumulator with a code byte relative to DPTR	0x93	1	4
MOVC A,@A+PC	Load accumulator with a code byte relative to PC	0x83	1	4
MOVX A,@Ri	1) Move external RAM (8-bit addr.) to accumulator	0xE2-0xE3	1	5-12
MOVX A,@DPTR	1) Move external RAM (16-bit addr.) to accumulator	0xE0	1	4-11
MOVX @Ri,A	1) Move accumulator to external RAM (8-bit addr.)	0xF2-0xF3	1	6-13
MOVX @DPTR,A	1) Move accumulator to external RAM (16-bit addr.)	0xF0	1	5-12
PUSH direct	Push directly addressed data onto stack	0xC0	2	4
POP direct	Pop directly addressed location from stack	0xD0	2	3
XCH A,Rn	Exchange register with accumulator	0xC8-0xCF	1	2
XCH A,direct	Exchange directly addressed location with accumulator	0xC5	2	3
XCH A,@Ri	Exchange indirect RAM with accumulator	0xC6-0xC7	1	4
XCHD A,@Ri	Exchange low-order nibbles of indirect and accumulator	0xD6-0xD7	1	5
Program branches				
ACALL addr11	Absolute subroutine call	xxx10001b	2	4
LCALL addr16	Long subroutine call	0x12	3	4
RET	Return from subroutine	0x22	1	5
RETI	Return from interrupt	0x32	1	5

Mnemonic	Description	Code	Bytes	Cycles
AJMP addr11	Absolute jump	xxx00001b	2	3
LJMP addr16	Long jump	0x02	3	4
SJMP rel	Short jump (relative address)	0x80	2	3
JMP @A+DPTR	Jump indirect relative to the DPTR	0x73	1	3
JZ rel	Jump if accumulator is zero	0x60	2	3
JNZ rel	Jump if accumulator is not zero	0x70	2	3
JC rel	Jump if carry flag is set	0x40	2	3
JNC	Jump if carry flag is not set	0x50	2	3
JB bit,rel	Jump if directly addressed bit is set	0x20	3	5
JNB bit,rel	Jump if directly addressed bit is not set	0x30	3	5
JBC bit,rel	Jump if directly addressed bit is set and clear bit	0x10	3	5
CJNE A,direct,rel	Compare directly addressed data to accumulator and jump if not equal	0xB5	3	5
CJNE A,#data,rel	Compare immediate data to accumulator and jump if not equal	0xB4	3	4
CJNE Rn,#data,rel	Compare immediate data to register and jump if not equal	0xB8-0xBF	3	4
CJNE @Ri,#data,rel	Compare immed. to ind. and jump if not equal	B6-B7	3	6
DJNZ Rn,rel	Decrement register and jump if not zero	D8-DF	2	4
DJNZ direct,rel	Decrement directly addressed location and jump if not zero	D5	3	5
NOP	No operation	00	1	1
CLR C	Clear carry flag	0xC3	1	1
CLR bit	Clear directly addressed bit	0xC2	2	4
SETB bit	Set directly addressed bit	0xD2	2	4
CPL C	Complement carry flag	0xB3	1	1
CPL bit	Complement directly addressed bit	0xB2	2	4
ANL C,bit	AND directly addressed bit to carry flag	0x82	2	3
ANL C,/bit	AND complement of directly addressed bit to carry	0xB0	2	3
ORL C,bit	OR directly addressed bit to carry flag	0x72	2	3
ORL C,/bit	OR complement of directly addressed bit to carry	0xA0	2	3
MOV C,bit	Move directly addressed bit to carry flag	0xA2	2	3
MOV bit,C	Move carry flag to directly addressed bit	0x92	2	4

Table 6-1：Instruction Set

6.4.1 Read-Modify-Write

Some instructions are used to read a byte from I/O port (P0-P3), modify it and rewrite it back. They are called "read-modify-write" instructions. These instructions read the latch rather than the pin.

Mnemonic	Description	Code	Bytes	Cycles
ANL direct,A	AND accumulator to direct	0x52	2	3
ANL direct,#data	AND immediate data to direct	0x53	3	4
ORL direct,A	OR accumulator to direct	0x42	2	3
ORL direct,#data	OR immediate data to direct	0x43	3	4
XRL direct,A	Exclusive OR accumulator to direct	0x62	2	3
XRL direct,#data	Exclusive OR immediate data to direct	0x63	3	4
JBC bit, rel	Jump if bit is set and clear bit	0x10	3	4
CPL bit	Complement bit	0xB2	2	3
INC direct	Increment direct	0x05	2	3
INC @Ri	Increment indirect	0x06-0x07	1	3
DEC direct	Decrement direct	0x15	2	3
DEC @Ri	Decrement indirect	0x16-0x17	1	3
DJNZ direct,rel	Decrement and jump if not zero	0xD5	3	4
MOV bit,C	Move carry flag to direct bit	0x92	2	3
CLR bit	Clear bit	0xC2	2	3
SETB bit	Set bit	0xD2	2	3

Table 6-2：Read-Modify-Write Instruction

6.4.2 Special Function Register Description

SFR Register – E0/F0/D0/80/90/A0/B0/81/87h

Basic MCU Register

Address	Mnemonic	Bits	Description	
E0h	**ACC**	**7:0**	**Default : 0x00**	**Access : R/W**
	A	7:0	**Accumulator** Accumulator is used by most of the 8051 instructions to hold the operand and to store the result of an operation	
F0h	**B**	**7:0**	**Default : 0x00**	**Access : R/W**
	B	7:0	**B Register** The B register is used during multiplying and division instructions	
D0h	**PSW**	**7:0**	**Default : 0x00**	**Access : R/W**
	cy	7	**Carry flag** Carry bit in arithmetic operations and accumulator for Boolean operations.	
	ac	6	**Auxiliary Carry flag** Set if there is a carry-out from 3rd bit of Accumulator in BCD operations	
	f0	5	**General purpose Flag 0** General purpose flag available for user	
	rs1	4	**Register bank select control bit 1** It is used to select working register bank	
	rs0	3	**Register bank select control bit 0** It is used to select working register bank	
	ov	2	**Overflow flag** Set in case of overflow in Accumulator during arithmetic operations	
	f1	1	**General purpose Flag 1** General purpose flag available for user	
	p	0	**Parity flag** Reflects the number of ‘1’s in the Accumulator. P = ‘1’ if Accumulator contains an odd number of ‘1’s P = ‘0’ if Accumulator contains an even number of ‘1’s	

Address	Mnemonic	Bits	Description	
80h	**P0**	**7:0**	**Default : 0xFF**	**Access : R/W**
	P0	7:0	**Port 0** The port is open-drain and requires pull-ups.	
90h	**P1**	**7:0**	**Default : 0xFF**	**Access : R/W**
	P1	7:0	**Port 1** The port is open-drain and requires pull-ups.	
a0h	**P2**	**7:0**	**Default : 0xFF**	**Access : R/W**
	P2	7:0	**Port 2** The port is open-drain and requires pull-ups.	
b0h	**P3**	**7:0**	**Default : 0xFF**	**Access : R/W**
	P3	7:0	**Port 3** The port is open-drain and requires pull-ups.	
81h	**SP**	**7:0**	**Default : 0x07**	**Access : R/W**
	SP	7:0	**Stack Pointer** This register points to the top of stack in internal data memory space	
87h	**PCON**	**7:0**	**Default : 0x08**	**Access : R/W**
	smod	7	UART 0 baud rate select As UART0 is in mode2 (sm0=1 , sm1=0) , Smod = 1 : baud rate is Fclk/32 Smod= 0 : baud rate is Fclk/64	
	wdt_tm	6	**Watchdog Timer Test Mode flag** When set to 1, the fclk/12 divider at the input of the Watchdog Timer is skipped	
	fix_zero	5:4	NO use , fix zero This 2 bits must be fixed as ‘00’.	
	fix_one	3	NO use , fix one This bit must be fixed as ‘1’.	
	fix_zero	2:0	NO use , fix zero This 3 bits must be fixed as ‘000’.	

Table 6-3：Basic MCU Registers

6.5 Data pointer

The Data Pointer is a 16-bit register used as indirect address source for MOVX @DPTR, MOVC @A+DPTR or JMP @A+DPTR instructions. There are two data pointers in MCU. They are accessible as four SFRs at locations 0x82 (DPL) , 0x83 (DPH) and 0x84 (DPL1) , 0x85 (DPH1). The “dps” affects only MOVX @DPTR, JMP @A+DPTR, MOVC A,@A+DPTR, INC DPTR, MOV DPTR,#data16. There is a dedicated arithmetic unit implemented to improve the DPTR-based data transfers.

The additional SFR named “dpc” located at address 0x93 chooses the type of DPTR auto-modification. The auto-modification is triggered by each DPTR-based data transfer instruction (MOVX A,@DPTR or MOVX @DPTR,A). The DPTR-related arithmetic unit performs the following operations on current DPTR (chosen by “dps”) depending on “dpc” settings:

dpc.2	dpc.1	Dpc.0	operation	Description
x	x	0	-	No auto-modifications
0	0	1	+1	Auto-increment by one
0	1	1	-1	Auto-decrement by one
1	0	1	+2	Auto-increment by two
1	1	1	-2	Auto-decrement by two

Table 6-4：DPC registers

SFR Register – 82-85h/92-93h

Data Pointer Register

Address	Mnemonic	Bits	Description	
92h	**DPS**	**7:0**	**Default : 0x00**	**Access : R/W**
	NU	7:1	NO USED	
	DPTR_SELECT	0	0 : DPTR is DPH and DPL 1: DPTR is DPH1 and DPL1	
93h	**DPC**	**7:0**	**Default:0x00**	**Access : R/W**
	NU	7:6	NO USED	
	NXT_DPTR	5:3	**Next Data Pointer Selection** The contents of this field is loaded to the “DPTR_SELECT” field of “dps” register after each MOVX @DPTR instruction. Note that this feature is always enabled, therefore for each of the “dps” registers this field has to contain a different value pointing to itself so that the auto-switching does not occur with default (reset) values.	

Address	Mnemonic	Bits	Description	
	DPC.2	2	**Auto-modification size** When zero, the current DPTR is automatically modified by 1 after each MOVX @DPTR instruction when dps.0=1. When one, the current DPTR is automatically modified by 2 after each MOVX @DPTR instruction when dps.0=1.	
	DPC.1	1	**Auto-modification direction** When zero, the current DPTR is automatically incremented after each MOVX @DPTR instruction when dps.0=1. When one, the current DPTR is automatically decremented after each MOVX @DPTR instruction when dps.0=1.	
	DPC.0	0	**Auto-modification enable** When set, enables auto-modification of the current DPTR after each MOVX @DPTR instruction	
82h	**DPL**	**7:0**	**Default:0x00**	**Access : R/W**
			The low byte of DPTR0 . When “DPTR_SELECT” =0 , DPL can be accessed by MOVC/MOVX instruction.	
83h	**DPH**	**7:0**	**Default:0x00**	**Access : R/W**
			The high byte of DPTR0 . When “DPTR_SELECT” =0 , DPH can be accessed by MOVC/MOVX instruction.	
84h	**DPL1**	**7:0**	**Default:0x00**	**Access : R/W**
			The low byte of DPTR1 . When “DPTR_SELECT” =1 , DPL1 can be accessed by MOVC/MOVX instruction.	
85h	**DPH1**	**7:0**	**Default:0x00**	**Access : R/W**
			The high byte of DPTR1 . When “DPTR_SELECT” =1 , DPH1 can be accessed by MOVC/MOVX instruction.	

Table 6-5：Data Pointer SFR

6.6 Watchdog Timer

The Watchdog Timer contains 15-bit counter, reload register and the clock can be pre-scaled by 2, 12, 16 according with some control bits of SFR. The below figure depicts the block diagram:

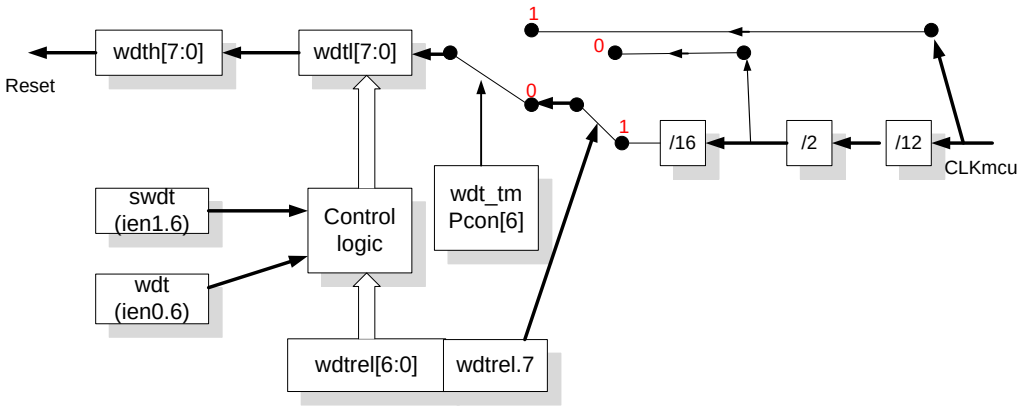


Figure 6-1：Watchdog Timer Block Diagram

The count rate of the Watchdog Timer depends on the MSB of the “wdtrel” register. When the “wdtrel.7”=1, the Watchdog Timer is incremented every 12*32=384 clock cycles, which makes the whole period to be 12*32*256*128=12582912 clock cycles long. When the “wdtrel.7”=0, the Watchdog Timer is incremented every 12*2=24 clock cycles, which makes the whole period to be 12*2*256*128= 786432 clock cycles long. When the “wdt_tm” test mode input is set to 1, the count rate of the Watchdog Timer is CLKmcu clock rate (all dividers – 1/12, 1/8, ½, 1/16 are omitted) to shorten the time required for the Watchdog to overflow (for verification purposes).

Start procedure

The only way to start the watchdog is by software. The instructions below will start the watchdog:

```
MOV     WDTREL, #07FH    ;setup the timer initial value
SETB    IEN0.6           ;start or refresh WDT timer
SETB    IEN1.6
```

Once started, the Watchdog Timer can only be stopped by the hardware reset.

When watchdog counter enters the state of 7FFCh, the internal reset is generated as the “wdts” output is active. The “wdts” flag of the “ip0” register is also set upon the Watchdog Timer reset, while it is cleared upon external hardware “reset” signal. The “wdts” signal does not reset the Watchdog, which remains running. When it overflows from 7FFFh to 0000h, the “wdts” output is deactivated, while the “wdts” flag of “ip0” register remains set to allow the software to determine whether the reset was caused by external input or by the Watchdog timeout.

To prevent resetting the MCU, the programmer must refresh the watchdog regularly. The method to refresh is

the same as the method to start. The first instruction sets the “wdt” bit of the “ien0” register and the second one sets the “swdt” flag of the “ien1” register. The maximum allowed delay between setting the “wdt” and “swdt” is 1 instruction cycles (that means the instructions which set both flags are not separated with any other instruction).

Watchdog timer Register (SFR Register- 86h)

Address	Mnemonic	Bits	Description	
86h	**wdtrel**	**7:0**	**Default : 0x00**	**Access : R/W**
	wdtrel.7	7	**Prescaler select** When set, the watchdog is clocked through an additional divide-by-16 prescaler.	
	wdtrelvle	6:0	**Watchdog reload value** Reload value for the highest 7 bits of the watchdog timer. This value is loaded to the Watchdog Timer when a refresh is triggered by a consecutive setting of bits wdt (ien0.6) and swdt (ien1.6).	
A8h	**IEN0**	**7:0**	**Default : 0x00**	**Access : R/W**
	wdt	6	**Watchdog timer refresh flag** Set to initiate a refresh of the watchdog timer. Must be set directly before swdt (ien1.6) is set to prevent an unintentional refresh of the watchdog timer. The wdt bit is cleared by hardware after the next instruction executed after the one that had set this bit, so that watchdog refresh can be done only with direct sequence of setting wdt and swdt.	
B8h	**IEN1**	**7:0**	**Default : 0x00**	**Access : R/W**
	swdt	6	**Watchdog timer start/refresh flag.** Set to activate/refresh the watchdog timer. When set directly after setting wdt (ien0.6), a watchdog timer refresh is performed. This bit is immediately cleared by hardware.	

Table 6-6：Watchdog Timer SFR

6.7 Timer0 & Timer1

Timer0 and Timer1 can be used either as timers or as event counters.

In mode 0:

Timer0 and Timer1 are configured as a 13-bit register. The upper 3 bits of “tl0” should be ignored.

In mode 1:

The Timer0 and Timer1 are configured as a 16-bit register.

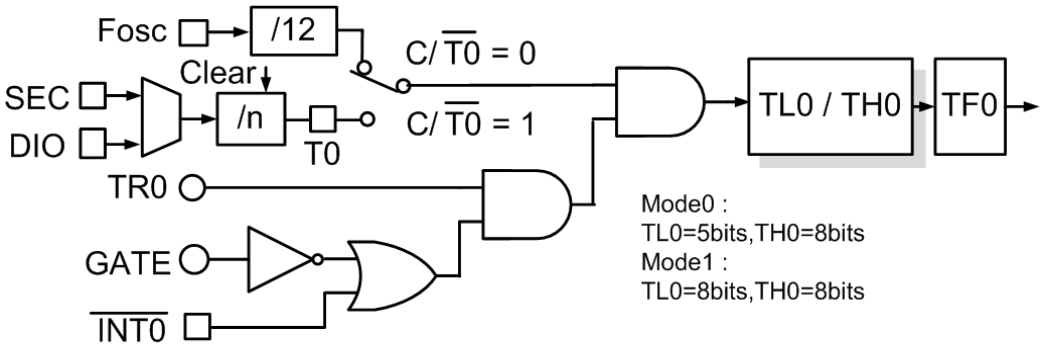


Figure 6-2：Timer0 in Mode0/Mode1

In mode 2:

The Timer0 and Timer1 are configured as an 8-bit register with auto-reload.

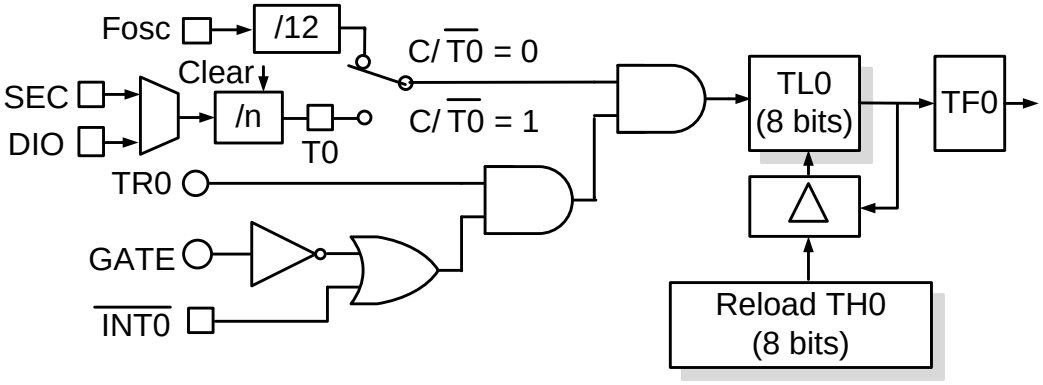


Figure 6-3：Timer0 in mode0/mode1

In mode 3:

Timer 0 is configured as one 8-bit timer/counter and one 8-bit timer.

In mode 3 Timer1 is stopped.

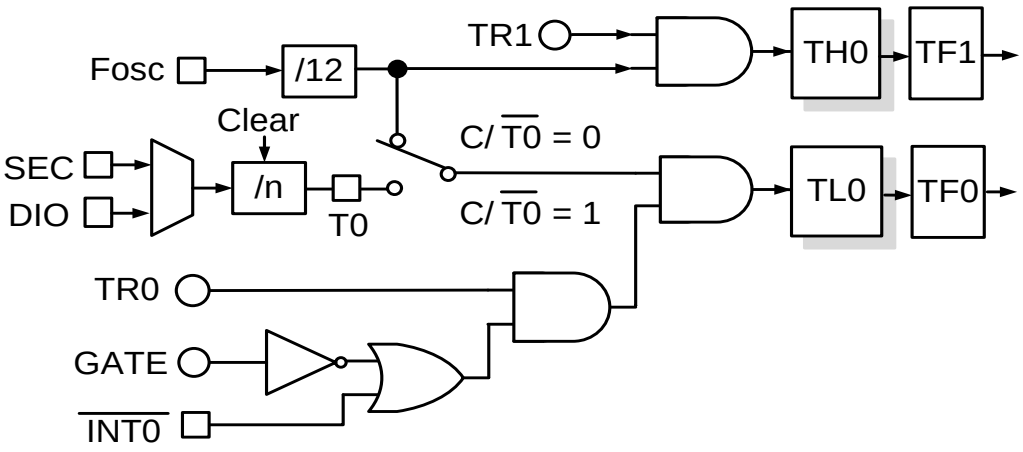


Figure 6-4：Timer0 in Mode 3

6.7.1 SFR Register – 88h~8Dh

Timer0 / Timer1 Register

Address	Mnemonic	Bits	Description	
88h	**TCON**	**7:0**	**Default : 0x00**	**Access : R/W**
	tf1	7	**Timer 1 overflow flag** Bit set by hardware when Timer1 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.	
	tr1	6	**Timer1 Run control** Set by the user to turn on Timer/Counter 1. If cleared, Timer 1 stops.	
	tf0	5	**Timer 0 overflow flag** Bit set by hardware when Timer 0 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.	
	tr0	4	**Timer0 Run control** Set by the user to turn on Timer/Counter 1. If cleared, Timer 1 stops.	
	ie1	3	**External interrupt 1 flag** Set by hardware, when external interrupt int1 (edge/level, depending on settings) is observed. Cleared by hardware when interrupt is processed.	
	it1	2	**External interrupt 1 type control** If set, external interrupt 1 is activated at falling edge on input pin. If cleared, external interrupt 1 is activated at low level on input pin.	
	ie0	1	**External interrupt 0 flag** Set by hardware, when external interrupt int0 (edge/level, depending on settings) is observed. Cleared by hardware when interrupt is processed.	
	it0	0	**External interrupt 0 type control** If set, external interrupt 0 is activated at falling edge on input pin. If cleared, external interrupt 0 is activated at low level on input pin.	
89h	**TMOD**	**7:0**	**Default : 0x00**	**Access : R/W**

Address	Mnemonic	Bits	Description	
	timer1gate	7	**Timer 1 gate control** If set, enables external gate control (pin “int(1)”) for Counter 1. Is incremented every falling edge on “t1” pin.	
	timer1 c/t	6	**Timer 1 counter/timer select** Selects Timer or Counter operation. When set to 1, a Counter operation is performed, when cleared to 0, the Timer/Counter 1 will function as a Time.	
	Timer1 m1	5	**Mode selection of timer1** m1 = 0 , m0 = 0 : mode 0 , 13-bit timer mode m1 = 0 , m0 = 1 : mode 1 , 16-bit timer mode m1 = 1 , m0 = 0 : mode 2 , 8-bit auto reload m1 = 1 , m0 = 1 : mode 3 , timer1 stop	
	Timer1 m0	4		
	Timer0gate	3	**Timer 0 gate control** If set, enables external gate control (pin “int(0)”) for Counter 0. Is incremented every falling edge on “t0” pin.	
	Timer0 c/t	2	**Timer 0 counter/timer select** Selects Timer or Counter operation. When set to 1, a Counter operation is performed, when cleared to 0, the Timer/Counter 0 will function as a Time.	
	Timer0 m1	1	**Mode selection of timer1** m1 = 0 , m0 = 0 : mode 0 , 13-bit timer mode m1 = 0 , m0 = 1 : mode 1 , 16-bit timer mode m1 = 1 , m0 = 0 : mode 2 , 8-bit auto reload m1 = 1 , m0 = 1 : mode 3 , timer0 split timer	
	Timer0 m0	0		
8Ah	**TL0**	**7:0**	**Default : 0x00**	**Access : R/W**
	TL0	7	Low byte of Timer 0	
8Bh	**TL1**	**7:0**	**Default : 0x00**	**Access : R/W**
	TL1	7	Low byte of Timer 1	
8Ch	**TH0**	**7:0**	**Default : 0x00**	**Access : R/W**
	TH0	7	High byte of Timer 0	
8Dh	**TH1**	**7:0**	**Default : 0x00**	**Access : R/W**
	TH1	7	High byte of Timer 1	

Table 6-7：TIMER0 & TIMER1 SFR

6.8 Timer2

Timer 2 has more functions than timer0/timer1. It can be configured for either counter or timer and compare operation. The CO[0] , CO[1] , CO[2] and CO[3] are the compare output.

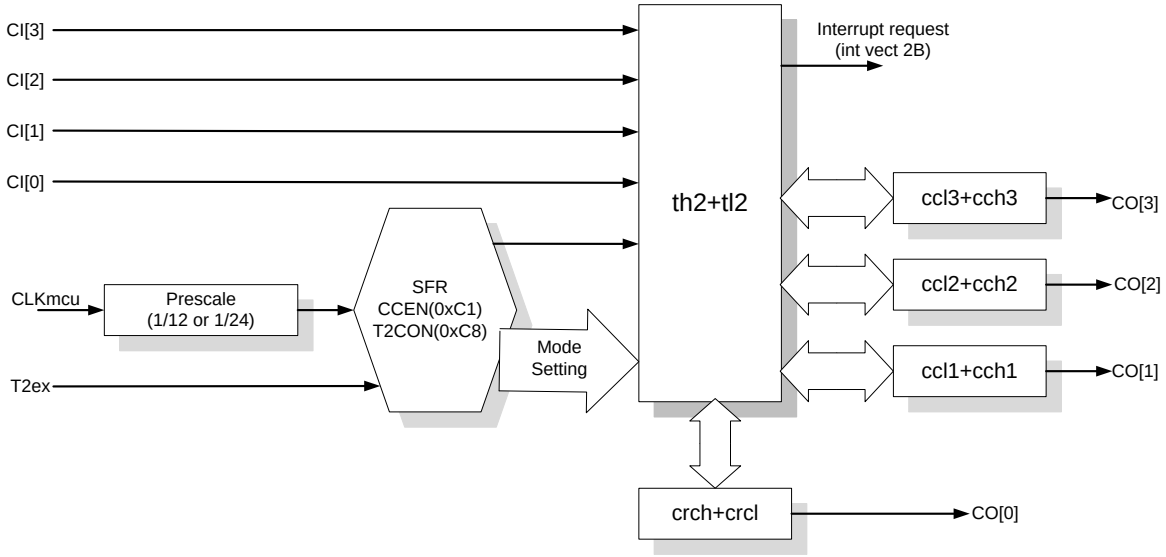


Figure 6-5：Timer2 Block Diagram

The SFR “CCEN” and “T2CON” control the Timer2 and decide which mode it is. Some bits of “T2CON” also decide the input of timer2 that is from prescaler or pin “t2ex”. There are total 10 SFR registers for counter/timer purpose. Eight of them are for 4-channel Compare:

CRCH, CRCL : for channel-0 Compare operation.
CCH1, CCL1 : for channel-1 Compare operation
CCH2, CCL2 : for channel-2 Compare operation
CCH3, CCL3 : for channel-3 Compare operation

The SFR TH2 and THL are the high-byte and low-byte of Timer2. One of four Compare function block is controlled by CCEN SFR register.

6.8.1 SFR Register – C1h~C8h/CAh~CCh

Timer2 Register

Address	Mnemonic	Bits	Description	
C1h	**CCEN**	**7:0**	**Default : 0x00**	**Access : R/W**
	cocah3 , cocal3	7:6	**compare/capture mode selection for channel 3** [cocah3 , cocal3] = 00: compare/capture disabled (timer/counter mode enable) 01: capture mode enable , Capture on rising edge at pin CI3 10: compare mode enable 11: capture mode enable , Capture on write operation into register CCL3	
	cocah2 , cocal2	5:4	**compare/capture mode selection for channel 2** [cocah2 , cocal2] = 00: compare/capture disabled (timer/counter mode enable) 01: capture mode enable , Capture on rising edge at pin CI2 10 : compare mode enable 11 : capture mode enable , Capture on write operation into register CCL2	
	cocah1 , cocal1	3:2	**compare/capture mode selection for channel 1** [cocah1 , cocal1] = 00: compare/capture disabled (timer/counter mode enable) 01: capture mode enable , Capture on rising edge at pin CI1 10 : compare mode enable 11 : capture mode enable , Capture on write operation into register CCL1	

Address	Mnemonic	Bits	Description
	cocah0 , cocal0	1:0	**compare/capture mode selection for channel 0** [cocah0 , cocal0] = 00: compare/capture disabled (timer/counter mode enable) 01: capture mode enable , Capture on rising edge at pin CI0 10 : compare mode enable 11 : capture mode enable , Capture on write operation into register CCL0
C8h	**T2CON**	**7:0**	**Default : 0x00** **Access : R/W**
	t2ps	7	**prescaler select** 0 : timer2 is clocked with 1/12 of CLKmcu frequency. 1 : timer2 is clocked with 1/24 of CLKmcu frequency.
	i3fr	6	**This bit has two functions** **"int3" active edge selection** Interrupt source "int3" active on 0 : falling edge 1 : rising edge **For capture channel 0 control** 0 : CI0 falling edge detect 1: CI0 rising edge detect Note : CI1 ~ CI3 are fixed rising-edge detect
	i2fr	5	**"int2" active edge selection** Interrupt source "int2" active on 0 : falling edge 1: rising edge
	t2r1	4	**Timer2 reload mode** 0x : reload disable 10 : mode 0 11 : mode 1
	t2r0	3	
	t2cm	2	**Timer2 compare mode** Please fixed as "0"
	t2i1	1	**Timer2 input select** 00 : timer2 stop

Address	Mnemonic	Bits	Description	
	t2i0	0	01 : 1/12 or 1/24 of frequency CLKmcu 10 : timer2 is incremented by falling edge of pin“t2” 11 : 1/12 or 1/24 of frequency CLKmcu , gated by pin “t2”	
CCh	**TL2**	**7:0**	**Default : 0x00**	**Access : R/W**
	TL2	7:0	Low byte of Timer 2	
CDh	**TH2**	**7:0**	**Default : 0x00**	**Access : R/W**
	TH2	7	High byte of Time 2	
CAh	**CRCL**	**7:0**	**Default : 0x00**	**Access : R/W**
	CRCL	7:0	Low byte of Compare/Reload/Capture Register	
CBh	**CRCH**	**7:0**	**Default : 0x00**	**Access : R/W**
	CRCH	7:0	High byte of Compare/Reload/Capture Register	
C2h	**CCL1**	**7:0**	**Default : 0x00**	**Access : R/W**
	CCL1	7:0	Low byte of COMPARE/CAPTURE REGISTER 1	
C3h	**CCH1**	**7:0**	**Default : 0x00**	**Access : R/W**
	CCH1	7:0	High byte of COMPARE/CAPTURE REGISTER 1	
C4h	**CCL2**	**7:0**	**Default : 0x00**	**Access : R/W**
	CCL2	7:0	Low byte of COMPARE/CAPTURE REGISTER 2	
C5h	**CCH2**	**7:0**	**Default : 0x00**	**Access : R/W**
	CCH2	7:0	High byte of COMPARE/CAPTURE REGISTER 2	
C6h	**CCL3**	**7:0**	**Default : 0x00**	**Access : R/W**
	CCL3	7:0	Low byte of COMPARE/CAPTURE REGISTER 3	
C7h	**CCH3**	**7:0**	**Default : 0x00**	**Access : R/W**
	CCH3	7:0	High byte of COMPARE/CAPTURE REGISTER 3	

Table 6-8：TIMER2 SFR

As mentioned above, Timer2 can operate in Timer/counter, and compare mode. It is necessary to describe every mode from user’s viewpoint.

(1) Timer/Event counter/Gated timer mode

When all cocahx, cocalx bits are '00', Timer2 is used as "Timer/Event counter/Gated timer". In this condition, if "t2i1" and "t2i0" bit of "T2CON" SFR are not "00", Timer2 will start operation. The below chart shows the block-diagram of "Timer/Event counter/Gated timer":

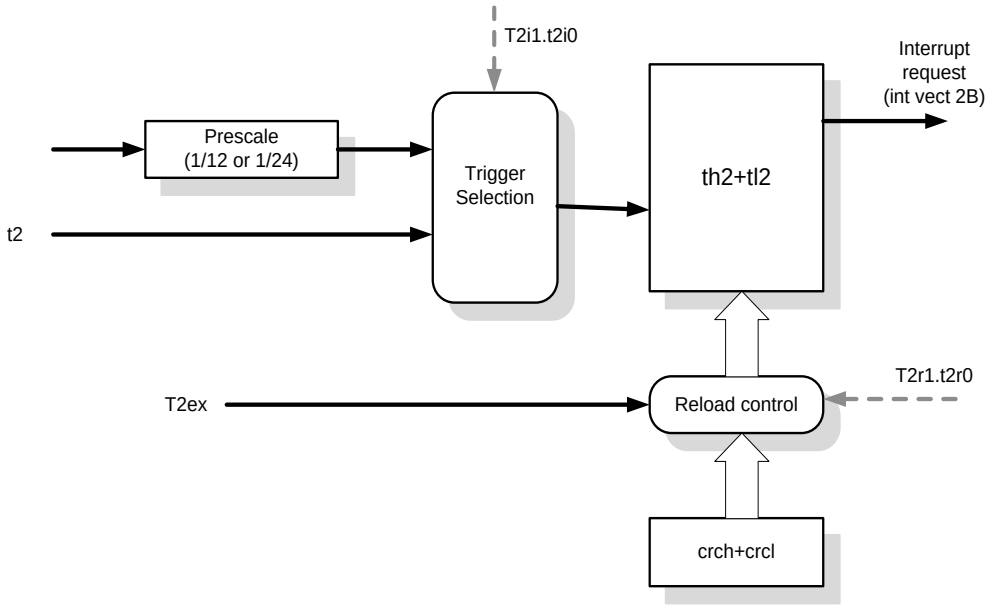


Figure 6-6：Block Diagram of Timer2 "Timer/Event Counter/Gated Timer"

The "t2r1" and "t2r0" bits of T2CON SFR decide the reload mode of TIMER2.

Reload Mode 0: Reload signal is generated by Timer 2 overflow (auto reload).

Reload Mode 1: Reload signal is generated by negative transition at the corresponding input pin "t2ex".

(a) Timer2 as one Timer

This mode is invoked by setting the "t2i0"=1 and "t2i1"=0 flags of "t2con" register. In this mode, the count rate is derived from the "CLKmcu". The Timer 2 is incremented every 12 or 24 clock cycles depending on the prescaler. The prescaler mode is selected by bit "t2ps" of "t2con" register when "t2ps"=0, the timer counts up every 12 clock cycles, otherwise every 24 cycles.

(b) Timer2 as one event counter

This mode is invoked by setting the "t2i0"=0 and "t2i1"=1 flags of "t2con" register. In this mode the Timer 2 is incremented when external signal "t2" changes its value from 1 to 0. The "t2" input is sampled at every rising edge of the clock. The Timer 2 is incremented in the cycle following the one in which the transition was detected. The maximum count rate is ½ of the clock frequency.

(c) Timer2 as one gated timer

This mode is invoked by setting the "t2i0"=1 and "t2i1"=1 flags of "t2con" register. In this mode the Timer 2 is incremented every 12 or 24 clock cycles (depending on "t2ps" flag) but additionally it is gated by

external signal “t2”. When “t2”=0, the Timer 2 is stopped. The “t2” input is sampled into a flip-flop and then it blocks the Timer 2 incrementation.

(2) Compare mode

Any one of four. cocahx, cocalx bits are ‘10’ will launch the compare function of Timer2. The below chart shows the block-diagram of compare function:

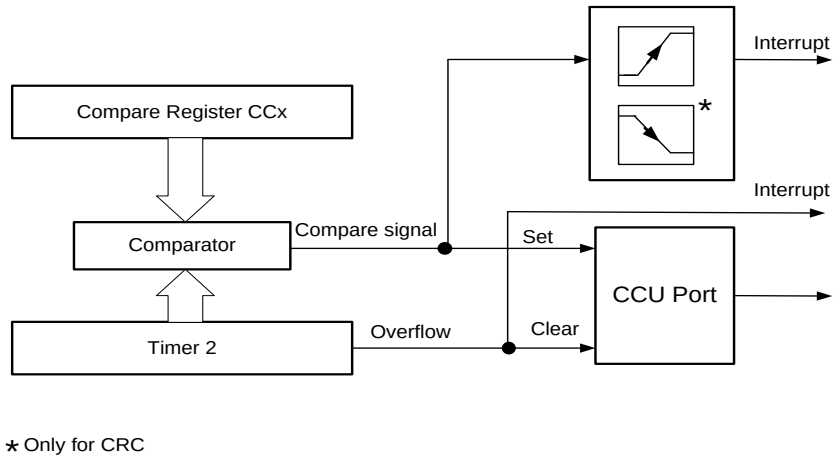


Figure 6-7：Compare Function of Timer2

The Compare Mode 0 is invoked by setting bit “t2cm”=0 of “t2con” register. When the value in Timer 2 equals the value of the compare register, the comparator output changes from low to high. It goes back low on timer 2 overflow. The port CO[0], CO[1], CO[2] and CO[3] are the compare outputs.

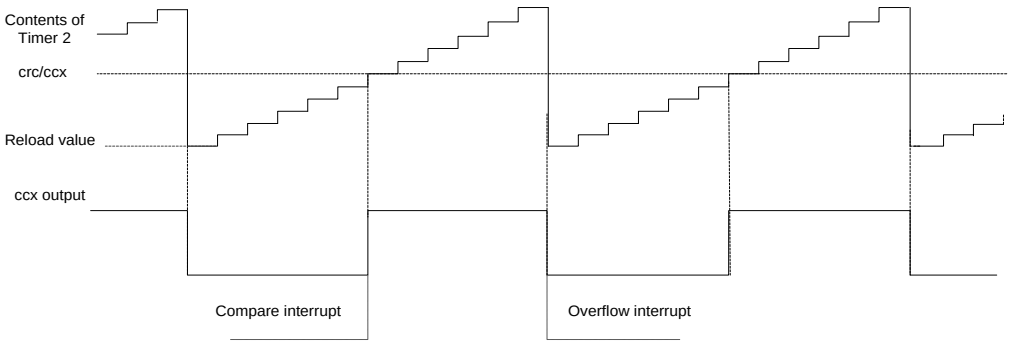


Figure 6-8：Compare Output of CO[0] , CO[1] , CO[2] and CO[3]

7. Energy Measurement

7.1 Block diagram

One of the most important functions of PL8331 is energy measurement. It can provide the information of the VRMS, IRMS, Active Power, Line frequency, etc. This section will describe how to use this function including the initialization, settings, and getting information. One hardware DSP is dedicated for energy measurement inside the PL8331. The simplified architecture of the HW DSP is shown below. There is no need to pay much attention to the internal design since all the metering measurement tasks are handled by the HW DSP.

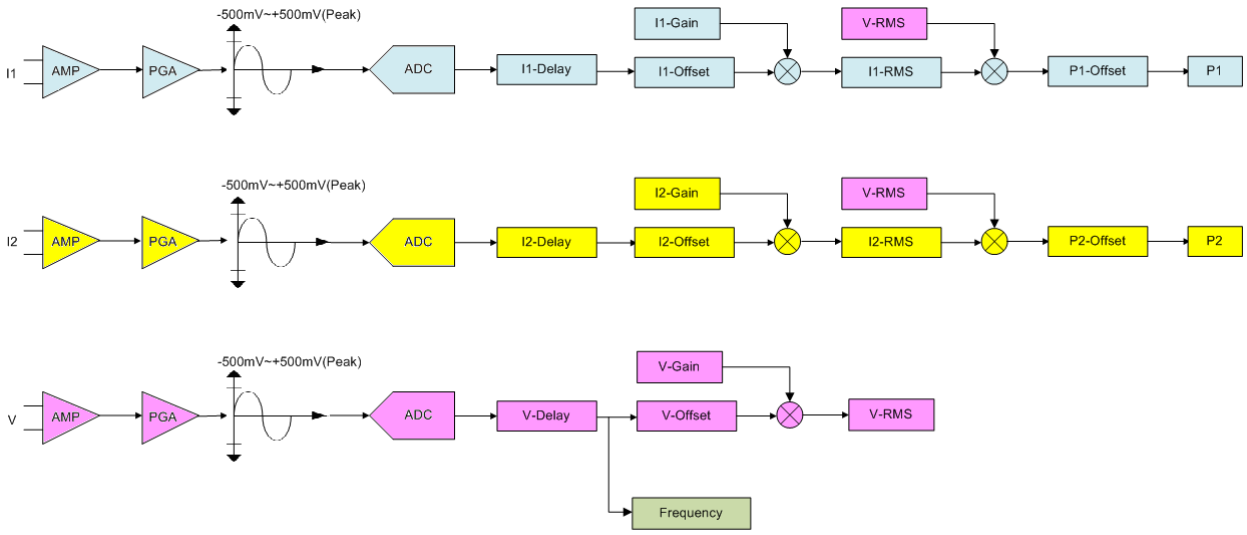


Figure 7-1：Energy Measurement Block diagram

7.1.1 Initialize HW DSP

Only need to use one bit setting to reset the HW DSP to restore the DSP to default setting.

PWRLV Control Registers - Indirect Accessing				
Address: PWRLVINDEX(CEh) / Data: PWRLVDATA(CFh)				
SFR-CEh	**SFR-CFh**	**Bits**	**Description**	
10h	**METER_CTL0**	**7:0**	**Default : 0x00**	**Access : R/W**
	DSP_SWRESET	0	Software Reset for meter DSP, high active	

Table 7-1：DSP Software Reset

Set the Clock of the HW DSP. The operation clock of the HW DSP is configurable. It is set by changing the divider of the PLL clock. To get good accuracy, follow these settings:

Normal Mode: 1M

Neutral Missing Mode: 256K

PADs Function Control Registers - Indirect Accessing				
Address: PAD_FUNCTION_INDEX(9Eh) / Data: PAD_FUNCTION_DATA(9Fh)				
SFR-9Eh	**SFR-9Fh**	**Bits**	**Description**	
02h	**DIVPM_SELECT**	**7:0**	**Default : 0x07**	**Access : R/W**
	DIVPM_SELSEL[7:0]	7:0	meter clock source selection 0x00: bypass; 0x01: divide by 2; …… 0xFF: divide by 256;	

Table 7-2：Meter Clock Source Selection

7.1.2 Indirect Accessing

To access DSP internal registers for the majority of energy measurements, indirect accessing way is used due to the space limitation of SFRs. The MADDPT register is for indirect access to internal DSP registers. MDATX, MDATL, MDATM and MDATH are data registers for reading and writing data.

SFR Registers		
Address	**Mnemonic**	**Description**
ABh	MADDPT	Meter Address
ACh	MDATX	Meter Data, Ext Byte
ADh	MDATL	Meter Data, Low Byte
AEh	MDATM	Meter Data, Middle Byte
AFh	MDATH	Meter Data, High Byte
B1h	WAVL	Meter WAV, Low Byte
B2h	WAVM	Meter WAV, Middle Byte
B3h	WAVH	Meter WAV, High Byte
B4h	WAV2L	Meter WAV2, Low Byte
B5h	WAV2M	Meter WAV2, Middle Byte
B6h	WAV2H	Meter WAV2, High Byte
BCh	WAV3L	Meter WAV3, Low Byte
BDh	WAV3M	Meter WAV3, Middle Byte
BEh	WAV3H	Meter WAV3, High Byte

Table 7-3：DSP Internal Registers

7.1.3 Writing to the DSP core Registers

When bit 7 of MADDPT SFR is set, the content of the MDATx SFRs is transferred to the DSP core. Because DSP core and MCU core are in different clock domain, when data is written to the DSP core registers, a small wait period needs to be implemented before another read or write to these registers can take place.

```
MDATH = DataH;
MDATM = DataM;
MDATL = DataL;
MDATX = DataX;
Delay(5);
MADDPT = Addr|0x80;
```

7.1.4 Reading the DSP core Registers

When bit 7 of MADDPT SFR is cleared, the content of the DSP registers designed by the address in MADDPT is transferred to the MDATx SFRs. Because DSP core and MCU core are in different clock domain, when data is read from the DSP core registers, a small wait period needs to be implemented before the MDATx SFRs are transferred to another SFR.

```
MADDPT = Addr;
Delay(5);
*DataH = MDATH;
*DataL = MDATL;
*DataM = MDATM;
*DataX = MDATX;
```

7.1.5 Analog Inputs

PL8331 has three fully differential ADC input channels. In meter application, one is for AC voltage signal (ex: voltage channel), the others are for current signal input (ex: current channel). The voltage channel signal can come from PT or direct input from line voltage by attenuator. The current channel signal can come from current transformers, shunts or di/dt current sensor. The maximum differential input range to ADC channel is ±0.5V(PGA gain=1).

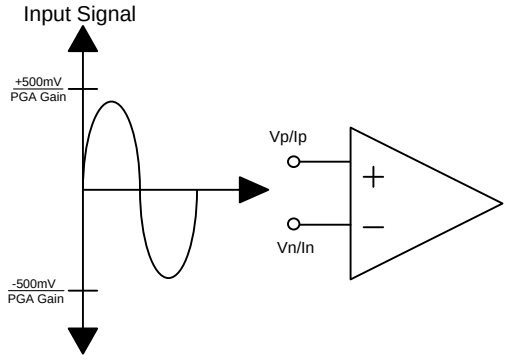


Figure 7-2：Analog Inputs

Each ADC input channel has a programmable gain amplifier (PGA) with gain selection of 1, 2, 4, 8, 16, 24 and 32. Below shows the block diagram of meter measurement:

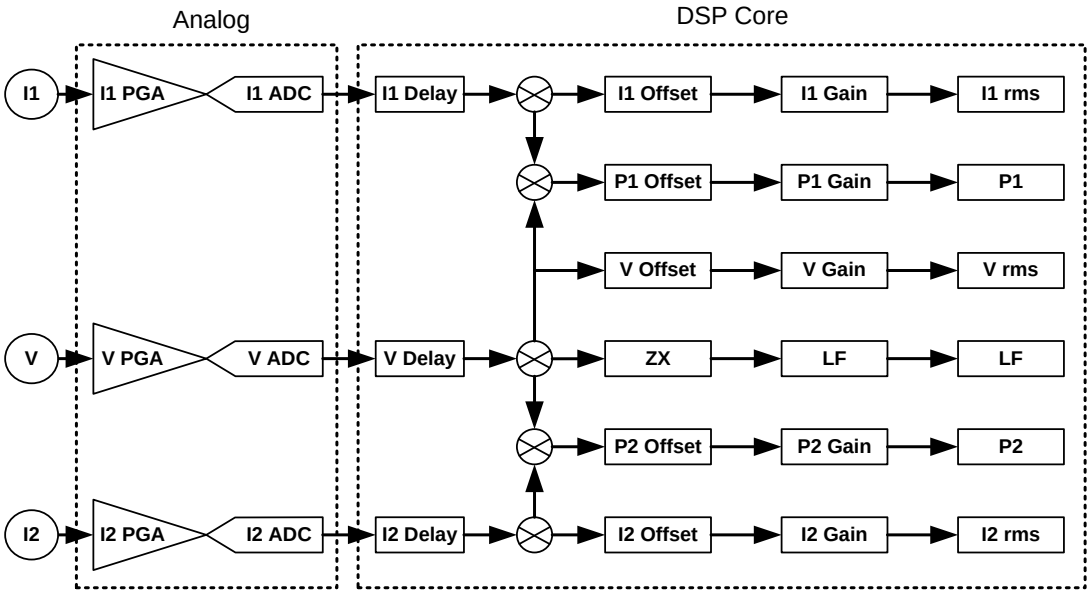


Figure 7-3：Block Diagram of Meter Measurement

ADC setting

Once the meter clock is set, a required setting is the number of ADC clocks per second in register 0x01[21:0]

DSP Control Registers - Indirect Accessing					
Address: MADP / Data: MDATH/MDATM/MDATL/MDATX					
SFR-ABh	**SFR-AFh/AEh/ADh/ACh**	**Bits**	**Value**	**Description**	
01h				**Default : 400DA7A6**	**Access : RO**
	NO_CLKS_1SEC	21:0	894886 (decimal)	Number of ADC clocks per second. Default is 894886Hz.	

Table 7-4：ADC Clock Setting

If the Meter Clock is 1M, then the setting of DSP register 0x01 [21:0] is 1024000 = 0xFA000.

DSP core

PL8331 embeds hardware digital signal processor to calculate energy data. The DSP core can provide power information as follows:

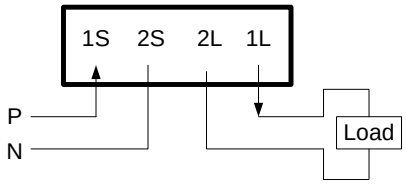
1. Active, Re-active and Apparent energy power
2. Voltage and current RMS value
3. Power factor, Line frequency

The DSP also provides some events for MCU to identify status like current fault event, zero-crossing event, no load event and SAG event.

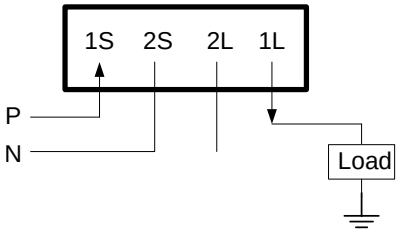
Fault Detection

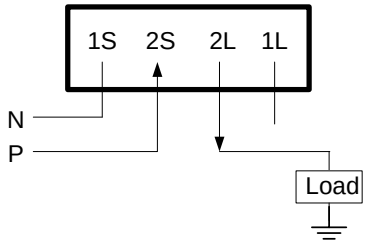
In normal operating condition, phase and neutral current should be equaled. A fault condition is defined when the difference between I1 and I2 is greater than the threshold of the active channel, the DSP automatically switch current measurement to the inactive channel. On power-up, I1 is the current input selected for calculation.

Normal condition in application:



Tampering:





To understand if fault condition happens, the DSP continues to monitor both current input channels, and provide 2 methods to determine fault event by comparing current value(Irms) and energy power value (active power).

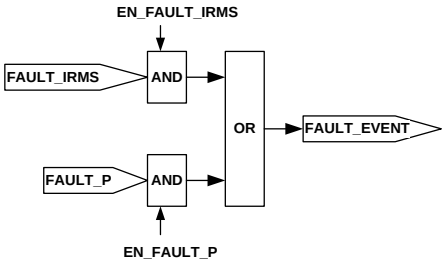


Figure 7-4：Fault Detection

7.2 Calibration method

7.2.1 Calibration Point

To achieve good performance, calibration for each meter is needed. Do the calibration at some specific conditions for different parameters.

Condition	Power Source	Purpose
Normal (Must)	240V, 5A, PF=0.5L	V-Gain, I1-Gain, I2-Gain, I1-Delay, I2-Delay Check by CF pulse
Small Current (Option)	240V, 10mA, PF=1	Calibrate I1-Offset and I2-Offset Check by reading I1RMS and I2RMS
Small Power (Option)	240V, 250mA, PF=1	Calibrated P1-Offset and P2-Offset Check by CF pulse

Table 7-5：Calibration at Some Specific Conditions for Different Parameters

There are 2 possible interfaces to do the calibration, JTAG and UART. For JTAG interface, it is done by the software with one JTAG calibration board to communicate with the meter, and then, with the auto-calibration algorithm in software. The calibration using UART interface is described in next section.

7.2.2 Calibration with UART Interface

To do the calibration via UART interface, the UART command parser is implemented in meter's firmware based on predefined protocol. The UART application will provide the source information to the meter via UART interface. Then the IC will do the auto calibration by firmware.

7.3 Analog PGA/ Digital Gain

7.3.1 Settings

To use the function of energy measure, the following settings is needed:

(1) Enable the ADC Channel

Originally, the 3 ADC channels are disabled. It must be enabled in order to measure the analog input of each channel. The related registers and sample codes are shown as follows:

PWRLV Control Registers - Indirect Accessing				
Address: PWRLVINDEX(CEh) / Data: PWRLVDATA(CFh)				
SFR-CEh	**SFR-CFh**	**Bits**	**Description**	
2Eh	**ANA_PD0**	**7:0**	**Default : 0xFE**	**Access : R/W**
		7	I2 ADC power down	
		6:3	I1 ADC power down	
		2	I1 ADC input buffer power down	
		1	I1 ADC power down	
2Fh	**ANA_PD1**	**7:0**	**Default : 0xFF**	**Access : R/W**
		7	V ADC power down When one of the V_ADC_PD is set , V ADC will power down	
		6	V ADC input buffer power down	
		5	V ADC power down When one of the V_ADC_PD is set , V ADC will power down	
		4:1	I2 ADC power down	
		0	I2 ADC input buffer power down	
30h	**ANA_PD2**	**7:0**	**Default : 0x07**	**Access : R/W**
		7:3	Reserved	
		2:0	V ADC power down	

Table 7-6：ADC SFR

To enable 3 ADC channels: 0x2E = 0x00; 0x2F = 0x00; 0x30 = 0x00;

7.3.2 Set the PGA Gain Settings

To set individual PGA gain for each channel:

PWRLV Control Registers - Indirect Accessing				
Address: PWRLVINDEX(CEh) / Data: PWRLVDATA(CFh)				
SFR-CEh	**SFR-CFh**	**Bits**	**Description**	
21h	**ANA_CTL0**	**7:0**	**Default : 0x00**	**Access : R/W**
		7:4	I2 channel gain setting 0000:x1 /0001:x2 /0101:X4 /0110: x8 /1110: x16 /1011: x24 /1111: x32 , others : Input short to VGND	
		3:0	I1 channel gain setting 0000:x1 /0001:x2 /0101:X4 /0110: x8 /1110: x16 /1011: x24 /1111: x32 , others : Input short to VGND	
22h	**ANA_CTL1**	**7:0**	**Default : 0x90**	**Access : R/W**
		3:0	V channel gain setting 0000:x1 , others : x2	

Table 7-7：PGA Gain SFR

Set the PGA Gain of V: 0x 22 = 0x91; Set the PGA Gain of I1 and I2: 0x21 = 0x1

7.3.3 Set the Digital Gain

There are 20 bits for each digital gain and the default value is 0x8000. During the calibration, adjust the digital gain. Usually, the calibrated parameters are stored in external EEPROM (or internal flash). Then, read and set parameters to the related DSP registers.

Digital Gain DSP Register

Digital Gain	DSP Register
V Channel	0x0E[3:0], 0x03[15:0]
I1 Channel	0x0E[7:4], 0x04[15:0]
I2 Channel	0x0E[11:8], 0x05[15:0]

DSP Control Registers - Indirect Accessing					
Address: MADP / Data: MDATH/MDATM/MDATL/MDATX					
SFR-ABh	**SFR-AFh/AEh/ADh/ACh**	**Bits**	**Value**	**Description**	
03h		**31:0**		**Default : 0xA3808000**	**Access : RO**
	ADC_GAIN_V[15:0]	15:0	8000h	Sets gain for V channel. Bit [15] corresponds to unit gain.	
04h		**31:0**		**Default : 0xC1808000**	**Access : RO**
	ADC_GAIN_I1[15:0]	15:0	8000h	Sets gain for I1 channel. Bit [15] corresponds to unit gain.	
05h		**31:0**		**Default : 0x41808000h**	**Access : RO**
	ADC_GAIN_I2[15:0]	15:0	8000h	Sets gain for I2 channel. Bit [15] corresponds to unit gain.	
0Eh		**31:0**		**Default : 0x80000000**	**Access : RW**
	ADC_GAIN_I2[19:16]	11:8	0	Sets gain for I2 channel.	
	ADC_GAIN_I1[19:16]	7:4	0	Sets gain for I1 channel.	
	ADC_GAIN_V[19:16]	3:0	0	Sets gain for V channel.	

Table 7-8： Digital Gain SFR

7.4 Phase Compensation

The PL8331 must work with transducers that can have inherent phase errors. For example, a phase error of 0.1° to 0.3° is not uncommon for a current transformer (CT). These phase errors can vary from part to part, and must be corrected to perform accurate power calculations. The errors associated with phase mismatch are particularly noticeable at low power factors. The PL8331 provide a means for digitally calibrating these small phase errors. The part allows a small time delay or time advance to be introduced into the signal processing chain to compensate for small phase errors. Because the compensation is in time, this technique should be used only for small phase errors in the range of 0.1° to 0.5°. Correcting large phase errors using a time shift technique may introduce significant phase errors at higher harmonics.

The phase calibration register (PHCAL[7:0], Address 0x10) is a twos complement, signed, single-byte register that has values ranging from 0x82 (−126d) to 0x68 (+104d). The PHCAL register is centered at 0x40, meaning that writing 0x40 to the register gives 0 delay. By changing this register, the time delay in the voltage channel signal path can change from −231.93 µs to +48.83 µs (MCLK = 4.096 MHz). One LSB is equivalent to a 1.22 µs (4.096 MHz/5) time delay or advance. A line frequency of 60 Hz gives a phase resolution of 0.026° at the fundamental (that is, 360° × 1.22 µs × 60 Hz).

Due to the part to part variation between current sensor and the components of anti-aliasing filter (LPF). These phase errors must be corrected to perform accurate power calculations. DSP core provide a means of digitally calibrating these phase errors, and the maximum range will depend on ADC clock selection.

For example:

If ADC input clock is 819.2KHz, and line frequency is 60Hz, then the maximum range will be 6.724°.

(1/819.2K)/(1/60)*360=0.02637°

0.02637°*255(Delay code)=6.724°

7.5 RMS

7.5.1 Enable the Calculation of the RMS of Each Channel

Item	DSP Register
Enable the calculation of RMS for V	0x03[26]
Enable the calculation of RMS for I1	0x04[26]
Enable the calculation of RMS for I2	0x05[26]

DSP Control Registers - Indirect Accessing					
Address: MADP / Data: MDATH/MDATM/MDATL/MDATX					
SFR-ABh	**SFR-AFh/AEh/ADh/ACh**	**Bits**	**Value**	**Description**	
03h		**31:0**		**Default : 0xA3808000**	**Access : RO**
	EN_RMS_V_sw	26	0	Enables the calculation of RMS for V by finding the square root of the average of V*V.	
04h		**31:0**		**Default : 0xC1808000**	**Access : RO**
	EN_RMS_I1_ii_sw	26	0	Enables the calculation of the wide-band RMS for I1 by finding the square root of the average of I1*I1.	
05h		**31:0**		**Default : 0x41808000h**	**Access : RO**
	EN_RMS_I2_ii_sw	26	0	Enables the calculation of the wide-band RMS for I2 by finding the square root of the average of I2*I2.	

Table 7-9：RMS Control SFR

7.5.2 Performance Setting

Item	DSP Register
Enable the Double HPF	0x01[24, 23]
Enable the SINC filter for V	0x03[24]
Enable the SINC filter for I1	0x04[24]
Enable the SINC filter for I2	0x05[24]
enable the SINC compensation filter	0x23[15]
Enable the HPF filter in V, I1 and I2 channel	0x26[26, 25, 24]

DSP Control Registers - Indirect Accessing					
Address: MADP / Data: MDATH/MDATM/MDATL/MDATX					
SFR-ABh	**SFR-AFh/AEh/ADh/ACh**	**Bits**	**Value**	**Description**	
01h		**31:0**		**Default : 0x400DA7A6**	**Access : RO**
	HPF_sel	24	0	Select the cutoff frequency of HPF. The higher HPF_SEL, the higher cutoff frequency. 0: suggested for 819.2 kHz ADC clock and decimation factor 64. 1: cutoff frequency doubled.	
	VI_LPF_sel	23	0	Select the cutoff frequency for the LPF after the multiplications of V and I. The higher VI_LPF_SEL, the larger the bandwidth. 0: suggested for 819.2 kHz ADC clock and decimation factor 64. 1: cutoff frequency doubled.	
03h		**31:0**		**Default : 0xA3808000**	**Access : RO**
	EN_PWR_HPF_V	24	1	If set to 1, DC-removed V is used for the calculation of active power and RMS.	
04h		**31:0**		**Default : 0xC1808000**	**Access : RO**
	EN_PWR_HPF_I1	24	1	If set to 1, DC-removed I1 is used for the calculation of active power and RMS.	
05h		**31:0**		**Default : 0x41808000h**	**Access : RO**
	EN_PWR_HPF_I2	24	1	If set to 1, DC-removed I2 is used for the calculation of active power and RMS.	

23h		**31:0**		**Default : 0x87033000**	**Access : R/W**

	EN_COMP	15	0	Setting this bit enable the SINC compensation filter.	
26h		**31:0**		**Default : 0x00090000**	**Access : R/W**
	EN_HPF_V_sw	26	0	Setting this bit enables the HPF in V channel.	
	EN_HPF_I1_sw	25	0	Setting this bit enables the HPF in I1 channel.	
	EN_HPF_I2_sw	24	0	Setting this bit enables the HPF in I2 channel.	

Table 7-10：RMS Performance Setting SFR

7.5.3 Get the Information

The output of the hardware DSP is stored in the DSP registers. Following is the table indicating the index.

Items	**Register**
VRMS	0x50[31:0]
I1RMS	0x68[31:0]
I2RMS	0x69[31:0]
PF1	0x5E[31:0]
PF2	0x5F[31:0]
Active Power1	0x58[31:0]
Active Power2	0x59[31:0]
Line Frequency	0x49[31:0]

DSP Control Registers - Indirect Accessing					
Address: MADP / Data: MDATH/MDATM/MDATL/MDATX					
SFR-ABh	**SFR-AFh/AEh/ADh/ACh**	**Bits**	**Value**	**Description**	
49h		**31:0**		**Default : 0x00000000**	**Access : RO**
		31:26	0	Reserved	
	LINE_FREQ[25:2]	25:2			
		1:0	0	Reserved	
50h		**31:0**		**Default : 0x00000000**	**Access : RO**
	RMS_V	31:0	0	Voltage channel RMS. Scaled by ADC_GAIN_V.	
58h		**31:0**		**Default : 0x00000000**	**Access : RO**
	P1	31:0	0	Active power for I1. Scaled by ADC_GAIN_V / I1.	
59h		**31:0**		**Default : 0x00000000**	**Access : RO**
	P2	31:0	0	Active power for I2. Scaled by ADC_GAIN_V / I2.	
5Eh		**31:0**		**Default : 0x00000000**	**Access : RO**

DSP Control Registers - Indirect Accessing					
Address: MADP / Data: MDATH/MDATM/MDATL/MDATX					
	PF1	31:0	0	Power factor derived from V and I1.	
5Fh		**31:0**		**Default : 0x00000000**	**Access : RO**
	PF2	31:0	0	Power factor derived from V and I2.	
68h		**31:0**		**Default : 0x00000000**	**Access : RO**
	RMS_I1_ii	31:0	0	Current RMS of I1 derived from I1 * I1. Scaled by ADC_GAIN_I1. (Wide-band.)	
69h		**31:0**		**Default : 0x00000000**	**Access : RO**
	RMS_I2_ii	31:0	0	Current RMS of I2 derived from I2 * I2. Scaled by ADC_GAIN_I2. (Wide-band.)	

Table 7-11：ADC, V , I1 and I2 Registers

All the data is stored with 4 bytes format of DataH[31:24], DataM[23:16],DataL[15:8], DataX[7:0]. The 4 bytes sent by the metering units are the priority format defined as below:

Floating point format (Ignore the DataX and use 3 bytes only)

DataH DataM DataX
SI MMMMMM MMMMMMMM MMMMMMMM
+- Mantissa * 2 ^exponent
S = -2.0
I = +1.0
M = (0.99999976158142089843 75)
=(1/2)+(1/4)+(1/8)+(1/16)+(1/32)+(1/64)+..+(1/4194304)

Hence, the range of the output value will be -2~1.9999999. Multiply the constant for the output value to make the output value in proper page.

Energy Type	Constant
Voltage	1500
Current	200
Active Power	300000
Line Frequency	16384 (2^{14})

To make the computation easier, PL8331 provides the hardware computation to convert the raw data to BCD format.

7.6 Meter Constants

The meter requires constants based on the voltage and current transformers/shunts. The following describes how to calculate the PL8331 meter constants.

Under the setting of Meter Clock = 1M,

CF1_DEN =0xEF; // Fixed Value

Meter Constant =6400: CF1_PWRGain =0x2000
Meter Constant =3200: CF1_PWRGain =0x4000
Meter Constant =1600: CF1_PWRGain =0x8000

7.7 Active Power No Load Detection

The PL8331 includes a no load threshold feature on the active power that eliminates any creep effects in the meter. The part accomplishes this by not accumulating energy if the multiplier output is below the no load threshold. When the active power is below the no load threshold, the APNOLOAD flag (Bit 0) in the Interrupt Status 1 SFR (MIRQSTL, Address 0x A5h) is set.

A4h	MIRQSTX	Meter Interrupt Status, Ext Byte
A5h	MIRQSTL	Meter Interrupt Status, Low Byte
A6h	MIRQSTM	Meter Interrupt Status, Middle Byte
A7h	MIRQSTH	Meter Interrupt Status, High Byte

If the APNOLOAD bit (Bit 0) is set in the Interrupt Enable 1 SFR (MIRQENL, Address 0x95), the 8052 core has a pending interrupt. The interrupt stays active until the APNOLOAD status bit is cleared (see the Energy Measurement Interrupts section).

95h	MIRQENL	Meter Interrupt Enable, Low Byte
96h	MIRQENM	Meter Interrupt Enable, Middle Byte
97h	MIRQENH	Meter Interrupt Enable, High Byte

8. Interfaces

The structure of the peripherals and blocks consists of:

PORTS – parallel I/O port controller, serves 4 parallel 8-bit I/O ports to be used in combination with off-core buffers, compatible to classic 80C51, but without multiplexed memory feature and without alternate functions.

UART0 – contains a Serial Port 0, a flexible synchronous/UART controller compatible with standard 80C51 serial port, and with additional baud rate generator.

MDU – Multiplication-Division Unit, provides fast extended arithmetic operations like 16-bit multiplication, 32-bit division, shifting and normalizing.

WATCHDOG – system supervisor, generating microcontroller reset when not refreshed in specified time.

ISR – Interrupt Service Routine, provides 80515-like interrupt enable and priority registers, priority decoder and interrupt vector generation.

OCDS – JTAG debug port, provides development functions such as run/stop/step control and software/hardware breakpoints of program execution.

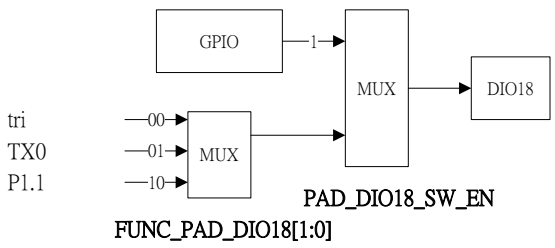
I2C – provides a flexible master – slave I2C interface

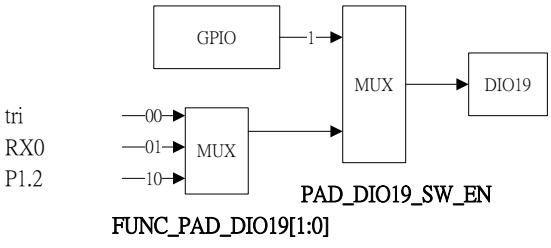
SPI – provides a flexible master – slave SPI interface

FLASH CONTROLLER – provides FLASH access and security protection

8.1 GPIO

The I/O pin of PL8331 could be used as GPIO or different functions by the software settings and configurations. Here describes the concepts of the software control PAD and how to use it in the application. For example, PAD_DIO18 as TX0 and DIO19 as the RX0. The diagram is shown below.





The I/O functions are controlled by indirect registers via SFR address D4h and D5h as shown in following table.

SFR	Mnemonic	Bits	Description	
D4h	**PAD_GPIO_INDEX**	**7:0**	**Default : 0x00**	**Access : R/W**
	PAD_WE_EN	7	Register Write Enable 1: enable to write Indirect register	

SFR	Mnemonic	Bits	Description	
	PAD_GPIO_ADDR	6:0	Register Address Port	
D5h	**PAD_GPIO_DATA**	**7:0**	**Default : 0x00**	**Access : R/W**
	PAD_GPIO_DATA	7:0	Register DATA Port	

Example:

Set DIO18 as UART_TX0 function and DIO19 as RX0, follow the table and steps below:

PADs GPIO Control Registers - Indirect Accessing				
Address: PAD_GPIO_INDEX(D4h) / Data: PAD_GPIO_DATA(D5h)				
SFR-D4h	**SFR-D5h**	**Bits**	**Description**	
05h	**PAD_DIO21_16_SW_ENABLE**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PAD_DIO19_SW_EN	3	Software control enable 1 = PAD_DIO16~PAD_DIO21 play as digital I/O 0 = Disable digital GPIO function [5:4] Reserved	
	PAD_DIO18_SW_EN	2		
09h	**PAD_DIO21_16_INTPUT_DISABLE**	**7:0**	**Default : 0xF3**	**Access : R/W**
	PAD_DIO19_IN_DIS	3	1 = Disable input function of PAD_DIO16 ~ PAD_DIO21 0 = Enable [5:4] Reserved	
	PAD_DIO18_IN_DIS	2		

1. **Switch 1st MUX by setting PAD_DIO18/19_SW_EN and IUPUT DIS bit**

PAD_GPIO_INDEX=0x85 //bit 7=1 to enable write accessing

PAD_GPIO_DATA&=(~0xC0)

PAD_ GPIO_INDEX = 0x89;

PAD_ GPIO_DATA &= (~0x08);

PAD_ GPIO_DATA |= 0x04;

2. **Switch 2nd MUX by setting Function**

PAD_FUNCTION_INDEX = 0x85;

PAD_FUNCTION_DATA |= 0x11; //Set PAD_DIO19 as Rx0 , PAD_DIO18 as Tx0

SFR	Mnemonic	Bits	Description	
9Eh	**PAD_FUNCTION_INDEX**	**7:0**	**Default : 0x00**	**Access : R/W**
	PAD_FUNCTION_WE_EN	7	Register Write Enable 1: enable to write Indirect register	
	PAD_FUNCTION_ADDR	6:0	Register Address Port	
9Fh	**PAD_FUNCTION_DATA**	**7:0**	**Default : 0x00**	**Access : R/W**
	PAD_FUNCTION_DATA	7:0	Register DATA Port	

05h	**PAD_DIO19_18_FUNC_CTL**	**7:0**	**Default : 0x00**	**Access : R/W**
	FUNC_PAD_DIO19[1:0]	5:4	PAD_DIO19 function **00: Disable** 01: UART_RX0, 10: P1.2	
	FUNC_PAD_DIO18[1:0]	1:0	PAD_DIO18 function **00: Disable** 01: UART_TX0, 10: P1.1	

8.2 UART0

The UART0 provides a flexible full-duplex synchronous/asynchronous receiver/transmitter. It can operate in four modes.

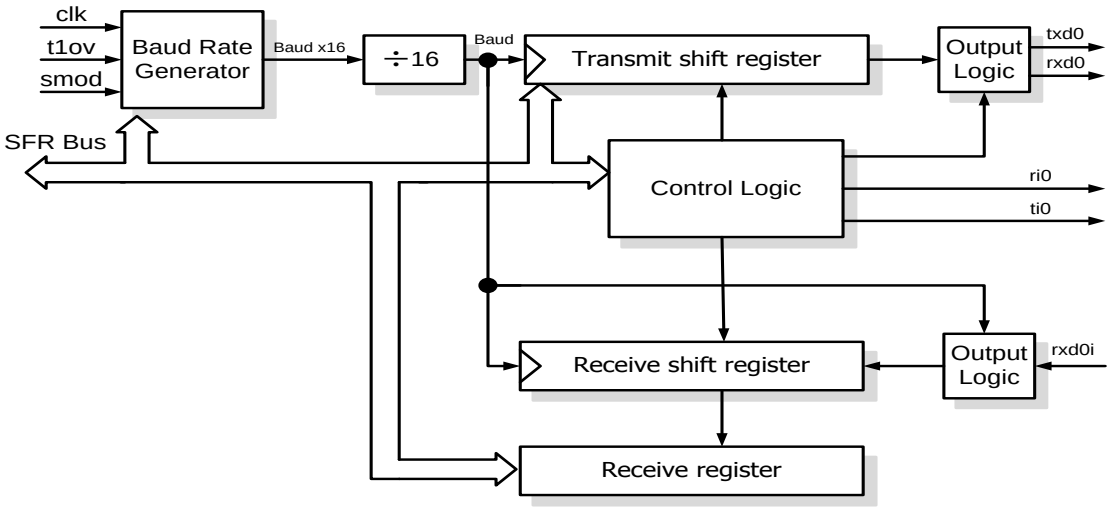


Figure 8-1 : Block Diagram of UART0

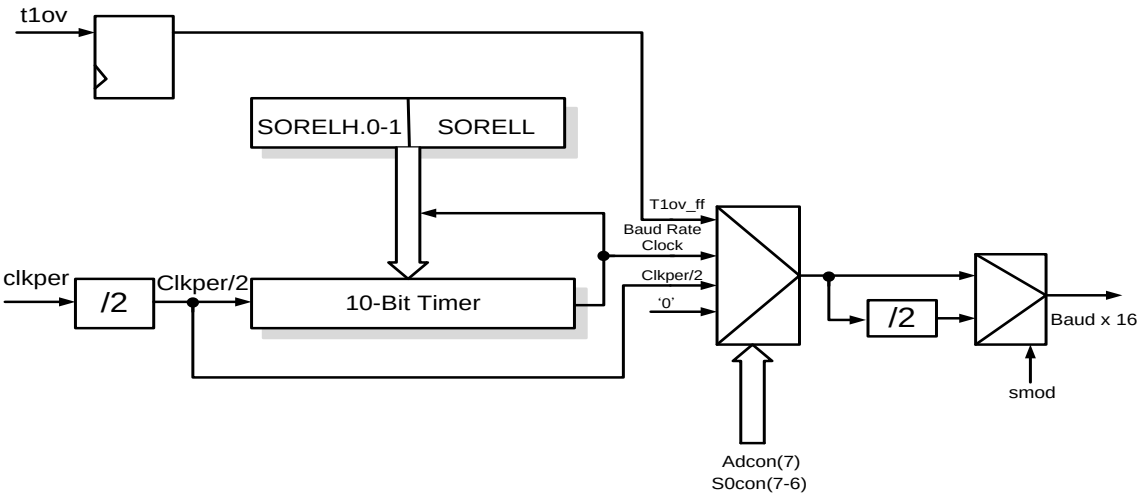


Figure 8-2 : Baud Rate Generator of UART0

mode	SYNCH/ASYNCH	START/STOP	DATA BITS	9TH BIT FUNCTION	SM0 , SM1
0	SYNCH	none	8	none	
1	ASYNCH	1 start , 1 stop	8	none	
2	ASYNCH	1 start , 1 stop	9	0 ,1 , parity	
3	ASYNCH	1 start , 1 stop	9	0,1 , parity	

Table 8-1 : Modes of UART0

8.2.1 MODE 0

In mode 0 the Serial Port 0 operates as synchronous transmitter/receiver. The "txd0" outputs the shift clock. The “rxd0o” outputs data and the “rxd0i” inputs data. 8 bits are transmitted with LSB first. The baud rate is fixed at 1/12 of the CLKmcu frequency. Reception is started by setting the“ren0” = 1 flag “s0con” register, and clearing the “ri0”flag. Transmission is started by writing data to “s0buf” register.

8.2.2 MODE1

In Mode 1, the baud rate is a function of timer overflow. This makes the baud rate programmable by the user depending on the setting of “bd” bit of “adcon” register, either Timer 1 overflow or “s0relh”, “s0rell” baud rate generator is used. Additionally the baud rate can be doubled with the use of the “smod” bit of the “pcon” register. Transmission is started by writing to the “s0buf” register. The “txd0” pin outputs data. The first bit transmitted is a start bit (always 0), then 8 bits of data proceed, after which a stop bit (always 1) is transmitted.

8.2.3 MODE2

In Mode 2, the Serial Port 0 operates as asynchronous transmitter/receiver with 9 data bits and baud rate fixed Fclkper/32 or Fclkper/64, depending on the setting of “smod” bit of “pcon” register This mode is an asynchronous mode that transmits a total of 11 bits. These include 1 start bit, 9 data bits (the ninth data bit being programmable), and 1 stop bit.

8.2.4 MODE3

This mode has the same functionality as Mode 2, but generates baud rates like Mode 1. That is, this mode transmits 11 bits, but generates baud rates via the timers. Additionally the baud rate can be doubled with the use of the “smod” bit of the “pcon” register.

sm0	sm1	mode	Baud rate	
0	0	Mode 0	Baud rate =Clkmcu/12	
0	1	Mode 1	Depend on **bd** (adcon.7)	
			bd = 0	Baud rate = $\frac{2^{SMOD} * Fclk}{32} * (Timer\ 1\_overflow\ \_rate)$
			bd = 1	$\frac{2^{SMOD} * Fclk}{64 * (2^{10} - s0rel)}$
1	0	Mode 2	Depends on smod (pcon.7) value	
			smod=0	Fclk/64
			Smod=1	Fclk/32
1	1	Mode 3	Depend on **bd** (adcon.7)	
			bd = 0	Baud rate =

				$\frac{2^{SMOD} * Fclk}{32} * (Timer\ 1\_overflow\ \_rate)$
			bd = 1	$\frac{2^{SMOD} * Fclk}{64 * (2^{10} - s0rel)}$

Table 8-2 : Baud Rate of UART0

Notes:

smod (pcon.7) – Serial Port 0 baud rate select flag

s0rel – the contents of S0REL registers (s0relh, s0rell)

bd (adcon.7) – the MSB of ADCON register

UART0 Register (SFR Register – 98h~99h/AAh/BAh/D8h)

Address	Mnemonic	Bits	Description	
98h	**S0CON**	**7:0**	**Default : 0x00**	**Access : R/W**
	sm0	7	**Serial port mode select** [sm0 , sm1] = '00' : mode 0 = '01' : mode 1 = '10' : mode 2 = '11' : mode 3	
	sm1	6		
	NC	5	**No use** FIXED ZERO	
	ren0	4	**Serial reception enable** If set HIGH serial reception at Serial Port 0 is enabled. Otherwise serial reception at Serial Port 0 is disabled.	
	tb80	3	**Transmitter bit 8** This bit is used while transmitting data through Serial Port 0 in Modes 2 and 3. The state of this bit corresponds with the state of the 9th transmitted bit (e.g. parity check or multiprocessor communication). It is controlled by software.	
	rb80	2	**Received bit 8** This bit is used while receiving data through Serial Port 0 in Modes 2 and 3. It reflects the state of the 9th received bit. In Mode 1, if multiprocessor communication is enabled (sm20 = 0), this bit is the stop bit that was received). In Mode 0 this bit is not used.	

Address	Mnemonic	Bits	Description
	ti0	1	**Transmit interrupt flag** It indicates completion of a serial transmission at Serial Port 0. It is set by hardware at the end of bit 8 in mode 0 or at the beginning of a stop bit in other modes. It must be cleared by software.
	ri0	0	**Receive interrupt flag** It is set by hardware after completion of a serial reception at Serial Port 0. It is set by hardware at the end of bit 8 in mode 0 or in the middle of a stop bit in other modes. It must be cleared by software
99h	**S0BUF**	**7:0**	**Default : 0x00** **Access : R/W**
	S0BUF	7:0	**Serial port 0 Data Buffer** Writing data into this register will start to transmit UART0 Reading from the S0BUF reads data from the serial receive buffer
AAh	**S0RELL**	**7:0**	**Default : 0XD9** **Access : R/W**
	S0RELL	7:0	**Low byte of Serial Port 0 Reload Register** Serial Port 0 Reload Register is used for Serial Port 0 baud rate generation
BAh	**S0RELH**	**7:0**	**Default : 0x03** **Access : R/W**
	NU	7:2	**NO USE**
	S0RELH[1:0]	1:0	**High byte of Serial Port 0 Reload Register**
D8h	**ADCON**	**7:0**	**Default : 0x00** **Access : R/W**
	bd	7	Serial Port 0 baud rate select (in modes 1 and 3) When 1, additional internal baud rate generator is used, otherwise Timer 1 overflow is used
	NU	6:0	NO USE

Table 8-3 : UART0 SFR

8.3 MDU

The MDU (Multiplication-Division Unit) is an on-chip arithmetic co-processor which enables the PL8331 to perform additional extended arithmetic operations. This unit provides 32-bit division, 16-bit multiplication, shift and normalize operations. All operations are unsigned integer operations. The MDU is handled by seven registers, which are memory mapped as Special Function Registers. The arithmetic unit allows performing operations concurrently to and independent of the CPU's activity. Operands and results are stored in "md0" to "md5" registers. The module is controlled by the "arcon" register. Any calculation of the MDU overwrites its operands.

The operation of the MDU consists of three phases:

(a) writing the mdx registers – there are total four MDU operations: "32bit/16bit" , "16bit/16bit" , "16bit*16bit", shifting and normalizing. MDU registers write sequence determine which operation will execute.

(b) executing – every operation has its own executing cycle time.

(c) readout the result – every operation has its own read out sequence.

Write sequence	**32bit/16bit**	**16bit/16bit**	**16bit * 16bit**	**shift normalizing**
meaning	**[md3,md2,md1,md0] / [md5,md4]** Where md0 , md4 are LSB	**[md1,md0] / [md5,md4]** Where md0 , md4 are LSB	**[md1,md0]*[md5,md4]** Where md0, md4 are LSB	**[md3,md2,md1,md0]** Where md0 is LSB
1st write	Md0	Md0	Md0	Md0
2nd write	Md1	Md1	Md4	Md1
3rd write	Md2	Md4	Md1	Md2
4th write	Md3	Md5	Md5	Md3
5th write	Md4			arcon
6th write	Md5			

Table 8-5 : Writing Sequence of MDU Registers for Different Operation

operation	**Number of clock cycles**	
32bit/16bit	17 clock cycles	
16bit/16bit	9 clock cycles	
16bit * 16bit	11 clock cycles	
shift	min 3 clock cycles (sc = 01h)	max 18 clock cycles (sc = 1Fh)
normalizing	min 4 clock cycles (sc <- 01h)	max 19 clock cycles (sc <- 1Fh)

Table 8-6 : Executing Cycle Time of MDU

Read sequence	32bit/16bit	16bit/16bit	16bit * 16bit	shift normalizing
meaning	**[md3,md2,md1,md0] is quotient [md5,md4] is remainder** Where md0 , md4 are LSB	**[md1,md0] is quotient [md5,md4] is remainder** Where md0 , md4 are LSB	**[md3,md2,md1,md0] is product** Where md0 is LSB	**[md3,md2,md1,md0]** Where md0 is LSB
1st Read	Md0	Md0	Md0	Md0
2nd Read	Md1	Md1	Md1	Md1
3rd Read	Md2	Md4	Md2	Md2
4th Read	Md3	Md5	Md3	Md3
5th Read	Md4			
6th Read	Md5			

Table 8-7 : Readout-Result Sequence of MDU Registers for Different Operation

Normalizing operation

All leading zeroes of 32-bit integer variable stored in “md0” to “md3” registers (the latter contains the most significant byte) are removed by shift left operations. The whole operation is completed when the MSB (most significant bit) of “md3” register contains a ’1’. After normalizing, bits “arcon.4” (MSB) … “arcon.0” (LSB), contain the number of shift left operations which were done.

Shifting operation

In shift operation, 32-bit integer variable stored in “md0” to ”md3” registers (the latter contains the most significant byte) is shifted left or right by a specified number of bits. The “slr” bit (“arcon.5”) defines the shift direction, and bits “arcon.4” to “arcon.0” specify the shift count (which must not be 0). During shift operation, zeroes come into the left end of “md3” for shifting right or right end of the “md0” for shifting left.

MDU Register(SFR Register – E9h~EFh)

Address	Mnemonic	Bits	Description	
EFh	**ARCON**	**7:0**	**Default : 0x00**	**Access : R/W**
	mdef	7	**MDU Error flag MDEF** Indicates an improperly performed operation (when one of the arithmetic operations has been restarted or interrupted by a new operation).	
	mdov	6	**MDU Overflow flag MDOV** Overflow occurrence in the MDU operation	

Address	Mnemonic	Bits	Description	
	slr	5	**Shift direction** slr = 0 - shift left operation. slr = 1 - shift right operation	
	sc	4:0	**Shift counter** When at least one of these bit is set, a high shift operation is selected. The number of shifts performed is determined by the number written to “sc.4” to “sc.0”, where “sc.4” is the MSB. When set to all ‘0’s, normalize operation is selected. After normalization, the “sc.0” … “sc.4” contain(s) the number of normalizing shifts performed.	
E9h	**MD0**	**7:0**	**Default : 0x00**	**Access : R/W**
		7:0	Multiplication/Division Register 0	
EAh	**MD1**	**7:0**	**Default : 0x00**	**Access : R/W**
		7:0	Multiplication/Division Register 1	
EBh	**MD2**	**7:0**	**Default : 0x00**	**Access : R/W**
		7:0	Multiplication/Division Register 2	
ECh	**MD3**	**7:0**	**Default : 0x00**	**Access : R/W**
		7:0	Multiplication/Division Register 3	
EDh	**MD4**	**7:0**	**Default : 0x00**	**Access : R/W**
		7:0	Multiplication/Division Register 4	
EEh	**MD5**	**7:0**	**Default : 0x00**	**Access : R/W**
		7:0	Multiplication/Division Register 5	

Table 8-8 : MDU SFR

8.4 Interrupt Pin(INT0/INT1/Others)

The interrupt control is 80515-like that has 4 priority levels and 18 interrupt sources. All interrupt requests are divided into 6 groups. If user do not use “IP0”, “IP1” SFRs to change the priority of interrupt group. Every interrupt-group has its own natural priority. For example, Group0 has the highest natural priority.

Interrupt group	Natural priority	Highest priority in group	Middle priority in group	Lowest priority in group
Group0	highest	Int_vect_03 (External Interrupt 0)	Int_vect_83 (UART 1 interrupt)	Int_vect_43 (External Interrupt 7 / I2C interrupt)

Group1		Int_vect_0B (Timer 0 overflow)	Int_vect_8B (External Interrupt 8)	Int_vect_4B (External Interrupt 2 / SPI interrupt)
Group2		Int_vect_13 (External Interrupt 1)	Int_vect_93 (External Interrupt 9)	Int_vect_53 (External Interrupt 3)
Group3		Int_vect_1B (Timer 1 overflow)	Int_vect_9B (External Interrupt 10)	Int_vect_5B (External Interrupt 4)
Group4		Int_vect_23 (UART0 interrupt)	Int_vect_A3 (External Interrupt 11)	Int_vect_63 (External Interrupt 5)
Group5	lowest	Int_vect_2B (Timer 2 overflow)	Int_vect_AB (External Interrupt 12)	Int_vect_6B (External Interrupt 6)

Table 8-9 : 18 Interrupt Sources, 6 Interrupt Group, and Natural Priority

Level	Priority	IP1.x bit	IP0.x bit
Level0	Lowest	0	0
Level1		0	1
Level2		1	0
Level3	Highest	1	1

Table 8-10 : Level of Interrupt Group

No	**Interrupt request input**	**Interrupt enable bit**	**Interrupt request source**	**Trigger condition**
00	int_vect_03	ien0(0)	External Interrupt 0 (P00)	Low level / falling edge
01	int_vect_0B	ien0(1)	Timer 0 overflow	
02	int_vect_13	ien0(2)	External Interrupt 1 (P01~P07)	Low level / falling edge
03	int_vect_1B	ien0(3)	Timer 1 overflow	
04	int_vect_23	ien0(4)	UART0 interrupt	
05	int_vect_2B	ien0(5)	Timer 2 overflow	
06	int_vect_33			
07	int_vect_3B			
08	int_vect_43	ien1(0)	External Interrupt 7 / I2C interrupt	Rising edge
09	int_vect_4B	ien1(1)	External Interrupt 2 (P08~P15) / SPI interrupt	Rising edge / falling edge (default falling edge)
10	int_vect_53	ien1(2)	External Interrupt 3 (IU3)	Rising edge / falling edge (default falling edge)
11	int_vect_5B	ien1(3)	External Interrupt 4 (RTC)	Rising edge

12	int_vect_63	ien1(4)	External Interrupt 5 (PM)	Rising edge
13	int_vect_6B	ien1(5)	External Interrupt 6 (Temperature)	Rising edge
14	int_vect_73			
15	int_vect_7B			
16	int_vect_83	ien2(0)	UART1 Interrupt	
17	int_vect_8B	ien2(1)	External Interrupt 8 (PWR)	Rising edge
18	int_vect_93	ien2(2)	External Interrupt 9 (IU4)	Rising edge
19	int_vect_9B	ien2(3)	External Interrupt 10 (SE37~SE41)	Rising edge
20	int_vect_A3	ien2(4)	External Interrupt 11 (BCD)	Rising edge
21	int_vect_AB	ien2(5)	External Interrupt 12	Rising edge

Table 8-11 : Interrupt Source

All priority types are taken into account when more than one interrupt is requested. The most important is the priority level set by “ip0” and “ip1” registers, then the natural priority between groups, and at last the priority inside each group. To determine which interrupt has the highest priority (which must be serviced in the first order) the following steps are performed:

1. The group with the highest priority level among all the group is chosen.
2. Among those with the highest priority level, the group with highest natural priority between groups is chosen.
3. Within the group with highest priority, the interrupt with the highest priority inside the group is chosen.

ISR Register(SFR Register – A8/B8/9A/A9/B9/C0/BFh)

Address	Mnemonic	Bits	Description	
A8h	**IEN0**	**7:0**	**Default : 0x00**	**Access : R/W**
	eal	7	**Interrupts enable** When set to 0 – all interrupts are disabled Otherwise enabling each interrupt is done by setting the corresponding interrupt enable bit	
	wdt	6	**Watchdog timer refresh flag** Set to initiate a refresh of the watchdog timer. Must be set directly before swdt (ien1.6) is set to prevent an unintentional refresh of the watchdog timer. The wdt bit is cleared by hardware after the next instruction executed after the one that had set this bit, so that watchdog refresh can be done only with direct sequence of setting wdt and swdt.	

Address	Mnemonic	Bits	Description	
	et2	5	**Timer2 interrupt enable** When et2=0 timer2 interrupt is disabled. When et2=1 and eal=1 timer2 interrupt is enabled.	
	es0	4	**Serial Port 0 interrupt enable** When es0=0 Serial Port 0 interrupt is disabled. When es0=1 and eal=1 Serial Port 0 interrupt is enabled.	
	et1	3	**Timer1 overflow interrupt enable** When et1=0 timer0 overflow interrupt is disabled. When et1=1 and eal=1 timer1 overflow interrupt is enabled.	
	ex1	2	**External interrupt 1 enable** When ex1=0 external interrupt 1 is disabled. When ex1=1 and eal=1 external interrupt 1 is enabled	
	et0	1	**Timer0 overflow interrupt enable** When et0=0 timer0 overflow interrupt is disabled. When et0=1 and eal=1 timer0 overflow interrupt is enabled.	
	ex0	0	**External interrupt 0 enable** When ex0=0 external interrupt 0 is disabled. When ex0=1 and eal=1 external interrupt 0 is enabled.	
B8h	**IEN1**	**7:0**	**Default : 0x00**	**Access : R/W**
	exen2	7	**Timer2 external reload interrupt enable** When exen2=0, timer2 external reload interrupt 2 is disabled. When exen2=1 and eal=1, timer2 external reload interrupt 2 is enabled.	
	swdt	6	**Watchdog timer start/refresh flag.** Set to activate/refresh the watchdog timer. When set directly after setting wdt (ien0.6), a watchdog timer refresh is performed. This bit is immediately cleared by hardware.	
	ex6	5	**External interrupt 6 enable** When ex6=0 external interrupt 6 is disabled. When ex6=1 and eal=1 external interrupt 6 is enabled.	
	ex5	4	**External interrupt 5 enable** When ex5=0 external interrupt 5 is disabled. When ex5=1 and eal=1 external interrupt 5 is enabled.	

Address	Mnemonic	Bits	Description	
	ex4	3	**External interrupt 4 enable** When ex4=0 external interrupt 4 is disabled. When ex4=1 and eal=1 external interrupt 4 is enabled.	
	ex3	2	**External interrupt 3 enable** When ex3=0 external interrupt 3 is disabled. When ex3=1 and eal=1 external interrupt 3 is enabled.	
	ex2	1	**External interrupt 2 enable** When ex2=0 external interrupt 2 is disabled. When ex2=1 and eal=1 external interrupt 2 is enabled.	
	ex7	0	**External interrupt 7 enable** When ex7=0 external interrupt 7 is disabled. When ex7=1 and eal=1 external interrupt 7 is enabled	
9Ah	**IEN2**	**7:0**	**Default : 0x00**	**Access : R/W**
	NU	7:6	NO USE	
	ex12	5	**External interrupt 12 enable** When ex12=0 external interrupt 12 is disabled. When ex12=1 and eal=1 external interrupt 12 is enabled.	
	ex11	4	**External interrupt 11 enable** When ex11=0 external interrupt 11 is disabled. When ex11=1 and eal=1 external interrupt 11 is enabled.	
	ex10	3	**External interrupt 10 enable** When ex10=0 external interrupt 10 is disabled. When ex10=1 and eal=1 external interrupt 10 is enabled.	
	ex9	2	**External interrupt 9 enable** When ex9=0 external interrupt 9 is disabled. When ex9=1 and eal=1 external interrupt 9 is enabled	
	ex8	1	**External interrupt 8 enable** When ex8=0 external interrupt 8 is disabled. When ex8=1 and eal=1 external interrupt 8 is enabled.	
		0		
A9h	**IP0**	**7:0**	**Default : 0x00**	**Access : R/W**
	NU	7	No use	

<table>
<tr><th>Address</th><th>Mnemonic</th><th>Bits</th><th>Description</th></tr>
<tr><td></td><td>wdts</td><td>6</td><td>Watchdog timer status flag
Set by hardware when the watchdog timer reset occurs</td></tr>
<tr><td></td><td>--</td><td>5:0</td><td>Interrupt priority
Each bit together with corresponding bit from IP0 register specifies the priority level of the respective interrupt priority group.
[ip1.0 , ip0.0] decide Interrupt Group0 priority.
[ip1.1 , ip0.1] decide Interrupt Group1 priority
[ip1.2 , ip0.2] decide Interrupt Group2 priority
[ip1.3 , ip0.3] decide Interrupt Group3 priority
[ip1.4 , ip0.4] decide Interrupt Group4 priority
[ip1.5 , ip0.5] decide Interrupt Group5 priority

The priority rule are:

<table>
<tr><th>ip1.x</th><th>Ip0.x</th><th>Group priority</th></tr>
<tr><td>0</td><td>0</td><td>Level 0 (lowest)</td></tr>
<tr><td>0</td><td>1</td><td>Level 1</td></tr>
<tr><td>1</td><td>0</td><td>Level 2</td></tr>
<tr><td>1</td><td>1</td><td>Level 3 (highest)</td></tr>
</table>
</td></tr>
<tr><td>B9h</td><td>IP1</td><td>7:0</td><td>Default : 0x00</td><td>Access : R/W</td></tr>
<tr><td></td><td>NU</td><td>7:6</td><td colspan="2">No use</td></tr>
</table>

<table>
<tr><th>Address</th><th>Mnemonic</th><th>Bits</th><th>Description</th></tr>
<tr><td></td><td>--</td><td>5:0</td><td>Interrupt priority
Each bit together with corresponding bit from IP0 register specifies the priority level of the respective interrupt priority group.
[ip1.0 , ip0.0] decide Interrupt Group0 priority.
[ip1.1 , ip0.1] decide Interrupt Group1 priority
[ip1.2 , ip0.2] decide Interrupt Group2 priority
[ip1.3 , ip0.3] decide Interrupt Group3 priority
[ip1.4 , ip0.4] decide Interrupt Group4 priority
[ip1.5 , ip0.5] decide Interrupt Group5 priority

The priority rule are:

<table>
<tr><th>ip1.x</th><th>Ip0.x</th><th>Group priority</th></tr>
<tr><td>0</td><td>0</td><td>Level 0 (lowest)</td></tr>
<tr><td>0</td><td>1</td><td>Level 1</td></tr>
<tr><td>1</td><td>0</td><td>Level 2</td></tr>
<tr><td>1</td><td>1</td><td>Level 3 (highest)</td></tr>
</table>
</td></tr>
<tr><td>C0h</td><td>IRCON</td><td>7:0</td><td>Default : 0x00</td><td>Access : R/W</td></tr>
<tr><td></td><td>exf2</td><td>7</td><td colspan="2">Timer 2 external reload flag</td></tr>
<tr><td></td><td>tf2</td><td>6</td><td colspan="2">Timer 2 overflow flag</td></tr>
<tr><td></td><td>iex6</td><td>5</td><td colspan="2">External interrupt 6 edge flag</td></tr>
<tr><td></td><td>iex5</td><td>4</td><td colspan="2">External interrupt 5 edge flag</td></tr>
<tr><td></td><td>iex4</td><td>3</td><td colspan="2">External interrupt 4 edge flag</td></tr>
<tr><td></td><td>iex3</td><td>2</td><td colspan="2">External interrupt 3 edge flag</td></tr>
<tr><td></td><td>iex2</td><td>1</td><td colspan="2">External interrupt 2 edge flag</td></tr>
<tr><td></td><td>iex7</td><td>0</td><td colspan="2">External interrupt 7 edge flag</td></tr>
<tr><td>BFh</td><td>IRCON2</td><td>7:0</td><td>Default : 0x00</td><td>Access : R/W</td></tr>
<tr><td></td><td>NU</td><td>7:5</td><td colspan="2">NO USE</td></tr>
<tr><td></td><td>iex12</td><td>4</td><td colspan="2">External interrupt 12 edge flag</td></tr>
<tr><td></td><td>iex11</td><td>3</td><td colspan="2">External interrupt 11 edge flag</td></tr>
<tr><td></td><td>iex10</td><td>2</td><td colspan="2">External interrupt 10 edge flag</td></tr>
<tr><td></td><td>iex9</td><td>1</td><td colspan="2">External interrupt 9 edge flag</td></tr>
</table>

Address	Mnemonic	Bits	Description
	iex8	0	External interrupt 8 edge flag

Table 8-12 : ISR SFR

8.5 SPI

The SPI interface provides full-duplex, synchronous, serial communication. There are two modes, master and slave for this interface. The master mode has one chip-select pin output, “SPSSN0”, so it can communicate with one SPI-slave device. On the other hand, the master and slave mode has common data ports, “MOSI”, “MISO” and clock port, “SCLK”.

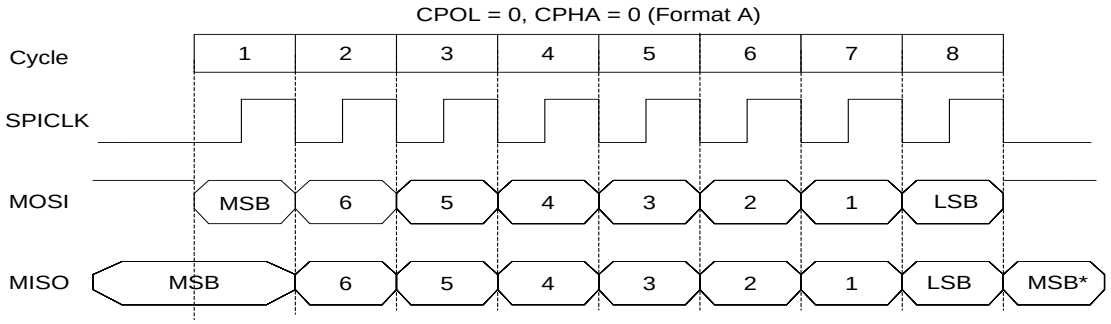
The SPI can also use interrupt to control communication flow. Its interrupt request is “int_vect_4B” which is shared with “External Interrupt 2”.

When SPI is as MASTER , Its pin connection is :

“MOSI” --- master output
“MISO” --- master input
“SPSSN0” --- output, slave select
“SCLK” ---- output, serial shift clock

When SPI is as SLAVE , Its pin connection is :

“MOSI” --- slave input
“MISO” --- slave output
“SSN” --- input, slave select
“SCLK” ---- input, serial shift clock



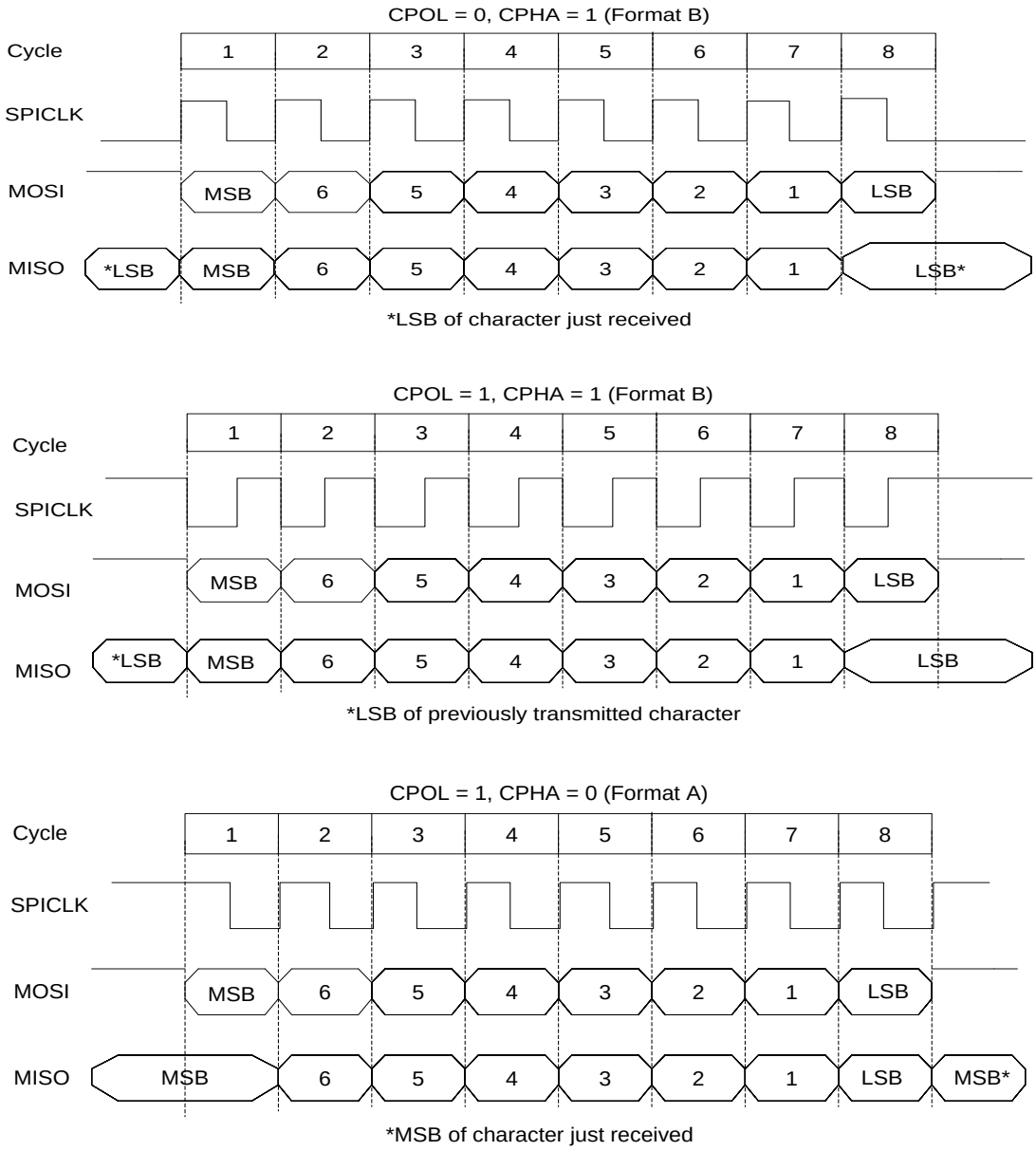


Figure 8-5 : SPI Transfer Format

SPI Register()SFR Register – E1h~E4

Address	Mnemonic	Bits	Description	
E1h	**SPSTA**	**7:0**	**Default : 0x00**	**Access : R/W**
	Spif	7	**Serial Peripheral Data Transfer Flag** Set by hardware upon data transfer completion. Cleared by hardware when data transfer is in progress. Can be also cleared by reading the “spsta” register with the “spif” bit set, and then reading the “spdat” register.	

Address	Mnemonic	Bits	Description	
	Wcol	6	**Write Collision Flag** Set by hardware upon write collision to “spdat”. Cleared by hardware upon data transfer completion when no collision has occurred. Can be also cleared by an access to “spsta” register and an access to “spdat” register.	
	sserr	5	**Synchronous Serial Slave Error Flag** Set by hardware when “ssn” input is de-asserted before the end of receive sequence. Cleared by disabling the SPI module (clearing “spen” bit in “spcon” register).	
	modf	4	**Mode Fault Flag** Set by hardware when the “ssn” pin level is in conflict with actual mode of the SPI_MS controller (configured as master while externally selected as slave). Cleared by hardware when the “ssn” pin is at appropriate level. Can be also cleared by software by reading the “spsta” register with “modf” bit set.	
	NU	3:0	**NO USE**	
E2h	**SPCON**	**7:0**	**Default : 0x00**	**Access : R/W**
	spr2	7	**Serial Peripheral Rate 2** Together with “spr1” and “spr0” defines the clock rate in master mode.	
	spen	6	**Serial Peripheral Enable** When cleared disables the SPI interface. When set enables the SPI interface.	
	ssdis	5	When cleared enables the “ssn” input in both Master and Slave modes. When set disables the “ssn” input in both Master and Slave modes. In Slave mode, this bit has no effect if “cpha”=0. When “ssdis” is set, no “modf” interrupt request will be generated.	
	mstr	4	**Serial Peripheral Master** When cleared configures the SPI as a Slave. When set configures the SPI as a Master.	
	cpol	3	**Clock Polarity** When cleared, the “sclk” is set to 0 in idle state. When set, the “sclk” is set to 1 in idle state	

<table>
<tr><th>Address</th><th>Mnemonic</th><th>Bits</th><th>Description</th></tr>
<tr><td rowspan="3"></td><td>cpha</td><td>2</td><td>Clock Phase
When cleared, data is sampled when the “sclk” leaves the idle state (see “cpol”). When set, data is sampled when the “sclk” returns to idle state (see “cpol”).</td></tr>
<tr><td>spr1</td><td>1</td><td rowspan="2">Serial Peripheral Rate
Together with “spr2” specify the serial clock rate in Master mode.
Fclk is the frequency of MCU
<table><tr><th>spr2</th><th>spr1</th><th>spr0</th><th>Serial Peripheral Rate</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Fclk / 2</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Fclk / 4</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Fclk / 8</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Fclk / 16</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Fclk / 32</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Fclk / 64</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Fclk / 128</td></tr><tr><td>1</td><td>1</td><td>1</td><td>the master clock is not generated (when “cpol” = ‘1’ on the “sclk” output is high level, otherwise is low level)</td></tr></table></td></tr>
<tr><td>spr0</td><td>0</td></tr>
<tr><td rowspan="2">E3h</td><td rowspan="2">SPDAT</td><td>7:0</td><td>Default : 0x00</td><td>Access : R/W</td></tr>
<tr><td>7:0</td><td colspan="2">While writing to the SPDAT data is placed directly into the shift register (there is no transmit buffer).
Reading the SPDAT returns the value located in the receive buffer, not the shift register.</td></tr>
<tr><td rowspan="3">E4h</td><td>SPSSN</td><td>7:0</td><td>Default : 0xFF</td><td>Access : R/W</td></tr>
<tr><td>NU</td><td>7:1</td><td colspan="2">NO USE</td></tr>
<tr><td>spssn0</td><td>0</td><td colspan="2">Data written to this register is directly available on the “spssn0” output.</td></tr>
</table>

Table 8-13 : SPI SFR

8.6 I2C

The I2C interface uses two wires to transfer information between devices. This kind of bus can have a few masters (not only one) and slaves at the same time, so the circuit has to manage the bus confliction. This interface meets the Philips I2C bus specification and supports all transfer modes from and to the I2C bus. This bus has two bi-directional open-drain lines, “SDA” and “SCLK”. Note that it needs one pull-up resistor on I2C bus. The “SDA” and “SCLK” lines referred further are the actual I2C bus signals, while the I2C component is connected to them with the use of open-drains.Each device connected to the bus is software addressable by a unique address. The I2C is a true multi-master bus including collision detection and arbitration to prevent data corruption if two or more masters simultaneously initiate data transfer.

The I2C interface has four operation modes:

Master Transmitter Mode:

Serial data output through “SDA” while “SCLK” outputs the serial clock. The first byte transmitted contains the slave address of the receiving device (7 bits) and the data direction bit. In this case the data direction bit (R/W) will be logic 0, and for example that a “W” is transmitted. Thus the first byte transmitted is SLA+W. Serial data is transmitted 8 bits at a time. After each byte is transmitted, an acknowledge bit is received. START and STOP conditions are output to indicate the beginning and the end of a serial transfer.

Master Receiver Mode:

The first byte transmitted contains the slave address of the transmitting device (7 bits) and the data direction bit. In this case the data direction bit (R/W) will be logic 1, and we say that an “R” is transmitted. Thus the first byte transmitted is SLA+R. Serial data is received via “SDA” while “SCL” outputs the serial clock. Serial data is received 8 bits at a time. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are output to indicate the beginning and end of a serial transfer.

Slave Receiver Mode:

Serial data and the serial clock are received through “SDA” and “SCLK” After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.

Slave Transmitter Mode:

The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted via “SDA” while the serial clock is input through “SCLK”. START and STOP conditions are recognized as the beginning and end of a serial transfer.

In the master mode, the arbitration logic checks that every transmitted high state (‘1’) on “SDA” actually appears as high state (‘1’) on the I2C bus “SDA”. If another device on the bus overrides high and pulls the “SDA” line low (‘0’), arbitration is lost and the I2C immediately changes from master transmitter to slave receiver. The synchronization logic synchronizes the serial clock generator with the clock pulses on the “SCLK” line from another device.

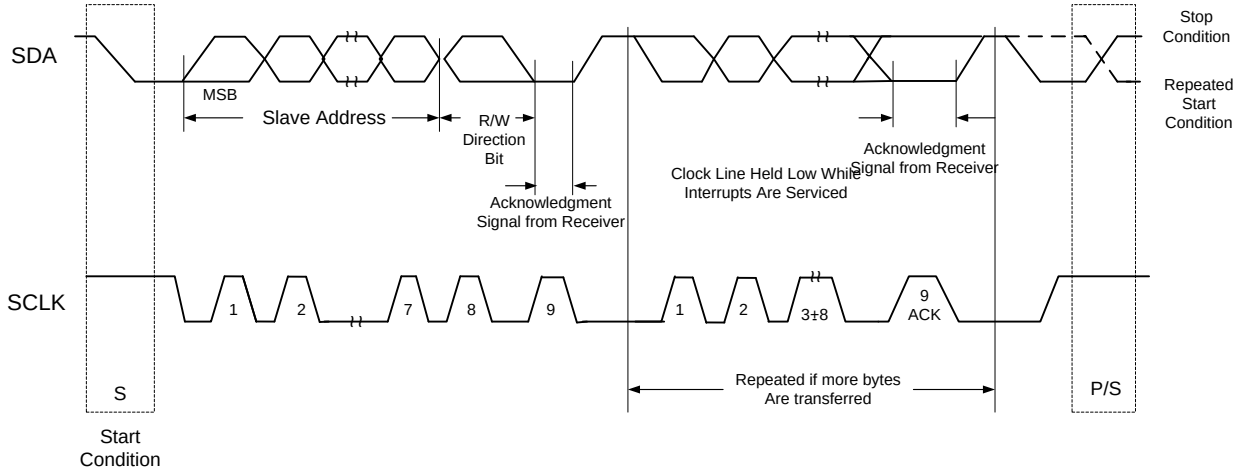


Figure 8-6 : Waveform of I2C Bus

8.6.1 Serial Clock Rate of I2C

One programmable clock pulse generator provides the SCLK clock when I2C block is in master mode. The programmable output clock frequencies ranges from Fclk/60 to Fclk/256 and the Timer 1 overflow rate divided by eight.

cr2	cr1	Cr0	SCLK frequency
0	0	0	Fclk divided by 256
0	0	1	Fclk divided by 224
0	1	0	Fclk divided by 192
0	1	1	Fclk divided by 160
1	0	0	Fclk divided by 960
1	0	1	Fclk divided by 120
1	1	0	Fclk divided by 60
1	1	1	“Timer1 overflow” divided by 8

Table 8-14 : Clock Rate of I2C

The “si“ flag of the “i2ccon” register is set by hardware when one of 25 out of 26 possible I2C states is entered. The only state that does not set the “si” is state F8h, which indicates that no relevant state information is available. The “si” flag must be cleared by software. In order to clear the “si” bit, ‘0’ must be written to this bit. Writing a ‘1 ’ to’ si bit does not change value of the “si”. The I2C interrupt vector is shared

with the External Interrupt 7. The “si”signal is OR-ed with the External Interrupt 7 edge flag, before it comes into the Interrupt Controller (ISR). To determine the actual source of that interrupt, the “si” flag has to be investigated by the interrupt service routine. Since the External Interrupt 7 flag is automatically cleared after vectoring to the service subroutine, only the state of the “si” flag brings the information of the actual source of the interrupt.

Statues in Master Transmitter Mode							
Status code	Status of the I2C	Application Software response					Next action taken by I2C hardware
		to/from I2DAT	to I2CCON				
			sta	sto	si	aa	
08H	A START condition has been transmitted	Load SLA+W	X	O	O	X	SLA+W will be transmitted; ACK bit will be received
10H	A repeated START condition has been transmitted	Load SLA+W or Load SLA+R	X X	O O	O O	X X	As above SLA+W will be transmitted; SIO1 will be switched to MST/REC mode
18H	SLA+W has been transmitted; ACK has been received	Load data byte Or no action Or no action Or no action	0 1 0 1	0 0 1 1	0 0 0 0	X X X X	Data byte will be transmitted; ACK bit will be received Repeated START will be transmitted; STOP condition will be transmitted; STO flag will be reset STOP condition followed by a START condition will be transmitted; STO flag will be reset
20H	SLA+W has been transmitted; NOT ACK has been received	Load data byte Or no action Or no action Or no action	0 1 0 1	0 0 1 1	0 0 0 0	X X X X	Data byte will be transmitted; ACK bit will be received Repeated START will be transmitted; STOP condition will be transmitted; STO flag will be reset STOP condition followed by a START condition will be transmitted; STO flag will be reset
28H	Data byte in S1DAT has been transmitted; ACK has been received	Load data byte Or no action Or no action Or no action	0 1 0 1	0 0 1 1	0 0 0 0	X X X X	Data byte will be transmitted; ACK bit will be received Repeated START will be transmitted; STOP condition will be transmitted; STO flag will be reset STOP condition followed by a

							START condition will be transmitted; STO flag will be reset
30H	Data byte in S1DAT has been transmitted; NOT ACK has been received	Load data byte Or no action Or no action Or no action	0 1 0 1	0 0 1 1	0 0 0 0	X X X X	Data byte will be transmitted; ACK bit will be received Repeated START will be transmitted; STOP condition will be transmitted; STO flag will be reset STOP condition followed by a START condition will be transmitted; STO flag will be reset
38H	Arbitration lost in SLA+R/W or Data bytes	no action Or no action	0 1	0 0	0 0	X X	I2C bus will be released; not addressed slave will be entered A START condition will be transmitted when the bus becomes free

Table 8-15 : Statues in I2C Master Transmitter Mode

Statues in Master Receive Mode							
Status code	Status of the I2C	Application Software response					Next action taken by I2C hardware
		to/from I2DAT	to I2CCON				
			sta	sto	si	aa	
08H	A START condition has been transmitted	Load SLA+R	X	O	O	X	SLA+R will be transmitted; ACK will be received
10H	A repeated START condition has been transmitted	Load SLA+W or Load SLA+R	X X	O O	O O	X X	As above SLA+W will be transmitted; SIO1 will be switched to Master/Receive mode
38H	Arbitration lost in SLA+R/W or Data bytes	no action Or no action	0 1	0 0	0 0	X X	I2C bus will be released; not addressed slave will be entered. A START condition will be transmitted when the bus becomes free
40H	SLA+R has been transmitted; ACK has been received	no action Or no action	0 0	0 0	0 0	0 1	Data byte will be received; NOT ACK bit will be returned Data byte will be received; ACK bit will be returned
48H	SLA+R has been	no action	1	0	0	X	Repeated START condition will be

	transmitted; NOT ACK has been received	Or no action Or no action	0 1	1 1	0 0	X x	transmitted STOP condition will be transmitted; STO flag will be reset STOP condition followed by a START condition will be transmitted; STO flag will be reset
50H	Data byte has been received; ACK has been returned	Read data byte or read data byte	0 0	0 0	0 0	0 1	Data byte will be received; NOT ACK bit will be returned Data byte will be received; ACK bit will be returned
58H	Data byte has been received; NOT ACK has been returned	Read data byte or read data byte or read data byte	1 0 1	0 1 1	0 0 0	X X x	Repeated START condition will be transmitted STOP condition will be transmitted; STO flag will be reset STOP condition followed by a START condition will be transmitted; STO flag will be reset

Table 8-16 : Statues in I2C Master Receive Mode

Statues in Slave Transmitter Mode							
Status code	Status of the I2C	Application Software response					Next action taken by I2C hardware
		to/from I2DAT	to I2CCON				
			sta	sto	si	aa	
A8H	Own SLA+R has been received; ACK has been returned	Load data byte or load data byte	X X	O O	O O	0 1	Last data byte will be transmitted and ACK bit will be received Data byte will be transmitted; ACK will be received
B0H	Arbitration lost in SLA+R/W as master; Own SLA+R has been received, ACK has been returned	Load data byte or load data byte	X X	O O	O O	0 1	Last data byte will be transmitted and ACK bit will be received Data byte will be transmitted; ACK bit will be received
B8H	Data byte in I2CDAT has been transmitted; ACK has been received	Load data byte or load data byte	X X	O O	O O	0 1	Last data byte will be transmitted and ACK bit will be received Data byte will be transmitted; ACK bit will be received
C0H	Data byte in I2CDAT has been transmitted;	no action	0	0	0	0	Switched to “not addressed slave” mode; no recognition of own slave

	NOT ACK has been received	Or no action	0	0	0	1	address or general call address. Switched to “not addressed slave” mode; own slave address or general call address will be recognized.
		Or no action	1	0	0	0	Switched to “not addressed slave” mode; no recognition of own slave address or general call address; START condition will be transmitted when the bus becomes free
		Or no action	1	0	0	1	Switched to “not addressed slave” mode; own slave address or general call address will be recognized; START condition will be transmitted when the bus becomes free
C8H	Last data byte in I2CDAT has been transmitted (AA = 0);	no action	0	0	0	0	Switched to “not addressed slave” mode; no recognition of own slave address or general call address
	ACK has been received	Or no action	0	0	0	1	Switched to “not addressed slave” mode; own slave address or general call address will be recognized
		Or no action	1	0	0	0	Switched to “not addressed slave” mode; no recognition of own slave address or general call address; START condition will be transmitted when the bus becomes free
		Or no action	1	0	0	1	Switched to “not addressed slave” mode; own slave address or general call address will be recognized; START condition will be transmitted when the bus becomes free

Table 8-17 : Statues in I2C Slave Transmitter Mode

Statues in Slave Receive Mode							
Status code	Status of the I2C	Application Software response					Next action taken by I2C hardware
		to/from I2DAT	to I2CCON				
			sta	sto	si	aa	
60H	Own SLA+W has	no action	X	O	O	0	Data byte will be received and NOT

	been received; ACK has been returned	Or no action	X	O	O	1	ACK will be returned. Data byte will be received and ACK will be returned.
68H	Arbitration lost in SLA+R/W as master; Own SLA+W has been received, ACK returned	no action Or no action	X X	O O	O O	0 1	Data byte will be received and NOT ACK will be returned. Data byte will be received and ACK will be returned.
70H	General call address (00H) has been received; ACK has been returned	no action Or no action	X X	O O	O O	0 1	Data byte will be received and NOT ACK will be returned. Data byte will be received and ACK will be returned.
78H	Arbitration lost in SLA+R/W as master; General call address has been received, ACK has b	no action Or no action	X X	O O	O O	0 1	Data byte will be received and NOT ACK will be returned. Data byte will be received and ACK will be returned.
80H	Previously addressed with own SLV address; DATA has been received; ACK has been returned	Read data byte or read data byte	X X	O O	O O	0 1	Data byte will be received and NOT ACK will be returned. Data byte will be received and ACK will be returned.
88H	Previously addressed with own SLA; DATA byte has been received; NOT ACK has been returned	Read data byte or read data byte or read data byte or read data byte	0 0 1 1	0 0 0 0	0 0 0 0	0 1 0 1	Switched to “not addressed slave” mode; no recognition of own slave address or general call address. Switched to “not addressed slave” mode; own slave address or general call address will be recognized. Switched to “not addressed slave” mode; no recognition of own slave address or general call address; START condition will be transmitted when the bus becomes free. Switched to “not addressed slave” mode; own slave address or general call address will be recognized; START condition will be transmitted when the bus becomes free.
90H	Previously addressed	Read data byte	X	O	O	0	Data byte will be received and NOT

	with General Call; DATA byte has been received; ACK has been returned	or read data byte	X	O	O	1	ACK will be returned Data byte will be received and ACK will be returned
98H	Previously addressed with General Call; DATA byte has been received; NOT ACK has been returned	Read data byte or	0	0	0	0	Switched to “not addressed slave” mode; no recognition of own slave address or general call address.
		read data byte or	0	0	0	1	Switched to “not addressed slave” mode; own slave address or general call address will be recognized.
		read data byte or	1	0	0	0	Switched to “not addressed slave” mode; no recognition of own slave address or general call address; START condition will be transmitted when the bus becomes free.
		read data byte	1	0	0	1	Switched to “not addressed slave” mode; own slave address or general call address will be recognized; START condition will be transmitted when the bus becomes free.
A0H	A STOP condition or repeated START condition has been received while still addressed as SLAVE/RECEIVE or SLAVE/TRANSIMITTER	no action	0	0	0	0	Switched to “not addressed slave” mode; no recognition of own slave address or general call address
		Or no action	0	0	0	1	Switched to “not addressed slave” mode; own slave address or general call address will be recognized
		Or no action	1	0	0	0	Switched to “not addressed slave” mode; no recognition of own slave address or general call address; START condition will be transmitted when the bus becomes free.
		Or no action	1	0	0	1	Switched to “not addressed slave” mode; own slave address or general call address will be recognized; START condition will be transmitted when the bus becomes free.

Table 8-18 : Tatues in I2C Slave Receive Mode

8.6.2 IIC Register(SFR Register – DAh~DDh)

Address	Mnemonic	Bits	Description	
DAh	**I2CDAT**	**7:0**	**Default : 0x00**	**Access : R/W**
		7:0	**I2C DATA REGISTER** contains a byte to be transmitted through I2C bus or a byte which has just been received through I2C bus.	
DBh	**I2CADR**	**7:0**	**Default : 0x00**	**Access : R/W**
	adr	7:1	**Own I2C address** 7-bit address	
	gc	0	**General Call Address Acknowledge** If this bit is set, the general call address is recognized; otherwise it is ignore	
DCh	**I2CCON**	**7:0**	**Default : 0x00**	**Access : R/W**
	cr2	7	clock rate 2	
	ens1	6	**I2C enable bit** When ens1='0' the "sdao" and "sclo" outputs are set to 1, that drives the output pads of the chip in high impedance, and "sdai" and "scli" input signals are ignored. When ens1='1' I2C component is enabled.	
	sta	5	**Start flag** When sta='1', the I2C component checks the I2C bus status and if the bus is free a START condition is generated.	
	sto	4	**Stop flag** When sto='1' and I2C interface is in master mode, a STOP condition is transmitted to the I2C bus.	
	si	3	**Serial interrupt Flag** The "si "is set by hardware when one of 25 out of 26 possible I2C states is entered. The only state that does not set the "si" is state F8h, which indicates that no relevant state information is available. The "si" flag must be cleared by software. In order to clear the "si" bit, '0' must be written to this bit. Writing a '1' to si bit does not change value of the "si".	

Address	Mnemonic	Bits	Description
	aa	2	**Assert acknowledge** When aa='1', an "acknowledge" will be returned when: - the "own slave address" has been received - the general call address has been received while gc bit in i2caddr register was set - a data byte has been received while I2C was in master receiver mode - a data byte has been received while I2C was in slave receiver mode When aa='0', an "not acknowledge" will be returned when: ata byte has been received while I2C was master receiver mode ata byte has been received while I2C was in slave receiver mode
	cr1	1	**clock rate bit 1**
	cr0	0	**clock rate bit 0**
DDh	**I2CSTA**	**7:0**	**Default : 0x00** **Access : R/W**
	status	7:3	**I2C Status code** indicate the 26 status of I2C
	NU	2:0	**NO use**

Table 8-19 : I2C SFR

9. LCD

Using shared pins, the LCD module is capable of directly driving an LCD panel of 4 × 25 segments without compromising any PL8331 functions. It is capable of driving LCDs with 4× multiplexing. The external resistor ladder for LCD waveform voltage generation is supported. Each PL8331 has an embedded LCD control circuit, driver, and power supply circuit.

9.1 Power Control

PL8331 supports the LCD to 25 segments with 4 COM. Before using that, we need to have following initialization steps:

1. Enable the power of LCD and LCD driver
2. Set the PAD of LCD Segments as LCD usage
3. Set the PAD is output direction
4. Set the LCD clock

9.2 Initialize

The initial setting on the LCD as the IO set. First of all is enabling the power of LCD and LCD driver, then make the PADSE00-39 as LCD, not GPIO. Second, disable the SW of PADSE00-39 and input function, then enable the output function. And then set the LCD clock select to allow the display data to be updated. Settings are as follows:

```
LCDCON |=0x80          //Enable the LCD Driver
LCDCON|=0x03           //4x Multiplexing
LCDCON|=0x20           //Enable the Blink
LCDCLK|=0xC0           //The Blink rate is set by LCD_OFF_SEL
LCDPIN|=0x80           //LCD_PIN Sequence Selection Enable
```

9.3 LCD Setup

The LCD configuration SFR (LCDCON, Address 0xE5) configures the LCD module to drive the type of LCD in the user end system. The COM0~COM3 & SE0~SE23 pins(PIN28~55) default to LCD segment lines. Selecting the 4× multiplex level in the LCD configuration SFR (LCDCON, Address 0xE5) by setting LMUX[1:0] to 11 .

9.4 LCD Timing and Waveforms

An LCD segment acts like a capacitor that is charged and discharged at a certain rate. This rate, the refresh rate, determines the visual characteristics of the LCD. A slow refresh rate results in the LCD blinking on and off between refreshes. A fast refresh rate presents a screen that appears to be continuously lit. In addition, a faster refresh rate consumes more power. The frame rate, or refresh rate, for the LCD module is derived from the LCD clock, fLCDCLK. The LCD clock is selected by the bit (Bit 3:0) in the LCD configuration

SFR (LCDCLK, Address 0xE6). The minimum refresh rate needed for the LCD to appear solid (without blinking) is independent of the multiplex level. The LCD waveform frequency, fLCD, is the frequency at which the LCD switches the active common line. Thus, the LCD waveform frequency depends heavily on the multiplex level. The frame rate and LCD waveform frequency are set by fLCDCLK, the multiplex level, and the FD frame rate selection bits in the LCD clock SFR (LCDCLK, Address 0xE6[3:0]).

The LCD module provides 16 different frame rates for fLCDCLK = 2048 Hz, ranging from 8 Hz to 128 Hz for an LCD with 4× multiplexing. Fewer options are available with fLCDCLK = 1024 Hz, ranging from 8 Hz to 128 Hz for a 4× multiplexed LCD. The 128 Hz clock is beneficial for battery operation because it consumes less power than the 2048 Hz clock. The frame rate is set by the FD bits in the LCD clock SFR (LCDCLK, Address 0xE6[3:0]). The LCD waveform is inverted at twice the LCD waveform frequency, fLCD. This way, each frame has an average dc offset of 0. ADC offset degrades the lifetime and performance of the LCD.

9.5 LCD Control Registers (SFR Registers –E5h~E8h/F8h~FCh)

LCD Control Registers				
SFR	**Mnemonic**	**Bits**	**Description**	
E5h	**LCDCON**	**7:0**	**Default : 0x00**	**Access : R/W**
	LCDEN	7	LCD Enable. If this bit is set, the LCD driver is enabled.	
	LCDRST	6	LCD Data Register Reset. If this bit is set, the LCD data registers are reset to zero.	
	BLINKEN	5	Blink Mode Enable Bit. If this bit is set, blink mode is enabled. The blink mode is configured by the BLKMOD[1:0] and BLKFREQ[1:0] bits in the LCD Clock SFR.	
	LCDPSM2	4	Force LCD off when in PSM2(Sleep Mode). “0” The LCD is disabled or enabled in PSM2 by LCDEN bit. “1” The LCD is disabled in PSM2 regardless of LCDEN setting.	
	-	3	Reserved	
	-	2	Reserved	
	LMUX	1:0	“11” = 4x Multiplexing.	
E6h	**LCDCLK**	**7:0**	**Default : 0x00**	**Access : R/W**
	BLKMOD	7:6	“00” The blink rate is controlled by software. The display is off. “01” The blink rate is controlled by software. The display is on. “10” The blink rate is 2 Hz. “11” The blink rate is set by LCD_OFF_SEL (RTC 0x0E)	
	-	5:4	Reserved	

LCD Control Registers				
SFR	**Mnemonic**	**Bits**	**Description**	
	FR[3:0]	3:0	LCD Frame Rate Selection Bits	
E7h	**LCDPIN**	**7:0**	**Default : 0x00**	**Access : R/W**
	LCD_PINEN	7	LCD_PIN Sequence Selection Enable	
	LCDPIN_SEQ[2:0]	6:4	LCD Pin-out Sequence Selection 110: CM0~CM3 + SE0~SE24 111: SE23~SE0 + CM3~CM0	
	-	3:0	Reserved.	
E8h	**LCDCONX**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7:0	Reserved.	
F8h	**LCDPTR**	**7:0**	**Default : 0x00**	**Access : R/W**
	R/W	7	Read or Write LCD Bit. If this bit is set, the data in LCDDAT is written to the address indicated by the LCDPTR[5:0]	
	ADDRESS	6:0	LCD Data Address	
F9h	**LCDDAT**	**7:0**	**Default : 0x00**	**Access : R/W**
			Data to be written into or read out of the LCD Memory SFRs.	
FAh	**LCDCONY**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	INI_LVL	6	Frame Inversion Mode Enable Bit. If this bit is set, frames are inverted every other frame. If this bit is cleared, frames are not inverted.	
	-	5:1	Reserved.	
	REFRESH	0	Refresh LCD Memory Bit. This bit should be set by the user. When set, the LCD driver does not use the data in the LCD data registers to update the display. The LCD data registers can be updated by the 8052. When cleared, the LCD driver uses the data in the LCD data registers to update display at the next frame.	
FBh	**LCDSEGE2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved	
		3	The segment order reverse “0” = SEG0 - > SEG31 “1” = SEG31 -> SEG0	

LCD Control Registers				
SFR	**Mnemonic**	**Bits**	**Description**	
		2	The COM order reverse "0" = COM0 - > COM3 "1" = COM3 -> COM0	
	-	1:0	Reserved	
FCh	**LCDSEGE3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:0	Reserved.	

Table 9-1 : LCD Control Registers (SFR Registers)

9.6 Memory for LCD Buffer

Using the indirect access to LCDPTR and LCDDAT SFR allows to display something. Following is the memory mapping for the LCD bufferL

LCD Memory Address **LCD Pointer SFR** **(LCDPTR,0XF8)**	**LCD Data SFR(LCDDAT,0XF9)**							
	COM3	**COM2**	**COM1**	**COM0**	**COM3**	**COM2**	**COM1**	**COM0**
	Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
0x0C					SEG24	SEG24	SEG24	SEG24
0x0B	SEG23	SEG23	SEG23	SEG23	SEG22	SEG22	SEG22	SEG22
0x0A	SEG21	SEG21	SEG21	SEG21	SEG20	SEG20	SEG20	SEG20
0x09	SEG19	SEG19	SEG19	SEG19	SEG18	SEG18	SEG18	SEG18
0x08	SEG17	SEG17	SEG17	SEG17	SEG16	SEG16	SEG16	SEG16
0x07	SEG15	SEG15	SEG15	SEG15	SEG14	SEG14	SEG14	SEG14
0x06	SEG13	SEG13	SEG13	SEG13	SEG12	SEG12	SEG12	SEG12
0x05	SEG11	SEG11	SEG11	SEG11	SEG10	SEG10	SEG10	SEG10
0x04	SEG9	SEG9	SEG9	SEG9	SEG8	SEG8	SEG8	SEG8
0x03	SEG7	SEG7	SEG7	SEG7	SEG6	SEG6	SEG6	SEG6
0x02	SEG5	SEG5	SEG5	SEG5	SEG4	SEG4	SEG4	SEG4
0x01	SEG3	SEG3	SEG3	SEG3	SEG2	SEG2	SEG2	SEG2
0x00	SEG1	SEG1	SEG1	SEG1	SEG0	SEG0	SEG0	SEG0

LCD Frame Rate Selection for fLCDCLK=2048Hz

FD3	FD2	FD1	FD0	2*Multiplexing		3* Multiplexing		4* Multiplexing	
				f_{LCD}(Hz)	Frame Rate(Hz)	f_{LCD}(Hz)	Frame Rate(Hz)	f_{LCD}(Hz)	Frame Rate(Hz)
0	0	0	1	-	-	-	-	-	-
0	0	1	0	170.7	85.3	341.3	113.8[1]	341.3	85.3
0	0	1	1	128	64	256	85.3	256	64
0	1	0	0	102.4	51.2	204.8	68.3	204.8	51.2
0	1	0	1	85.3	42.7	170.7	56.9	170.7	42.7
0	1	1	0	73.1	36.6	146.3	48.8	146.3	36.6
0	1	1	1	64	32	128	42.7	128	32
1	0	0	0	56.9	28.5	113.8	37.9	113.8	28.5
1	0	0	1	51.2	25.6	102.4	34.1	102.4	25.6
1	0	1	0	46.5	23.25	93.1	31	93.1	23.25
1	0	1	1	42.7	21.35	85.3	28.4	85.3	21.35
1	1	0	0	39.4	19.7	78.8	26.3	78.8	19.7
1	1	0	1	36.6	18.3	73.1	24.4	73.1	18.3
1	1	1	0	34.1	17.05	68.3	22.8	68.3	17.05
1	1	1	1	32	16	64	21.3	64	16
0	0	0	0	16	8	32	10.7	32	8

RTC Control Registers - Indirect Accessing				
Address: RTC_INDEX(D2h) / Data: RTC_DATA(D3h)				
SFR-D2h	**SFR-D3h**	**Bits**	**Description**	
0Fh	**RTC_CONF_F_reg**	**7:0**	**Default : 0x30**	**Access : R/W**
	LCD_CLKSEL	3:2	LCD clock select “00” : Disable LCD clock. “01” : Disable LCD clock. “10” :LCD clock decide by LCD_CLK_FD[1:0]. “11” :128 Hz.	
	LCD_CLK_FD	1:0	“00” :2048 Hz “01” :1024 Hz “10” :4096 Hz “11” :8192 Hz	

10. RTC

One Real Time Clock (RTC) is embedded inside PL8331. The external 32.768 kHz crystal is used as the clock source for the RTC. Calibration is provided to compensate the nominal crystal frequency and for variations in the external crystal frequency over temperature. By default, the RTC is active in all the power saving modes. The RTC counters retain their values through watchdog resets and external resets and are reset only during a power-on reset.

RTC	-- Built-In RTC -- Provide the information of Hour/Min/Sec -- HW Calendar included -- Interrupt for Time interval/ Midnight events

The PL8331 provides two ways to access the RTC data: by direct access through SFRs for configuration and by indirect access through address and data SFRs for the timekeeping registers and some other configurations. The address and data SFRs act as pointers to the RTC internal registers.

This section describes how to use the internal RTC, including read/write time information, setting the interrupt, and calibration.

10.1 Read/Write the RTC register

Since the RTC is embedded, the MCU can get the time information by indirect register access. The control register for RTC block access is in 0xD2 (RTC_INDEX) and 0xD3 (RTC_DATA).

SFR Registers		
Address	**Mnemonic**	**Description**
D2h	**RTC_INDEX**	**Real time clock Indirect control register**
D3h	**RTC_DATA**	
D9h	**KEYREG**	**RTC Key**

SFR	**Mnemonic**	**Bits**	**Description**	
D2h	**RTC_INDEX**	**7:0**	**Default : 0x00**	**Access : R/W**
	RTC_ACCESS_EN	7	Register Access Enable 1: enable to access Indirect register	

SFR	Mnemonic	Bits	Description	
	RTC_WE_EN	6	Register Write Enable 1: enable to write Indirect register	
	-	5	Reserved.	
	RTC_ADDR	4:0	Register Address Port	
D3h	**RTC_DATA**	**7:0**	**Default : 0x00**	**Access : R/W**
	RTC_DATA	7:0	Register DATA Port	

Before accessing the RTC block, user must enable the RTCKEY in 0xD9. The key must be set as 0xAC before read/write the RTC block register.

The information of the second/minutes/hours are in the RTC block register 0x03~0x05.

RTC Control Registers - Indirect Accessing				
Address: RTC_INDEX(D2h) / Data: RTC_DATA(D3h)				
SFR-D2h	**SFR-D3h**	**Bits**	**Description**	
04h	**SEC**	**7:0**	**Default : 0x00**	**Access : R/W**
			This counter updates every second, referenced from the calibrated 32.768 kHz. It overflows from 59 to 0, incrementing the minutes counter (MIN). This register is retained during a watchdog reset. It is reset after a POR.	
05h	**MIN**	**7:0**	**Default : 0x00**	**Access : R/W**
			This counter updates every minute, referenced from the calibrated 32.768 kHz. It overflows from 59 to 0, incrementing the hours counter (HOUR). This register is retained during a watchdog reset. It is reset after a POR.	
06h	**HOUR**	**7:0**	**Default : 0x00**	**Access : R/W**
			This counter updates every hour, referenced from the calibrated 32.768 kHz clock. If the TFH bit in the RTC Configuration SFR is set, the HOUR SFR overflow from 23 to 0, setting the MIDNIGHT bit and creating a pending RTC interrupt. If the TFH bit is cleared, the HOUR SFR overflows from 255 to 0, setting the MIDNIGHT bit and creating a pending RTC interrupt. This register is retained during a watchdog reset or an external reset. It is reset after a POR.	

10.2 Interrupt Setting

The RTC provides the events for “Midnight Event” and “Interval Alarm Event”. When the RTC rolls over 00:00:00, the Midnight event will be issued. User can handle the event in the interrupt. The interrupt vector for RTC interrupt is 11.

To enable the interrupt for RTC, you need to enable the interrupt in register 0x31 in PWRHV block.

31h	**PWR_INT_EN**	**7:0**	**Default : 0xC0**	**Access : R/W**
	INT_EN_MIN_NIGHT	6	Interrupt enable for RTC Mid-Night	
	INT_EN_RESET	5	Interrupt enable for RESET	
	INT_EN_RTC	4	Interrupt enable for RTC Alarm	

There are 3 interval timers supported in the embedded RTC. You can have 3 different time intervals for each alarm. To use the alarm in RTC, correct settings are needed:

- Set the interval base
- Set the interval
- Enable the interval Timer

	Carry Out Base
Alarm 0	1/128 second, Seconds, Minutes, Hours
Alarm 1	Seconds, Minutes
Alarm 2	Seconds, Minutes

0Bh	**INTVAL_0**	**7:0**	**Default : 0x00**	**Access : R/W**
	INTVAL_0	7:0	The interval timer counts according to the time base established in the ITS_0 bits of the RTC Configuration SFR. Once the number of counts is equal to INTVAL_0, the ALARM_0 flag is set and a pending RTC interrupt is created.	

10.3 RTC Calibration and Compensation

Like common electrical components, crystals have tolerance associated with them. A crystal that is specified to have a nominal frequency of 32.768 kHz at 25°C may actually have a frequency ±20ppm.The frequency also changes over temperature. For this reason, it is important to compensate the crystal frequency variation to keep the RTC accuracy. PL8331 makes it easy to achieve this with automatic hardware compensation of the RTC and an embedded temperature sensor and SAR ADC. This section will explain how to do the RTC calibration and compensation.

Do the RTC calibration and compensation with the register “RTCCOMP” and “TEMPCAL”. Please refer to the register table. RTCCOMP is register 0x10 and 0x11 in RTC Block. And TEMPCAL is 0x12 and 0x13 in RTC block. To check the accuracy of RTC, output the clock and compare it with the RTC reference to determine the error. Choose one I/O pad as the RTC CAL output and set the output frequency as 500/512/16384 Hz depending on the setting in register 0x0E in RTC block.

11. Clock System

11.1 32K OSC

PLL = 1.024/2.048/4.096/8.192 MHz

IIC up to 400Kbps

SPI up to 1Mbps

UART up to 115.2Kbps

MCLK clock source from PLL and can be divided into 1~255 (8.192M~32.1255K Hz)

ADCLK clock source from PLL and can divide into 4~255 (2.048M~32.1255K Hz)

RTC calibration frequency output = 1Hz/500Hz

11.2 PLL

External 32.768KHz crystal is used with internal PLL as the clock system for the chip operation. The clock of the PLL could be set by the register. The PLL setting is controlled by register 0x32[6] and 0x31[1:0] in PWRLV Block

31h	**ANA_CTL13**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved	
	PLLCTL_STATUS	4	PLL Clock Status Read	
	DG_PD[6]	3	PLL power down 1: power down	
	-	2	Reserved	
	PLLFREQ[1:0] (DG_REG[54:53])	1:0	PLL output frequency select (See PLLFREQ[2:0]) (When PLL_TESTMODE = 0) 00: 8MHz, 01: 4MHz, 10: 2MHz, 11: 1MHz	

Table 11-1 : Registers for PLL Clock Setting

Not only is the PLL clock configurable, but also the MCU and meter clock. It is implemented by the clock divider after the PLL clock as shown below:

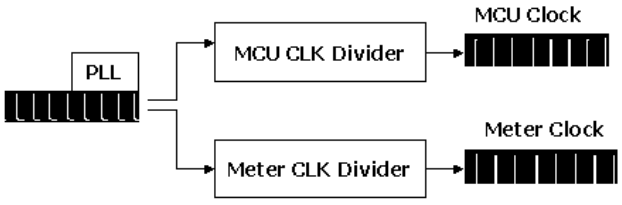


Figure 11-1 : Clock Divider for MCU and DSP

The setting for the MCU clock divider and meter clock divider is at register 0x01 and 0x02 in PAD_FUNC block.

PADs Function Control Registers - Indirect Accessing				
Address: PAD_FUNCTION_INDEX(9Eh) / Data: PAD_FUNCTION_DATA(9Fh)				
SFR-9Eh	**SFR-9Fh**	**Bits**	**Description**	
01h	**DIV51_SELECT**	**7:0**	**Default : 0x0B**	**Access : R/W**
	DIV51_SELSEL[7:0]	7:0	8051 clock source selection 0x00: bypass; 0x01: divide by 2; …… 0xFF: divide by 256;	
02h	**DIVPM_SELECT**	**7:0**	**Default : 0x07**	**Access : R/W**
	DIVPM_SELSEL[7:0]	7:0	meter clock source selection 0x00: bypass; 0x01: divide by 2; …… 0xFF: divide by 256;	

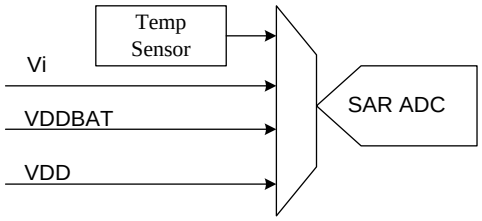
Table 11-2 : Registers for MCU and DSP Divider

For power consumption consideration, it is suggested setting MCU clock as 256K~1M and set Meter clock as 1M to get good accuracy in metering applications. User can also speed up the MCU clock if they have requirements for heavy computing loading.

12. SAR ADC and Internal Temperature Sensor

12.1 Block Diagram

There is one temperature sensor and 10-bit SAR ADC built in the PL8331 series. It can be used for monitoring the temperature in applications. This section describes how to use this function for advanced applications.



12.2 Description

There is one 10-bit SAR ADC to measure the analog input and one MUX is in front of the ADC to select the scanning channel. To monitor the temperature sensor, switch the scan channel to temperature sensor. The related settings will be described in the succeeding sections.

To use the temperature sensor, do the following steps:

(1) Enable the temperature sensor

(2) Enable the SAR ADC

(3) Trigger the Scan

(4) Read the SAR code

(5) Compute the temperature based on the read SAR code

12.2.1 Enable the Temperature Sensor

Disable the power down of SAR and Temperature SAR by setting Register 0x14[8:7] as “1” in PWRHV block.

PWRHV Control Registers - Indirect Accessing				
Address: PWRHVINDEX(FEh) / Data: PWRHVDATA(FFh)				
SFR-FEh	**SFR-FFh**	**Bits**	**Description**	
14h	**SAR_CTL11**	**7:0**	**Default : 0x00**	**Access : R/W**
		7	SAR Power Down Disable	
		6	TEMP SAR Power Down Disable	

12.2.2 Enable the SAR ADC

Disable the related power-down setting for SAR ADC in Register 0x67[4:0] in PWRHV Block.

67h	**ANA_PD1**	**7:0**	**Default : 0x1F**	**Access : R/W**
		4:0	SAR power down When one of these bits is set , SAR will power down	

It is required to set the pre-defined key to use the SAR ADC. The register for the SAR key is at 0x03 of PWRHV block.

PWRHV Control Registers - Indirect Accessing				
Address: PWRHVINDEX(FEh) / Data: PWRHVDATA(FFh)				
SFR-FEh	**SFR-FFh**	**Bits**	**Description**	
03h	**SAR_KEY**	**7:0**	**Default : 0x00**	**Access : R/W**
		7:0	SAR Register write key (8'hE8)	

12.2.3 Set the PGA Gain of the SAR ADC

For temperature, the PGA gain of the SAR ADC needs to be x16. It is set in Register0x05[5:3] in PWRHV block.

05h	**SAR_CTL0_SHADOW**	**7:0**	**Default : 0x10**	**Access : R/W**
		5:3	Gain Setting for Channel 001: x1/2 , 010: x1 , 011: x2 , 111:x16 , others : x1	

12.2.4 Select the Channel for Scanning

To scan the SAR value from the temperature sensor, trigger the scanning by setting the scan bit in register 0x04 of PWRHV block. For temperature SAR, it is in Bit[7].

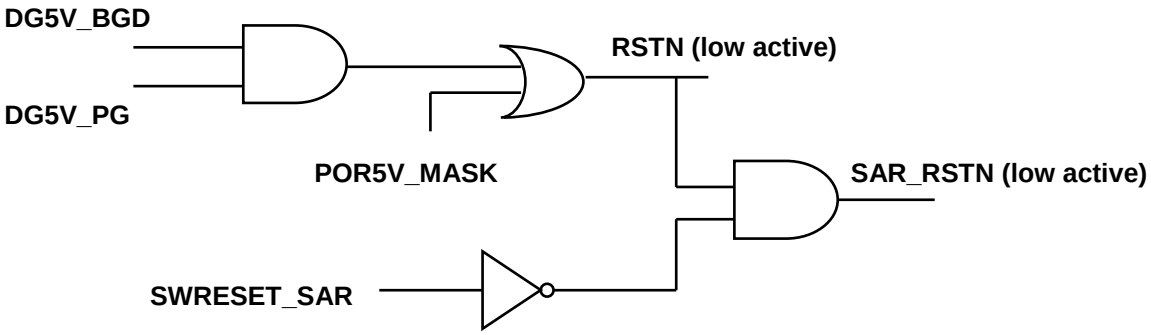
12.2.5 Read the SAR code

Once the SAR ADC completes the scan, the scan flag will be issued in Bit[4] of Register 0x11 in PWRHV block.

11h	**SAR_FLAG3**	**7:0**	**Default : 0x00**	**Access : R/W0C**
		4	Flag for Channel 7 One Time Scan	

After the scan is done, we can read out the SAR code from register 0x02[1:0] and 0x01[7:0] in PWRHV block. The implementation is illustrated in function "OneTimeScan()".

13. Reset System



The 3.3V power domain reset source comes from Bandgap and 3.3V power. It resets all circuits of the 3.3V domain. During sleep mode, the reset is blocked (POR5V_MASK is set by hardware in sleep mode). The circuit of SAR can be manually reset by setting Bit[1:0] of register 0x34 in PWRHV block.

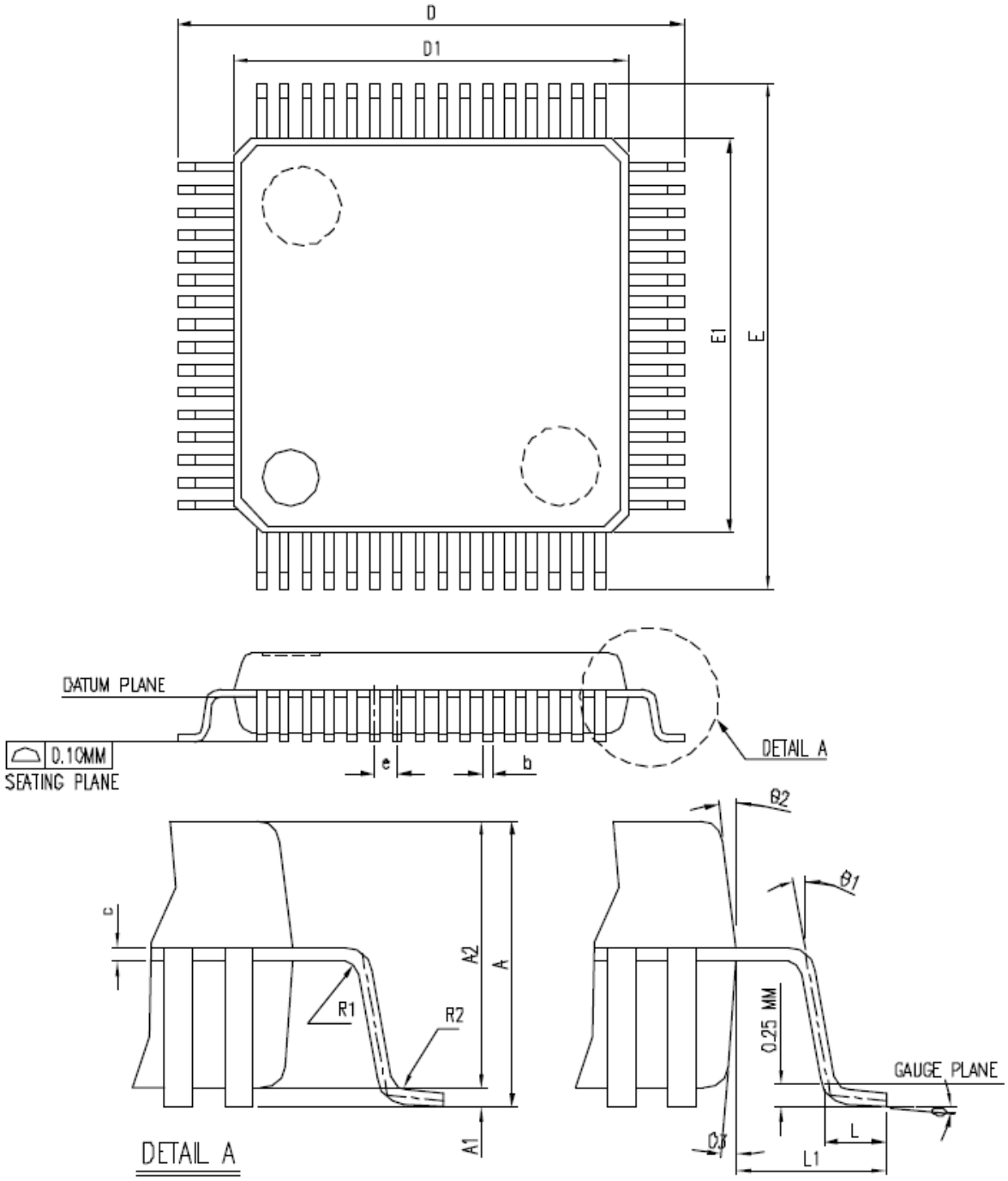
PWRHV Control Registers - Indirect Accessing				
Address: PWRHVINDEX(FEh) / Data: PWRHVDATA(FFh)				
SFR-FEh	**SFR-FFh**	**Bits**	**Description**	
34h	**SAR_CTL0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAR_HWRESET	1	Hardware Reset for SAR , high active	
	SAR_SWRESET	0	Software Reset for SAR , high active	

The DSP reset also can be triggered manually. There are two kinds. One is for all DSP/PM circuits. It can be triggered by setting Bit[0] of the register 0x10 in PWRLV block.

PWRLV Control Registers - Indirect Accessing				
Address: PWRLVINDEX(CEh) / Data: PWRLVDATA(CFh)				
SFR-CEh	**SFR-CFh**	**Bits**	**Description**	
10h	**METER_CTL0**	**7:0**	**Default : 0x02**	**Access : R/W**
	DSP_SWRESET	0	Software Reset for meter DSP , high active	

The other kind is only for DSP control register. It can be triggered by setting Bit[17:0] = 0x3FFFF of the register 0x2F in DSP Control Register.

14. Package Outline Dimensions – PL8331 (7x7 - 64 pins)



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.0019		0.0059
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
c	0.09		0.20	0.0035		0.0078
e	0.40 BASIC			0.016 BASIC		
D	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E	9.00 BASIC			0.354 BASIC		
E1	7.00 BASIC			0.276 BASIC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
R1	0.08			0.0031		
R2	0.08		0.20	0.0031		0.0078
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
JEDEC	MS-026 (BBD)					

*NOTES : DIMENSIONS " D1 " AND " E1 " DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. " D1 " AND " E1 " ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

Figure 14-1 : PL8331 Package Outline Dimension

15. Ordering Information

15.1 Packaging Information

Device	Package Type	Pins	Temperature Range	ECO	Notes
PL8331	LQFP (7x7)	64	-40°C ~ +80°C	Green (RoHS)	

Table 15-1：Packaging Information

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