

# PLA133-47

## Low-Power DC to 160 MHz 1:4 Fanout Buffer IC for Automotive

#### **Features**

- · Automotive AEC-Q100 Qualified
- 1:4 LVCMOS Output Fanout Buffer from DC to 160 MHz
- · Low Additive Phase Jitter of 60 fs RMS
- · 8 mA Output Drive Strength
- Low Power Consumption for Portable Applications
- · Automotive Applications Grade Compliant
- · Low Input-Output Delay
- Output-Output Skew <250 ps
- 2.5V to 3.3V, ±10% Operation
- 1.8V +10%/-5% Operation up to 67 MHz
- Wide Temperature Range: -40°C to +125°C
- · Available in 8-Pin SOIC Package

#### **Applications**

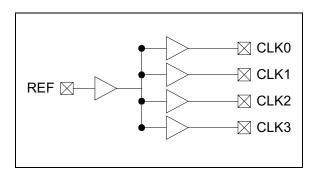
- · Automotive Applications:
  - ADAS Vision System
  - Infotainment and Dashboard

#### **General Description**

The PLA133-47 is an advanced fanout buffer designed for automotive applications and other high performance, low-power, small form factor applications. The PLA133-47 accepts a reference clock input from DC to 160 MHz and provides four outputs of the same frequency with ultra-low additive jitter. The device is AEC-Q100 qualified.

The PLA133-47 is available in a SOIC-8L package.

### **Functional Block Diagram**



## 1.0 ELECTRICAL CHARACTERISTICS

## **Absolute Maximum Ratings †**

Supply Voltage to Ground Potential	
DC Input Voltage	V <sub>SS</sub> –0.5V to +4.6V
Static Discharge Voltage	
(Per MIL-STD-883, Method 3015)	>2000V

## **Operating Ratings †**

**† Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

#### **ELECTRICAL CHARACTERISTICS**

Parameter	Symbol	Min.	Тур.	Max.	Units	Conditions
Input Low Voltage	V <sub>IL</sub>	-		$0.3xV_{DD}$	V	Note 1
Input High Voltage	V <sub>IH</sub>	$0.7xV_{DD}$	1	_	V	Note 1
Input Low Current	I <sub>IL</sub>		ı	50	μΑ	V <sub>IN</sub> = 0V
Input High Current	I <sub>IH</sub>	_	_	100	μΑ	$V_{IN} = V_{DD}$
Supply Current	$I_{DD}$	_	-	32	mA	66.67 MHz with unloaded outputs
			-	0.5		$I_{O} = 8 \text{ mA}, V_{DD} = 3.3 \text{V}$
Output Low Voltage	$V_{OL}$	_	_	0.5	V	$I_{O} = 6 \text{ mA}, V_{DD} = 2.5 \text{V}$
		_	-	0.5		I <sub>O</sub> = 4 mA, V <sub>DD</sub> = 1.8V
		V <sub>DD</sub> - 0.5	-	_		$I_{O} = -8 \text{ mA}, V_{DD} = 3.3 \text{V}$
Output High Voltage	V <sub>OH</sub>	V <sub>DD</sub> - 0.5	_		V	$I_{O} = -6 \text{ mA}, V_{DD} = 2.5 \text{V}$
		V <sub>DD</sub> - 0.5	-	_		$I_{O} = -4 \text{ mA}, V_{DD} = 1.8V$
			l	30		Load Capacitance, below 100 MHz, V <sub>DD</sub> > 2.25V
Load Capacitance				10	pF	Load Capacitance between 100 MHz and 134 MHz, V <sub>DD</sub> > 2.25V
Luau Capacitance	CL			5		Load Capacitance, above 134 MHz, V <sub>DD</sub> > 2.25V
			l	15		Load Capacitance, below 67 MHz, 1.71V < V <sub>DD</sub> < 2.25V
Input Capacitance	C <sub>IN</sub>			7	pF	_
Power-Up Time	t <sub>PU</sub>	0.05	_	50	ms	Power-up time for all V <sub>DD</sub> to reach minimum specified voltage (power ramps must be monotonic)

Note 1: REF input has a threshold voltage of V<sub>DD</sub>/2.

#### **SWITCHING CHARACTERISTICS Note 2**

Parameter	Symbol	Min.	Тур.	Max.	Units	Conditions
Operating Frequency	f	DC	_	160	MHz	V <sub>DD</sub> = 3.3V, 2.5V
Operating Frequency	ļ ļ	DC	_	67	MHz	V <sub>DD</sub> = 1.8V
Duty Cycle = t <sub>2</sub> ÷ t <sub>1</sub>	_	40	50	60	%	Measured at 1.4V, Input is 50%
Rise Time	t <sub>3</sub>	_	_	1.5	ns	Measured between 0.8V and 2.0V
Fall Time	t <sub>4</sub>	_	_	1.5	ns	Measured between 0.8V and 2.0V
Output to Output Skew Note 1	t <sub>5</sub>			250	ps	All outputs equally loaded
Propagation Delay, REF Rising Edge to CLKX Rising Edge Note 1	t <sub>6</sub>	1	5	9.2	ns	Measured at V <sub>DD</sub> /2

**Note 1:** Parameter is guaranteed by design and characterization.

2: All parameters are specified with loaded outputs.

#### **NOISE CHARACTERISTICS**

Parameter	Symbol	Min.	Тур.	Max.	Units Conditions	
Additive Phase Jitter	_	_	60	_	fs	V <sub>DD</sub> = 3.3V, Frequency = 100 MHz Integration range 12 kHz - 20 MHz

## **TEMPERATURE SPECIFICATIONS (Note 1)**

Parameters	Symbol	Min.	Тур.	Max.	Units	Conditions		
Temperature Ranges								
Ambient Operating Temperature	T <sub>A</sub>	-40	_	+125	°C	Commercial		
Junction Temperature	TJ	_	_	+150	°C	_		
Storage Temperature Range	T <sub>S</sub>	-65	_	+150	°C	_		
Package Thermal Resistance								
8-Lead SOIC	$R_{\theta JA}$	_	_	103.2	°C/W	_		

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T<sub>A</sub>, T<sub>J</sub>, θ<sub>JA</sub>). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.

## 2.0 PIN DESCRIPTIONS

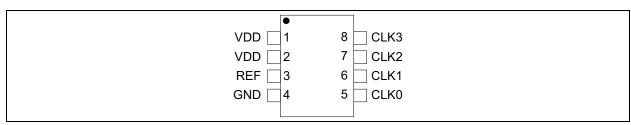


FIGURE 2-1: Pin Configuration, 8-Lead SOIC Package.

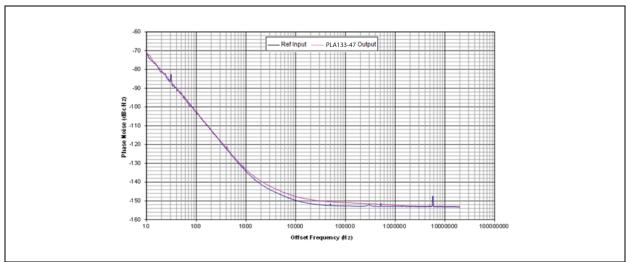
The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Туре	Description		
1, 2	VDD	Р	VDD connection		
3	REF	I	Input reference frequency		
4	GND	Р	GND connection		
5	CLK0	0	Buffered clock output		
6	CLK1	0	Buffered clock output		
7	CLK2	0	Buffered clock output		
8	CLK3	0	Buffered clock output		

#### 3.0 NOMINAL PERFORMANCE CHARACTERISTICS

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.



**FIGURE 3-1:** PLA133-47 Additive Phase Jitter:  $V_{DD} = 3.3V$ , CLK-100 MHz, Integration Range 2 kHz - 20 MHz, 0.059 ps Typical.

When a buffer is used to pass a signal then the buffer will add a little bit of its own noise. The phase noise on the output of the buffer will be a little bit more than the phase noise in the input signal. The noise added by the buffer to the input signal is quantified by the additive phase jitter defined by the following formula:

#### **EQUATION 3-1:**

$$Additive Phase Jitter = \sqrt{(Output Phase Jitter)^2 - (Input Phase Jitter)^2}$$

## 4.0 SWITCHING WAVEFORMS

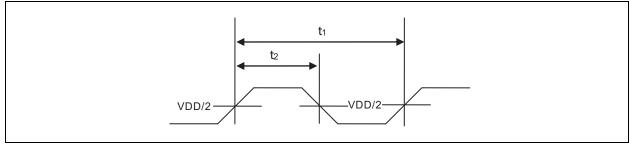


FIGURE 4-1: Duty Cycle Timing.

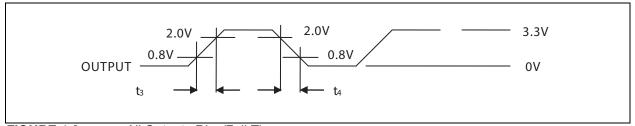


FIGURE 4-2: All Outputs Rise/Fall Time.

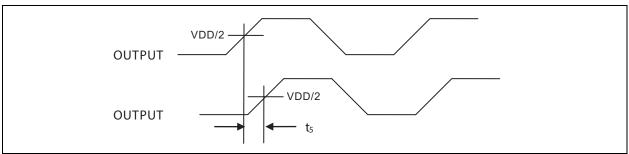


FIGURE 4-3: Output to Output Skew.

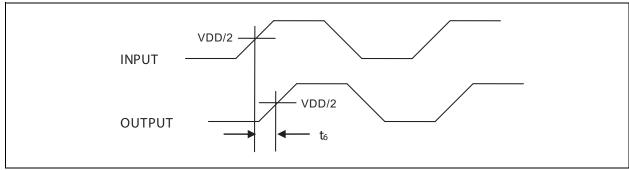


FIGURE 4-4: Input-Output Propagation Delay.

## 5.0 TEST CIRCUIT

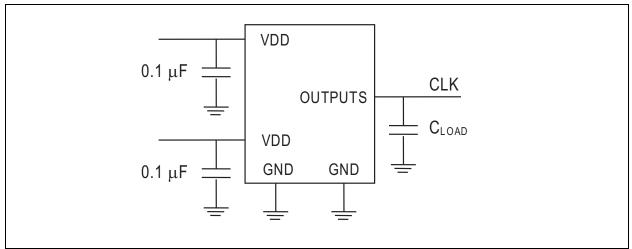


FIGURE 5-1: Test Circuit.

#### 6.0 LAYOUT RECOMMENDATIONS

The following guidelines are to assist you with a performance optimized PCB design:

## 6.1 Signal Integrity and Termination Considerations

- Keep traces short
- Trace = Inductor. With a capacitive load this equals ringing
- Long trace = Transmission Line. Without proper termination this will cause reflections ringing and waveforms and degradations.
- Use stripline or microstrip with defined impedance for long traces (> 1 inch)
- Match traces on one side of the board to avoid reflections bouncing back and forth.

# 6.2 Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the VDD pin(s) to limit noise from the power supply
- Addition of a ferrite bead in series with VDD can help prevent noise from other board sources
- Value of decoupling capacitor is frequency dependant. Typical values to use are 0.1 μF for designs using frequencies <50 MHz and 0.01 μF for designs using frequencies >50 MHz

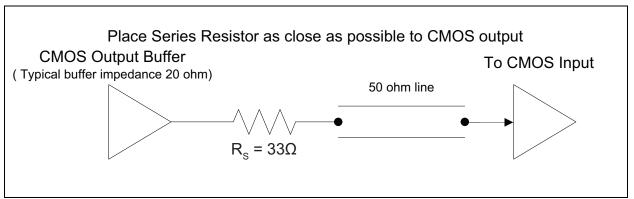


FIGURE 6-1: Typical CMOS Termination.

#### 7.0 PACKAGING INFORMATION

#### 7.1 **Package Marking Information**

8-Lead SOIC\*

XXXXXXX WWNNN

Example

P133-47 SA 16524

Legend: XX...X Product code, customer-specific information, or frequency in MHz

without printed decimal point

Year code (last digit of calendar year) ΥY Year code (last 2 digits of calendar year) WW Week code (week of January 1 is week '01')

Alphanumeric traceability code NNN

**e**3 Pb-free JEDEC<sup>®</sup> designator for Matte Tin (Sn)

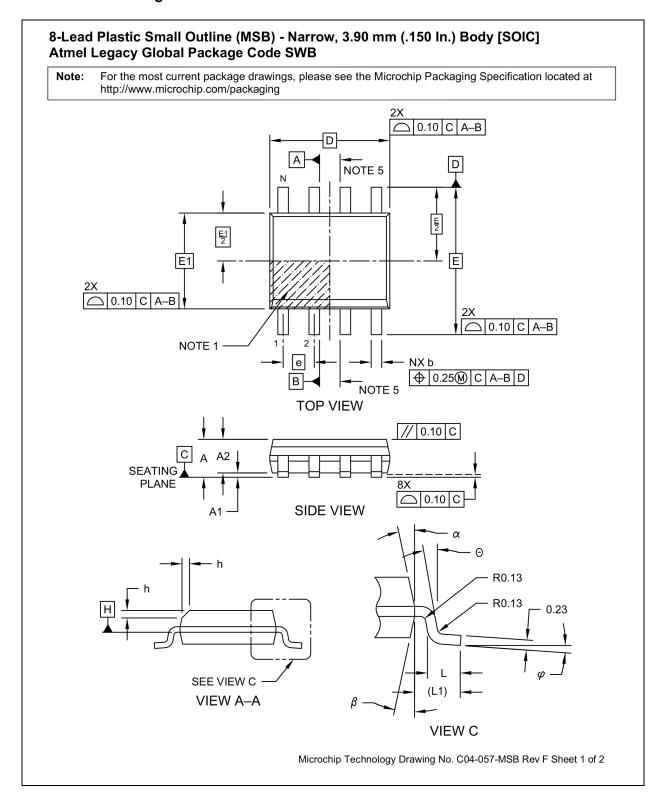
This package is Pb-free. The Pb-free JEDEC designator (@3) can be found on the outer packaging for this package.

•, ▲, ▼ Pin one index is identified by a dot, delta up, or delta down (triangle mark).

In the event the full Microchip part number cannot be marked on one line, it will Note: be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

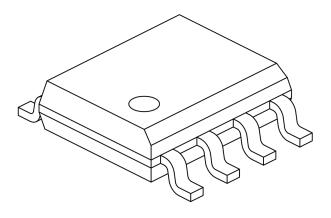
Underbar ( ) and/or Overbar ( ) symbol may not be to scale.

## 8-Lead SOIC Package Outline and Recommended Land Pattern



## 8-Lead Plastic Small Outline (MSB) - Narrow, 3.90 mm (.150 ln.) Body [SOIC] Atmel Legacy Global Package Code SWB

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX
Number of Pins	N		8	
Pitch	е		1.27 BSC	
Overall Height	Α	ı	ı	1.75
Molded Package Thickness	A2	1.25	ı	-
Standoff §	A1	0.10	ı	0.25
Overall Width	Е	6.00 BSC		
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	С	0.17 - 0.25		
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5° - 15°		
Mold Draft Angle Bottom	β	5°	-	15°

#### Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic
- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

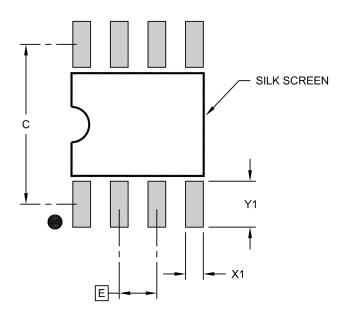
REF: Reference Dimension, usually without tolerance, for information purposes only.

5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-MSB Rev F Sheet 2 of 2  $\,$ 

# 8-Lead Plastic Small Outline (MSB) - Narrow, 3.90 mm (.150 ln.) Body [SOIC] Atmel Legacy Global Package Code SWB

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



#### RECOMMENDED LAND PATTERN

	N	IILLIMETER:	S	
Dimension	MIN	NOM	MAX	
Contact Pitch	Е	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

#### Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-MSB Rev F

PI	Δ	1	33	-4	7
		١.		, T	

NOTES:

#### APPENDIX A: REVISION HISTORY

## Revision A (June 2020)

 Initial release of PLA133-47 as Microchip data sheet DS20006357A.

## **Revision B (October 2020)**

• Changed the operating frequency to 160 MHz which was wrongly input as 150 MHz.

#### Revision C (December 2020)

• Changed the description for Pins 1, 2, and 7 in the Pin Descriptions table.

## **Revision D (February 2021)**

 Updated all instances of SOP package to reflect the new SOIC package.

PI	Δ	1	33	-4	7
		١.		, T	

NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.		<u>x</u>	<u>X</u>	<u>x</u>	XXX
Device		Package	Temperature Range	Media Type	Automotive Suffix
Device:	PLA133-47 S =	: Low-Power DC to 160 Mi IC for Automotive 8-Lead SOIC Package	Hz 1:4 Fanout Buffer	<b>Examples:</b> a) PLA133-47SAVAO	Low-Power DC to 160 MHz 1:4 Fanout Buffer IC, SOIC Package, –40°C to +125°C, 100/ Tube, Standard automotive
Temperature Range:	A = (blank) = R =	-40°C to +125°C 100/Tube 3,300/Reel		b) PLA133-47SA-RVA	
Automotive Suffix:	Micro	motive Suffix in which "XX" i ochip. Standard value "AO" i ve part.		catalog par used for ord the device	teel identifier only appears in the t number description. This identifier is dering purposes and is not printed on package. Check with your Microchip e for package availability with the teel option.

P	ΙΔ	1	33	<b>-47</b>
		١.		-TI

NOTES:

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