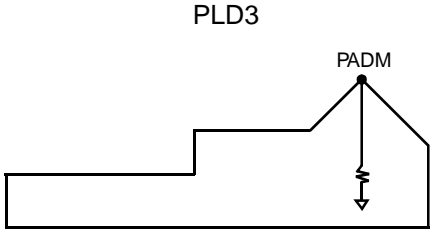


## AMI5HG 0.5 micron CMOS Gate Array

### Description

PLD3 is an active pull-down buffer piece.

Logic Symbol	Truth Table	Pin Loading
 <p>The logic symbol for PLD3 is a buffer with a pull-down resistor. The output is labeled PADM. The symbol shows a step-up buffer with a pull-down resistor connected to the output node.</p>	<p>N/A</p>	<p>N/A</p>

### HDL Syntax

Verilog ..... PLD3 *inst\_name* (PADM);

VHDL ..... *inst\_name*: PLD3 port map (PADM);

### Power Characteristics

Parameter	Value	Units
Static $I_{DD}$ ( $T_J = 85^\circ\text{C}$ )	TBD	nA
$EQL_{pd}$	149.8	Eq-load

See page 2-15 for power equation.