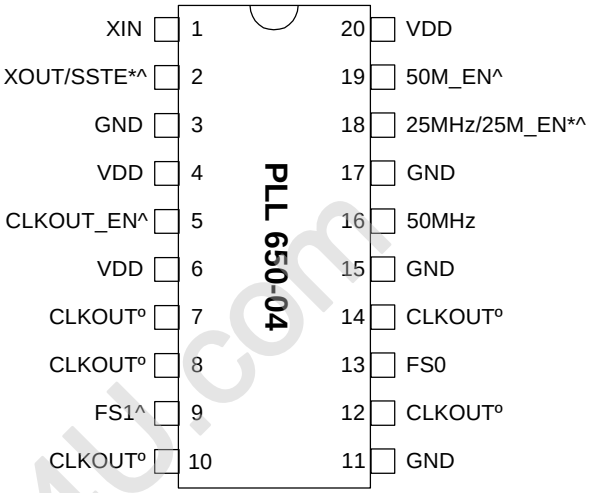
# Low EMI Clock for 10/100 PHY and Gigabit Ethernet

## FEATURES

- Full CMOS output swing with 25-mA output drive capability at TTL level.
- Advanced, low power, sub-micron CMOS processes.
- 25 MHz fundamental crystal or clock input.
- Low jitter (< 80ps cycle-to-cycle)
- 25 MHz and 50 MHz outputs
- Five CLKOUT selectable between 90, 100, 125, 133, 145 and 150 MHz.
- SSTE (SST Enable) Low EMI selector for CLKOUT.
- Output enable functionality.
- Zero PPM synthesis error in all clocks.
- Ideal for Network switches.
- 3.3V operation.
- Available in 20-Pin 150mil SSOP.

## PIN CONFIGURATION




**Note:** ^: Internal pull-up resistor *: Bi-directional pin º: Low EMI output

## DESCRIPTION

The PLL 650-04 is a low cost, low jitter, and high performance clock synthesizer. With PhaseLink proprietary analog Phase Locked Loop techniques, the chip accepts 25.0 MHz crystal, and produces multiple output clocks for networking chips. A CLKOUT signal of selectable frequency (25MHz, 48MHz, 50MHz, 90MHz, 100MHz, 125MHz, 133MHz, 145MHz or 150 MHz) is available at 5 output pins. Through an SST enable (SSTE) selector, the CLKOUT signal can be modulated to reduce EMI through Spread Spectrum Technology. Output enable selectors are available to enable/disable the output signals.

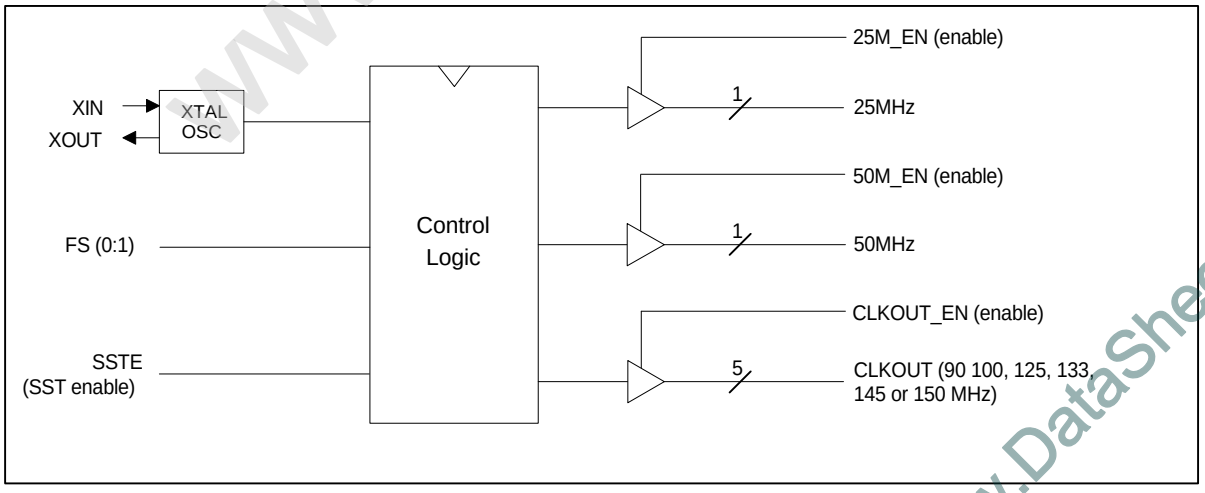
## SELECTION TABLE

| FS1 | FS0 | CLKOUT |
|---|---|---|
| 0 | 0 | 90 MHz |
| 0 | M | 100 MHz |
| 0 | 1 | 125 MHz |
| 1 | 0 | 133 MHz |
| 1 | M | 145 MHz |
| 1 | 1 | 150 MHz |

Tri-level input pins: 0 = connect to GND
M= not connected, 1 = connect to VDD

| SSTE | SST MODULATION |
|---|---|
| 0 | +0.25% Center spread |
| 1 | OFF |

## BLOCK DIAGRAM



## PIN DESCRIPTIONS

| Name | Number | Type | Description |
|---|---|---|---|
| XIN | 1 | I | Crystal input to be connected to a 25MHz fundamental parallel mode crystal ($C_L$=20pF). |
| XOUT/SSTE | 2 | B | Crystal connector. At power-up, the SSTE value that enables/disables the spread spectrum function is latched in. 120kΩ internal pull up resistor. |
| GND | 3,11,15,17 | P | Ground. |
| VDD | 4,6,20 | P | 3.3V power supply. |
| CLKOUT_EN | 5 | I | CLKOUT enable pin. Disables CLKOUT to tri-state if 'low' (logical 0). Internal 60kΩ pull-up resistor defaults it to 'high' (logical 1). |
| CLKOUT | 7,8,10,12,14 | O | CLKOUT outputs with selectable frequency through FS(0:1). CLKOUT can be modulated using SST to reduce EMI through SSTE. CLKOUT can be disabled to tri-state with CLKOUT_EN. |
| FS0 | 13 | TL | Tri-level frequency selector pin (See selection table on p.1). 0: connected to GND, 1: connected to VDD, M: not connected. |
| FS1 | 9 | I | Frequency selector pin (standard bi-level '1' or '0'). See table on p.1. Internal 60kΩ pull-up resistor defaults it to 'high' (logical 1). |
| 50 MHz | 16 | O | 50 MHz output. This output is not modulated with Spread Spectrum. This output can be disabled to tri-state with 50M_EN. |
| 25 MHz/25M_EN | 18 | B | 25 MHz output, not modulated with Spread Spectrum. Bi-directional pin: at power-up, the input value 25M_EN is latched-in. If 25M_EN (25MHz output enable) is low, the pin will be disabled to tri-state after power-up, if 25M_EN is high, the out pin will be enabled and provide a 25 MHz output signal after power-up. Internal 60kΩ pull-up resistor defaults it to 'high' (logical 1). |
| 50M_EN | 19 | I | 50 MHz output enable pin. Disables the 50MHz output to tri-state if 'low' (logical 0). Internal 60kΩ pull-up resistor defaults it to 'high' (logical 1). |

## FUNCTIONAL DESCRIPTION

### Selectable spread spectrum and output frequencies

The PLL650-04 provides selectable spread spectrum modulation and selectable output frequencies for the CLKOUT signal. Selection is made by connecting specific pins to a logical "zero" or "one", according to the frequency and spread spectrum selection tables shown on page 1.

In order to reduce the number of pins on the chip, the PLL650-04 uses bi-directional pins that serve as inputs upon power-up, and as outputs as soon as the inputs have been latched.

Pins 2 (SSTE) is a bi-directional pin used as input to enable/disable the spread spectrum modulation upon power-up, and used as XOUT crystal connection after the SSTE input signal has been latched. Pin 18 (25M_EN) is a bi-directional pin used to enable/disable the 25MHz output upon power-up. After the input signal has been latched, pin 18 will serve as 25 MHz output or will be disabled, depending on the power-up value of 25M_EN.

## Connecting a selection pin to a logical "one"

The output enable and spread spectrum selection pins have an internal pull-up resistor (60kΩ for all selection pins except for pin 2 (SSTE), which has a 120kΩ internal pull-up). This internal pull-up resistor will pull the input value to a logical "one" (pull-up) by default, i.e. when no resistive load is connected between the pin and GND. No external pull-up resistor is therefore required for connecting a logical "one" upon power-up. ***Note:*** *when the output load presents a low impedance in comparison to the internal pull-up resistor, the internal pull-up resistor may not be sufficient to pull the input up to a logical "one", and an external pull-up resistor may be required.*

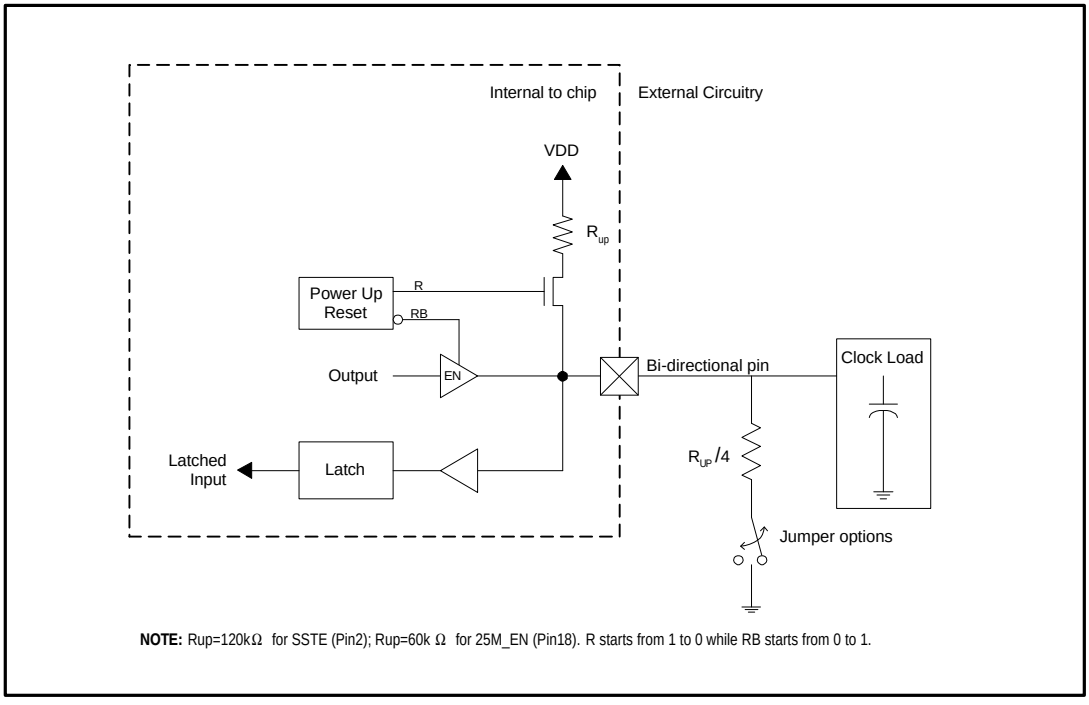
## Connecting a selection pin to a logical "zero"

Connecting the bi-directional pin to a logical "zero" does require the use of an external loading resistor between the pin and GND that has to be sufficiently small (compared to the internal pull-up resistor) so that the pin voltage be pulled below 0.8V (logical "zero"). In order to avoid loading effects when the pin serves as output, the value of the external pull-down resistor should however be kept as large as possible. In general, it is recommended to use an external resistor of around one sixth to one quarter of the internal pull-up resistor (see Application Diagram). ***Note:*** *when the output is used to drive a load presenting an small resistance between the output pin and VDD, this resistance is in essence connected in parallel to the internal pull-up resistor. In such a case, the external pull-down resistor may have to be dimensioned smaller to guarantee that the pin voltage will be low enough achieve the desired logical "zero". This is particularly true when driving 74FXX TTL components.*

## Selecting the output frequency (CLKOUT) with the tri-level selection pin

The CLKOUT frequency is selected with the tri-level FS(0:1) input pins, as per the frequency selection table on page 1. Unlike the other bi-level selection pins, the tri-level input pins are in the "M" (mid) state when not connected. In order to connect a tri-level pin to a logical "zero", the pin must be connected to GND. Similarly, in order to connect a tri-level pin to a logical "one", the pin must be connected to VDD. No external pull-up or pull-down resistor is required with the tri-level selector pins.

## APPLICATION DIAGRAM




**NOTE:** Rup=120kΩ for SSTE (Pin2); Rup=60k Ω for 25M_EN (Pin18). R starts from 1 to 0 while RB starts from 0 to 1.

## Electrical Specifications

### 1. Absolute Maximum Ratings

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS |
|---|---|---|---|---|
| Supply Voltage Range | $V_{CC}$ | -0.5 | 7 | V |
| Input Voltage Range | $V_I$ | -0.5 | $V_{CC}$+0.5 | V |
| Output Voltage Range | $V_O$ | -0.5 | $V_{CC}$+0.5 | V |
| Soldering Temperature | | | 260 | °C |
| Storage Temperature | $T_S$ | -65 | 150 | °C |
| Ambient Operating Temperature | | 0 | 70 | °C |

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

### 2. AC Specification

| PARAMETERS | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|
| Input Frequency | | 10 | 24 | 27 | MHz |
| Output Rise Time | 0.8V to 2.0V with no load | | | 1.5 | ns |
| Output Fall Time | 2.0V to 0.8V with no load | | | 1.5 | ns |
| Duty Cycle | At VDD/2 | 45 | 50 | 60 | % |
| Max. Absolute Jitter | Short term | | ±150 | | ps |
| Max. Jitter, cycle to cycle | | | | 80 | ps |

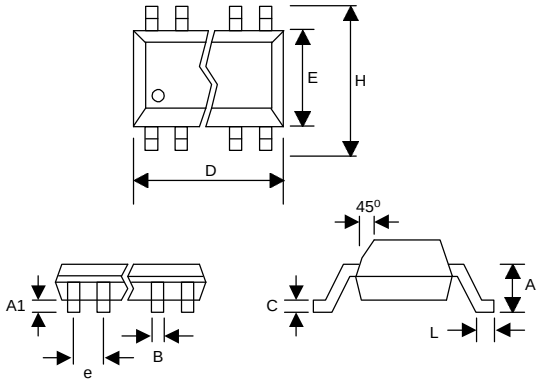
## 3. DC Specification

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| Operating Voltage | VDD | | 3.13 | | 3.47 | V |
| Input High Voltage | $V_{IH}$ | | | VDD/2 | | V |
| Input Low Voltage | $V_{IL}$ | | | VDD/2 | VDD/2 - 1 | V |
| Input High Voltage | $V_{IH}$ | For all Tri-level input | VDD-0.5 | | | V |
| Input Low Voltage | $V_{IL}$ | For all Tri-level input | | | 0.5 | V |
| Input High Voltage | $V_{IH}$ | For all normal input | 2 | | | V |
| Input Low Voltage | $V_{IL}$ | For all normal input | | | 0.8 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -25mA | 2.4 | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 25mA | | | 0.4 | V |
| Output High Voltage At CMOS Level | $V_{OH}$ | $I_{OH}$ = -8mA | VDD-0.4 | | | V |
| Operating Supply Current | $I_{DD}$ | No Load | | 35 | | mA |
| Short-circuit Current | $I_S$ | | | ±100 | | mA |
| Internal pull-up resistor | $R_{up}$ | Pins 5,18,19 | | 60 | | kΩ |
| Internal pull-up resistor | $R_{up}$ | Pin 2 | | 120 | | kΩ |

## PACKAGE INFORMATION

20 PIN Narrow SSOP (inches)

| | SSOP | |
|---|---|---|
| Symbol | Min. | Max. |
| A | 0.053 | 0.069 |
| A1 | 0.004 | 0.010 |
| B | 0.008 | 0.012 |
| C | 0.007 | 0.010 |
| D | 0.337 | 0.344 |
| E | 0.150 | 0.157 |
| H | 0.228 | 0.244 |
| L | 0.016 | 0.050 |
| e | 0.025 BSC | |




## ORDERING INFORMATION

***For part ordering, please contact our Sales Department:***
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

***PART NUMBER***

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

**PLL650-04 X C**

*PART NUMBER*

TEMPERATURATURE
C=COMMERCIAL
M=MILITARY
I=INDUSTRAL

PACKAGE TYPE
X=SSOP