

# Programmable logic sequencers

## (14 × 48 × 6)

PLS167/A

### DESCRIPTION

The PLS167 and PLS167A are bipolar, Programmable Logic State machines of the Mealy type. The Programmable Logic Sequencers (PLS) contain logic AND/OR gate arrays with user programmable connections which control the inputs of on-chip State and Output Registers. These consist respectively of 8 Q<sub>p</sub>, and 4 Q<sub>r</sub> edge-triggered, clocked S/R flip-flops, with an asynchronous Preset Option.

All flip-flops are unconditionally preset to "1" during power turn-on.

The AND array combines 14 external inputs, I0-13, with 8 internal inputs, P0-7, fed back from the State Register to form up to 48 transition terms (AND terms). In addition, P0 and P1 of the internal State Register are brought off-chip to allow extending the Output Register to 6 bits, if so desired.

All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the Low-to-High transition of the Clock pulse.

Both True and Complement transition terms can be generated by optional use of the internal variable (C) from the Complement Array. Also, if desired, the Preset input can be converted to output-enable function, as an additional user programmable option.

Order codes are listed in the Ordering Information Table.

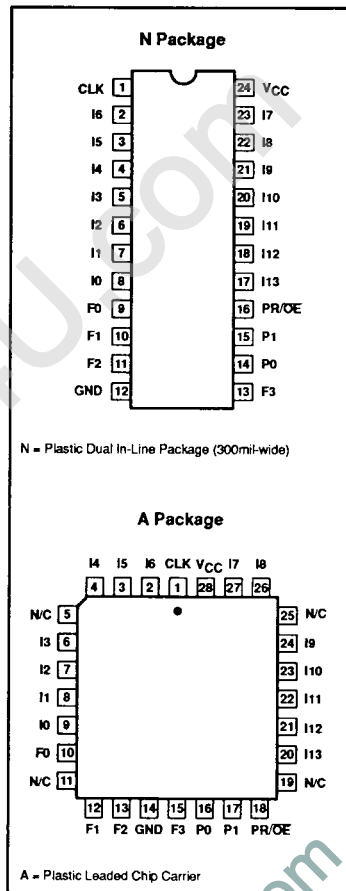
### FEATURES

- PLS167
  - f<sub>MAX</sub> = 13.9MHz
  - 20MHz clock rate
- PLS167A
  - f<sub>MAX</sub> = 20MHz
  - 25MHz clock rate
- Field-Programmable (Ni-Cr link)
- 14 True/Complement buffered inputs
- 48 programmable AND gates
- 25 programmable OR gates
- 8-bit State Register
- 2-bit shared State/Output Register
- 4-bit Output Register
- Transition Complement Array
- Programmable Asynchronous Preset/Output Enable
- Positive edge-triggered clock
- Power-on preset to logic "1" of all registers
- Automatic logic "HOLD" state via S/R flip-flops
- On-chip Test Array
- Power: 600mW (typ.)
- TTL compatible
- 3-State outputs
- Single +5V supply

### APPLICATIONS

- Interface protocols
- Sequence detectors
- Peripheral controllers
- Timing generators
- Sequential circuits
- Security locking systems

### PIN CONFIGURATIONS



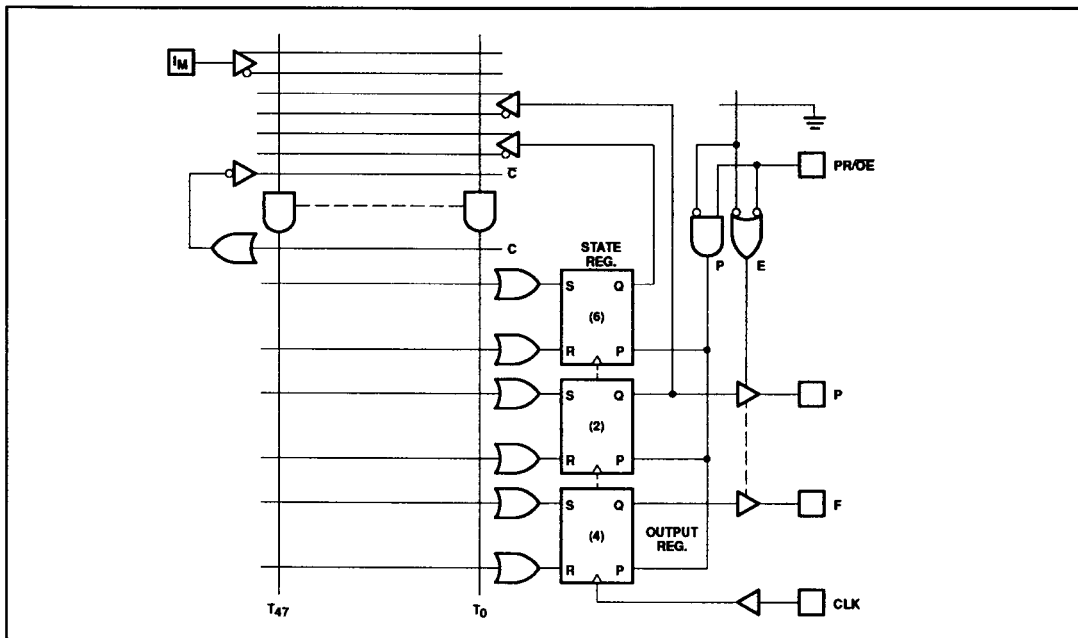
### ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
24-Pin Plastic Dual In-Line Package (300mil-wide)	PLS167N, PLS167AN	0410D
28-Pin Plastic Leaded Chip Carrier	PLS167A, PLS167AA	0401F

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## FUNCTIONAL DIAGRAM



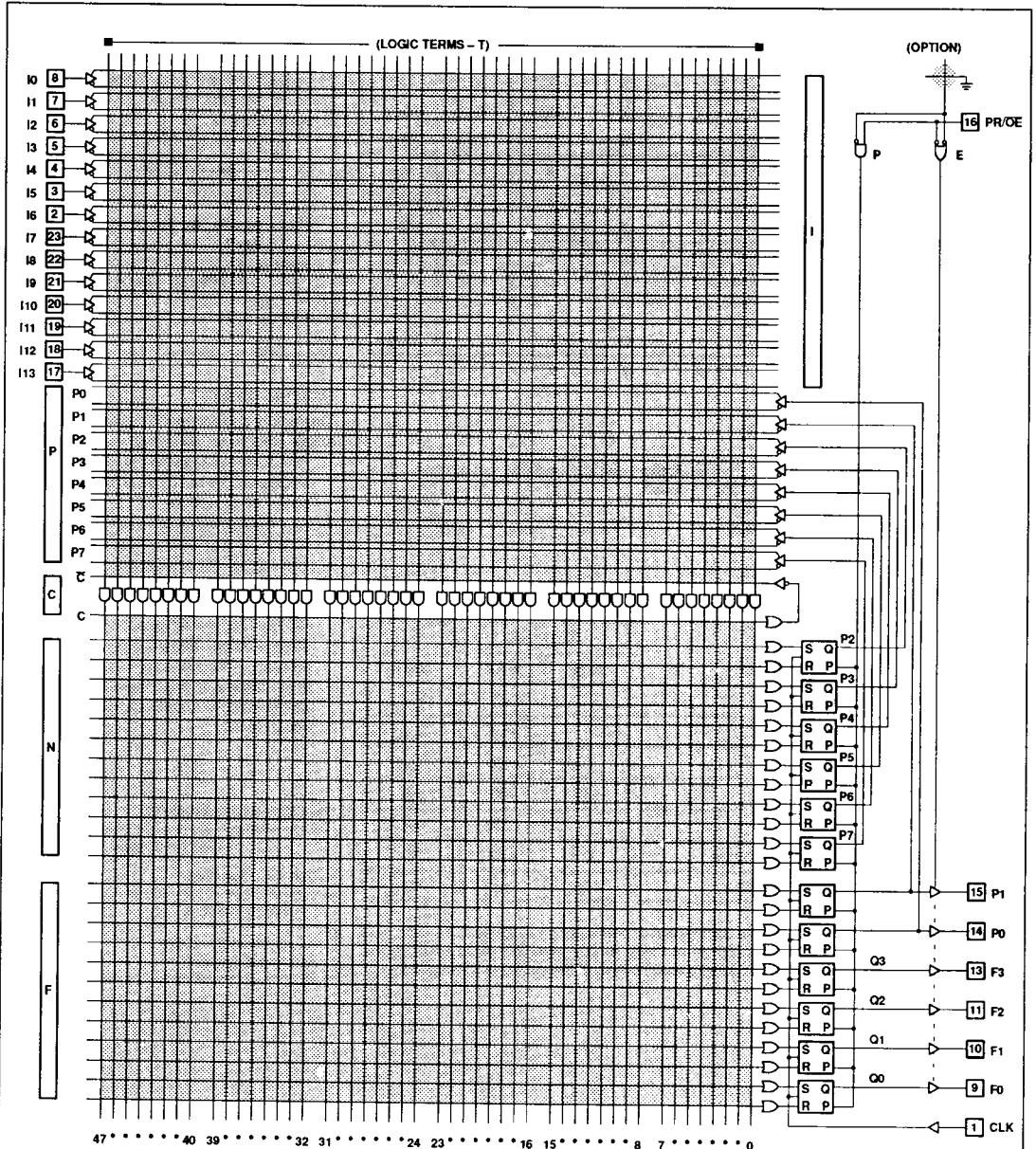
## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CLK	<b>Clock:</b> The Clock input to the State and Output Registers. A Low-to-High transition on this line is necessary to update the contents of both registers.	Active-High
2 – 7 17 – 23	I1 – I13	<b>Logic Inputs:</b> The 13 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence.	Active-High/Low
8	I0	<b>Logic/Diagnostic Input:</b> A 14th external logic input to the AND array, as above, when exercised with standard TTL levels. When I0 is held at +10V, device outputs F0 – 3 and P0 – 1 reflect the contents of State Register bits P2 – 7 (see Diagnostic Output Mode diagram). The contents of flip-flops P0 – 1 and F0 – 3 remain unaltered.	Active-High/Low
9 – 11 13	F0 – 3	<b>Logic/Diagnostic Outputs:</b> Four device outputs which normally reflect the contents of Output Register bits Q0 – 3, when enabled. When I0 is held at +10V, F0 – 3 = (P2 – 5).	Active-High
14 – 15	P0 – 1	<b>Logic/Diagnostic Outputs:</b> Two register bits with shared function as least Significant State Register bits, or most significant Output Register bits. When I0 is held at +10V, P0 – 1 = (P6 – 7).	Active-High
16	PR/OE	<b>Preset or Output Enable Input:</b> A user programmable function: <ul style="list-style-type: none"> <li>• <b>Preset:</b> Provides an Asynchronous Preset to logic "1" of all State and Output Register bits. Preset overrides Clock, and when held High, clocking is inhibited and P0 – 7 and F0 – 3 are High. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after Preset goes Low.</li> <li>• <b>Output Enable:</b> Provides an Output Enable function to all output buffers.</li> </ul>	Active-High (H)  Active-Low (L)

# Programmable logic sequencers (14 × 48 × 6)

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## LOGIC DIAGRAM



- NOTES:**
1. All AND gate inputs with a blown link float to a logic "1".
  2. All OR gate inputs with a blown fuse float to logic "0".
  3. Programmable connection.

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TRUTH TABLE 1, 2, 3, 4, 5, 6

V <sub>CC</sub>	OPTION		I <sub>0</sub>	CK	S	R	Q <sub>P/F</sub>	F
	PR	OE						
+5V	H		*	X	X	X	H	H
	L		+10V	X	X	X	Q <sub>n</sub>	(Q <sub>P</sub> ) <sub>n</sub>
	L		X	X	X	X	Q <sub>n</sub>	(Q <sub>F</sub> ) <sub>n</sub>
		H	*	X	X	X	Q <sub>n</sub>	Hi-Z
		L	+10V	X	X	X	Q <sub>n</sub>	(Q <sub>P</sub> ) <sub>n</sub>
		L	X	X	X	X	Q <sub>n</sub>	(Q <sub>F</sub> ) <sub>n</sub>
		L	X	↑	L	L	Q <sub>n</sub>	(Q <sub>F</sub> ) <sub>n</sub>
		L	X	↑	L	H	L	L
		L	X	↑	H	L	H	H
		L	X	↑	H	H	IND.	IND.
↑	X	X	X	X	X	X	H	

## NOTES:

- Positive Logic:  
S/R = T<sub>0</sub> + T<sub>1</sub> + T<sub>2</sub> + ... T<sub>47</sub>  
T<sub>n</sub> = C(I<sub>0</sub> I<sub>1</sub> I<sub>2</sub> ... ) (P<sub>0</sub> P<sub>1</sub> ... P<sub>7</sub>)
- Either Preset (Active-High) or Output Enable (Active-Low) are available, but not both. The desired function is a user-programmable option.
- ↑ denotes transition from Low-to-High level.
- R = S = High is an illegal input condition.
- \* = H or L or +10V.
- X = Don't Care (≤5.5V)

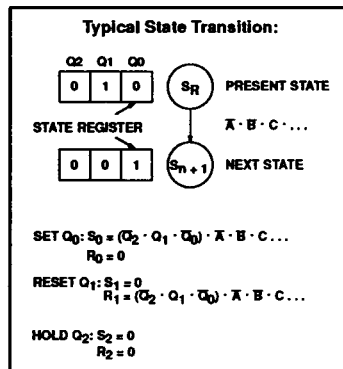
ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V <sub>CC</sub>	Supply voltage		+7	V <sub>DC</sub>
V <sub>IN</sub>	Input voltage		+5.5	V <sub>DC</sub>
V <sub>OUT</sub>	Output voltage		+5.5	V <sub>DC</sub>
I <sub>IN</sub>	Input currents	-30	+30	mA
I <sub>OUT</sub>	Output currents		+100	mA
T <sub>amb</sub>	Operating temperature range	0	+75	°C
T <sub>stg</sub>	Storage temperature range	-65	+150	°C

## NOTES:

- Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

## LOGIC FUNCTION



## VIRGIN STATE

The factory shipped virgin device contains all fusible links intact, such that:

- PR/OE option is set to PR. Thus, all outputs will be at "1", as preset by initial power-up procedure.
- All transition terms are disabled (0).
- All S/R flip-flop inputs are disabled (0).
- The device can be clocked via a Test Array pre-programmed with a standard test pattern.

NOTE: The Test Array pattern MUST be deleted before incorporating a user program. This is accomplished automatically by any Philips Semiconductors qualified programming equipment.

## THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

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### DC ELECTRICAL CHARACTERISTICS

 $0^{\circ}\text{C} \leq T_{\text{amb}} \leq +75^{\circ}\text{C}$ ,  $4.75\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$ 

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN	TYP <sup>1</sup>	MAX	
<b>Input voltage<sup>2</sup></b>						
$V_{\text{IH}}$	High	$V_{\text{CC}} = \text{MAX}$	2.0			V
$V_{\text{IL}}$	Low	$V_{\text{CC}} = \text{MIN}$			0.8	V
$V_{\text{IC}}$	Clamp <sup>3</sup>	$V_{\text{CC}} = \text{MIN}$ , $I_{\text{IN}} = -12\text{mA}$		-0.8	-1.2	V
<b>Output voltage<sup>2</sup></b>						
$V_{\text{OH}}$	High <sup>4</sup>	$V_{\text{CC}} = \text{MIN}$	2.4			V
$V_{\text{OL}}$	Low <sup>5</sup>	$I_{\text{OH}} = -2\text{mA}$ $I_{\text{OL}} = 9.6\text{mA}$		0.35	0.45	V
<b>Input current</b>						
$I_{\text{IH}}$	High	$V_{\text{IN}} = 5.5\text{V}$		<1	80	$\mu\text{A}$
$I_{\text{IL}}$	Low	$V_{\text{IN}} = 0.45\text{V}$		-10	-100	$\mu\text{A}$
$I_{\text{IL}}$	Low (CK input)	$V_{\text{IN}} = 0.45\text{V}$		-50	-250	$\mu\text{A}$
<b>Output current</b>						
$I_{\text{O(OFF)}}$	Hi-Z state <sup>5, 6</sup>	$V_{\text{CC}} = \text{MAX}$ $V_{\text{OUT}} = 5.5\text{V}$		1	40	$\mu\text{A}$
$I_{\text{OS}}$	Short circuit <sup>9, 7</sup>	$V_{\text{OUT}} = 0.45\text{V}$ $V_{\text{OUT}} = 0\text{V}$	-15	-1	-40	$\mu\text{A}$
$I_{\text{CC}}$	$V_{\text{CC}}$ supply current <sup>8</sup>	$V_{\text{CC}} = \text{MAX}$		120	180	mA
<b>Capacitance<sup>5</sup></b>						
$C_{\text{IN}}$	Input	$V_{\text{CC}} = 5.0\text{V}$ $V_{\text{IN}} = 2.0\text{V}$		8		pF
$C_{\text{OUT}}$	Output	$V_{\text{OUT}} = 2.0\text{V}$		10		pF

**NOTES:**

- All typical values are at  $V_{\text{CC}} = 5\text{V}$ ,  $T_{\text{amb}} = +25^{\circ}\text{C}$ .
- All voltage values are with respect to network ground terminal.
- Test one at a time.
- Measured with  $V_{\text{IL}}$  applied to  $\overline{\text{OE}}$  and a logic high stored, or with  $V_{\text{IH}}$  applied to PR.
- Measured with a programmed logic condition for which the output is at a low logic level, and  $V_{\text{IL}}$  applied to PR/ $\overline{\text{OE}}$ . Output sink current is supplied through a resistor to  $V_{\text{CC}}$ .
- Measured with  $V_{\text{IH}}$  applied to PR/ $\overline{\text{OE}}$ .
- Duration of short circuit should not exceed 1 second.
- $I_{\text{CC}}$  is measured with the PR/ $\overline{\text{OE}}$  input grounded, all other inputs at 4.5V and the outputs open.

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## AC ELECTRICAL CHARACTERISTICS

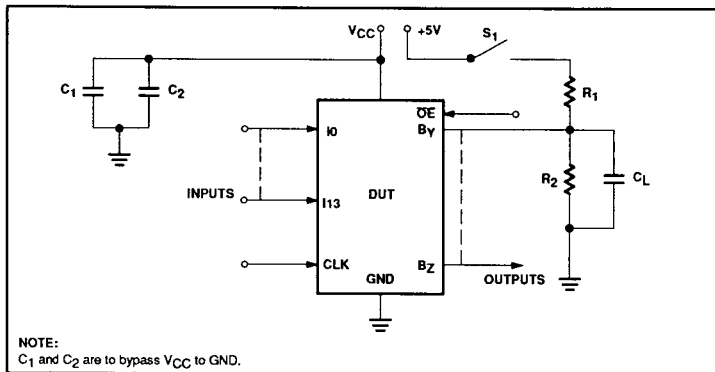
$R_1 = 470\Omega$ ,  $R_2 = 1k\Omega$ ,  $C_L = 30pF$ ,  $0^\circ C \leq T_{amb} \leq +75^\circ C$ ,  $4.75^\circ C \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	FROM	TO	LIMITS						UNIT
				PLS167			PLS167A			
				MIN	TYP <sup>1</sup>	MAX	MIN	TYP <sup>1</sup>	MAX	
<b>Pulse width<sup>3</sup></b>										
$t_{CKH}$	Clock <sup>2</sup> High	CK +	CK -	25	15		20	15		ns
$t_{CKL}$	Clock Low	CK -	CK +	25	15		20	15		ns
$t_{CKP}$	Clock Period	CK +	CK +	50	30		40	30		ns
$t_{PRH}$	Preset pulse	PR +	PR -	25	15		25	15		ns
<b>Setup time<sup>3</sup></b>										
$t_{S1A}$	Input	Input ±	CK +	60			40			ns
$t_{S1B}$	Input	Input ±	CK +	50			30			ns
$t_{S1C}$	Input	Input ±	CK +	42			N/A			ns
$t_{S2A}$	Input (through Complement Array)	Input ±	CK +	90			70			ns
$t_{S2B}$	Input (through Complement Array)	Input	CK +	80			60			ns
$t_{S2C}$	Input (through Complement Array)	Input	CK +	72			N/A			ns
$t_{VS}$	Power-on preset	$V_{CC} +$	CK -	0	-10		0	-10		ns
$t_{PRS}$	Preset	PR -	CK -	0	-10		0	-10		ns
<b>Hold time</b>										
$t_{IH}$	Input	CK +	Input ±	5	-10		5	-5		ns
<b>Propagation delay</b>										
$t_{CKO}$	Clock	CK +	Output ±		15	30		15	20	ns
$t_{OE}$	Output enable <sup>4</sup>	OE -	Output -		20	30		20	30	ns
$t_{OD}$	Output disable <sup>4</sup>	OE +	Output +		20	30		20	30	ns
$t_{PR}$	Preset	PR +	Output +		18	30		18	30	ns
$t_{PPR}$	Power-on preset	$V_{CC} +$	Output +		0	10		0	10	ns
<b>Frequency of operation<sup>3</sup></b>										
$f_{MAXC}$	Without Complement Array			13.9			20.0			MHz
$f_{MAXC}$	With Complement Array			9.8			12.5			MHz

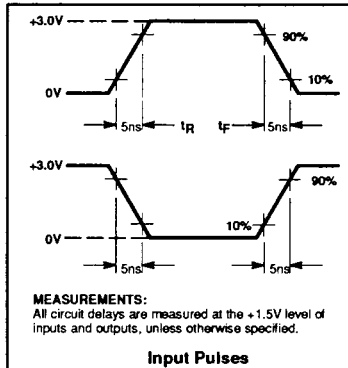
**NOTES:**

1. All typical values are at  $V_{CC} = 5V$ ,  $T_{amb} = +25^\circ C$ .
2. To prevent spurious clocking, clock rise time (10% - 90%)  $\leq 30ns$ .
3. See "Speed vs. OR Loading" diagrams.
4. For 3-State output; output enable times are tested with  $C_L = 30pF$  to the 1.5V level, and  $S_1$  is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with  $C_L = 5pF$ . High-to-High impedance tests are made to an output voltage of  $V_T = (V_{OH} - 0.5V)$  with  $S_1$  open, and Low-to-High impedance tests are made to the  $V_T = (V_{OL} + 0.5V)$  level with  $S_1$  closed.

**TEST LOAD CIRCUIT**



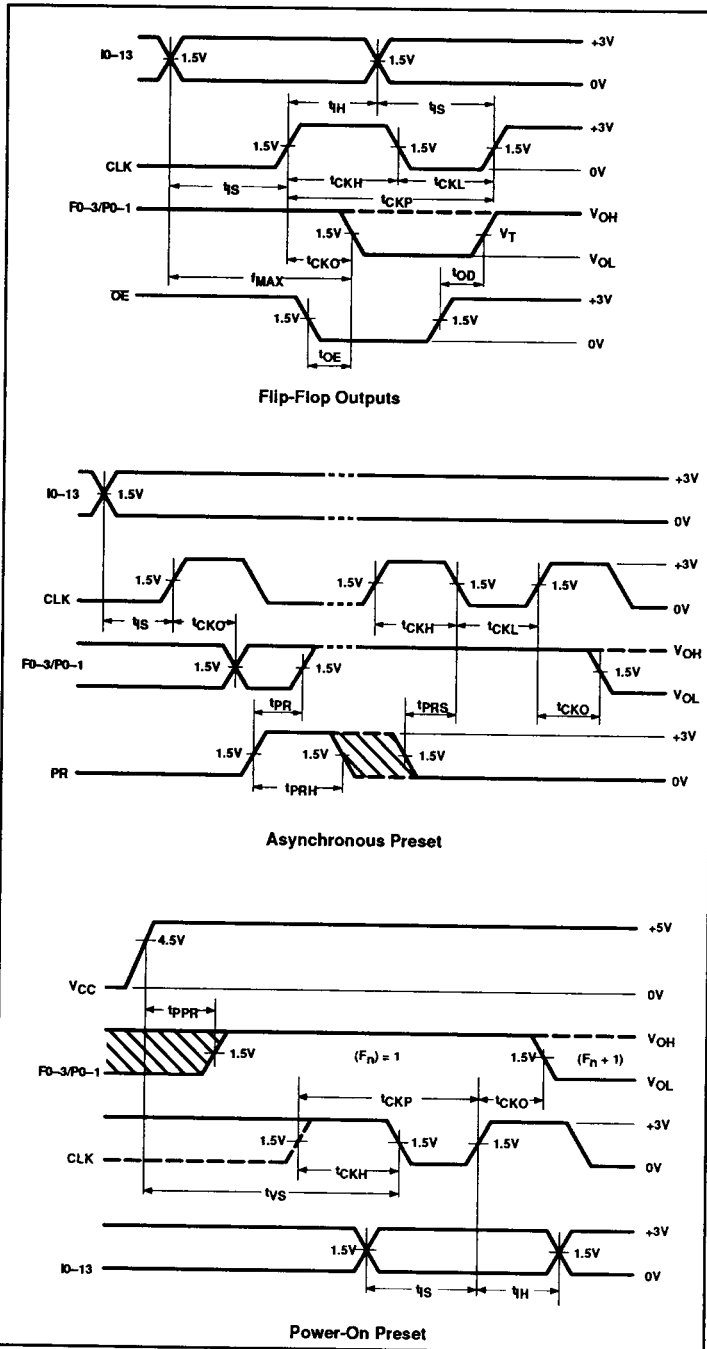
**VOLTAGE WAVEFORMS**



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## TIMING DIAGRAMS



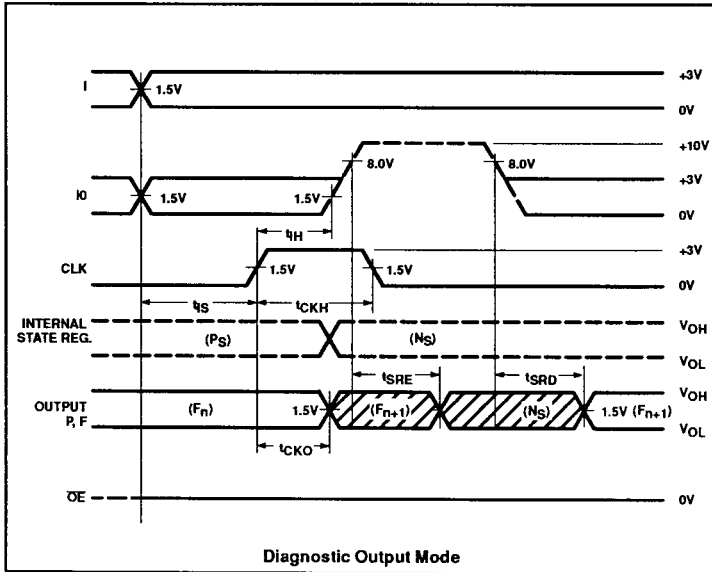
## TIMING DEFINITIONS

SYMBOL	PARAMETER
$t_{CKH}$	Width of input clock pulse.
$t_{CKL}$	Interval between clock pulses.
$t_{CKP}$	Minimum guaranteed clock period.
$t_{IS1}$	Required delay between beginning of valid input and positive transition of clock.
$t_{IS2}$	Required delay between beginning of valid input and positive transition of clock, when using optional Complement Array (two passes necessary through the AND array).
$t_{VS}$	Required delay between $V_{CC}$ (after power-on) and negative transition of clock preceding first reliable clock pulse.
$t_{PRS}$	Required delay between negative transition of asynchronous Preset and negative transition of clock preceding first reliable clock pulse.
$t_{IH}$	Required delay between positive transition of clock and end of valid input data.
$t_{CKO}$	Delay between positive transition of clock and when outputs become valid (with PR/OE Low).
$t_{OE}$	Delay between beginning of Output Enable Low and when outputs become valid.
$t_{OD}$	Delay between beginning of Output Enable High and when outputs are in the OFF-State.
$t_{SRE}$	Delay between input $I_0$ transition to Diagnostic mode and when the outputs reflect the contents of the State Register.
$t_{SRD}$	Delay between input $I_0$ transition to Logic mode and when the outputs reflect the contents of the Output Register.
$t_{PR}$	Delay between positive transition of Preset and when outputs become valid at "1".
$t_{PPR}$	Delay between $V_{CC}$ (after power-on) and when outputs become preset at "1".
$t_{PRH}$	Width of preset input pulse.
$f_{MAX}$	Minimum guaranteed operating frequency.

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## TIMING DIAGRAMS (Continued)



## SPEED VS. "OR" LOADING

The maximum frequency at which the PLS can be clocked while operating in *sequential mode* is given by:

$$(1/f_{MAX}) = t_{CY} = t_{IS} + t_{CKO}$$

This frequency depends on the number of transition terms  $T_n$  used. Having all 48 terms connected in the AND array does not appreciably impact performance; but the number of terms connected to each OR line affects  $t_{IS}$ , due to capacitive loading. The effect of this loading can be seen in Figure 1, showing the variation of  $t_{IS1}$  with the number of terms connected per OR.

The PLS167 AC electrical characteristics contain three limits for the parameters  $t_{IS1}$  and  $t_{IS2}$  (refer to Figure 1). The first,  $t_{IS1A}$  is guaranteed for a device with 48 terms connected to any OR line.  $t_{IS1B}$  is guaranteed for a device with 32 terms connected to any OR line. And  $t_{IS1C}$  is guaranteed for a device with 24 terms connected to any OR line.

The three other entries in the AC table,  $t_{IS2}$  A, B, and C are corresponding 48, 32, and 24 term limits when using the on-chip Complement Array.

The PLS167A AC electrical characteristics contain two limits for the parameters  $t_{IS1}$  and  $t_{IS2}$  (refer to Figure 2). The first,  $t_{IS1A}$  is guaranteed for a device with 24 terms connected to any OR line.  $t_{IS1B}$  is guaranteed for a device with 16 terms connected to any OR line.

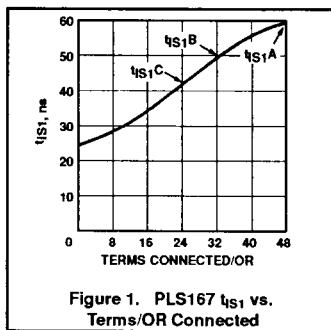


Figure 1. PLS167  $t_{IS1}$  vs. Terms/OR Connected

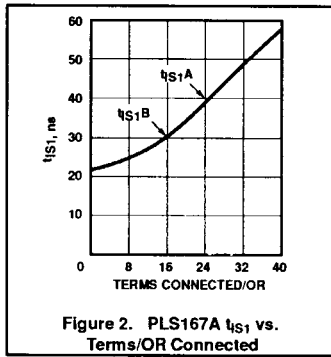


Figure 2. PLS167A  $t_{IS1}$  vs. Terms/OR Connected

The two other entries in the AC table,  $t_{IS2}$  A and B are corresponding 24 and 16 term limits when using the on-chip Complement Array.

The worst case of  $t_{IS}$  for a given application can be determined by identifying the OR line with the maximum number of  $T_n$  connections. This can be done by referring to the interconnect pattern in the PLS logic diagram, typically illustrated in Figure 3, or by counting the maximum number of "H" or "L" entries in one of the columns of the device Program Table.

This number plotted on the curve in Figure 1 or Figure 2 will yield the worst case  $t_{IS}$  and, by implication, the maximum clocking frequency for reliable operation.

Note that for maximum speed all UNUSED transition terms should be disconnected from the OR array.

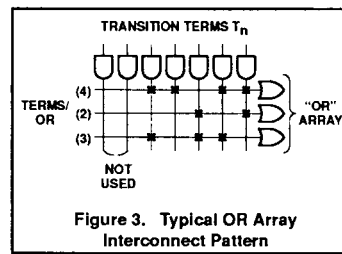


Figure 3. Typical OR Array Interconnect Pattern



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## LOGIC PROGRAMMING

The PLS167/A devices are fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Philips Semiconductors' SNAP design software package, ABEL™ CUPL™ and PALASM® 90 design software packages also support the PLS167/A architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

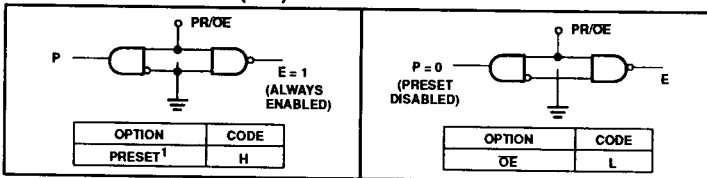
PLS167/A logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Philips Semiconductors SNAP PLD design software package.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

## PROGRAMMING AND SOFTWARE SUPPORT

Refer to Section 9 (*Development Software*) and Section 10 (*Third-party Programmer/Software Support*) of this data handbook for additional information.

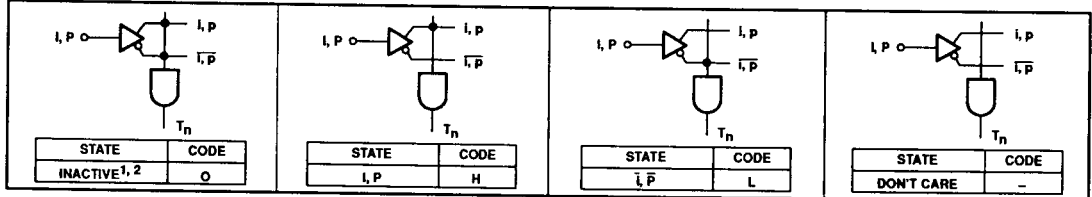
### PRESET/OE OPTION – (P/E)



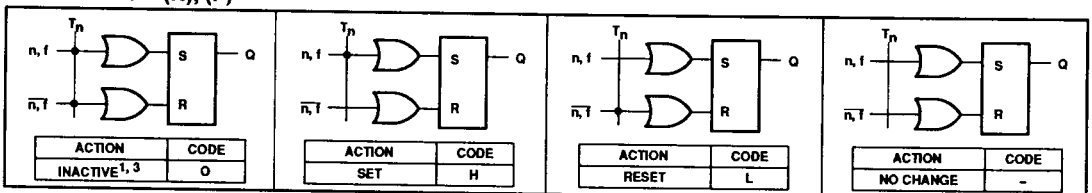
#### PROGRAMMING:

The PLS167/A has a power-up preset feature. This feature insures that the device will power-up in a known state with all register elements (State and Output Register) at logic High (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.

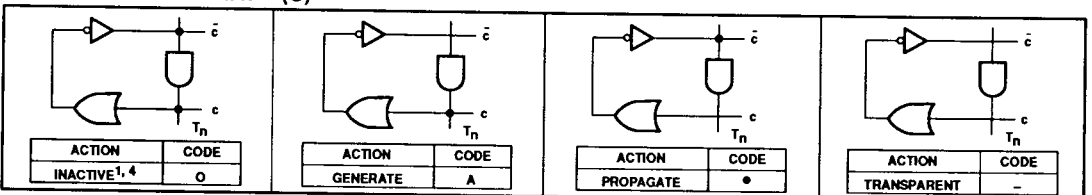
### “AND” ARRAY – (I), (P)



### “OR” ARRAY – (N), (F)



### “COMPLEMENT” ARRAY – (C)



#### NOTES:

1. This is the initial unprogrammed state of all links.
2. Any gate  $T_n$  will be unconditionally inhibited if both the true and complement of any input (I, P) are left intact.
3. To prevent simultaneous Set and Reset flip-flop commands, this state is not allowed for N and F link pairs coupled to active gates  $T_n$  (see flip-flop truth tables).
4. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates  $T_n$ .

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## PROGRAM TABLE

### PROGRAM TABLE ENTRIES

CUSTOMER NAME _____ PURCHASE ORDER # _____ PHILIPS DEVICE # _____ CF (XXXX) CUSTOMER SYMBOLIZED PART # _____ TOTAL NUMBER OF PARTS _____ PROGRAM TABLE _____ REV _____ DATE _____										<b>AND</b> INACTIVE : 0 GENERATE : A PROPAGATE : • TRANSPARENT : — <hr/> INACTIVE : 0 I, P : H I, P̄ : L DON'T CARE : —					<b>OR</b> INACTIVE : 0 SET : H RESET : L NO CHANGE : — <hr/> <b>OPTION</b> PRESET : H OE : L																																			
<b>AND</b>										<b>OPTION (P/E)</b>																																								
TERM	C <sub>n</sub>	INPUT (I <sub>m</sub> )														PRESENT STATE (P <sub>s</sub> )														REMARKS	NEXT STATE (N <sub>e</sub> )														OUTPUT (Fr)					
		13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0	3	2	1	0														
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PIN NO.		17	18	19	20	21	22	23	2	3	4	5	6	7	8																		15	14	13	11	10	9												
VARIABLE NAME																																																		

**NOTES:**

1. The device is shipped with all links initially intact. Thus, a background of "0" for all Terms, and an "H" for the P/E option, exists in the table, shown BLANK instead for clarity.
2. Unused C<sub>n</sub>, I<sub>m</sub>, and P<sub>s</sub> bits are normally programmed Don't Care (-).
3. Unused Transition Terms can be left blank for future code modification, or programmed as (-) for maximum speed.
4. Letters in variable fields are used as identifiers by logic type programmers.

# Programmable logic sequencers (14 × 48 × 6)

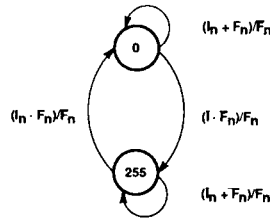
PLS167/A

## TEST ARRAY

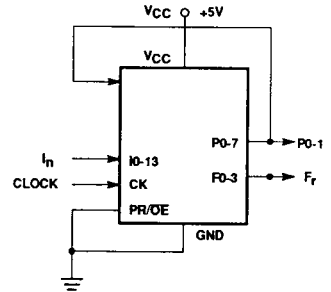
The PLS may be subjected to AC and DC parametric tests prior to programming via an on-chip test array.

The array consists of test transition terms 48 and 49, factory programmed as shown below.

Testing is accomplished by clocking the PLS and applying the proper input sequence to  $I_{0-13}$  as shown in the test circuit timing diagram.



State Diagram



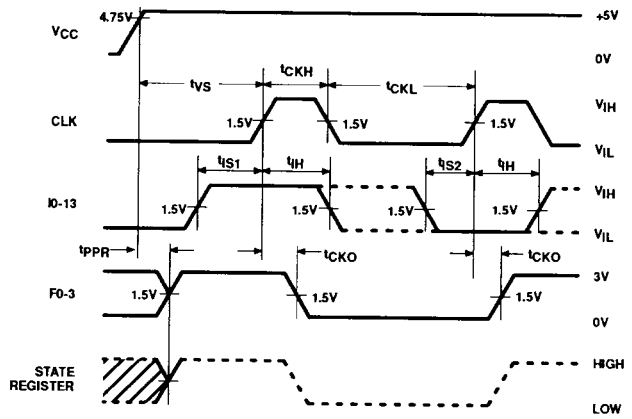
PLS Under Test

T E R M	C	AND																		
		INPUT (I <sub>m</sub> )																		
48	A	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
49	.	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L

OPTION (P/E)																		H	
OR																			
NEXT STATE (N <sub>e</sub> )									OUTPUT (F <sub>r</sub> )										
7	6	5	4	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

Test Array Program

Both terms 48 and 49 must be deleted during user programming to avoid interfering with the desired logic function. This is accomplished automatically by any Signetic's qualified programming equipment.



Test Circuit Timing Diagram

T E R M	C	AND																		
		INPUT (I <sub>m</sub> )																		
48	-	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
49	.	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L

OPTION (P/E)																		H	
OR																			
NEXT STATE (N <sub>e</sub> )									OUTPUT (F <sub>r</sub> )										
7	6	5	4	3	2	1	0	5	4	3	2	1	0	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Test Array Deleted

Programmable logic sequencers  
(14 × 48 × 6)

PLS167/A

SNAP RESOURCE SUMMARY DESIGNATIONS

