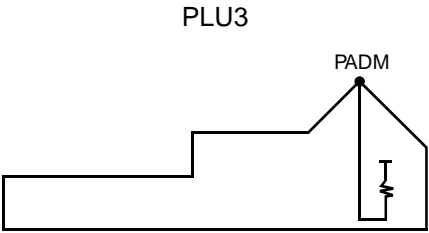


AMI5HG 0.5 micron CMOS Gate Array

Description

PLU3 is an active pull-up buffer piece.

Logic Symbol	Truth Table	Pin Loading
 <p>The logic symbol for PLU3 is a buffer with a pull-up resistor. The output of the buffer is connected to a node labeled PADM, which is also connected to a pull-up resistor. The resistor is represented by a vertical line with a horizontal bar at the bottom, connected to a ground symbol.</p>	<p>N/A</p>	<p>N/A</p>

HDL Syntax

Verilog PLU3 *inst_name* (PADM);

VHDL *inst_name*: PLU3 port map (PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} ($T_J = 85^\circ\text{C}$)	TBD	nA
EQL_{pd}	149.7	Eq-load

See page 2-15 for power equation.

Delay will vary with input conditions. See page 2-17 for interconnect estimates.