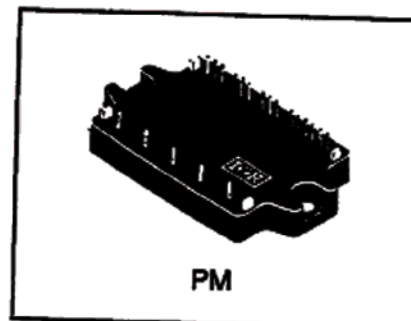


IGBT INTELLIGENT MODULE
Features

- 3 phase IGBT bridge with drive and protection circuit.
- 2kW output power at 300VDC, 8kHz, $T_C = 85^\circ\text{C}$
- "UltraFast"™ IGBT and "HEXFRED"™ Ultrafast, Soft Recovery Diodes.
- Over current short circuit, earth fault, under voltage and over temperature protection.
- Fault feedback.
- Carrier frequencies up to 25kHz


Description

The PM15CMA060 is a 3 phase intelligent IGBT bridge with gate drive and protection circuit. It contains IR "UltraFast"™ series IGBTs and "HEXFRED"™ Ultrafast, soft recovery diodes, rendering it suitable for 5 to 25 kHz switching frequencies. Built-in driver and protection circuit makes it the ideal building block for AC Motor Speed Controllers, Brushless Servo Drives, UPS and other inverter systems.

Absolute Maximum Ratings:
Power Circuit

	Parameter	Max.	Units
$I_C @ T_C = 25^\circ\text{C}$	Continuous Collector Current, each IGBT, one IGBT in conduction	15	A
$I_C @ T_C = 85^\circ\text{C}$	Continuous Collector Current, each IGBT, one IGBT in conduction	7.0	
V_{CE}	Continuous Collector-to-Emitter Voltage	600	V
V_{CC}	Supply Voltage Between P-N	450	
$P_D @ T_C = 85^\circ\text{C}$	Power Dissipation, One IGBT in Conduction	22	W
T_J	Operating Junction Temperature Range	-20 to 150	

Driver and Protection Circuit

	Parameter	Max.	Units
V_D	Driver Supply Voltage	20	V
V_{IN}	Logic Input Voltage Between Input Pin and GND	-0.30 to 5.3	
V_{FO}	Open Collector Fault Output Voltage	-0.3 to $V_D+0.3$	
I_{DA}	Average Input Supply Current	15	mA
I_{FO}	Fault Output Current	20	

Total System

	Parameter	Max.	Units
$V_{CC} \text{ (PROTECTED)}$	Supply Voltage Protected Against OC and SC Faults①	400	V
V_{ISOL}	RMS Isolation Voltage, Any Terminal to Case, 1 Minute	2500	
T_C	Case Operating Temperature Range	-20 to 100	$^\circ\text{C}$
T_{STG}	Storage Temperature	-40 to 125	
	Mounting Torque	2.0	Nm

Revision 4

PM15CMA060

IGOR

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified):

Power Circuit

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{CE(on)}$	Collector to Emitter Saturation Voltage	—	2.7	—	V	$V_{GE} = 15\text{V}$, $I_C = 8\text{A}$, $T_J = 150^\circ\text{C}$
V_{FM}	Diode Forward Voltage	—	—	1.6	V	$I_C = 8\text{A}$, $T_J = 150^\circ\text{C}$
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	μA	$V_{CE} = 600\text{V}$, $V_{GE} = 0\text{V}$

Driver and Protection Circuit

	Parameter	Min.	Typ.	Max.	Units	Conditions
V_D	Supply Voltage	13.5	15	16.5	V	
V_{DUV+}	Under Voltage Set Level	—	—	9.5	V	
V_{DUR-}	Under Voltage Reset Level	8.2	—	—	V	
V_{IH}	Logic "0" Input Voltage (OUT=LO)	2.2	—	—	V	
V_{IL}	Logic "1" Input Voltage (OUT=HI)	—	—	0.8	V	
I_{DA}	Average Supply Current	—	11	15	mA	
I_{DP}	Peak Supply Current	—	—	600	mA	20 μs Initial Bootstrap Charging
I_{IN+}	Logic "1" Input Bias Current (OUT=HI)	—	—	900	μA	
I_{IN-}	Logic "0" Input Bias Current (OUT=LO)	—	—	500	μA	
f_C	PWM Carrier Frequency	—	—	25	kHz	
t_{DT}	Dead Time	—	2.5	—	μs	
$t_{FLT(IN)}$	Input Filter Time (All Six Inputs)	—	310	—	ns	$V_{IN} = 0\text{V}$ & 5V
R_{IN}	Logic Input Pull-up Resistor	—	50	—	k Ω	
I_{SC}	Short Circuit Current Trip Level	—	40	—	A	
I_{OC}	Over Current Trip Level	16	19	—	A	
t_{OC}	Over Current Delay Time	—	20	—	μs	
I_{EF}	Earth Fault Current Trip Level	—	32	—	A	
t_{EF}	Earth Fault Delay Time	—	2.0	—	μs	
T_{OT}	Over Temperature Trip Level, at Case	—	100	—	$^\circ\text{C}$	
t_{DET}	Fault Detect. to Power Stage Shut Down Delay	—	2.0	—	μs	
t_{D1}	Internal Shut Down to Fault Output "low" Delay	—	1.5	—	μs	
$t_{FLT(OUT)}$	Fault Output Pulse Width	—	2.0	—	ms	
$t_{FLT(CLR)}$	Fault Clear Time, LIN U,V,W, Kept High	—	10	—	μs	
t_{D2}	Fault Clear Recognition to Fault Reset Delay	—	3.0	—	μs	
$I_{F(OUT)}$	Open Collector Fault Current	—	—	20	mA	
C_{ISO}	Capacitance between Pin & Module Case	—	150	—	pF	

Thermal Resistance:

	Parameter	Typ.	Max.	Units
R_{JC} (IGBT)	Junction-to-Case, each IGBT, one IGBT in conduction	—	2.9	$^\circ\text{C/W}$
R_{JC} (DIODE)	Junction-to-Case, each diode, one diode in conduction	—	4.3	$^\circ\text{C/W}$
R_{CS} (MODULE)	Case-to-Sink, flat, greased surface	0.05	—	$^\circ\text{C/W}$
Wt	Weight of Module	80	—	g

Notes:

① $V_D = 13.5$ to 16.5V , $T_J = 125^\circ\text{C}$ at Start

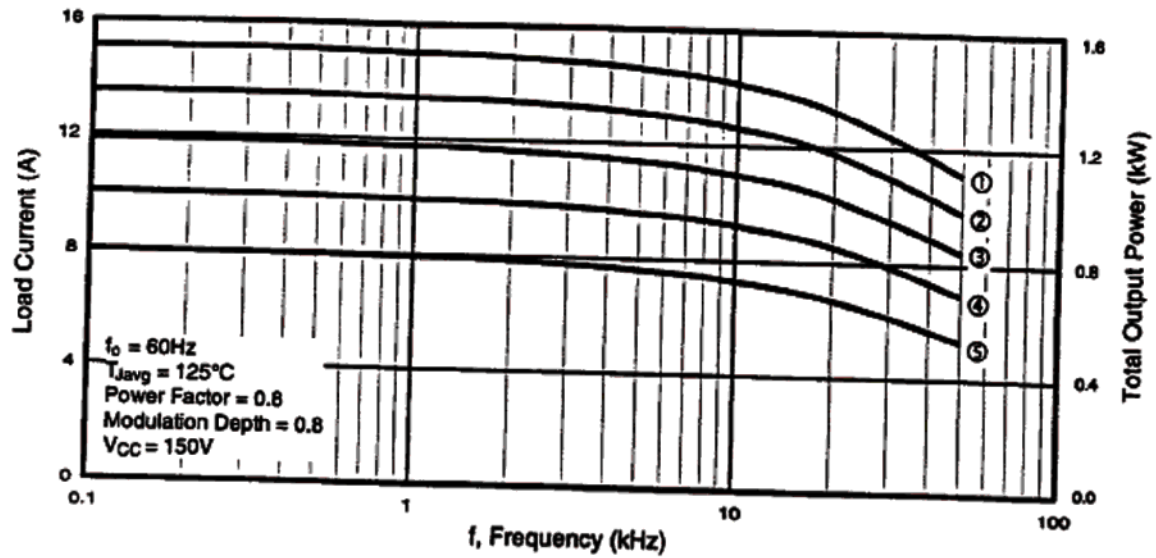


Fig. 1 - Typical Output Power and Current vs. Switching Frequency, at 150VDC

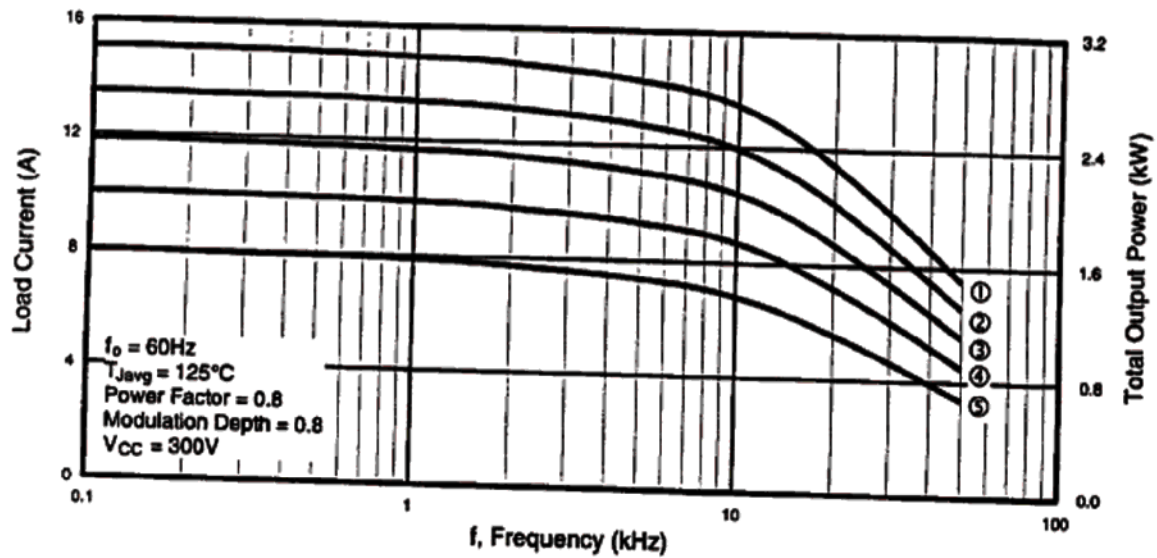


Fig. 2 - Typical Output Power and Current vs. Switching Frequency, at 300VDC

Curve	1	2	3	4	5
$T_{\text{SINK}}, ^\circ\text{C}$	60	70	80	90	100
P_D Total, W	140	118	96	75	53

Table Common for Figure 1 and Figure 2

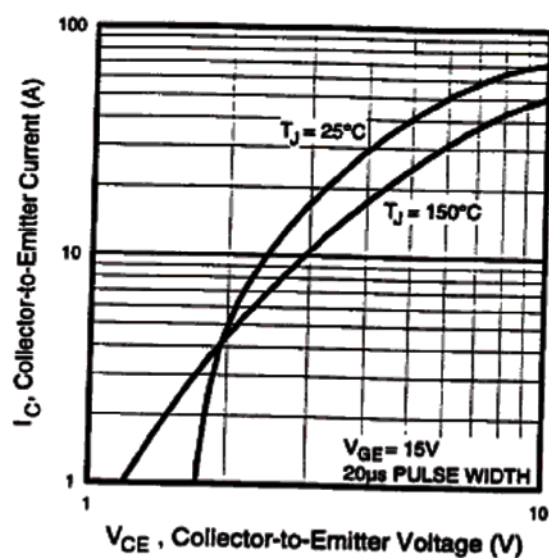


Fig. 3 - Typical Output Characteristics

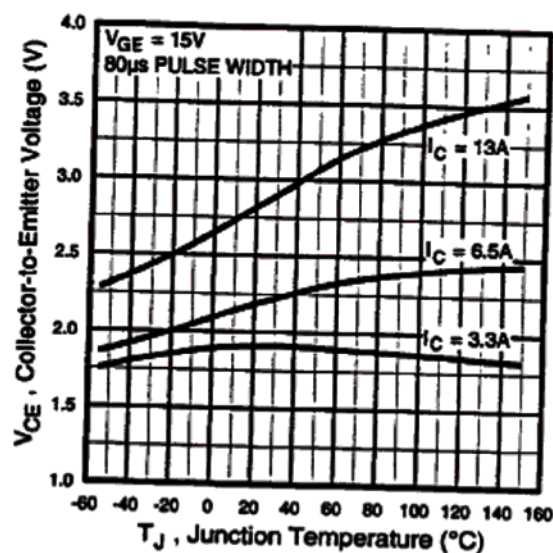


Fig. 4 - Collector-to-Emitter Voltage vs. Junction Temperature

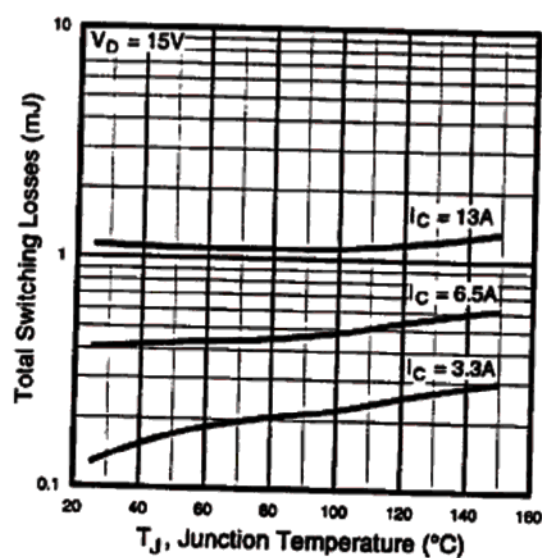


Fig. 5 - Typical Switching Losses vs. Junction Temperature

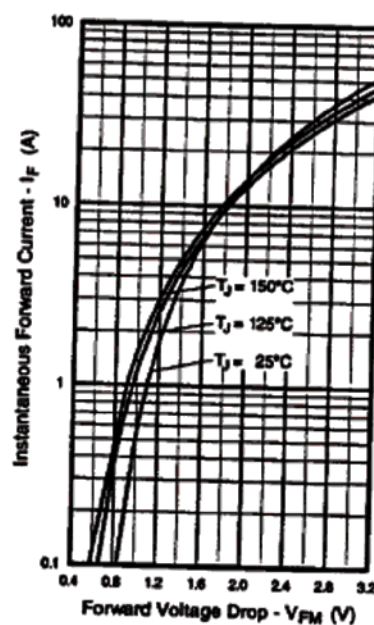


Fig. 6 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

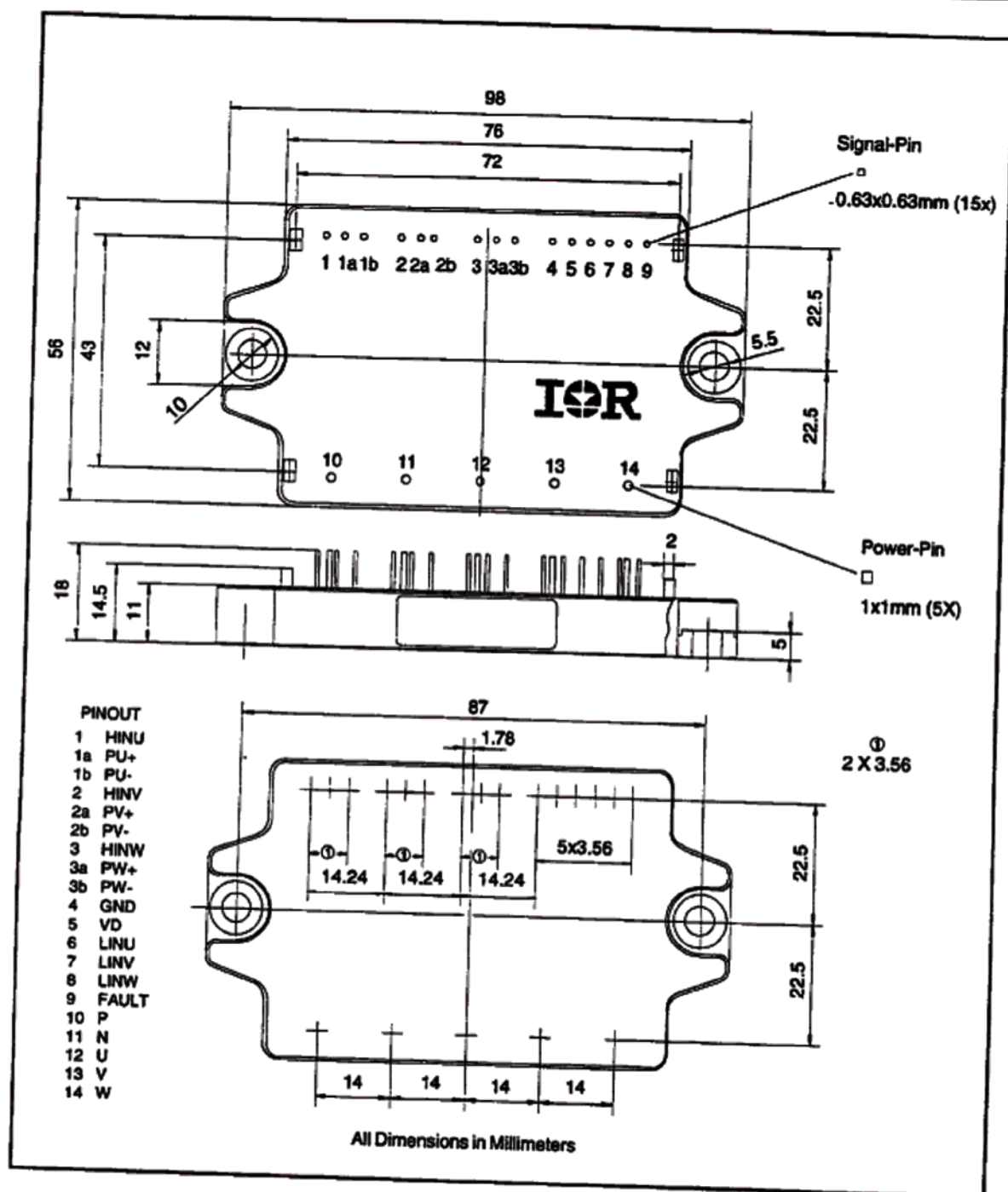


Fig. 7 - Package Outline

Application Information

Input Control Logic

Output of power stage is out of phase with input signal. Internal 50 k Ω pull-up resistor to V_D from all 6 inputs ensure that all transistors are off if the inputs are open circuited. A 300 ns filter at input prevents spurious triggering due to noise. Input logic provides deadtime when nearly coincident transitions take place at LIN and HIN pins of same channel and prevents shoot-through conditions. When driving the module inputs with open collector, external pull up resistor to V_D should be higher than 1 k Ω .

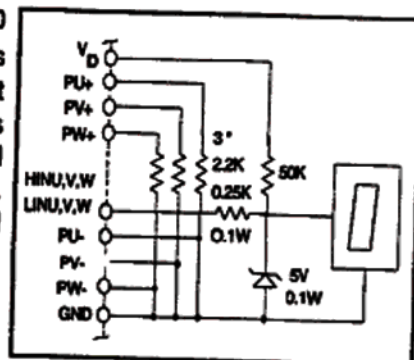


Figure 8: Input Stage

Bootstrap

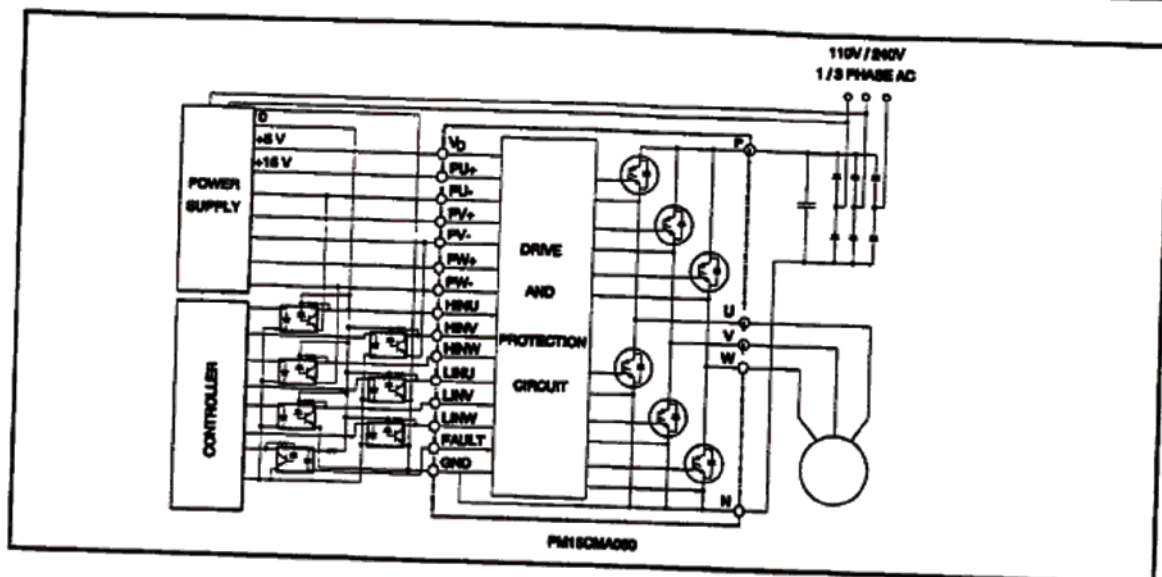
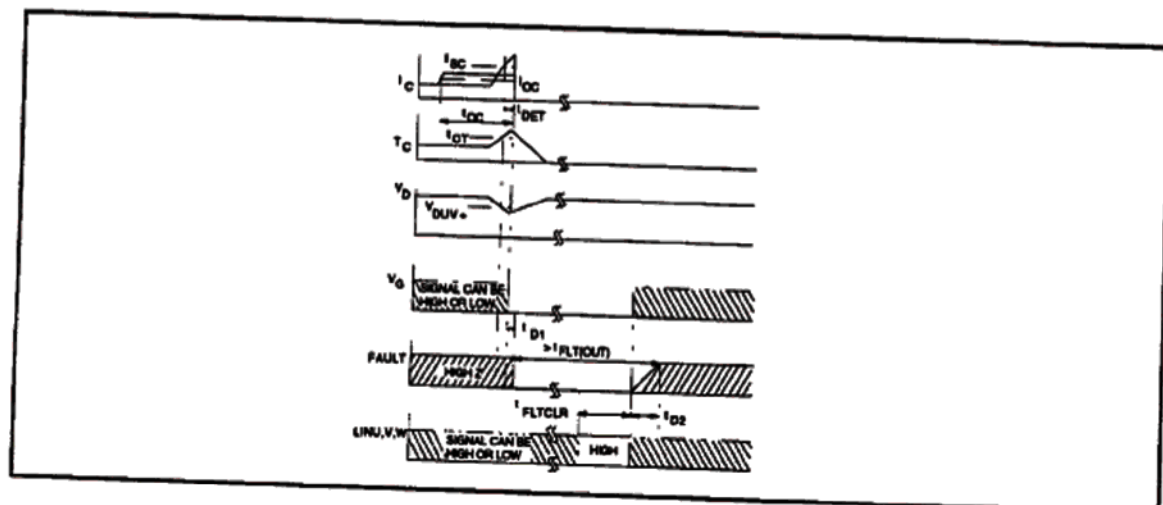
The floating power supplies - PU, PV and PW are connected to resistive loads and the drive is generated through bootstrap technique. Each high side device has 2.2 μ F bootstrap capacitor, fed through individual bootstrap diode and common 22 Ω charging resistor to V_D . At start-up or after an interruption in switching greater than 2 s, it is necessary to switch on all three low side transistors for at least 200 μ s before switching the high side transistors. Maximum on time for high side transistors is 200 ms.

Temperature Monitoring

Temperature is sensed in close proximity of the junction, minimizing errors caused by the module base plate thermal capacitance. Thermal protection is effective for symmetrical three phase loads.

Fault Logic

Short circuit, earth fault, over current, over temperature and V_D undervoltage conditions cause trips and are latched. Open collector FAULT output goes low for at least 2 ms when fault latch is set. It can be reset by holding all three LIN high for 12 μ s or cycling V_D through undervoltage condition. Bootstrap supply of high side switches is individually monitored for undervoltage and has cycle by cycle shutdown for the particular switch and is not latched. Active low open collector FAULT pin can be connected to logic circuit, fault indicator LED or optocoupler for feedback to controller.


Fig. 9 - Typical Application Scheme

Fig. 10 - Timing Diagram

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Data and specifications subject to change without notice.