Pm25LV080B / 016B

8 Mbit / 16 Mbit Single Operation Voltage Serial Flash Memory With 100 MHz SPI Bus Interface

FEATURES

• Single Power Supply Operation
- Low voltage range: 2.7 V - 3.6 V

• Memory Organization
- Pm25LV080B: 1M x 8 (8 Mbit)
- Pm25LV016B: 2M x 8 (16 Mbit)

• Cost Effective Sector/Block Architecture
- 8Mb : Uniform 4Kbyte sectors / Sixteen uniform 64Kbyte blocks
- 16Mb : Uniform 4Kbyte sectors / Thirty-two uniform 64Kbyte blocks
- Bottom sector is configurable as one 4Kbyte sector or four 1Kbyte sectors

• Serial Peripheral Interface (SPI) Compatible
- Supports SPI Modes 0 (0,0) and 3 (1,1)
- Maximum 33 MHz clock rate for normal read
- Maximum 100 MHz clock rate for fast read

• Page Program (up to 256 Bytes) Operation
- Typical 2 ms per page program

• Sector, Block or Chip Erase Operation
- Typical 40 ms sector, block or chip erase

• Software Write Protection
- The Block Protect (BP2, BP1, BP0) bits allow partial or entire memory to be configured as read-only

• Hardware Write Protection
- Protect and unprotect the device from write operation by Write Protect (WP#) Pin

• Low Power Consumption
- Typical 10 mA active read current
- Typical 15 mA program/erase current

• High Product Endurance
- Guarantee 100,000 program/erase cycles per single sector
- Minimum 20 years data retention

• Industrial Standard Pin-out and Package
- 8-pin 208mil SOIC
- 8-contact WSON
- Optional lead-free (Pb-free) package

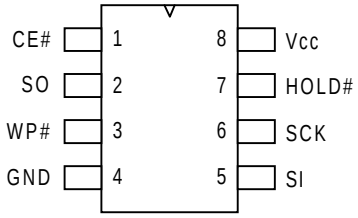
GENERAL DESCRIPTION

The Pm25LV080B/016B are 8 Mbit/16 Mbit 3.0 Volt-only Serial Peripheral Interface (SPI) Flash memories. The devices are designed to support 33 MHz fastest clock rate in the industry in normal read mode, 100 MHz in fast read mode and the bottom 4 Kbyte sector into four smaller 1 Kbyte sectors features. The devices use a single low voltage, ranging from 2.7 Volt to 3.6 Volt, power supply to perform read, erase and program operations. The devices can be programmed in standard EPROM programmers as well.

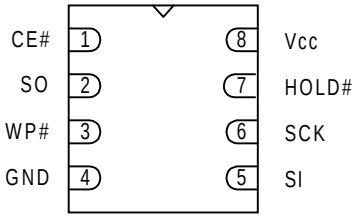
The Pm25LV080B/016B are accessed through a 4-wire SPI Interface consists of Serial Data Input (SI), Serial Data Output (SO), Serial Clock (SCK), and Chip Enable (CE#) pins. The devices support page program mode, 1 to 256 bytes data can be programmed into the memory in one program operation. These products are divided into uniform 4 Kbyte sectors or uniform 64 Kbyte blocks (sector group - consists of sixteen adjacent sectors). The devices have an innovative feature to configure the bottom 4 Kbyte sector into four smaller 1 Kbyte sectors for eliminating additional serial EEPROM needed for storing data. This is a further cost reduction for overall system.

The Pm25LV080B/016B are manufactured on pFLASH™'s advanced nonvolatile CMOS technology. The devices are offered in 8-pin SOIC 208mil and 8-contact WSON packages with operation frequency up to 100 MHz in fast read and 33 MHz in normal read mode.

CONNECTION DIAGRAMS



8-Pin SOIC

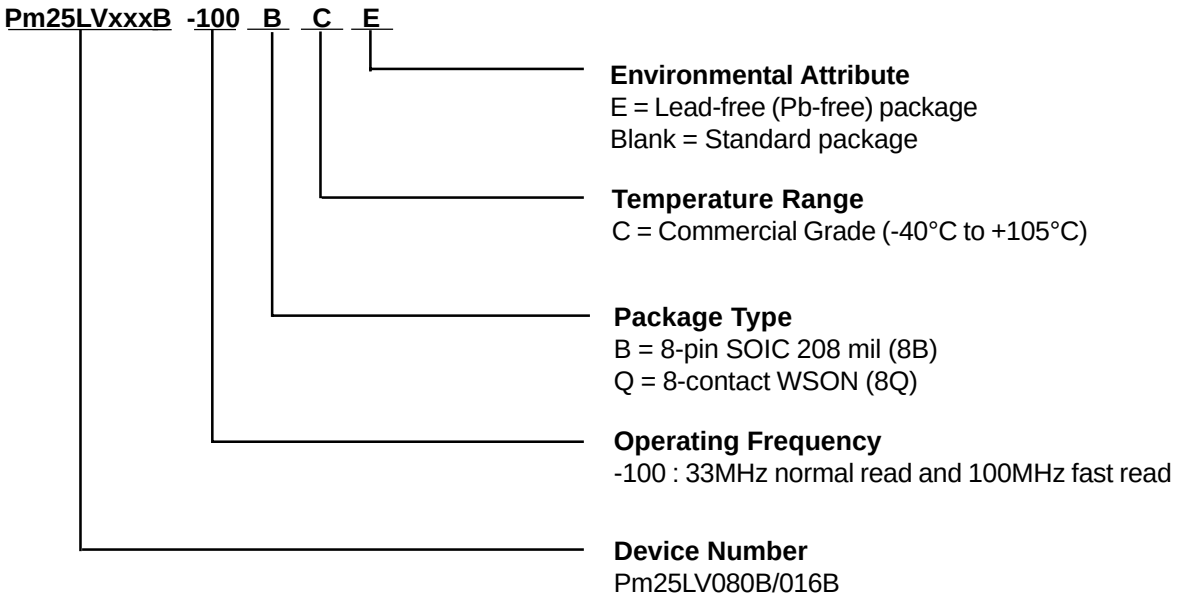


8-Contact WSON

PIN DESCRIPTIONS

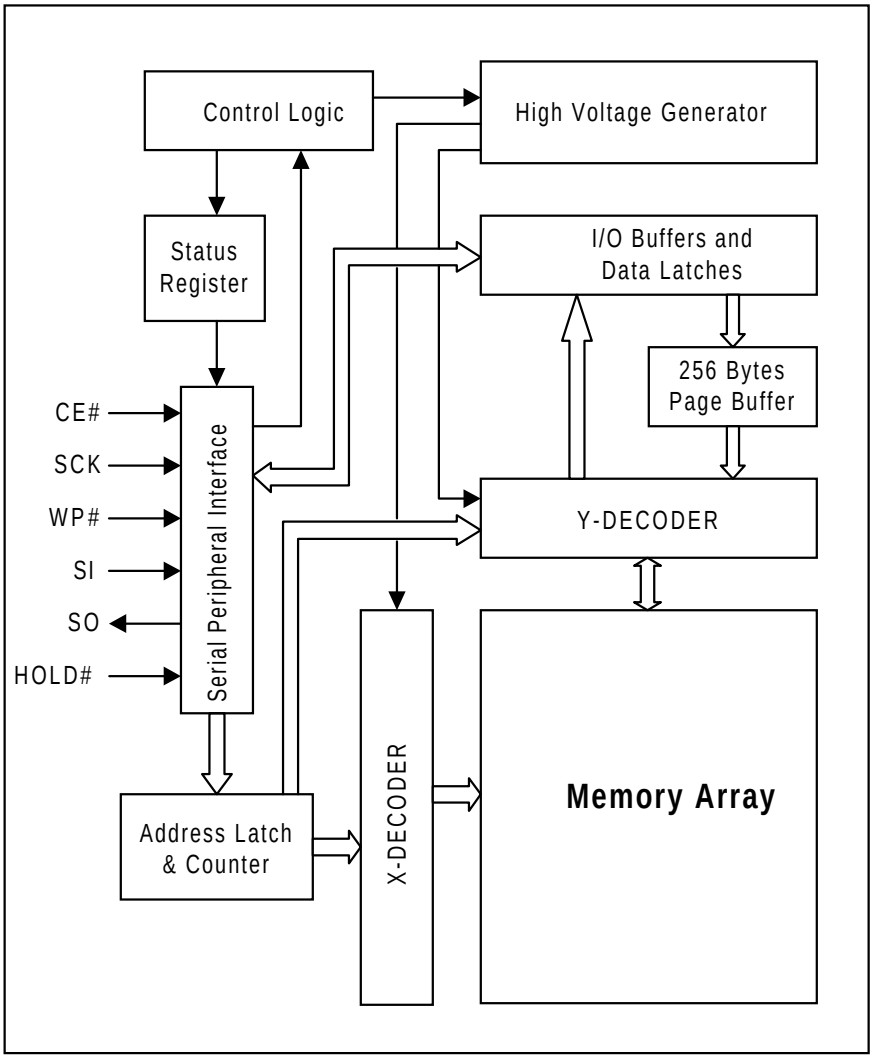
SYMBOL	TYPE	DESCRIPTION
CE#	INPUT	Chip Enable: CE# goes low activates the devices internal circuitries for device operation. CE# goes high deselects the devices and switches into standby mode to reduce the power consumption. When the devices are not selected, data will not be accepted via the serial input pin (SI), and the serial output pin (SO) will remain in a high impedance state.
SCK	INPUT	Serial Data Clock
SI	INPUT	Serial Data Input
SO	OUTPUT	Serial Data Output
GND		Ground
Vcc		Device Power Supply
WP#	INPUT	Write Protect: A hardware program/erase protection for all or partial of memory array. When the WP# pin is pulled to low, whole or partial of memory array is write protected depends on the setting of BP2, BP1 and BP0 bits in the Status Register. When the WP# is pulled high, the devices are not write protected.
HOLD#	INPUT	Hold: Pause serial communication with the master device without resetting the serial sequence.

PRODUCT ORDERING INFORMATION



Part Number	Operating Frequency (MHz)	Package	Temperature Range
Pm25LV080B-100BCE	100	8B 208mil SOIC	Commercial Grade (-40°C to +105°C)
Pm25LV016B-100BCE			
Pm25LV080B-100QCE	100	8Q WSON	
Pm25LV016B-100QCE			

BLOCK DIAGRAM



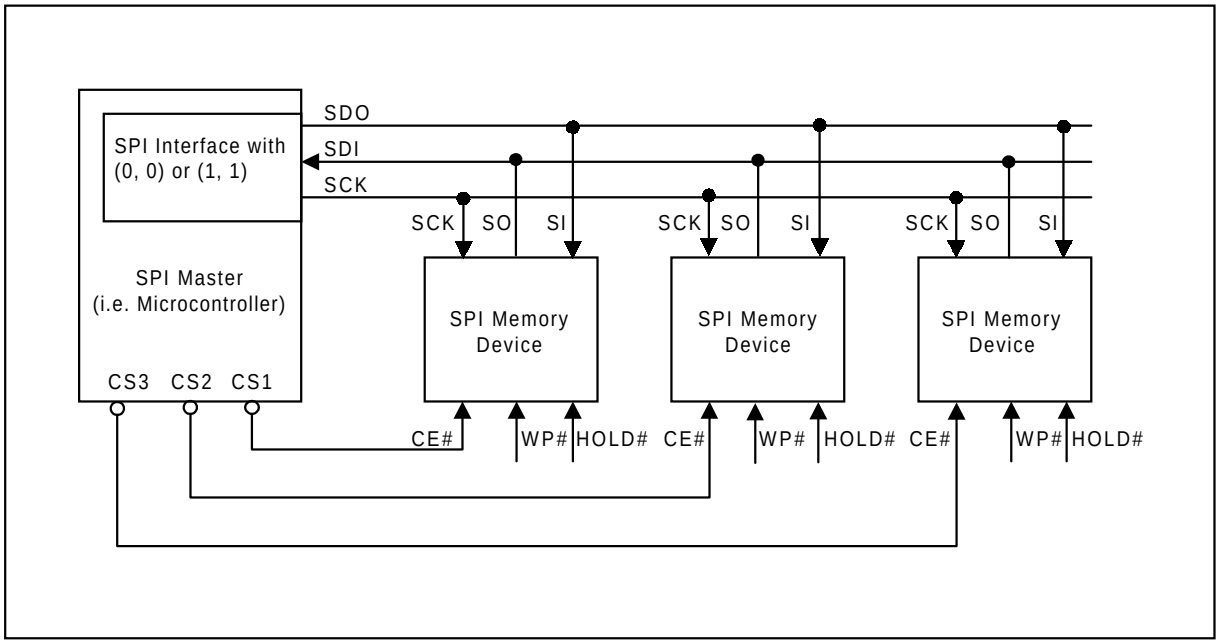
SPI MODES DESCRIPTION

Multiple Pm25LV080B/016B devices can be serially connected onto the SPI serial bus controlled by a SPI Master i.e. microcontroller as shown in Figure 1. The devices support either of the two SPI modes:

Mode 0 (0, 0)
Mode 3 (1, 1)

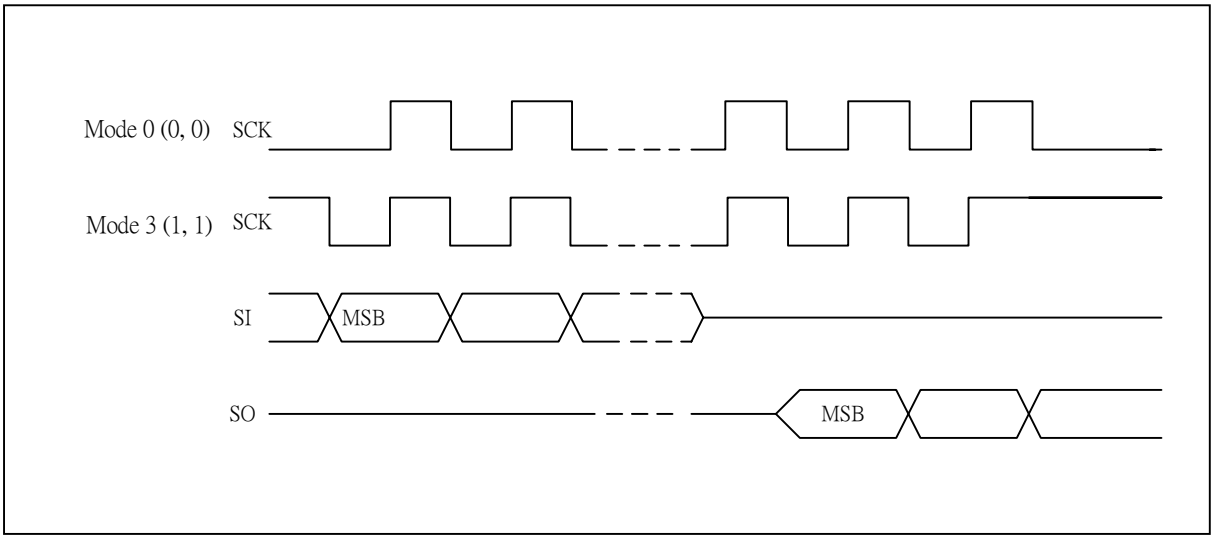
The difference between these two modes is the clock polarity when the SPI master is in Stand-by mode: the serial clock remains at "0" (SCK = 0) for Mode 0 and the clock remains at "1" (SCK = 1) for Mode 1. Please refer to Figure 2. For both modes, the input data is latched on the rising edge of Serial Clock (SCK), and the output data is available from the falling edge of SCK.

Figure 1. Connection Diagram among SPI Master and SPI Slaves (Memory Devices)



Note: 1. The Write Protect (WP#) and Hold (HOLD#) signals should be driven, High or Low as appropriate.

Figure 2. SPI Modes Supported



REGISTERS

The Pm25LV080B/016B are designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of Motorola MC68HCxx series of microcontrollers or all the SPI interface equipped system controllers.

The devices have two superset features can be enabled through the specific software instructions and Configuration Register:

1. Configurable sector size: The memory array of Pm25LV080B/160B are divided into uniform 4 Kbyte sectors or uniform 64 Kbyte blocks (sector group - consists of sixteen adjacent sectors).

   The devices have an option to configure the 4 Kbyte bottom sector (Sector 0) into four 1 Kbyte smaller sectors (Sector 0_0, Sector 0_1, Sector 0_2 and Sector 0_3). The finer granularity sector size architecture allows user to update data more efficiently. This feature allows user to eliminate the need of addtional serial EEPROM.

Refer to Table 1 for Configuration Register and Table 2 for Configuration Register Bit Definition.

Table 1. Configuration Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	SP0_3	SP0_2	SP0_1	SP0_0	SCFG

Table 2. Configuration Register Bit Definition

Bit	Name	Definition	Read/Write
Bit 0	SCFG	Sector Configuration: "0" indicates the bottom sector is one 4 Kbyte sector (default) "1" indicates the bottom sector is broken down to four 1 Kbyte sectors This feature can be implemented only when BP0,BP1&BP2 of status register were enabled to "1" which is in protection mode.	R/W
Bit 1	SP0_0	1 Kbyte Sector 0_0 Protection: "0" indicates sector protection is disabled (default) "1" indicates sector protection is enabled	R/W
Bit 2	SP0_1	1 Kbyte Sector 0_1Protection: "0" indicates sector protection is disabled (default) "1" indicates sector protection is enabled	R/W
Bit 3	SP0_2	1 Kbyte Sector 0_2 Protection: "0" indicates sector protection is disabled (default) "1" indicates sector protection is enabled	R/W
Bit 4	SP0_3	1 Kbyte Sector 0_3 Protection: "0" indicates sector protection is disabled (default) "1" indicates sector protection is enabled	R/W
Bit 5 - 6	RES	Reserved for future (don't care)	N/A
Bit 7	RES	Reserved for future (don't use)	N/A

REGISTERS (CONTINUED)

CONFIGURATION REGISTER

The Configuration Register is built by latchs need to be set each time after power-up before enabling the 1 Kbyte smaller sector size and 1 Kbyte sector write protection. The Bit 0 - Bit 7 of Configuration Register are set as "0"s after power-up reset. Therefore, the devices will be always set as normal mode - the bottom sector set as 4 Kbyte by default after power-up to maintain the backward-compatibility.

The function of Configuration Register is described as following:

SCFG bit: The 1 Kbyte smaller sector mode is enabled by writing "1" to SCFG bit, then Sector 0 is configured as Sector 0_0, Sector 0_1, Sector 0_2 and Sector 0_3. A Sector Erase (SECTOR_ER) instruction can be used to erase any one of those four 1 Kbyte sectors. The SCFG bit will be reset "0" state automatically at power on stage. Thus, the 1 Kbyte smaller sector mode is disabled at power on till SCFG bit was set.

The SCFG bit only can be enabled to "1" when BP0, BP1&BP2 of status register were "1" state which in protection mode. On the other word, SCFG bit will be cleared to "0" state when BPx were "0" to disable the protection mode.

SP0_x bits: The write protection to those four 1 Kbyte sectors can be activated by writing "1"s to the SP0_0, SP0_1, SP0_2 and SP0_3 bits. The 1 Kbyte sector write protection function can only be enabled when the SCFG is also enabled.

The Write Configuration Register (WRCR) instruction can be used to write "0"s or "1"s into Configuration Register. And the Read Configuration Register (RDCR) instruction can be used to read the setting of Configuration Register. Refer to Table 8 for Instruction Set.

STATUS REGISTER

The Status Register contains WIP and WEL status bits to indicate the status of the devices, the Block Protection Bits (BP0, BP1 and BP2) to define the portion of memory blocks to be write protected,

and SRWD control bits to be set for status register write protection. Refer to Table 3 and Table 4 for Status Register Format and Status Register Bit Definition.

The BP0, BP1, BP2, and SRWD are non-volatile memory cells that can be written by Write Status Register (WRSR) instruction. The default value of BP0, BP1, BP2, and SRWD bits were set as "0" at factory. Once those bits are written as "0" or "1", it will not be changed by devices power-up or power-down until next WRSR instruction alters its value. The Status Register can be read by Read Status Register (RDSR) instruction for its value and status. Refer to Table 8 for Instruction Set.

The function of Status Register is described as following:

WIP bit: The Write In Progress (WIP) bit can be used to detact the progress or completion of program or erase operation. When WIP bit is "0", the devices are ready for write status register, program or erase operation. When WIP bit is "1", the devices are busy.

WEL bit: The Write Enable Latch (WEL) bit indicates the status of internal write enable latch. When WEL bit is "0", the write enable latch is disabled, all write operations include write status register, write configuration register, page program, sector erase, block and chip erase operations are inhibited. When WEL bit is "1", the write enable latch is enabled. Then write operations are allowed. The WEL bit is enabled by Write Enable (WREN) instruction. All write register, program and erase instructions must be preceded by a WREN instruction every time. The WEL bit can be disabled by Write Disable (WRDI) instruction or automatically return to reset state after the completion of a write instruction.

BP2, BP1, BP0 bits: The Block Protection (BP2 , BP1, BP0) bits are used to define the portion of memory area to be protected. Refer to Table 5, 6 and 7 Block Write Protection Bits Setting . When one of the combination of BP2, BP1 and BP0 bits were set as "1", the relevant memory area is protected. Any program or erase operation to that area will be prohibited. Especially, the Chip Erase (CHIP_ER) instruction is executed only if all the Block Protection Bits are set as "0"s.

If SCFG bit was enabled to support 1KB x4 sectores on Sector 0, Sector 0's protection status will respect SP0_x in Configuration Register and ignore BPx bits status whatever protection status.

REGISTERS (CONTINUED)

SRWD bit: The Status Register Write Disable (SRWD) bit is operated in conjuction with the Write Protection (WP#) signal to provide a Hardware Protection Mode. When the SRWD is set to "0", the Status Register is not write protected. When the SRWD is set to "1" and the WP# is pulled low (V_{IL}), the non-volatile bits of Status Register (SRWD, BP2, BP1, BP0) become read-only and the WRSR instruction will be prohibited. If the SRWD is set to "1" but WP# is pulled high (V_{IH}), the Status Register is still changeable by WRSR instruction.

Table 3. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRWD	0	0	BP2	BP1	BP0	WEL	WIP

Table 4. Status Register Bit Definition

Bit	Name	Definition	Read-/Write	Non-Volatile bit
Bit 0	WIP	Write In Progress Bit: "0" indicates the device is ready "1" indicates the write cycle is in progress and the device is busy	R	No
Bit 1	WEL	Write Enable Latch: "0" indicates the device is not write enabled (default) "1" indicates the device is write enabled	R/W	No
Bit 2	BP0	Block Protection Bit: (See Table 5 and Table 6 for details) "0" indicates the specific blocks are not write protected (default) "1" indicates the specific blocks are write protected	R/W	Yes
Bit 3	BP1			
Bit 4	BP2			
Bits 5 - 6	N/A	Reserved: Always "0"s	N/A	
Bit 7	SRWD	Status Register Write Disable: (See Table 7 for details) "0" indicates the Status Register is not write protected (default) "1" indicates the Status Register is write protected	R/W	Yes

Table 5. Block Write Protect Bits for Pm25LV080B

Status Register Bits			Protected Memory Area
BP2	BP1	BP0	8 Mbit
0	0	0	None
0	0	1	Upper sixteenth (block : 15): 0F0000h - 0FFFFFh
0	1	0	Upper eighth (two blocks :14 and 15): 0E0000h - 0FFFFFh
0	1	1	Upper quarter (four blocks :12 to 15): 0C0000h - 0FFFFFh
1	0	0	Upper half (eight blocks :8 to 15): 080000h - 0FFFFFh
1	0	1	All blocks (sixteen blocks : 0 to 15): 000000h - 0FFFFFh
1	1	0	
1	1	1	

REGISTERS (CONTINUED)

Table 7. Block Write Protect Bits for Pm25LV016B

Status Register Bits			Protected Memory Area
BP2	**BP1**	**BP0**	**16 Mbit**
0	0	0	None
0	0	1	Upper 32nd (block : 31): 1F0000h - 1FFFFFh
0	1	0	Upper sixteenth (two blocks :30 and 31): 1E0000h - 1FFFFFh
0	1	1	Upper eighth (four blocks :28 to 31): 1C0000h - 1FFFFFh
1	0	0	Upper quarter (eight blocks :24 to 31): 180000h - 1FFFFFh
1	0	1	Upper half (sixteen blocks :10 to 31): 100000h - 1FFFFFh
1	1	0	All blocks (32 blocks : 0 to 31): 000000h - 1FFFFFh
1	1	1	

PROTECTION MODE

The Pm25LV080B/016B have two protection modes: hardware write protection and software write protection to prevent any irrelevant operation under a possible noisy environment and protect the data integrity.

HARDWARE WRITE PROTECTION

The devices provide two hardware write protection features:

a. When input any program, erase or write status register instruction, the number of clock pulse will be checked whether it is a multiple of eight before the execution of such instruction. Any incomplete instruction command sequence will be ignored.

b. The devices feature a Write Protection (WP#) pin to provide a hardware write protection method for BP2, BP1,BP0 abd SRWD in the Status Register.
(1)When the WP# is pulled low (V_{IL}), the Status Register is write protected if the SRWD bit is enabled (Refer to Table 7 for Hardware Write Protection on Status Register). Hence part or whole memory area can be write protected depends on the setting of BP2, BP1 and BP0 bits.
(2) When the WP# is pulled high (V_{IH}), the Status Register is not protected, BP2,BP1,BP0 and SRWD can be changed.

SOFTWARE WRITE PROTECTION

The Pm25LV080B/016B also provide two software write protection features:

a. Before the execution of any program, erase or write status register instruction, the Write Enable Latch (WEL) bit must be enabled by execution of the Write Enable (WREN) instruction. If the WEL bit is not enabled first, the program, erase or write register instruction will be ignored.
b. The Block Protection (BP2, BP1, BP0) bits allow part or whole memory area to be write protected.

Table 8. Hardware Write Protection on Status Register

SRWD	WP#	Status Register
0	Low	Writable
1	Low	Protected
0	High	Writable
1	High	Writable

DEVICE OPERATION

The Pm25LV080B/016B utilize an 8-bit instruction register. Refer to Table 8 Instruction Set for the detail Instructions and Instruction Codes. All instructions, addresses, and data are shifted in with the most significant bit (MSB) first on Serial Data Input (SI). The input data on SI is latched on the rising edge of Serial Clock (SCK) after the Chip Enable (CE#) is driven low (V_{IL}).

Every instruction sequence starts with a one-byte instruction code and might be followed by address bytes, data bytes, or address bytes and data bytes depends on the type of instruction. The CE# must be driven high (V_{IH}) after the last bit of the instruction sequence has been shifted in.

Table 9. Instruction Set

Instruction Name	Instruction Format	Hex Code	Operation	Maximum Frenquency
WREN	0000 0110	06h	Write Enable	100 MHz
WRDI	0000 0100	04h	Write Disable	100 MHz
RDSR	0000 0101	05h	Read Status Register	100 MHz
WRSR	0000 0001	01h	Write Status Register	100 MHz
READ	0000 0011	03h	Read Data Bytes from Memory at Normal Read Mode	33 MHz
FAST_READ	0000 1011	0Bh	Read Data Bytes from Memory at Fast Read Mode	100 MHz
RDID	1001 0000	90h	Read Manufacturer and Product ID	100 MHz
RDES	1010 1011	ABh	Read Electronic Signature	100 MHz
JEDEC ID READ	1001 1111	9Fh	Read Manufacturer and Prduct ID by JEDEC ID Command	100 MHz
PAGE_ PROG	0000 0010	02h	Page Program Data Bytes Into Memory	100 MHz
RDCR	1010 0001	A1h	Read Configuration Register	100 MHz
WRCR	1111 0001	F1h	Write Configuration Register	100 MHz
SECTOR_ER	1101 0111 0010 0000	D7h 20h	Sector Erase, support both D7h and 20h Command	100 MHz
BLOCK_ER	1101 1000	D8h	Block Erase	100 MHz
CHIP_ER	1100 0111 0110 0000	C7h 60h	Chip Erase	100 MHz

HOLD OPERATION

The HOLD# is used in conjunction with the CE# to select the Pm25LV080B/016B. When the devices are selected and a serial sequence is underway, HOLD# can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the HOLD# must be brought low while the SCK signal is low. To resume serial communication, the HOLD# is brought high while the SCK signal is low (SCK may still toggle during HOLD). Inputs to the SI will be ignored while the SO is in the high impedance state.

DEVICE OPERATION (CONTINUED)

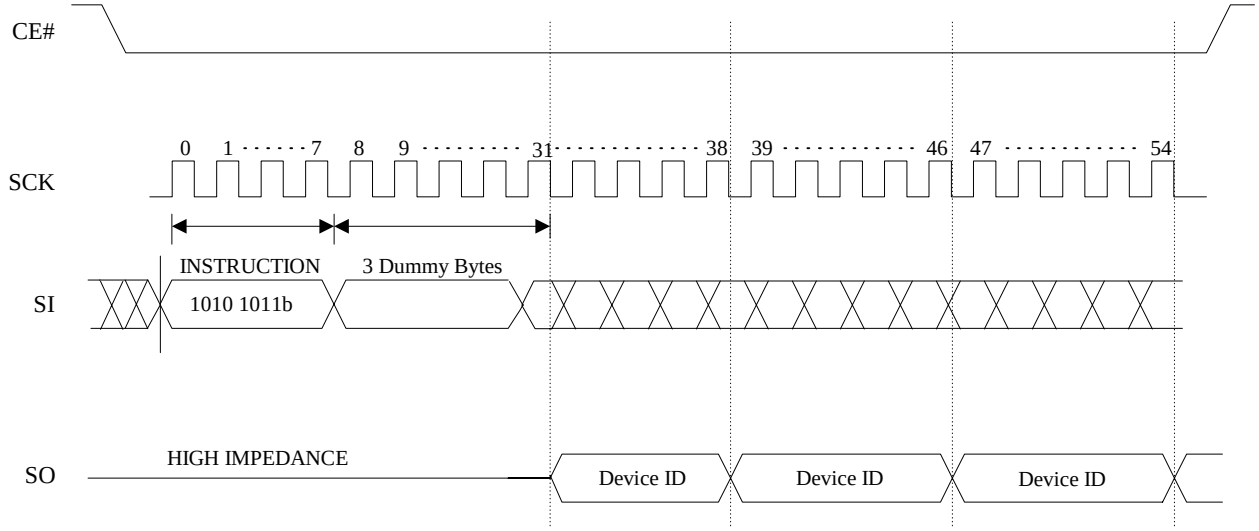
READ ELECTRONIC SIGNATURE OPERATION

The Read Electronic Signature (RDES) instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as table of ID Definitions. This is not same as RDID or JEDEC ID instruction. It's not recommended to use for new design. For new design , please use RDID or JEDEC ID instruction.
The RDES instruction code is followed by three dummy bytes, each bit being latched-in on SI during the rising edge of SCK. Then the Device ID is shifted out on SO with the MSB first, each bit been shifted out during the falling edge of SCK. The RDES instruction is ended by CE# goes high. The Device ID outputs repeatedly if continuously send the additional clock cycles on SCK while CE# is at low.

Table 10. Product Identification

Product Identification		Data
Manufacturer ID	First Byte	9Dh
	Second Byte	7Fh
Device ID:		
Pm25LV080B		13h
Pm25LV016B		14h

Figure 3. Read Electronic Signature Sequence



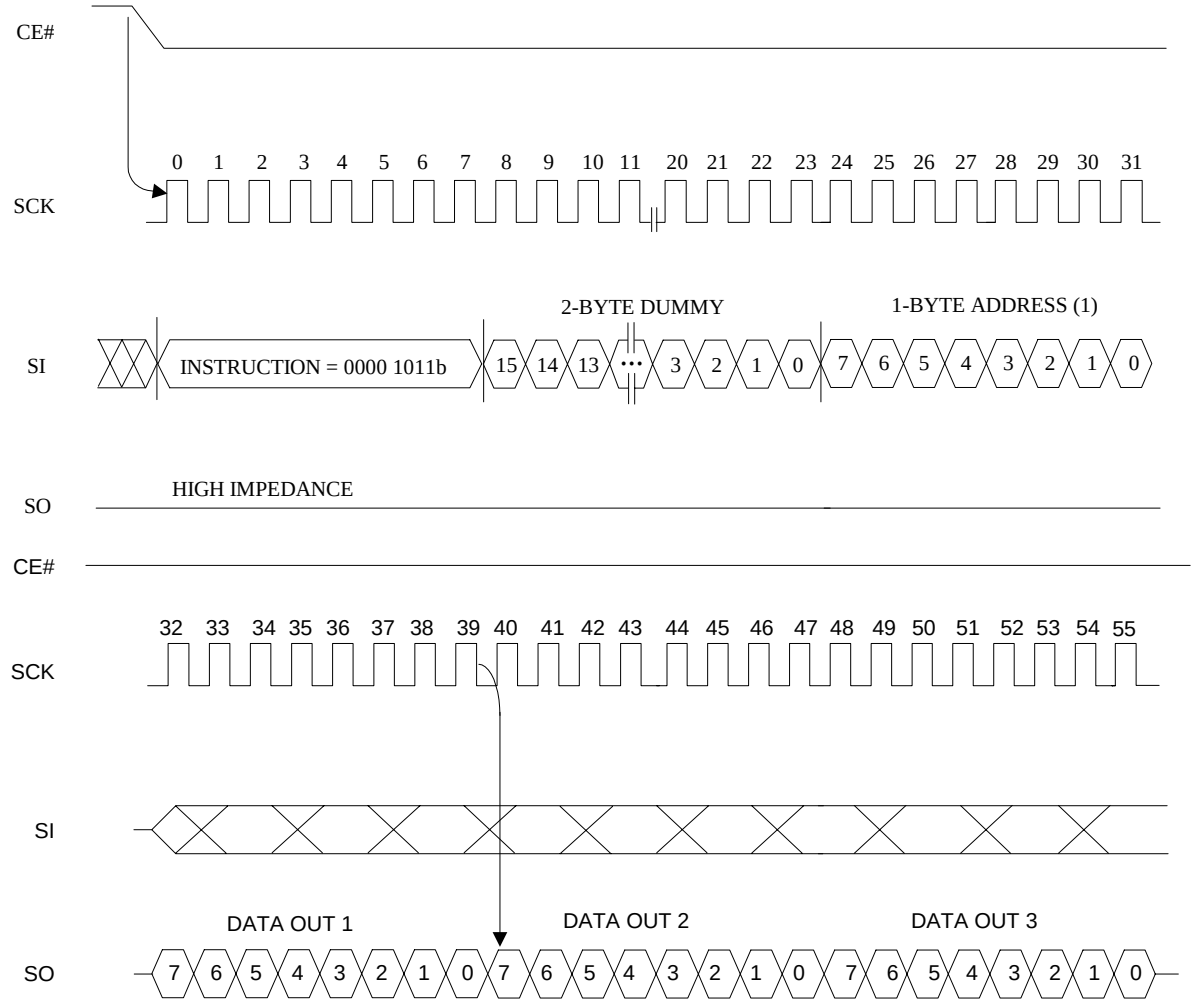
DEVICE OPERATION (CONTINUED)

READ PRODUCT IDENTIFICATION OPERATION

The Read Product Identification (RDID) instruction allows the user to read the manufacturer and product ID of the devices. Refer to Table 10 Product Identification for pFLASH™ manufacturer ID and device ID. The RDID instruction code is followed by two dummy bytes and one byte address (A7~A0), each bit being latched-in on SI during the rising edge of SCK. If one byte address is initially set to A0 = 0, then the first manufacturer ID (9Dh) is shifted out on SO with the MSB first, the device ID and the second manufacturer ID (7Fh), each bit been shifted out during the falling edge of SCK.

If one byte address is initially set to A0 = 1, then device ID will be read first, then followed by the first manufacture ID (9Dh) and then second manufacture ID (7Fh). The manufacture and device ID can be read continuously, alternating from one to the others. The instruction is completed by driving CE# high.

Figure 4. Read Product Identification Sequence



Note :

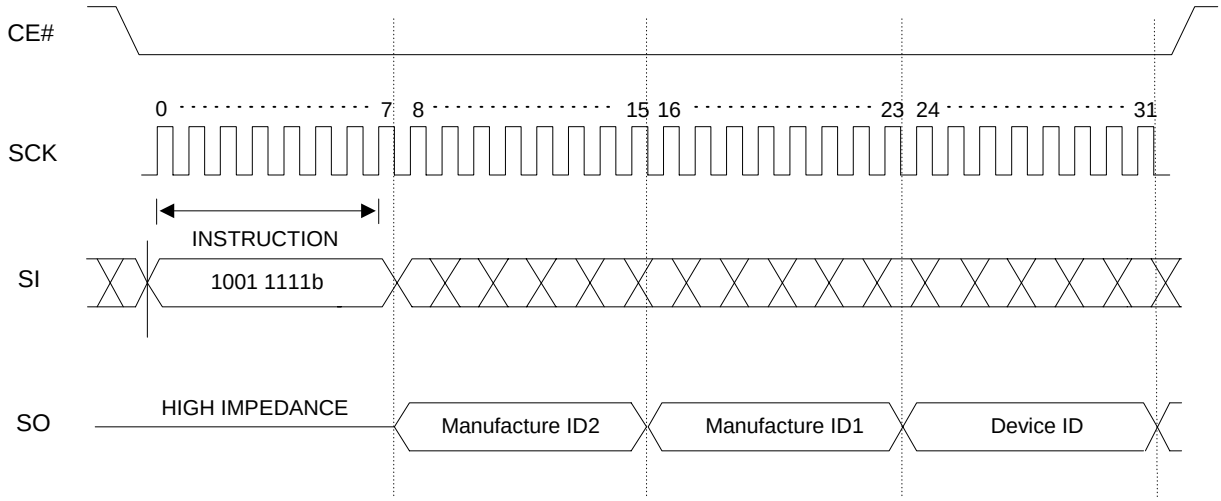
(1) ADDRESS A0 = 0, will output the 1st manufacture ID (9Dh) first -> device ID -> 2nd manufacture ID (7Fh)
ADDRESS A0 = 1, will output the device ID -> 1st manufacture ID (9D) -> 2nd manufacture ID (7Fh)

DEVICE OPERATION (CONTINUED)

READ PRODUCT IDENTIFICATION BY JEDEC ID COMMAND

The JEDEC ID READ instruction allows the user to read the manufacturer and product ID of the devices. Refer to Table 9 Product Identification for pFLASH™ manufacturer ID and device ID. The second manufacturer ID (7Fh) is shifted out on SO with the MSB first after JEDEC ID READ command input, followed by the first manufacturer ID (9Dh) and the device ID, each bit been shifted out during the falling edge of SCK.

Figure 5. Read Product Identification by JEDEC ID READ Sequence

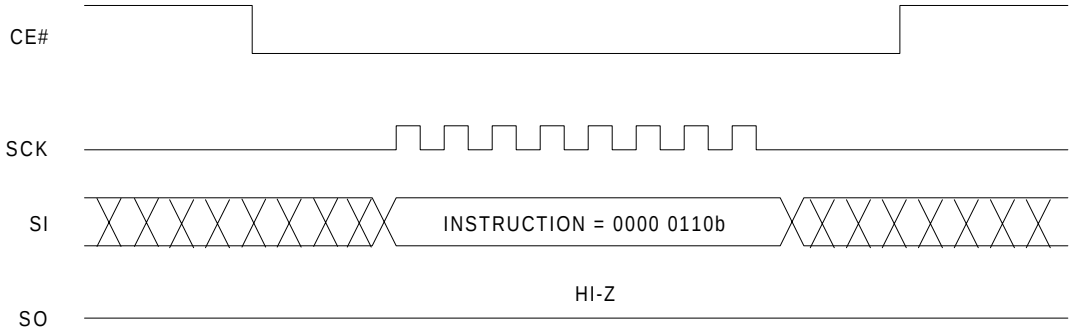


DEVICE OPERATION (CONTINUED)

WRITE ENABLE OPERATION

The Write Enable (WREN) instruction is used to set the Write Enable Latch (WEL) bit. The WEL bit of the Pm25LV080B/016B are set as write disable state after power-up. The WEL bit must be write enabled before any write operation includes sector, block and chip erase, page program, write status register, and write configuration register operations. The WEL bit will be reset back to write disable state automatically after the completion of a write operation. The WREN instruction is required before any above instruction is executed.

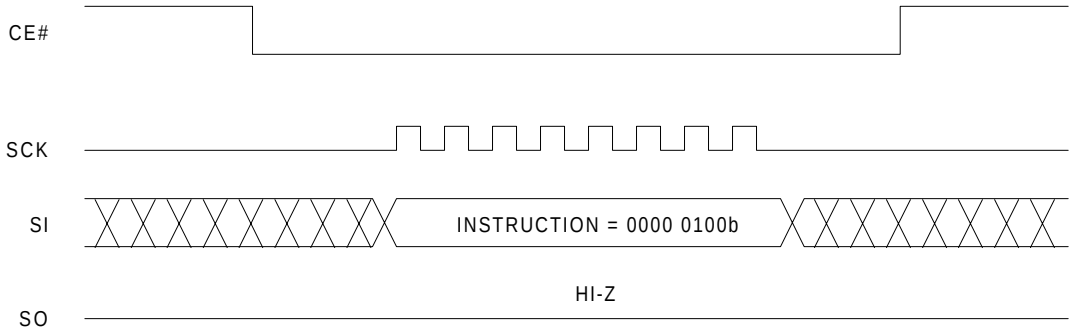
Figure 6. Write Enable Sequence



WRITE DISABLE OPERATION

To protect the device against inadvertent writes, the Write Disable (WRDI) instruction resets the WEL bit and disables all write instructions. The WRDI instruction is not required after the execution of a write instruction. The WEL will be automatically reset.

Figure 7. Write Disable Sequence

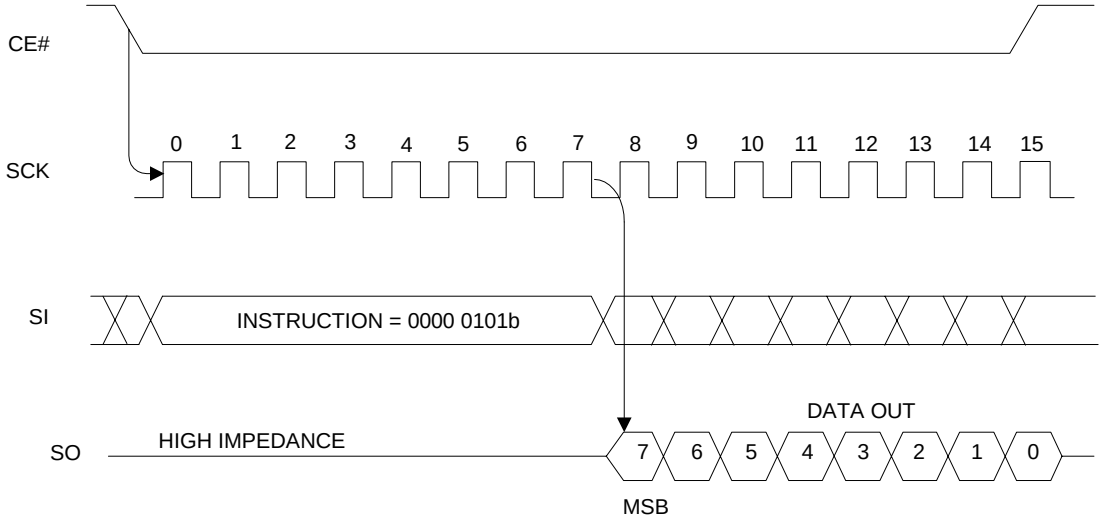


DEVICE OPERATION (CONTINUED)

READ STATUS REGISTER OPERATION

The Read Status Register (RDSR) instruction provides access to the status register. During the execution of a program, erase or write status register operation, all other instructions will be ignored except the RDSR instruction can be used for detecting the progress or completion of the operations by reading the WIP bit of status register.

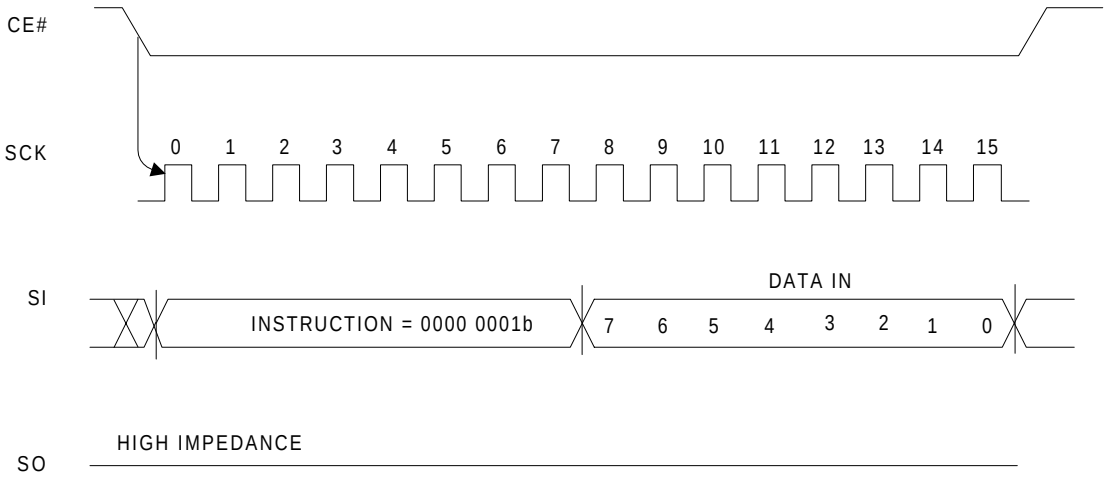
Figure 8. Read Status Register Sequence



WRITE STATUS REGISTER OPERATION

The Write Status Register (WRSR) instruction allows the user to enable or disable the block protection and status register write protection features by writting “0”s or “1”s into those non-volatile BP2, BP1, BP0 and SRWD bits. The erase operation for those non-volatile bits are not required.

Figure 9. Write Status Register Sequence

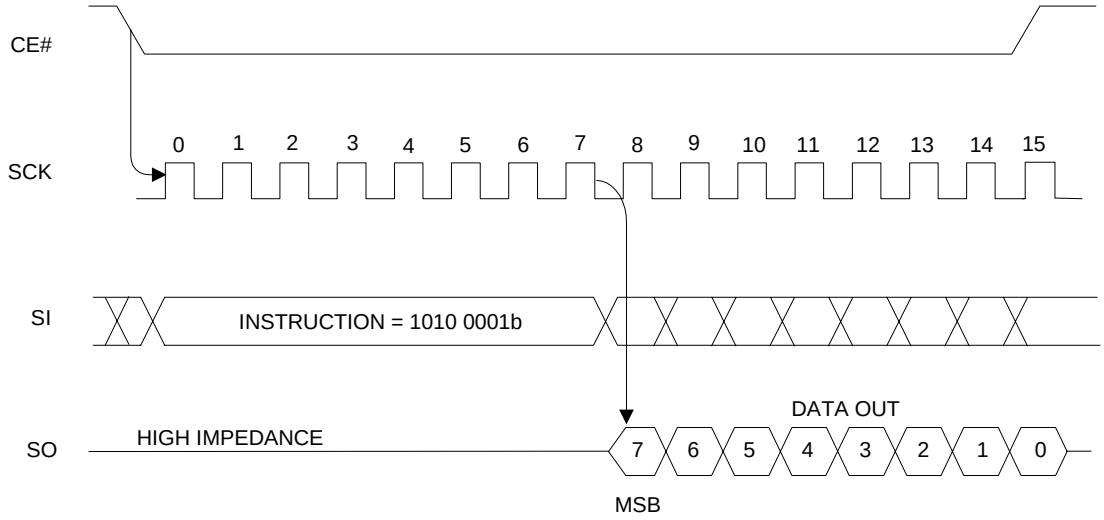


DEVICE OPERATION (CONTINUED)

READ CONFIGURATION REGISTER OPERATION

The Read Configuration Register (RDCR) instruction provides access to the Configuration Register. This instruction can be used to verify the configuration setting of bottom Sector 0 and the write protection setting for each individual 1 Kbyte sector (Sector 0_0 ~ Sector 0_3) within the Sector 0.

Figure 10. Read Configuration Register Sequence

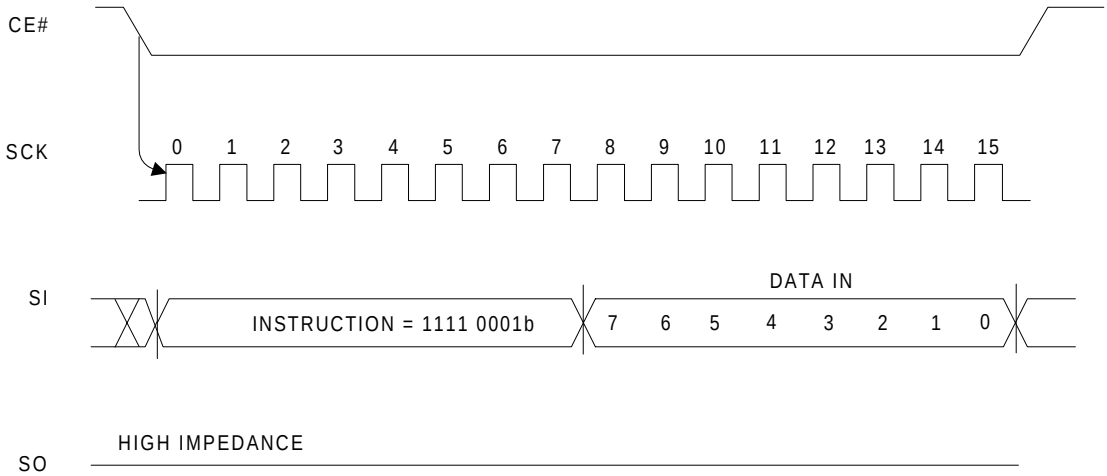


WRITE CONFIGURATION REGISTER OPERATION

The Write Configuration Register (WRCR) instruction allows user to enable or disable four smaller 1K byte sectors and protection for each 1K byte sector by writing “0”s or “1”s into SCFG and SP0_3 ~SP0_1 in the congiguration register. please refer table 2 for details.

Do not require WREN command before this WRCR operation. Because Configuration Register is a data latch architecture not a flash cell.

Figure 11. Write Configuration Register Sequence



DEVICE OPERATION (CONTINUED)

READ DATA OPERATION

The Read Data (READ) instruction is used to read memory data of Pm25LV080B/016B under normal mode running up to 33 MHz.

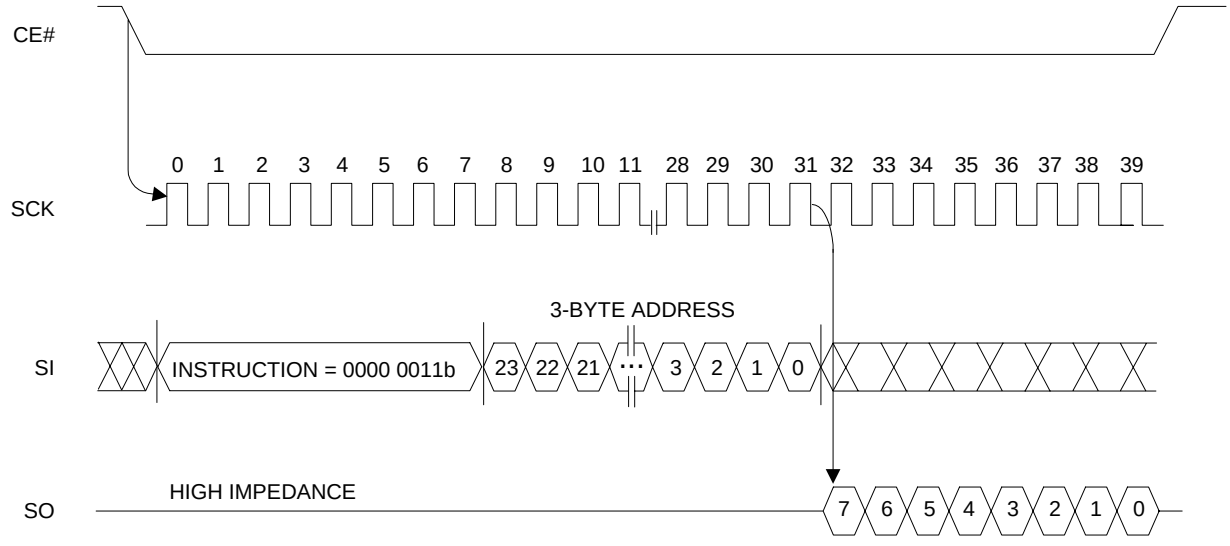
The READ instruction is activated by pulling the CE# line of the selected device to low (V_{IL}), and the READ instruction code is transmitted via the SI line followed by three bytes address (A23 - A0) to be read. There are total 24 address bits will be shifted in, only the A_{MS} (most-significant address) - A0 will be decoded and the rest of A23 - A_{MS} can be don't cared. Refer to Table 10 for the related Address Key. Upon completion, any data on the SI will be ignored.

The first byte data D7 - D0 addressed (can be at any location) is then shifted out onto the SO line. A single byte data or up to whole memory array can be read out in one READ instruction. The address is automatically increamented to the next higher address after each byte of data is shifted out. The read operation can be terminated any time by driving the CE# high (V_{IH}) after the data comes out. When the highest address of the devices is reached, the address counter will roll over to the 000000h address allowing the entire memory to be read in one continuous READ instruction.

Table 11. Address Key

Address	Pm25LV080B	Pm25LV016B
A_N	A19 - A0	A20 - A0
Don't Care Bits	A23 - A20	A23 - A21

Figure 12. Read Data Sequence



DEVICE OPERATION (CONTINUED)

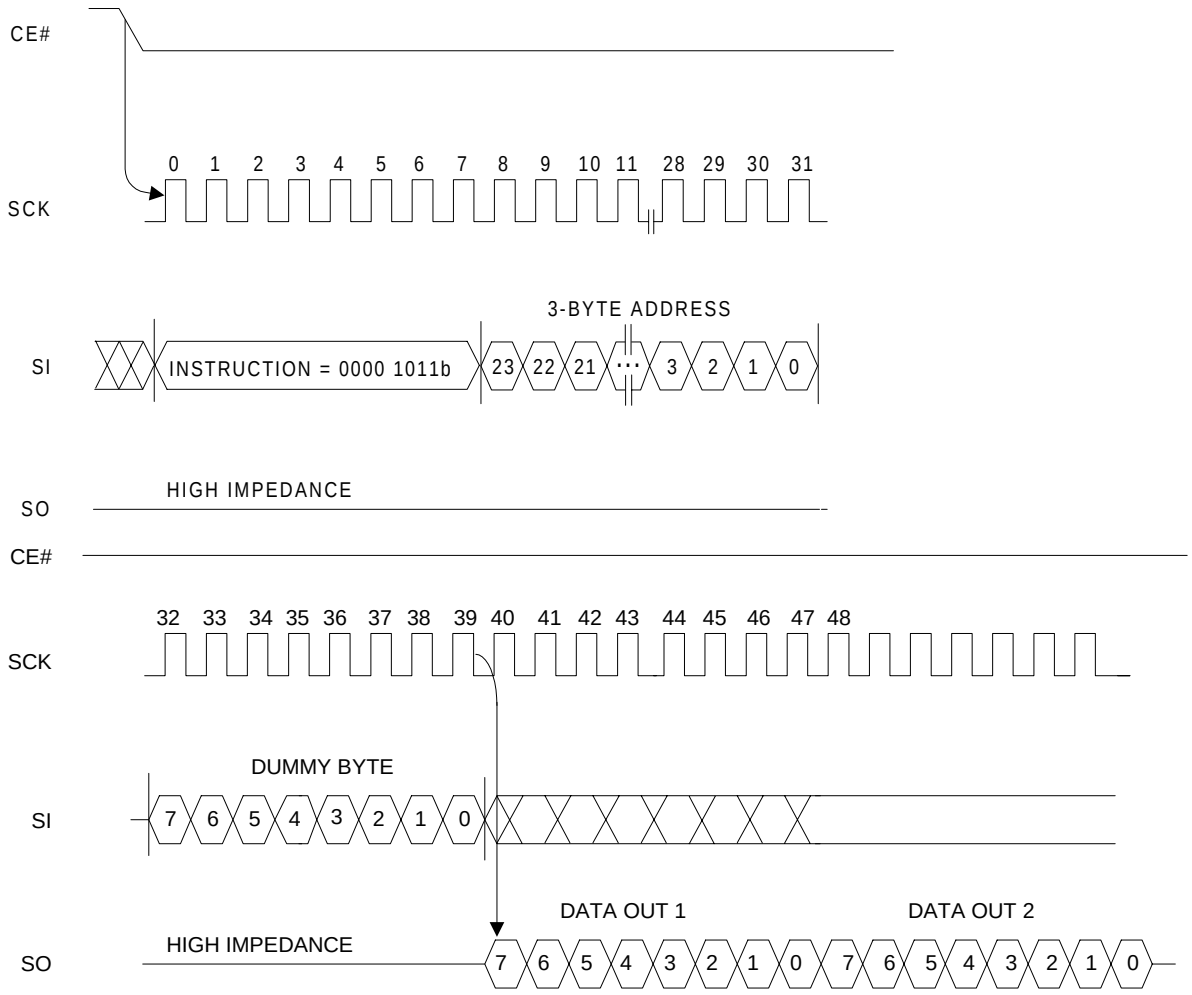
FAST READ DATA OPERATION

The Pm25LV080B/016B also feature a Fast Read (FAST_READ) instruction. This FAST_READ instruction is used to read memory data in 100MHz clock rate where the FAST_READ instruction proceeding.

The devices are first selected by driving CE# low (V_{IL}). The FAST_READ instruction code followed by three bytes address (A23 - A0) and a dummy byte (8 clocks) is trasmitted via the SI line, each bit being latched-in during the rising edge of SCK. Then the first data byte addressed is shifted out on SO line, each bit being shifted out at a maximum frequency f_{CT}, during the falling edge of SCK.

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address allowing the entire memory to be read with a single FAST_READ instruction. The FAST_READ instruction is terminated by driving CE# high (V_{IH}).

Figure 13. Fast Read Data Sequence



DEVICE OPERATION (CONTINUED)

PAGE PROGRAM OPERATION

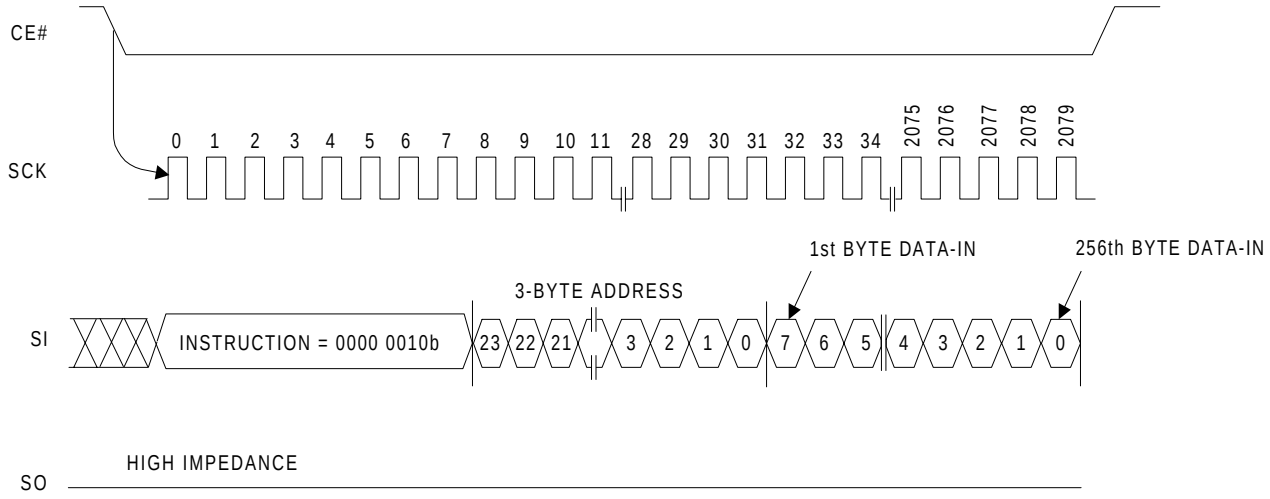
The Page Program (PAGE_PROG) instruction allow up to 256 bytes data to be programmed into memory in one program operation page by page. The destination of the memory to be programmed must be outside the protected memory area set by the Block Protection (BP2, BP1, BP0) bits. A PAGE_PROG instruction attemps to program into a page which is write protected will be ignored. Before the execution of PAGE_PROG instruction, the Write Enable Latch (WEL) must be enabled through a Write Enable (WREN) instruction.

The PAGE_PROG instruction is activated, after the CE# is pulled low to select the device and staying low during the entire instruction sequence, by shifting in the PAGE_PROG instruction code, three address bytes and program data (1 to 256 bytes) to be programmed via the SI line. Program operation will start immediately after the CE# is brought high, otherwise the PAGE_PROG instruction will not be executed. The internal control logic automatically handles the programming voltages and timing. During a program operation, all instructions will be ignored except the RDSR instruction. The progress or completion of the program operation can be determined by reading the WIP bit in Status Register through a RDSR instruction. If WIP bit = “1”, the program operation is still in progress. If WIP bit = “0”, the program operation has completed.

A single PAGE_PROG instruction programs 1 to 256 consecutive bytes within a page if it is not write protected. If more than 256 bytes data are sent to the devices, the address counter will roll over on the same page and the previously latched data are discarded and the last 256 bytes data are kept to be programmed into the page. The starting byte can be anywhere within the same page. When the end of the page is reached, the address will wrap around to the beginning of the same page. If the data to be programmed are less than a full page, the data of all other bytes on the same page will remain unchanged.

A program operation can alter “1”s into “0”s, but an erase operation is required to change “0”s back to “1”s. The same byte cannot be reprogrammed without erasing the whole sector or block first.

Figure 14. Page Program Sequence



DEVICE OPERATION (CONTINUED)

ERASE OPERATION

The memory array of Pm25LV080B/016B are organized into uniform 4 Kbyte sectors or 64 Kbyte uniform blocks (sector group - consists of sixteen adjacent sectors). The bottom sector (Sector 0) of the devices can be configured into four 1 Kbyte smaller sectors.

Before a byte can be reprogrammed, the sector or block which contains this byte must be erased first. In order to erase the devices, there are three erase instructions include Sector Erase (SECTOR_ER), Block Erase (BLOCK_ER) and Chip Erase (CHIP_ER) instructions can be used. A sector erase operation allows to erase any individual sector without affecting the data in others. A block erase operation allows to erase any individual block. And a chip erase operation allows to erase the whole memory array of the devices. Pre-programs the devices are not required prior to a sector erase, block erase or chip erase operation.

SECTOR ERASE OPERATION

A SECTOR_ER instruction erases a 4 Kbyte sector or a 1 Kbyte smaller sector (Sector 0_3, Sector 0_2, Sector 0_1, Sector 0_0) if the bottom Sector 0 has been configured as four smaller sectors. Before the execution of SECTOR_ER instruction, the Write Enable Latch (WEL) must be enabled through a Write Enable (WREN) instruction. The WEL will be reset automatically after the completion of sector erase operation.

The SECTOR_ER instruction is entered, after the CE# is pulled low to select the device and staying low during the entire instruction sequence, by shifting in the SECTOR_ER instruction code and three address bytes via the SI. Erase operation will start immediately after the CE# is pulled high, otherwise the SECTOR_ER instruction will not be executed. The internal control logic automatically handles the erase voltage and timing. Refer to Figure 13 for Sector Erase Sequence.

During a erase operation, all instruction will be ignored except the Read Status Register (RDSR) instruction. The progress or completion of the erase opertion can be determined by reading the WIP bit in Status Register through a RDSR instruction. If WIP bit = “1”, the erase operation is still in progress. If WIP bit = “0”, the erase operation has been completed.

BLOCK ERASE OPERATION

A Block Erase (BLOCK_ER) instruction erases a 64 Kbyte block for the Pm25LV080B/016B. Before the execution of BLOCK_ER instruction, the Write Enable Latch (WEL) must be enabled through a Write Enable (WREN) instruction. The WEL will be reset automatically after the completion of block erase operation.

The BLOCK_ER instruction is entered, after the CE# is pulled low to select the device and staying low during the entire instruction sequence, by shifting in the BLOCK_ER instruction code and three address bytes via the SI. Erase operation will start immediately after the CE# is pulled high, otherwise the BLOCK_ER instruction will not be executed. The internal control logic automatically handles the erase voltage and timing. Refer to Figure 14 for Block Erase Sequence.

CHIP ERASE OPERATION

A Chip Erase (CHIP_ER) instruction erases the whole memory array of Pm25LV080B/016B. Before the execution of CHIP_ER instruction, the Write Enable Latch (WEL) must be enabled through a Write Enable (WREN) instruction. The WEL will be reset automatically after the completion of chip erase operation.

The CHIP_ER instruction is entered, after the CE# is pulled low to select the device and staying low during the entire instruction sequence, by shifting in the CHIP_ER instruction code via the SI. Erase operation will start immediately after the CE# is pulled high, otherwise the CHIP_ER instruction will not be executed. The internal control logic automatically handles the erase voltage and timing. Refer to Figure 15 for Chip Erase Sequence.

DEVICE OPERATION (CONTINUED)

Figure 15. Sector Erase Sequence

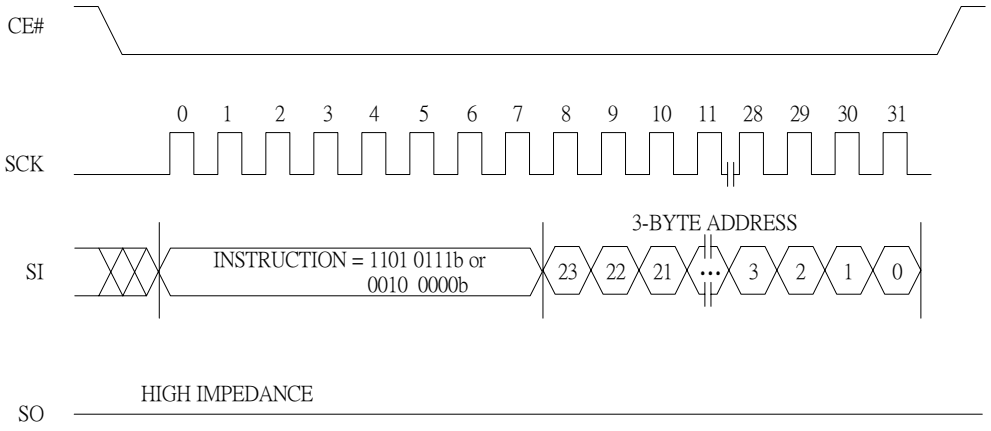


Figure 16. Block Erase Sequence

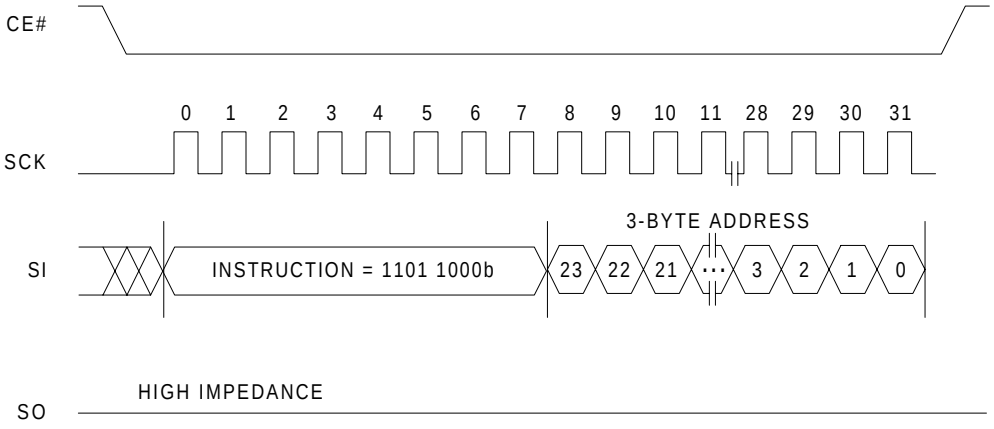
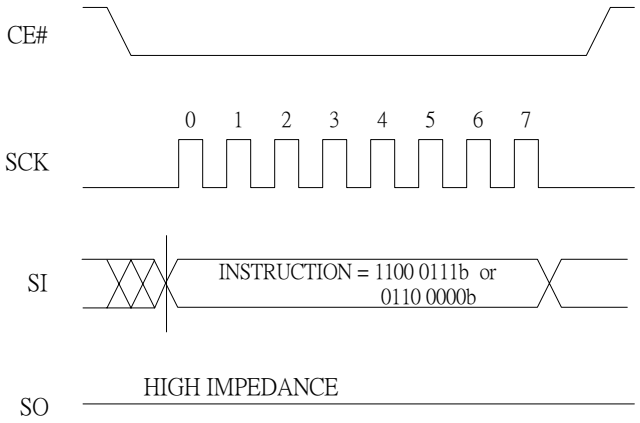


Figure 17. Chip Erase Sequence



BLOCK/SECTOR ADDRESS

Table 12. Block/Sector Addresses of Pm25LV080B/016B

Memory Density		Block No.	Block Size (Kbytes)	Sector No.	Sector Size (Kbytes)	Address Range
16 Mbit	8 Mbit	Block 0	64	Sector 0 (1)	4	000000h - 000FFFh
				Sector 1	4	001000h - 001FFFh
				:	:	:
				Sector 15	4	00F000h - 00FFFFh
		Block 1	64	Sector 16	4	010000h - 010FFFh
				Sector 17	4	011000h - 011FFFh
				:	:	:
				Sector 31	4	01F000h - 01FFFFh
		Block 2	64	:	:	020000h - 02FFFFh
		:	:	:	:	:
		:	:	:	:	:
		Block 13	64	:	:	0D0000h - 0DFFFFh
		Block 14	64	:	:	0E0000h - 0EFFFFh
		Block 15	64	:	:	0F0000h - 0FFFFFh
		:	:	:	:	:
		:	:	:	:	:
		:	:	:	:	:
		Block 29	64	:	:	1D0000h - 1DFFFFh
		Block 30	64	:	:	1E0000h - 1EFFFFh
		Block 31	64	:	:	1F0000h - 1FFFFFh

Note: 1. Sector 0 can be configured into four smaller 1 Kbyte sectors (Sector 0_0: 000000h - 0003FFh, Sector 0_1: 000400h - 0007FFh, Sector 0_2: 000800h - 000BFFh, and Sector 0_3: 000C00h - 000FFFh).

ABSOLUTE MAXIMUM RATINGS (1)

Temperature Under Bias		-65°C to +125°C
Storage Temperature		-65°C to +125°C
Surface Mount Lead Soldering Temperature	Standard Package	240°C 3 Seconds
	Lead-free Package	260°C 3 Seconds
Input Voltage with Respect to Ground on All Pins (2)		-0.5 V to V_{CC} + 0.5 V
All Output Voltage with Respect to Ground		-0.5 V to V_{CC} + 0.5 V
V_{CC} (2)		-0.5 V to +6.0 V

Notes:
1. Stresses under those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. The functional operation of the device or any other conditions under those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condition for extended periods may affected device reliability.
2. Maximum DC voltage on input or I/O pins are V_{CC} + 0.5 V. During voltage transitioning period, input or I/O pins may overshoot to V_{CC} + 2.0 V for a period of time up to 20 ns. Minimum DC voltage on input or I/O pins are -0.5 V. During voltage transitioning period, input or I/O pins may undershoot GND to -2.0 V for a period of time up to 20 ns.

DC AND AC OPERATING RANGE

Part Number	**Pm25LV080B/016B**
Operating Temperature (Commercial Grade)	-40°C to 105°C
Vcc Power Supply	2.7 V - 3.6 V

DC CHARACTERISTICS

Applicable over recommended operating range from:
T_{AC} = -40°C to +105°C, V_{CC} = 2.7 V to 3.6 V (unless otherwise noted).

Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{CC1}	Vcc Active Read Current	V_{CC} = 3.6V at 33 MHz, SO = Open			10	15	mA
I_{CC2}	Vcc Program/Erase Current	V_{CC} = 3.6V at 33 MHz, SO = Open			15	30	mA
I_{SB1}	Vcc Standby Current CMOS	V_{CC} = 3.6V, CE# = V_{CC}				50	µA
I_{SB2}	Vcc Standby Current TTL	V_{CC} = 3.6V, CE# = V_{IH} to V_{CC}				3	mA
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}				1	µA
I_{LO}	Output Leakage Current	V_{IN} = 0V to V_{CC}, T_{AC} = 0°C to 85°C				1	µA
V_{IL}	Input Low Voltage			-0.5		0.8	V
V_{IH}	Input HIgh Voltage			0.7V_{CC}		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	2.7V < V_{CC} < 3.6V	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage		I_{OH} = -100 µA	V_{CC} - 0.2			V

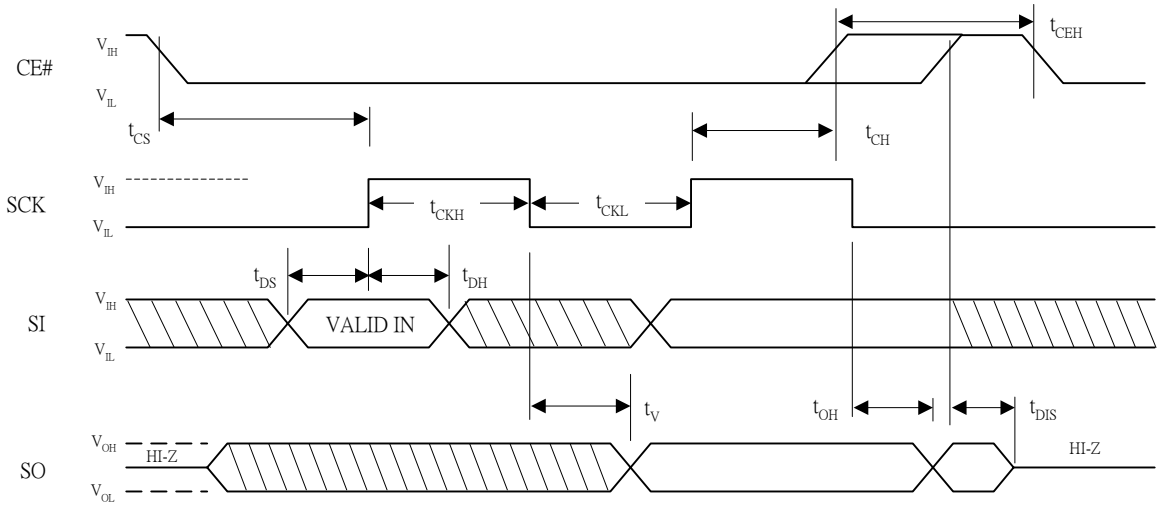
AC CHARACTERISTICS

Applicable over recommended operating range from T_A = -40°C to +105°C, V_{CC} = 2.7 V to 3.6 V
C_L = 1TTL Gate and 10 pF (unless otherwise noted).

Symbol	Parameter	Min	Typ	Max	Units
f_{CT}	Clock Frequency for fast read mode	0		100	MHz
f_C	Clock Frequency for read mode	0		33	MHz
t_{RI}	Input Rise Time			8	ns
t_{FI}	Input Fall Time			8	ns
t_{CKH}	SCK High Time	4			ns
t_{CKL}	SCK Low Time	4			ns
t_{CEH}	CE# High Time	25			ns
t_{CS}	CE# Setup Time	10			ns
t_{CH}	CE# Hold Time	10			ns
t_{DS}	Data In Setup Time	2			ns
t_{DH}	Data in Hold Time	2			ns
t_{HS}	Hold Setup Time	15			ns
t_{HD}	Hold Time	15			ns
t_V	Output Valid			8.5	ns
t_{OH}	Output Hold Time Normal Mode	0			ns
t_{LZ}	Hold to Output Low Z			200	ns
t_{HZ}	Hold to Output High Z			200	ns
t_{DIS}	Output Disable Time			100	ns
t_{EC}	Secter/Block/Chip Erase Time		40	100	ms
t_{PP}	Page Program Time		2	5	ms
t_W	Write Status Register Time		40	100	ms
t_{VCS}	V_{CC} Set-up Time	50			µs

AC CHARACTERISTICS (CONTINUED)

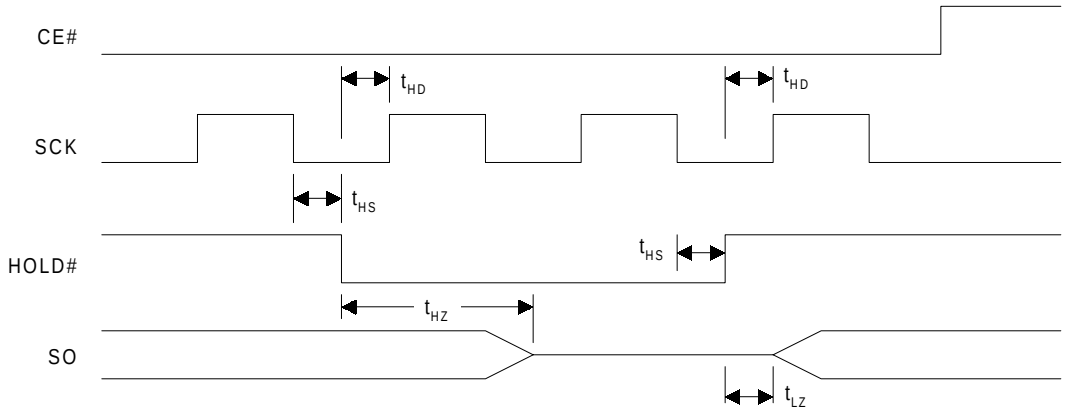
SERIAL INPUT/OUTPUT TIMING(1)



Note: 1. For SPI Mode 0 (0,0)

AC CHARACTERISTICS (CONTINUED)

HOLD TIMING

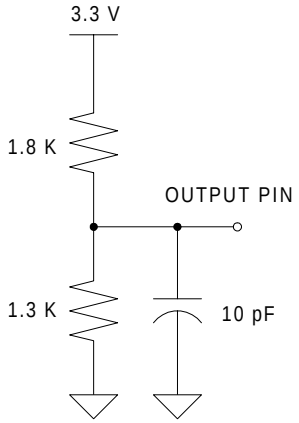


PIN CAPACITANCE (f = 1 MHz, T = 25°C)

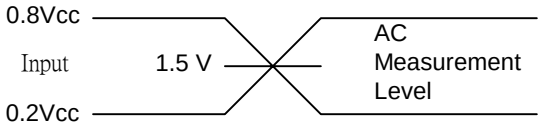
	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: These parameters are characterized but not 100% tested.

OUTPUT TEST LOAD



INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL



Note: 1. Input Pulse Voltage : 0.2Vcc to 0.8Vcc.
2. Input Timing Reference Voltages :
0.3Vcc to 0.7Vcc.
3. Output Timing Reference Voltage : Vcc/2.

POWER-UP AND POWER-DOWN

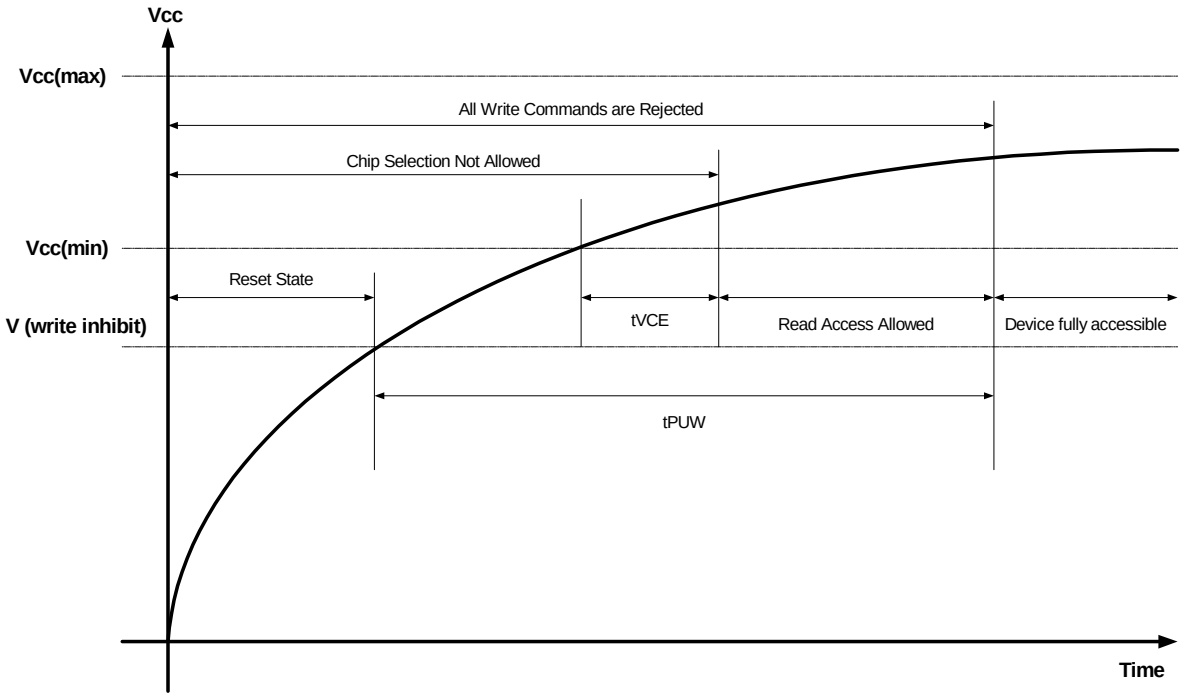
At Power-up and Power-down, the device must not be selected (CE# must follow the voltage applied on Vcc) until Vcc reaches the correct value:
- Vcc(min) at Power-up, and then for a further delay of tVCE
- Vss at Power-down

Usually a simple pull-up resistor on CE# can be used to insure safe and proper Power-up and Power-down.
To avoid data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is included. The logic inside the device is held reset while Vcc is less than the POR threshold value (Vwi) during power up, the device does not respond to any instruction until a time delay of tPUW has elapsed after the moment that Vcc rised above the VWI threshold. However, the correct operation of the device is not guaranteed if, by this time, Vcc is still below Vcc(min). No Write Status Register, Program or Erase instructions should be sent until the later of:
- tPUW after Vcc passed the VWI threshold
- tVCE after Vcc passed the Vcc(min) level

At Power-up, the device is in the following state:
- The device is in the Standby mode
- The Write Enable Latch (WEL) bit is reset

At Power-down, when Vcc drops from the operating voltage, to below the Vwi, all write operations are disabled and the device does not respond to any write instruction.

Power-up Timing



Symbol	Parameter	Min.	Max.	Unit
t_{VCE} *1	Vcc(min) to CE# Low	10		us
t_{PUW} *1	Power-Up time delay to Write instruction	1	10	ms
V_{WI} *1	Write Inhibit Voltage	2.1	2.3	V

Note : *1. These parameters are characterized only.

PROGRAM/ERASE PERFORMANCE

Parameter	Unit	Typ	Max	Remarks
Sector Erase Time	ms	40	100	From writing erase command to erase completion
Block Erase Time	ms	40	100	From writing erase command to erase completion
Chip Erase Time	ms	40	100	From writing erase command to erase completion
Page Programming Time	ms	2	5	From writing program command to program completion

Note: These parameters are characterized and are not 100% tested.

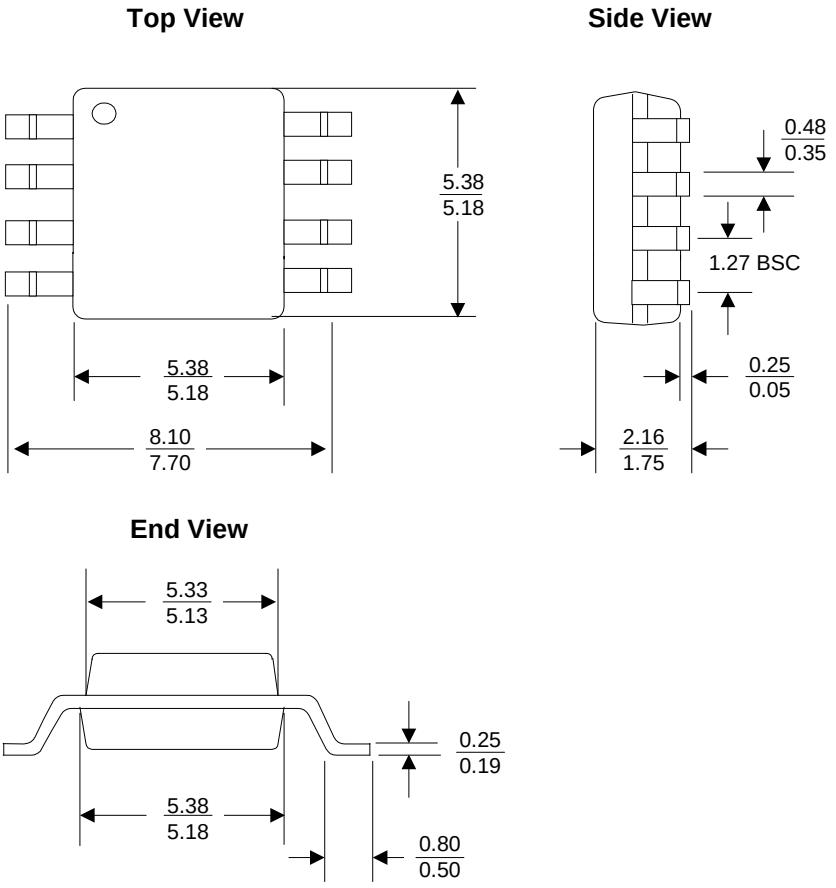
RELIABILITY CHARACTERISTICS

Parameter	Min	Typ	Unit	Test Method
Endurance	100,000		Cycles	JEDEC Standard A117
Data Retention	20		Years	JEDEC Standard A103
ESD - Human Body Model	2,000		Volts	JEDEC Standard A114
ESD - Machine Model	200		Volts	JEDEC Standard A115
Latch-Up	100 + I_{CC1}		mA	JEDEC Standard 78

Note: These parameters are characterized and are not 100% tested.

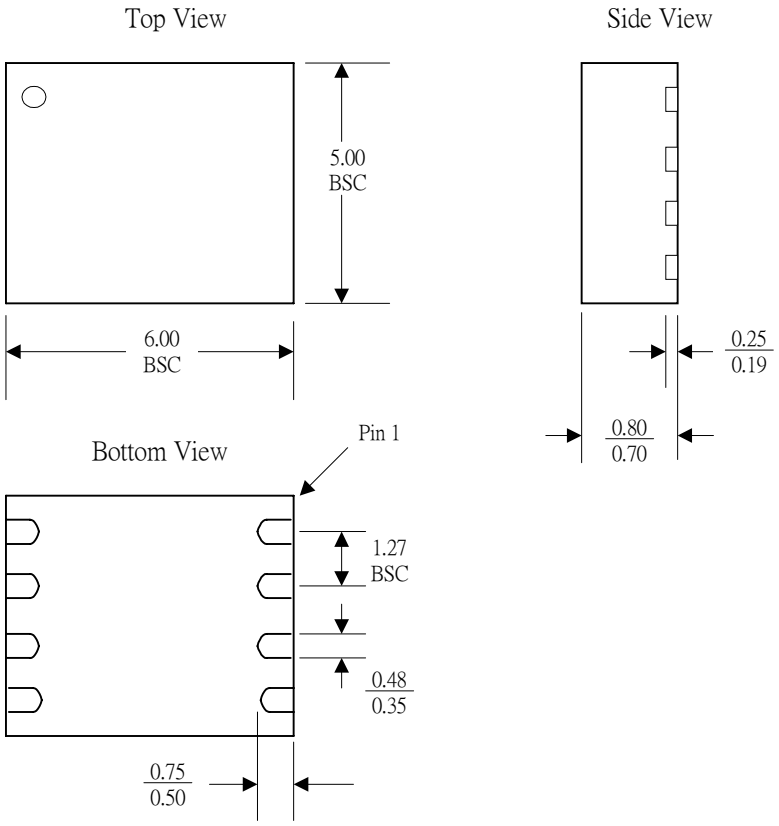
PACKAGE TYPE INFORMATION

8B
8-Pin JEDEC 208mil Broad Small Outline Integrated Circuit (SOIC) Package (measure in millimeters)



PACKAGE TYPE INFORMATION (CONTINUED)

8Q
8-Contact Ulta-Thin Small Outline No-Lead (WSON) Package (measure in millimeters)



REVISION HISTORY

Date	Revision No.	Description of Changes	Page No.
July, 2006	0.0	Advanced Product Specification	All
Octerber, 2006	0.1	Add power on/off sequence Support 60h /20h as chip/sector erase command	All