PM450DV1A120

FLAT-BASE TYPE
INSULATED PACKAGE

PM450DV1A120

FEATURE

a) Adopting new 5th generation Full-Gate CSTBT™ chip

b) The over-temperature protection which detects the chip surface temperature of CSTBT™ is adopted.

c) Error output signal is possible from all each protection upper and lower arm of IPM.

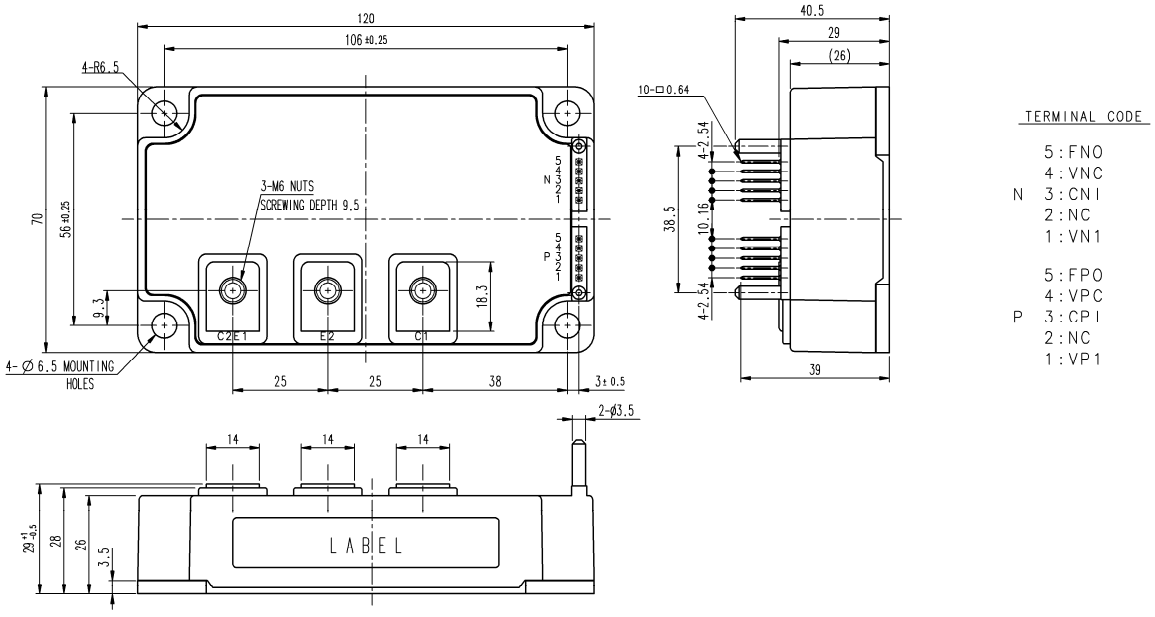
d) Compatible V-series package.

- Monolithic gate drive & protection logic
- Detection, protection & status indication circuits for, short-circuit, over-temperature & under-voltage.

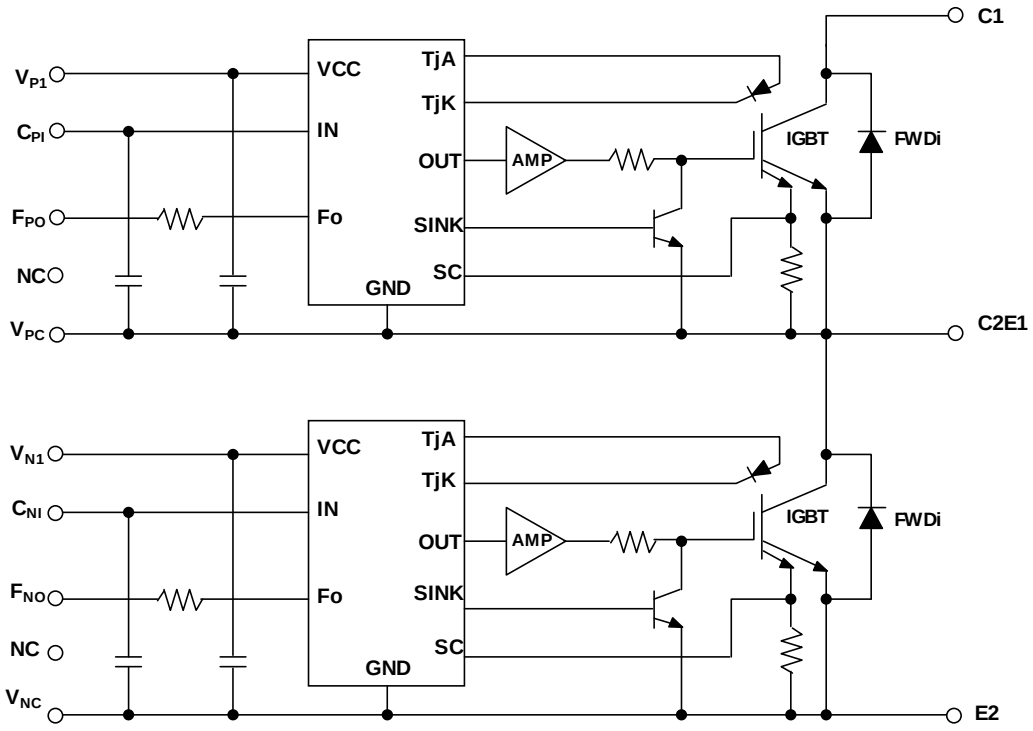
APPLICATION

General purpose inverter, servo drives and other motor controls

PACKAGE OUTLINES **Dimensions in mm**



INTERNAL FUNCTIONS BLOCK DIAGRAM



MAXIMUM RATINGS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Conditions	Ratings	Unit
V_{CES}	Collector-Emitter Voltage	V_D=15V, V_{CIN}=15V	1200	V
I_C	Collector Current	T_C=25°C	450	A
I_{CRM}		Pulse	900	
P_{tot}	Total Power Dissipation	T_C=25°C	2232	W
I_E	Emitter Current	T_C=25°C	450	A
I_{ERM}	(Free wheeling Diode Forward current)	Pulse	900	
T_j	Junction Temperature		-20 ~ +150	°C

*: Tc measurement point is just under the chip.

CONTROL PART

Symbol	Parameter	Conditions	Ratings	Unit
V_D	Supply Voltage	Applied between : V_{P1}-V_{PC}, V_{N1}-V_{NC}	20	V
V_{CIN}	Input Voltage	Applied between : C_{PI}-V_{PC}, C_{NI}-V_{NC}	20	V
V_{FO}	Fault Output Supply Voltage	Applied between : F_{PO}-V_{PC}, F_{NO}-V_{NC}	20	V
I_{FO}	Fault Output Current	Sink current at F_{PO}, F_{NO} terminals	20	mA

TOTAL SYSTEM

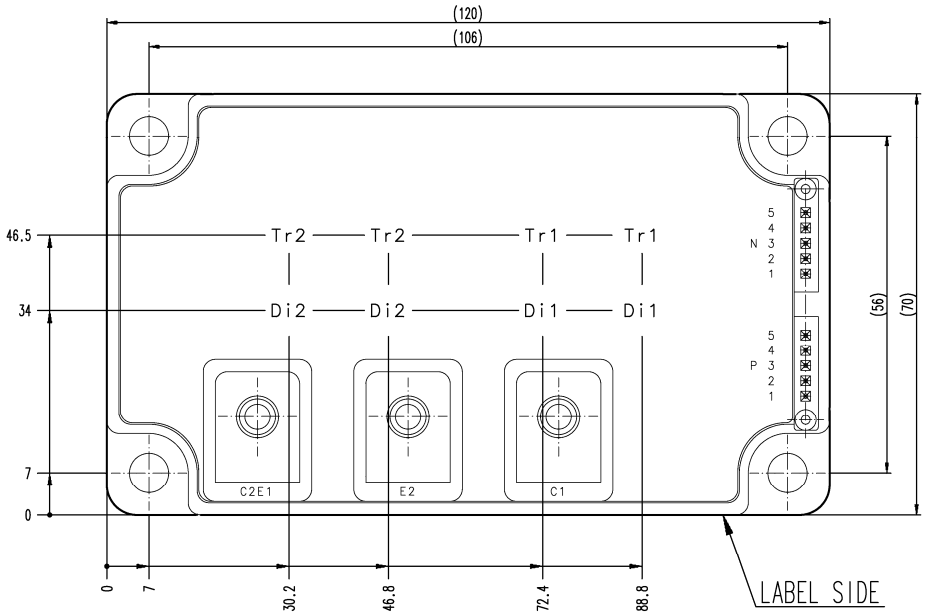
Symbol	Parameter	Conditions	Ratings	Unit
$V_{CC(PROT)}$	Supply Voltage Protected by SC	V_D =13.5V ~ 16.5V Inverter Part, T_j =+125°C Start	800	V
$V_{CC(surge)}$	Supply Voltage (Surge)	Applied between : C1-E2, Surge value	1000	V
T_C	Module case operating temperature		-20 ~ +100	°C
T_{stg}	Storage Temperature		-40 ~ +125	°C
V_{isol}	Isolation Voltage	60Hz, Sinusoidal, Charged part to Base plate, AC 1min, RMS	2500	V

*: T_C measurement point is just under the chip.

THERMAL RESISTANCE

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Thermal Resistance	Junction to case, IGBT (per 1 element) (Note.1)	-	-	0.056	K/W
$R_{th(j-c)D}$		Junction to case, FWDi (per 1 element) (Note.1)	-	-	0.079	
$R_{th(c-s)}$	Contact Thermal Resistance	Case to heat sink, (per 1 module) Thermal grease applied (Note.1)	-	0.018	-	

Note1: If you use this value, $R_{th(s-a)}$ should be measured just under the chips.



ELECTRICAL CHARACTERISTICS (Tj = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{CEsat}	Collector-Emitter Saturation Voltage	V_D=15V, I_C=450A V_{CIN}=0V, Pulsed (Fig. 1)	T_j=25°C	-	1.65	2.15	V
			T_j=125°C	-	1.85	2.35	
V_{EC}	Emitter-Collector Voltage	I_E=450A, V_D=15V, V_{CIN}= 15V (Fig. 2)		-	2.3	3.3	V
t_{on}	Switching Time	V_D=15V, V_{CIN}=0V⟷15V V_{CC}=600V, I_C=450A T_j=125°C Inductive Load (Fig. 3,4)		0.3	0.8	2.0	μs
t_{rr}				-	0.3	0.8	
$t_{c(on)}$				-	0.4	1.0	
t_{off}				-	2.4	3.3	
$t_{c(off)}$				-	0.4	1.2	
I_{CES}	Collector-Emitter Cut-off Current	V_{CE}=V_{CES}, V_D=15V , V_{CIN}=15V (Fig. 5)	T_j=25°C	-	-	1	mA
			T_j=125°C	-	-	10	

CONTROL PART

Symbol	Parameter	Conditions		Limits			Unit
				Min.	Typ.	Max.	
I_D	Circuit Current	V_D=15V, V_{CIN}=15V	V_{P1}-V_{PC}	-	2	4	mA
			V_{N1}-V_{NC}	-	2	4	
$V_{th(ON)}$	Input ON Threshold Voltage	Applied between : C_{PI}-V_{PC}, C_{NI}-V_{NC}		1.2	1.5	1.8	V
$V_{th(OFF)}$	Input OFF Threshold Voltage			1.7	2.0	2.3	
SC	Short Circuit Trip Level	-20≤T_j≤125°C, V_D=15V (Fig. 3, 6)		675	-	-	A
$t_{off(SC)}$	Short Circuit Current Delay Time	V_D=15V (Fig. 3, 6)		-	0.2	-	μs
OT	Over Temperature Protection	Detect Temperature of IGBT chip	Trip level	135	-	-	°C
$OT_{(hys)}$			Hysteresis	-	20	-	
UV	Supply Circuit Under-Voltage Protection	-20≤Tj≤125°C	Trip level	11.5	12.0	12.5	V
UV_r			Reset level	-	12.5	-	
$I_{FO(H)}$	Fault Output Current	V_D=15V, V_{FO}=15V (Note.2)		-	-	0.01	mA
$I_{FO(L)}$				-	10	15	
t_{FO}	Fault Output Pulse Width	V_D=15V (Note.2)		1.0	1.8	-	ms

Note.2: Fault output is given only when the internal SC, OT & UV protections schemes of either upper or lower arm device operate to protect it.

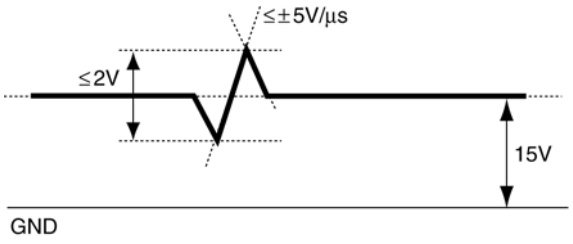
MECHANICAL RATINGS AND CHARACTERISTICS

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
M_s	Mounting Torque	Mounting part screw : M6	3.92	4.90	5.88	N·m
M_t		Main terminal part screw : M6	3.92	4.90	5.88	
m	Weight	-	-	510	-	g

RECOMMENDED CONDITIONS FOR USE

Symbol	Parameter	Conditions	Recommended value	Unit
V_{CC}	Supply Voltage	Applied across C1-E2 terminals	≤ 800	V
V_D	Control Supply Voltage	Applied between : V_{P1}-V_{PC}, V_{N1}-V_{NC} (Note.3)	15.0±1.5	V
$V_{CIN(ON)}$	Input ON Voltage	Applied between : C_{PI}-V_{PC}, C_{NI}-V_{NC}	≤ 0.8	V
$V_{CIN(OFF)}$	Input OFF Voltage		≥ 4.0	
f_{PWM}	PWM Input Frequency	Using Application Circuit of Fig. 8	≤ 20	kHz
t_{dead}	Arm Shoot-through Blocking Time	For IPM's each input signals (Fig. 7)	≥ 3.5	μs

Note.3: With ripple satisfying the following conditions: dv/dt swing ≤ ±5V/μs, Variation ≤ 2V peak to peak



PRECAUTIONS FOR TESTING

1. Before applying any control supply voltage (V_D), the input terminals should be pulled up by resistors, etc. to their corresponding supply voltage and each input signal should be kept off state.
   After this, the specified ON and OFF level setting for each input signal should be done.
2. When performing “SC” tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above V_{CES} rating of the device.
   (These test should not be done by using a curve tracer or its equivalent.)

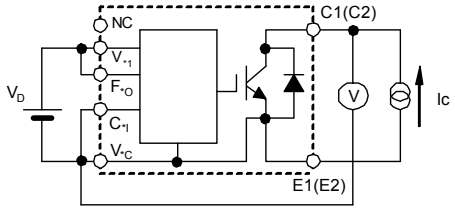


Fig. 1 V_{CEsat} Test

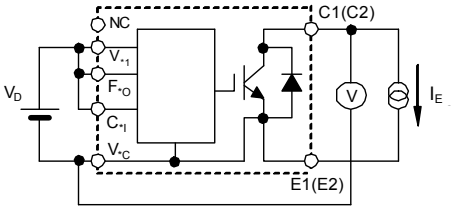


Fig. 2 V_{EC} Test

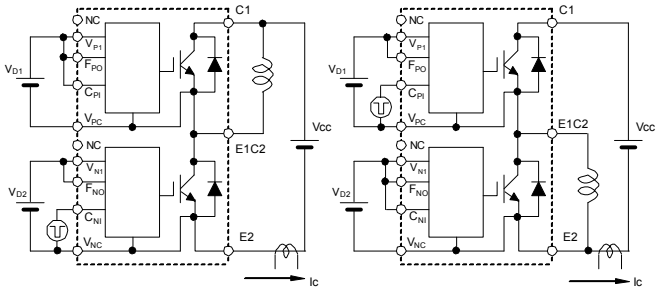


Fig. 3 Switching time and SC test circuit

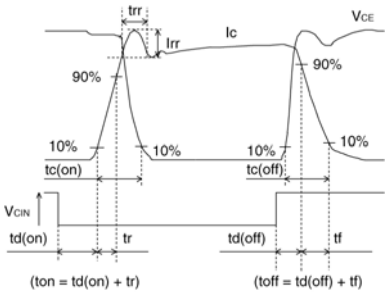


Fig. 4 Switching time test waveform

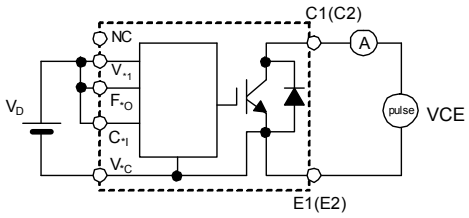


Fig. 5 I_{CES} Test

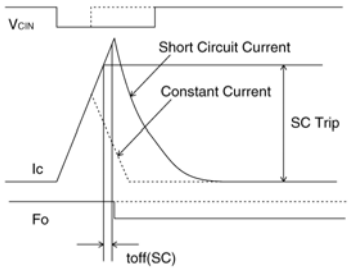
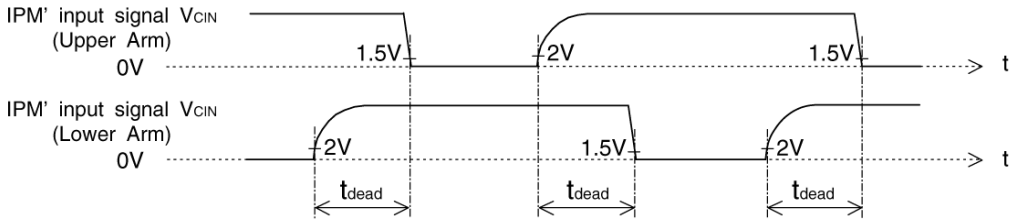


Fig. 6 SC test waveform



1.5V: Input on threshold voltage Vth(on) typical value, 2V: Input off threshold voltage Vth(off) typical value

Fig. 7 Dead time measurement point example

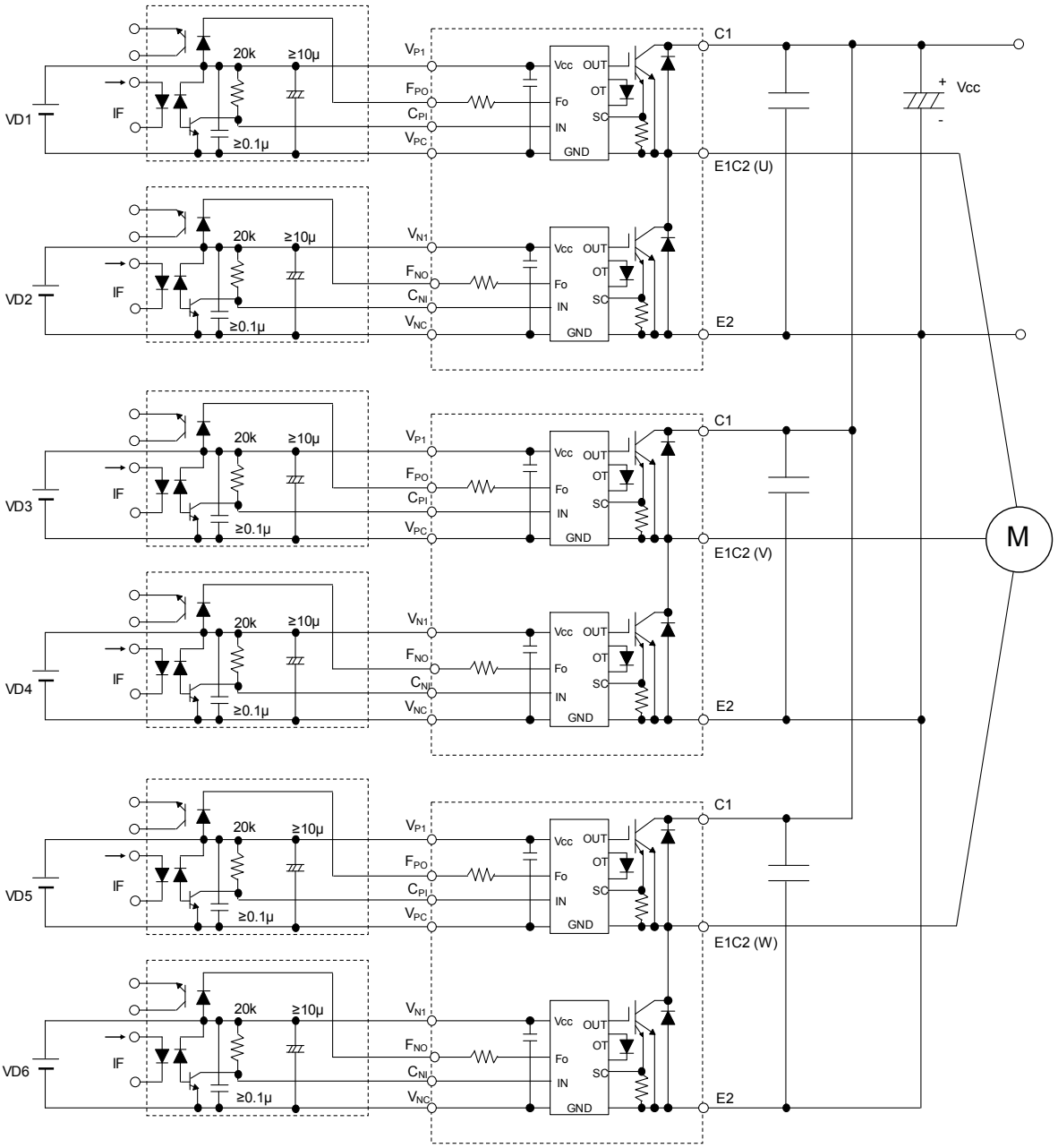


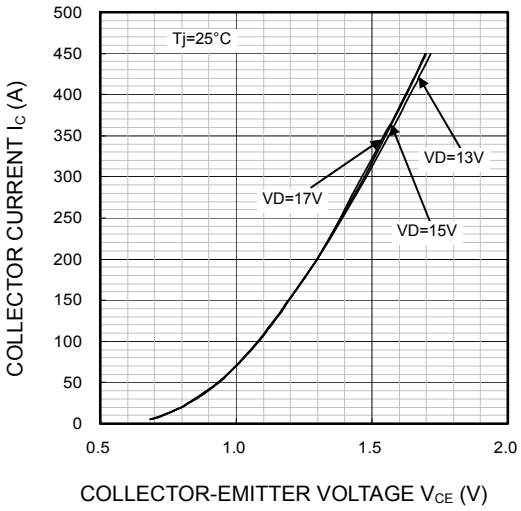
Fig. 8 Application Example Circuit

NOTES FOR STABLE AND SAFE OPERATION ;

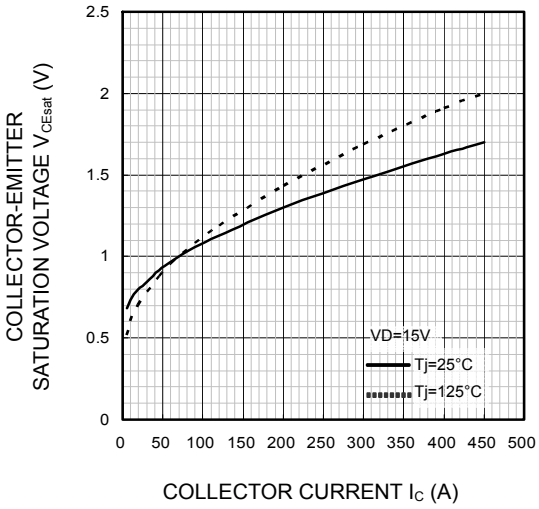
- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Connect low impedance capacitor between the Vcc and GND terminal of each fast switching opto-coupler.
- Fast switching opto-couplers: t_{PLH}, t_{PHL} ≤ 0.8μs, Use High CMR type.
- Slow switching opto-coupler: CTR > 100%
- Use 6 isolated control power supplies (V_D). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between C1 and E2 terminal.

PERFORMANCE CURVES

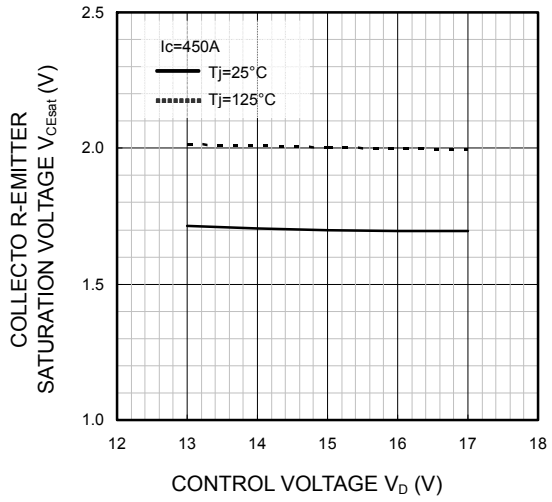
OUTPUT CHARACTERISTICS (TYPICAL)



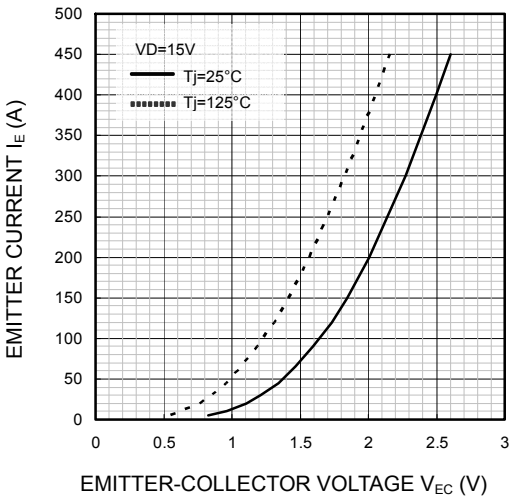
COLLECTOR-EMITTER SATURATION VOLTAGE (VS. Ic) CHARACTERISTICS (TYPICAL)



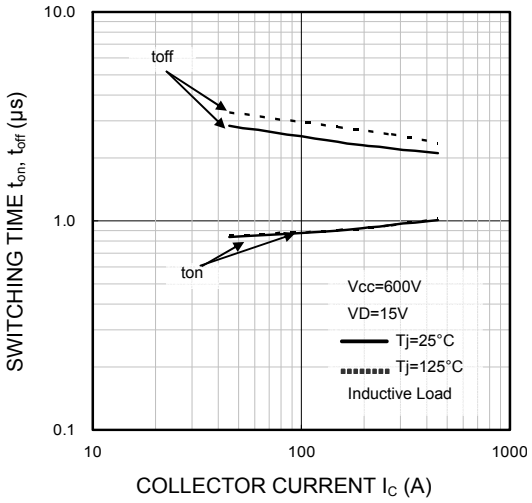
COLLECTOR-EMITTER SATURATION VOLTAGE (VS. V_D) CHARACTERISTICS (TYPICAL)



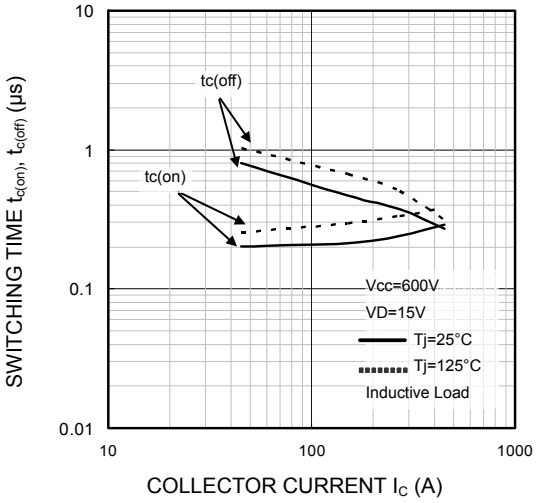
FREE WHEELING DIODE FORWARD CHARACTERISTICS (TYPICAL)



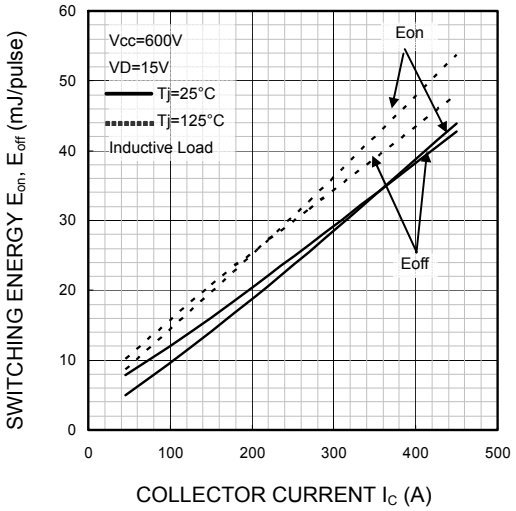
SWITCHING TIME (t_{on}, t_{off}) CHARACTERISTICS (TYPICAL)



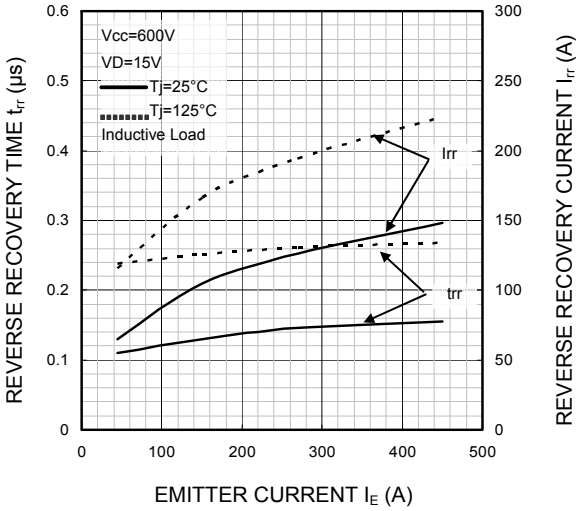
SWITCHING TIME ($t_{c(on)}$, $t_{c(off)}$) CHARACTERISTICS (TYPICAL)



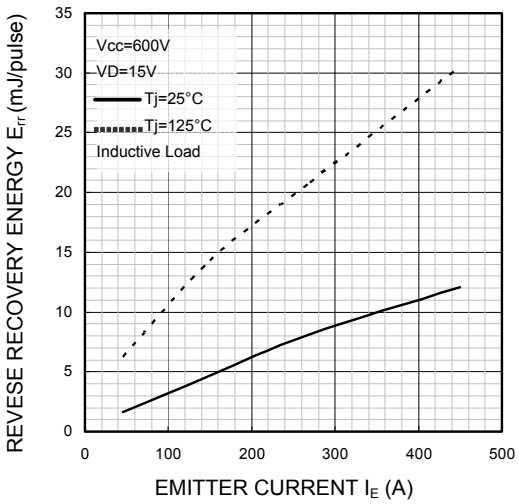
SWITCHING ENERGY CHARACTERISTICS (TYPICAL)



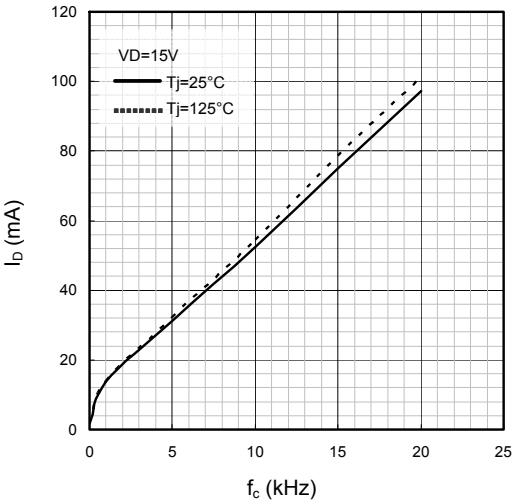
FREE WHEELING DIODE REVERSE RECOVERY CHARACTERISTICS (TYPICAL)



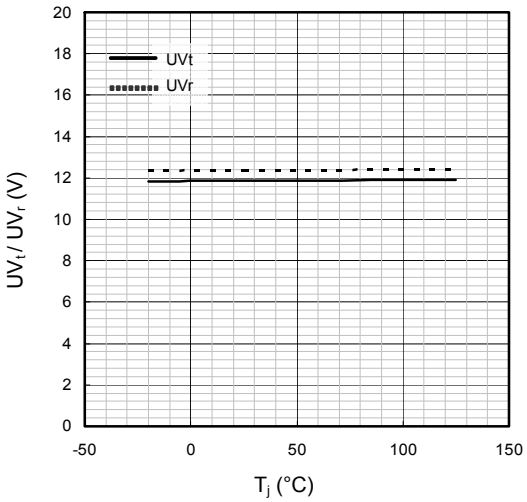
**FREE WHEELING DIODE
REVERSE RECOVERY ENERGY CHARACTERISTICS
(TYPICAL)**



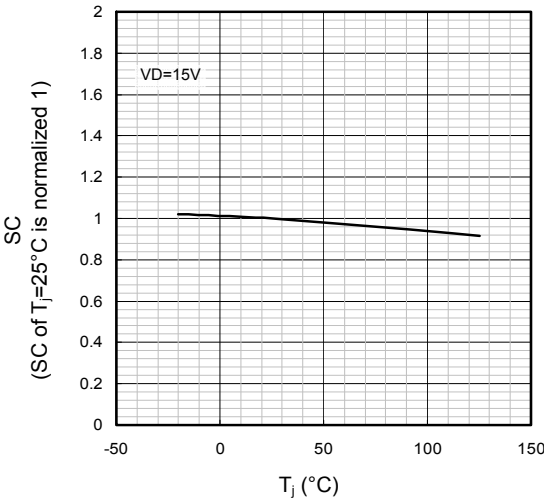
**I_D VS. f_c CHARACTERISTICS
(TYPICAL)**



**UV TRIP LEVEL VS. T_j CHARACTERISTICS
(TYPICAL)**



**SC TRIP LEVEL VS. T_j CHARACTERISTICS
(TYPICAL)**



TRANSIENT THERMAL IMPEDANCE CHARACTERISTICS