PM5348

S/UNI-155-DUAL™

S/UNI-155-DUAL

DUAL SATURN USER NETWORK INTERFACE 155.52 & 51.84 MBIT/S

DATA SHEET

ISSUE 7: JUNE 1998

PROPRIETARY AND CONFIDENTIAL TO PMC-SIERRA, INC., AND FOR ITS CUSTOMERS' INTERNAL USE

REVISION HISTORY

Issue No.	Issue Date	Details of Change
7	June 1997	Data Sheet Reformatted — No Change in Technical Content. Generated R7 data sheet from PMC-950716, R7
6	Feb 1997	Eng doc P6 revised

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1 FEATURES

- Single chip dual ATM User-Network Interface operating at 155.52 and 51.84 Mbit/s. Also capable of operating at ATM Forum mid-range PHY subrates of 25.92 and 12.96 Mbit/s.
- Provides essential hardware and software compatibility with industry-standard PM5346 S/UNI-LITE device.
- Implements the ATM Forum User Network Interface Specification and the ATM physical layer for Broadband ISDN according to CCITT Recommendation I.432.
- Processes two duplex 155.52 Mbit/s STS-3c/STM-1 or 51.84 Mbit/s STS-1 data streams with on-chip clock and data recovery and clock synthesis.
- Provides Saturn Compliant Interface - PHYsical layer (SCI-PHY™) FIFO buffers in both transmit and receive paths with parity support. Compatible with ATM Forum Utopia Level 2 specification. The FIFOs may be independently bypassed.
- Inserts and extracts the generic flow control (GFC) bits via a simple serial interface and provides a transmit XOFF function to allow for local flow control.
- Supports 8-bit and 16-bit multi-PHY modes and a direct dual 8-bit mode.
- Provides a generic 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Provides a 4-bit output port for external alarms and control.
- Provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan test purposes.
- Low power, +5 Volt, CMOS technology.
- 160 pin high performance plastic quad flat pack (MQFP) 28 mm x 28 mm package.

Each receiver section:

- Provides a serial interface at 155.52 or 51.84 Mbit/s

- Recovers the clock and data; frames to the recovered data stream; descrambles the received data; interprets the received payload pointer (H1, H2); and extracts the STS-3c or STS-1 synchronous payload envelope (VC4) and path overhead.

- Extracts ATM cells from the synchronous payload envelope using ATM cell delineation and provides optional ATM cell payload descrambling, header check sequence (HCS) error detection and error correction, and idle/unassigned cell filtering.

- Provides a synchronous 8-bit or 16-bit wide, four cell FIFO buffer.

- Detects loss of signal (LOS), out of frame (OOF), loss of frame (LOF), line alarm indication signal (LAIS), line remote defect indication (LRDI), loss of pointer (LOP), path alarm indication signal (PAIS), loss of cell delineation (LCD) and path remote defect indication (PRDI).

    - Detects signal degrade (SD) or signal fail (SF) threshold crossing alarms based on received B2 errors.

- Counts received section BIP-8 (B1) errors, received line BIP-8/24 (B2) errors, line far end block errors (M0 or M1), received path BIP-8 (B3) errors and path far end block errors (G1).

- Filters and captures the automatic protection switch channel (K1, K2) bytes in readable registers and detects APS byte failure.

- Captures the synchronization status (S1) byte in a readable register.

- Counts received cells with uncorrectable HCS errors and received cells with correctable HCS errors.

- Counts the total number of valid received cells (i.e. cells with an error-free HCS and cells with a correctable HCS error).

Each transmitter section:

- Provides a synchronous 8-bit or 16-bit wide, four cell FIFO buffer.

- Provides idle/unassigned cell insertion, HCS generation/insertion, and ATM cell payload scrambling; inserts ATM cells into the transmitted STS-3c (STM-1) or STS-1 synchronous payload envelope using H4 framing.

- Generates the transmit payload pointer (H1, H2) and inserts the path overhead; scrambles the transmitted STS-3c (STM-1) or STS-1 stream and inserts framing bytes (A1, A2).

- Synthesizes the 155.52 MHz or 51.84 MHz transmit clock from a one-eighth frequency reference.

- Provides a serial interface at 155.52 or 51.84 Mbit/s

- Inserts path alarm indication signal (PAIS), path remote defect indication (PRDI), line alarm indication signal (LAIS) and line remote defect indication (LRDI).

- Inserts path BIP-8 codes (B3), path far end block error (G1) indications, line BIP-8/24 codes (B2), line far end block error (M0 or M1) indications, section BIP-8 codes (B1) to allow performance monitoring at the far end.

- Optionally inserts register programmable APS (K1, K2) and synchronization status (S1) bytes.

- Allows forced insertion of all zeros data (after scrambling) or corruption of framing byte or section, line, or path BIP-8 codes for diagnostic purposes.

2 APPLICATIONS

- Workstations and Personal Computers
- Switches and Hubs
- Routers
- SONET or SDH ATM Interfaces

3 REFERENCES

- CCITT Recommendation G.709, "Synchronous Multiplexing Structure," 1990.
- CCITT Recommendation I.432, "B-ISDN User-Network Interface - Physical Interface Specification," June 1990.
- Bell Communications Research, "SONET Transport Systems: Common Generic Criteria, GR-253-CORE," Issue 1, December 1994.
- ATM Forum, "ATM User-Network Interface Specification," V3.1, September 1994.
- T1.105, "American National Standard for Telecommunications - Digital Hierarchy - Optical Interface Rates and Formats Specifications (SONET)," 1991
- IEEE 1149.1, "Standard Test Access Port and Boundary Scan Architecture," May 1990.

4 APPLICATION EXAMPLES

The PM5348 S/UNI-DUAL is typically used to implement the core of an ATM User Network Interface by which an ATM terminal is linked to an ATM switching system using SONET/SDH compatible transport. The S/UNI-DUAL is intended as a cost effective replacement for two PM5346 S/UNI-LITEs.

The S/UNI-DUAL finds application at either end of terminal-to-switch links or switch-to-switch links, typically in private network (LAN) situations. The S/UNI-DUAL may be loop timed internally (the recovered clock is used in the transmit direction) or source timed (separate transmit and receive clocks using one common reference clock).

In these applications, the S/UNI-DUAL interfaces on its line side with an optical transceiver. The drop side interfaces directly with ATM layer processors or an ATM Multi-PHY controller. The initial configuration and ongoing control and monitoring of the S/UNI-DUAL is provided via a generic microprocessor interface. The applications are shown in Figure 1 and Figure 2.

Figure 1 - Split-Bus 8-bit Direct-PHY ATM Switch Interface

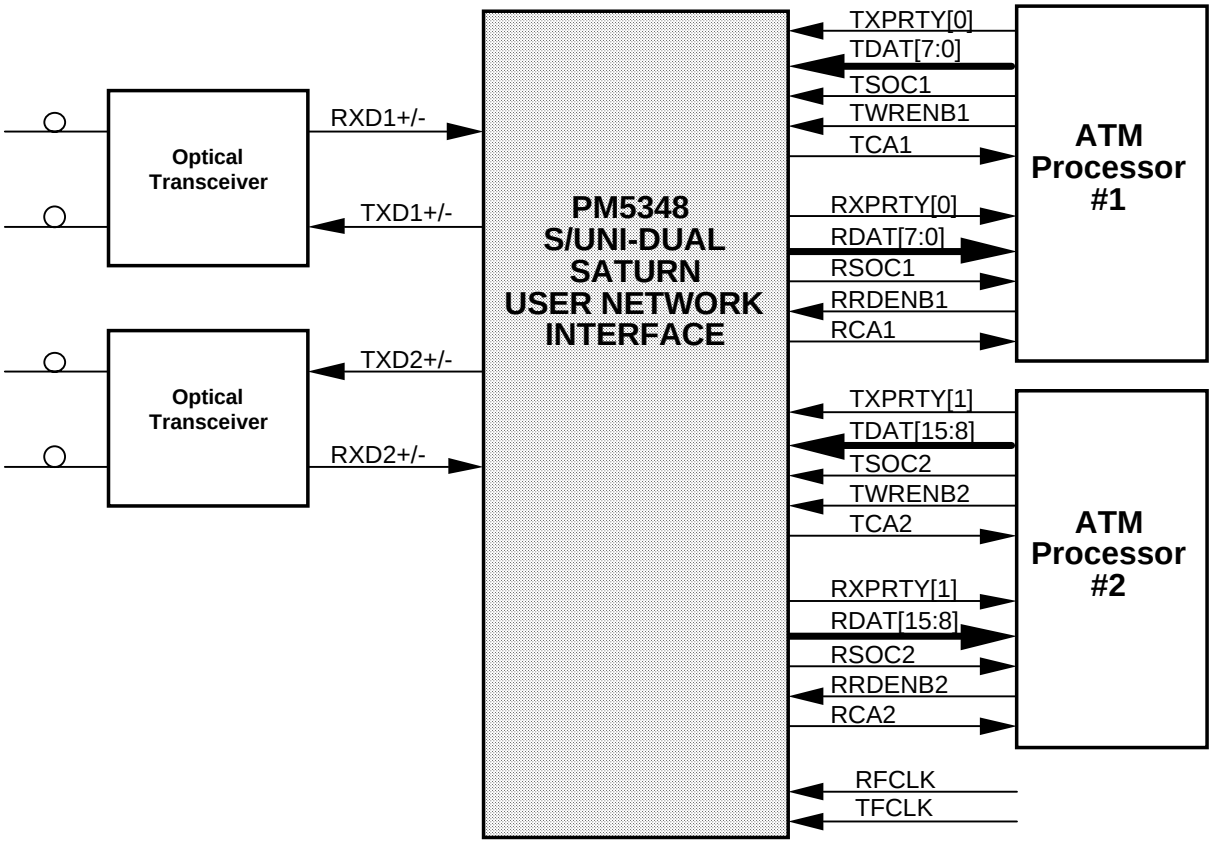
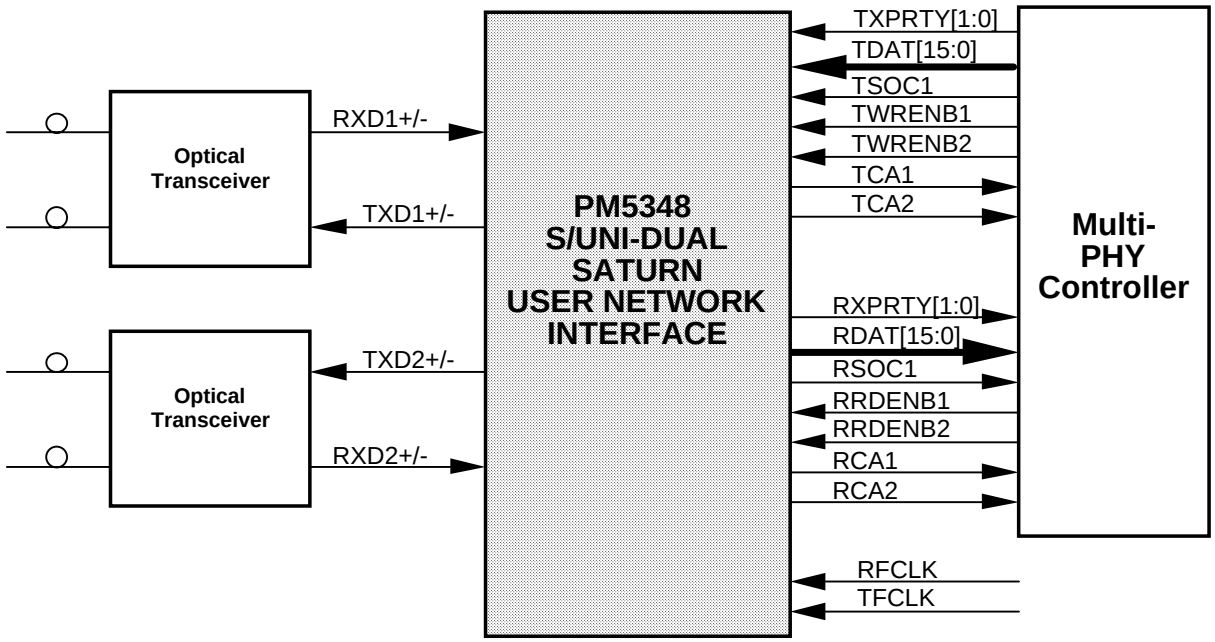
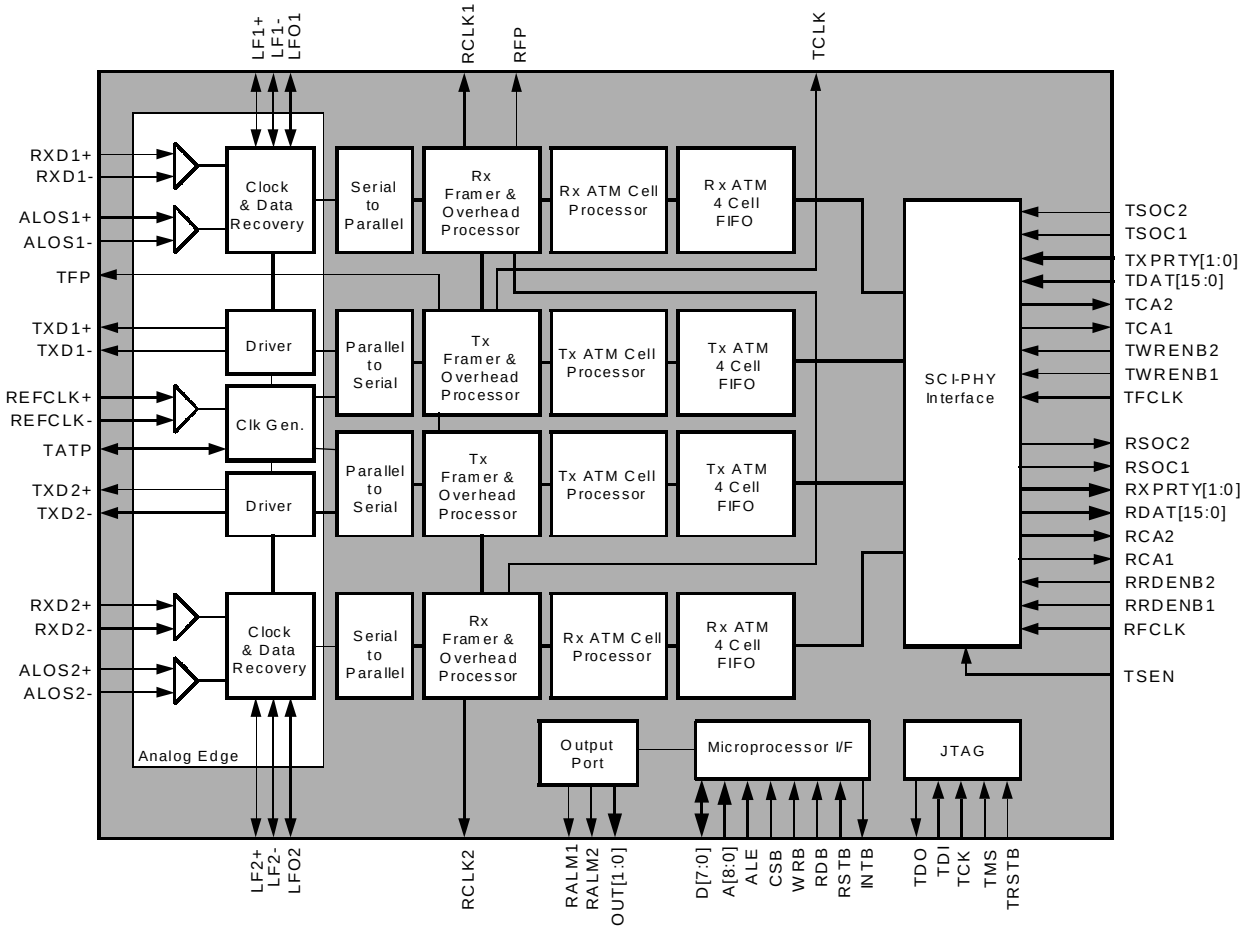


Figure 2 - Direct 8-bit or 16-bit Multi-PHY ATM Switch Interface



5 BLOCK DIAGRAM



6 DESCRIPTION

The PM5348 Dual SATURN User Network Interface (S/UNI-DUAL) is a monolithic integrated circuit that implements SONET/SDH processing and ATM mapping functions for two 155 Mbit/s or 51Mbit/s ATM User Network Interfaces. It is compliant with SONET and SDH requirements and ATM Forum User Network Interface specifications. The S/UNI-DUAL is software configurable, allowing feature selection without changes to external wiring.

The S/UNI-DUAL receives two SONET/SDH channels via separate bit serial interfaces, recovers their corresponding clock and data, and processes section, line and path overhead for each channel. Each channel performs framing (A1, A2), descrambling, detects alarm conditions, and monitors section, line, and path bit interleaved parity (B1, B2, B3), accumulating error counts at each level for performance monitoring purposes. Line and path far end block error indications (M0 or M1, G1) are also accumulated for each channel. Each channel of the S/UNI-DUAL interprets the received payload pointers (H1, H2) and extracts the synchronous payload envelope which carries the received ATM cell payload.

Each channel of the S/UNI-DUAL frames to the ATM payload using cell delineation. HCS error correction is provided. Idle/unassigned cells may be dropped according to a programmable filter. Cells are also dropped upon detection of an uncorrectable header check sequence error. The ATM cell payloads are descrambled. Legitimate ATM cells are written to a four cell FIFO buffer.

The ATM cells are read from each channel's FIFO via a synchronous interface with cell-based handshake using either a split 8 bit wide datapath, a direct 8 bit wide datapath or a direct 16 bit wide datapath. Counts of received ATM cell headers that are errored and uncorrectable, those that are errored and correctable, and all passed cells are accumulated independently for each channel's performance monitoring purposes.

The S/UNI-DUAL transmits two SONET/SDH channels via separate bit serial interfaces and formats section, line, and path overhead for each channel. Each channel performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and creates section, line, and path bit interleaved parity (B1, B2, B3) as required to allow performance monitoring at the far end. Line and path far end block error indications (M0 or M1, G1) are also inserted.

Each channel of the S/UNI-DUAL generates the payload pointer (H1, H2) and inserts the synchronous payload envelope which carries the ATM cell payload. It supports the insertion of a variety of errors into the transmit stream, such as

framing pattern errors, bit interleaved parity errors, and illegal pointers, which are useful for system diagnostics.

ATM cells are written to each channel's internally programmable-length 4-cell FIFO via a synchronous interface using either a split 8 bit wide datapath, a direct 8 bit wide datapath, or a direct 16 bit wide datapath. Idle/unassigned cells are automatically inserted when the internal FIFO contains less than one cell.

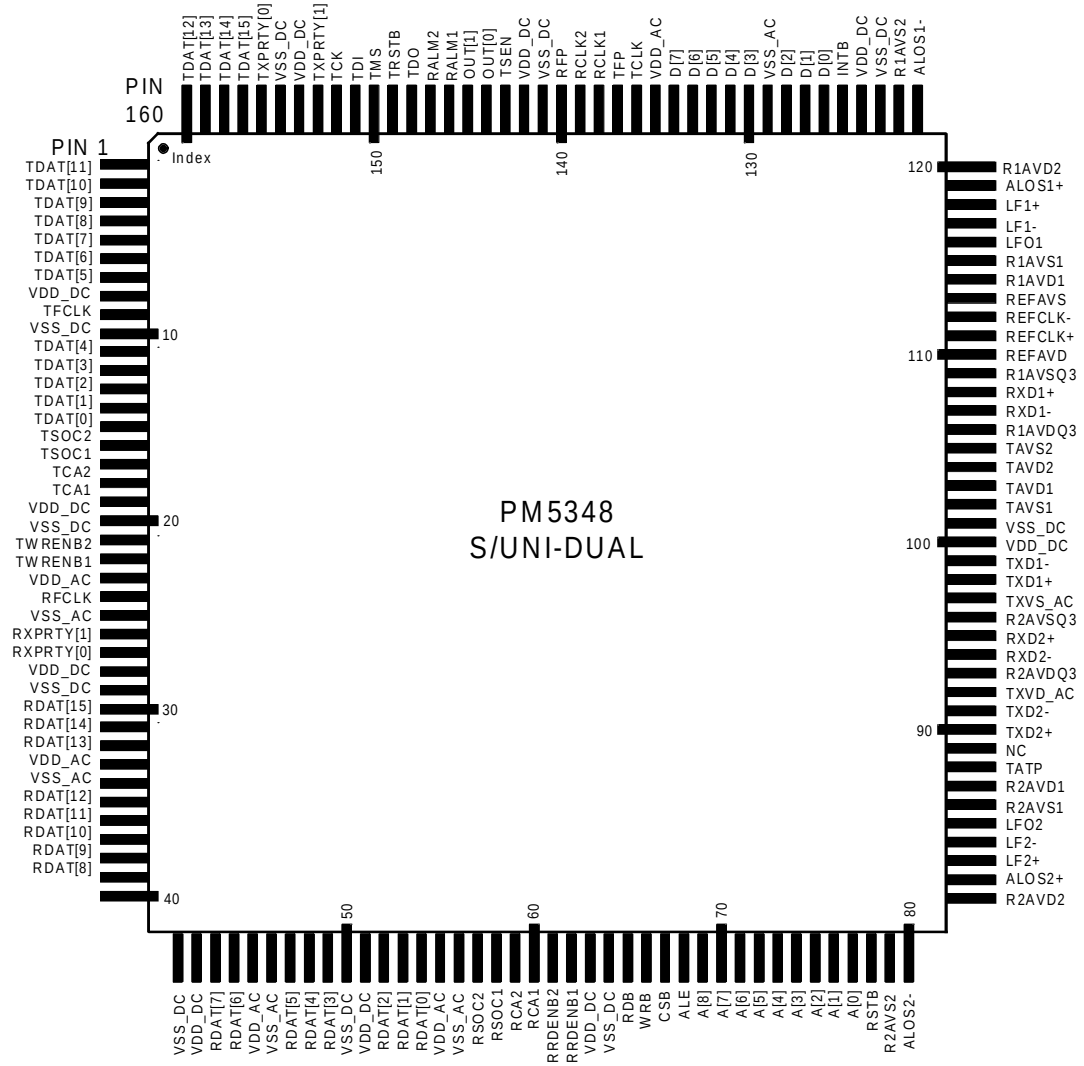
Each channel of the S/UNI-DUAL generates the header check sequence and scrambles the payload of the ATM cells. Payload scrambling can be disabled.

No line rate clocks are required directly by the S/UNI-DUAL as it synthesizes the transmit clock and recovers the receive clocks using a single 19.44 MHz or 6.48 MHz reference clock.

The S/UNI-DUAL is configured, controlled and monitored via a generic 8-bit microprocessor bus interface. It is implemented in low power, +5 Volt CMOS technology. It has TTL and pseudo-ECL (PECL) compatible inputs and TTL/CMOS compatible outputs and is packaged in a 160 pin MQFP package.

7 PIN DIAGRAM

The S/UNI-DUAL is packaged in a 160 pin MQFP package having a body size of 28mm by 28mm and a pin pitch of 0.65 mm.



8 PIN DESCRIPTION

Pin Name	Type	Pin No.	Function
RXD1+ RXD1-	PECL Input	108 107	The receive differential data inputs (RXD1+, RXD1-) contain the NRZ bit serial receive stream for channel #1. The receive clock for channel #1 is recovered from the RXD1+/- bit stream. RXD1+/- must be connected to a differential data source, single ended operation is not supported for these inputs. See note 11.
RXD2+ RXD2-	PECL Input	95 94	The receive differential data inputs (RXD2+, RXD2-) contain the NRZ bit serial receive stream for channel #2. The receive clock for channel #2 is recovered from the RXD2+/- bit stream. RXD2+/- must be connected to a differential data source, single ended operation is not supported for these inputs. See note 11.
REFCLK+ REFCLK-	PECL Input	111 112	The differential reference clock inputs (REFCLK+, REFCLK-) contain a jitter-free 19.44 MHz or 6.48 MHz reference clock. See note 11.
ALOS1+ ALOS1-	PECL Input	119 121	The channel #1 analog loss of signal (ALOS1+/-) differential inputs are used to indicate a loss of receive signal power. When ALOS1+/- is asserted, the data on the channel #1 receive data (RXD1+/-) pins is forced to all zeros and the phase locked loop switches to the reference clock (REFCLK+/-) to keep the recovered clock in range. These inputs must be DC coupled. See note 11.RATP may be bonded to pin 119 or may be accessed accessable during wafer probe. Channel #1 receive analog test point (RATP1) is provided for production test purposes. RATP1 is only available while the device is in Analog Test Mode.

Pin Name	Type	Pin No.	Function
ALOS2+ ALOS2-	PECL Input	82 80	The channel #2 analog loss of signal (ALOS2+/-) differential inputs are used to indicate a loss of receive signal power. When ALOS2+/- is asserted, the data on the channel #2 receive data (RXD2+/-) pins is forced to all zeros and the phase locked loop switches to the reference clock (REFCLK+/-) to keep the recovered clock in range. These inputs must be DC coupled. See note 11. RATP may be bonded to pin 82 or may be accessed accessable during wafer probe.Channel #2 receive analog test point (RATP2) is provided for production test purposes. RATP2 is only available while the device is in Analog Test Mode.
RCLK1	Output	138	The receive clock (RCLK1) output provides a timing reference for S/UNI-DUAL channel #1 receive outputs. RCLK1 is a divide by eight of the recovered clock. RALM1 is updated on the rising edge of RCLK1.
RCLK2	Output	139	The receive clock (RCLK2) output provides a timing reference for S/UNI-DUAL channel #2 receive outputs. RCLK2 is a divide by eight of the recovered clock. RALM2 is updated on the rising edge of RCLK2.

Pin Name	Type	Pin No.	Function
RALM1	Output	146	The channel #1 receive alarm (RALM1) output indicates the state of the receive framing. RALM1 is low if no receive alarms are active. RALM1 is high if line AIS, path AIS, loss of signal (LOS), loss of frame (LOF), loss of pointer (LOP) or loss of cell delineation (LCD) is detected in channel #1. RALM1 is updated on the rising edge of RCLK1. RALM1 can be configured to control the operation of external devices. In this configuration, the signal levels on RALM1 correspond to register settings.
RALM2	Output	147	The channel #2 receive alarm (RALM2) output indicates the state of the receive framing. RALM2 is low if no receive alarms are active. RALM2 is high if line AIS, path AIS, loss of signal (LOS), loss of frame (LOF), loss of pointer (LOP) or loss of cell delineation (LCD) is detected in channel #2. RALM2 is updated on the rising edge of RCLK2. RALM2 can be configured to control the operation of external devices. In this configuration, the signal levels on RALM2 correspond to register settings.
OUT[1] OUT[0]	Output	145 144	The parallel output port (OUT[1:0]) output is used to control the operation of external devices. The signal levels on the parallel output port correspond to register settings.

Pin Name	Type	Pin No.	Function
RFP	Output	140	The receive frame pulse (RFP) output is a selectable 8 kHz signal derived from either the channel #1 or the channel #2 receive line clock. RFP pulses high for one corresponding RCLK cycle every 2430 RCLK cycles for STS-3c (STM-1) TC mode or every 810 RCLK cycles for STS-1 TC mode. RFP is updated on the rising edge of the corresponding RCLK.
TXD1+ TXD1-	Output	98 99	The transmit differential data outputs (TXD1+, TXD1-) contain NRZ encoded data for channel #1.
TXD2+ TXD2-	Output	90 91	The transmit differential data outputs (TXD2+, TXD2-) contain NRZ encoded data for channel #2.
TFP	Output	137	The active high transmit framing pulse (TFP) output is an 8 kHz timing marker for the transmitters. Upon reset the TFP output is held in high impedance. TFP is enabled as an output using the TFP_TS bit of register 8. When enabled, TFP pulses high for one TCLK cycle every 2430 TCLK cycles for STS-3c (STM-1) TC mode or every 810 TCLK cycles for STS-1 TC mode. See the Transmit Section Overhead Processor section of the Functional Description for more details on this output. TFP is updated on the rising edge of TCLK.

Pin Name	Type	Pin No.	Function
TSEN	Input	143	The tristate enable (TSEN) input selects the configuration of the receive datapath (RDAT[15:0], RXPRTY[1:0], RSOC1 and RSOC2). When TSEN is tied high, the receive datapath operates as a tristate bus controlled by RRDENB2 and RRDENB1. When TSEN is tied low, the receive datapath is always driven, regardless of the state of RRDENB2 or RRDENB1. TSEN has an integral pull up resistor. See note 12.
RFCLK	Input	25	The receive read clock (RFCLK) is used to read ATM cells from the receive FIFOs. RFCLK must cycle at a 50 MHz or lower instantaneous rate, but at a high enough rate to avoid FIFO overflow. RRDENB1 and RRDENB2 are sampled using the rising edge of RFCLK. RSOC1, RSOC2, RDAT[15:0], RXPRTY[1:0], RCA1 and RCA2 are updated on the rising edge of RFCLK. See note 12.
RRDENB1	Input	62	The channel #1 active low receive read enable input (RRDENB1) is used to initiate reads from the channel #1 receive FIFO. RRDENB1 is sampled using the rising edge of RFCLK. RRDENB1 must operate in conjunction with RFCLK to access the FIFO at a high enough instantaneous rate as to avoid FIFO overflows. The ATM layer device may deassert RRDENB1 at anytime it is unable to accept another byte. See note 12.

Pin Name	Type	Pin No.	Function
RRDENB2	Input	61	The channel #2 active low receive read enable input (RRDENB2) is used to initiate reads from the channel #2 receive FIFO. RRDENB2 is sampled using the rising edge of RFCLK. RRDENB2 must operate in conjunction with RFCLK to access the FIFO at a high enough instantaneous rate as to avoid FIFO overflows. The ATM layer device may deassert RRDENB2 at anytime it is unable to accept another byte. See note 12.
RDAT[0]	Tristate Output	54	The receive cell data (RDAT[15:0]) bus carries the ATM cell octets that are read from the receive FIFOs. RDAT[15:0] is updated on the rising edge of RFCLK and is tristated when not valid, if the TSEN input is high. The RDAT[15:0] bus is always driven when TSEN is low, regardless of the level of RRDENB1 or RRDENB2. See note 12.
RDAT[1]		53	
RDAT[2]		52	
RDAT[3]		49	
RDAT[4]		48	
RDAT[5]		47	
RDAT[6]		44	
RDAT[7]		43	
RDAT[8]		40	
RDAT[9]		39	
RDAT[10]		38	
RDAT[11]		37	
RDAT[12]		36	
RDAT[13]		33	
RDAT[14]		32	
RDAT[15]		31	

Pin Name	Type	Pin No.	Function
RXPRTY[1] RXPRTY[0]	Tristate Output	27 28	The receive parity (RXPRTY[1:0]) signal indicates the parity of the RDAT[15:0] bus. Odd or even parity selection can be made using a register. RXPRTY[1:0] is updated on the rising edge of RFCLK and is tristated when not valid, if the TSEN input is high. RXPRTY[1:0] is always driven when TSEN is low, regardless of the level of RRDENB1 or RRDENB2. See note 12. See the Functional Timing and the RACP Register Description sections for more details regarding this output.
RSOC1	Tristate Output	58	The channel #1 receive start of cell (RSOC1) signal marks the start of cell on the receive cell data bus. When RSOC1 is high, the first octet of the cell is present on the receive cell data stream. RSOC1 is updated on the rising edge of RFCLK and is tristated when not valid, if the TSEN input is high. RSOC1 is always driven when TSEN is low, regardless of the level of RRDENB1 or RRDENB2. See note 12.
RSOC2	Tristate Output	57	The channel #2 receive start of cell (RSOC2) signal marks the start of cell on the channel #2 receive cell data bus (in Split-Bus mode). When RSOC2 is high, the first octet of the cell is present on the receive cell data stream. RSOC2 is updated on the rising edge of RFCLK and is tristated when not valid, if the TSEN input is high. RSOC2 is always driven when TSEN is low, regardless of the level of RRDENB2. See note 12.

Pin Name	Type	Pin No.	Function
RCA1	Output	60	The channel #1 receive cell available (RCA1) signal indicates when a cell is available in the channel #1 receive FIFO. When RCA1 is sampled asserted, it indicates that the channel #1 receive FIFO has at least one cell available to be read. When RCA1 is sampled deasserted, the channel #1 receive FIFO contains only four words or is empty (as selected in the RACP Configuration register). The active polarity of RCA1 defaults to active high and can be programmed in the S/UNI-DUAL Configuration register. RCA1 is updated on the rising edge of RFCLK. See note 12.
RCA2	Output	59	The channel #2 receive cell available (RCA2) signal indicates when a cell is available in the channel #2 receive FIFO. When RCA2 is sampled asserted, it indicates that the channel #2 receive FIFO has at least one cell available to be read. When RCA2 is sampled deasserted, the channel #2 receive FIFO contains only four words or is empty (as selected in the RACP Configuration register). The active polarity of RCA2 defaults to active high and can be programmed in the S/UNI-DUAL Configuration register. RCA2 is updated on the rising edge of RFCLK. See note 12.

Pin Name	Type	Pin No.	Function
TCLK	Output	136	The transmit byte clock (TCLK) is either a 19.44 MHz or a 6.48 MHz clock derived by dividing the transmit line rate by eight. The S/UNI Dual produces two independent transmit data streams which may have slightly different data rates depend on the operation mode. The transmit stream which TCLK is derived from is dictated by the configuration of the device. See the Transmit Section Overhead Processor section of the Functional Description for more details on this output.
TFCLK	Input	9	The transmit write clock (TFCLK) is used to write ATM cells to either four cell transmit FIFOs. TFCLK cycles at a 50 MHz or lower instantaneous rate. A complete 53 octet cell must be written to the FIFO before being inserted in the synchronous payload envelope (SPE). Idle/unassigned cells are inserted when a complete cell is not available. TDAT[15:0], TXPRTY[1:0], TWRENB1, TWRENB2, TSOC1 and TSOC2 are sampled on the rising edge of TFCLK. TCA1 and TCA2 are updated on the rising edge of TFCLK. See note 13.

Pin Name	Type	Pin No.	Function
TDAT[0] TDAT[1] TDAT[2] TDAT[3] TDAT[4] TDAT[5] TDAT[6] TDAT[7] TDAT[8] TDAT[9] TDAT[10] TDAT[11] TDAT[12] TDAT[13] TDAT[14] TDAT[15]	Input	15 14 13 12 11 7 6 5 4 3 2 1 160 159 158 157	The transmit cell data (TDAT[15:0]) bus carries the ATM cell octets. TDAT[15:0] is sampled on the rising edge of TFCLK and is considered valid only when TWRENB1 or TWRENB2 is simultaneously asserted. See note 13.
TXPRTY[1] TXPRTY[0]	Input	153 156	The transmit parity (TXPRTY[1:0]) signal indicates the parity of the TDAT[15:0] bus. Odd or even parity selection can be made using a register. TXPRTY[1:0] is sampled on the rising edge of TFCLK and is considered valid only when TWRENB1 or TWRENB2 is simultaneously asserted. See note 13. ••••••••••••••••´••••´•j`•••´•••••¨••Ù•••´•••´••••n••••e interrupt. Cells with parity errors are not filtered, so the TXPRTY[1:0] inputs may be unused. See the Functional Timing and the TACP register description sections for more details regarding this output.

Pin Name	Type	Pin No.	Function
TWRENB1	Input	23	The channel #1 active low transmit write enable inputs (TWRENB1) is used to initiate writes to the channel #1 transmit FIFO. TWRENB1 is sampled using the rising edge of TFCLK. A complete 53 octet cell must be written to the transmit FIFO before it is inserted into the SPE. Idle/unassigned cells are inserted when a complete cell is not available. See note 13.
TWRENB2	Input	22	The channel #2 active low transmit write enable inputs (TWRENB2) is used to initiate writes to the channel #2 transmit FIFO. TWRENB2 is sampled using the rising edge of TFCLK. A complete 53 octet cell must be written to the transmit FIFO before it is inserted into the SPE. Idle/unassigned cells are inserted when a complete cell is not available. See note 13.
TSOC1	Input	17	The channel #1 transmit start of cell (TSOC1) signal can be configured to mark a start of cell on the transmit cell data bus for channel #1 or channel #2 (in Multi-PHY mode). When TSOC1 is high, the first octet of the cell is present. It is not necessary for TSOC1 to be present at each cell. An interrupt may be generated if TSOC1 is high during any byte other than the first byte. TSOC1 is sampled on the rising edge of TFCLK. See note 13.

Pin Name	Type	Pin No.	Function
TSOC2	Input	16	The channel #2 transmit start of cell (TSOC2) signal can be configured to mark a start of cell on the transmit cell data bus for channel #2 in Split-Bus mode. When TSOC2 is high, the first octet of the cell is present. It is not necessary for TSOC2 to be present at each cell. An interrupt may be generated if TSOC2 is high during any byte other than the first byte. TSOC2 is sampled on the rising edge of TFCLK. See note 13.
TCA1	Output	19	The channel #1 transmit cell available (TCA1) signal indicates when space for a cell is available in the channel #1 transmit FIFO. When TCA1 is sampled asserted, it indicates that the channel #1 transmit FIFO is not full. When TCA1 is sampled deasserted, it indicates that either the channel #1 transmit FIFO is near full and can accept no more than four writes, or that the channel #1 transmit FIFO is full (as selected in the TACP FIFO Control register). In addition, to reduce FIFO latency, the FIFO cell depth can be programmed in the TACP FIFO Control register. The active polarity of TCA1 defaults to active high and can be programmed in the S/UNI-DUAL Configuration register. TCA1 is updated on the rising edge of TFCLK, (see note 13). TCA1 may become metastable when transitioning from a logic '1' to '0'.

Pin Name	Type	Pin No.	Function
TCA2	Output	18	The channel #2 transmit cell available (TCA2) signal indicates when space for a cell is available in the channel #2 transmit FIFO. When TCA2 is sampled asserted, it indicates that the channel #2 transmit FIFO is not full. When TCA2 is sampled deasserted, it indicates that either the channel #2 transmit FIFO is near full and can accept no more than four writes, or that the channel #2 transmit FIFO is full (as selected in the TACP FIFO Control register). In addition, to reduce FIFO latency, the FIFO cell depth can be programmed in the TACP FIFO Control register. The active polarity of TCA2 defaults to active high and can be programmed in the S/UNI-DUAL Configuration register. TCA2 is updated on the rising edge of TFCLK, (see note 13). TCA2 may become metastable when transitioning from a logic '1' to '0'.
TATP	Analog	88	Transmit analog test point (TATP) is provided for production test purposes. Connect this pin to ground.
LF1+, LF1-, LFO1	Analog	118 117 116	Passive components connected to the channel #1 recovery loop filter (LF1+, LF1- and LFO1) pins determine the dynamics of the channel #1 clock recovery unit. Refer to the Operation section for details.
LF2+, LF2-, LFO2	Analog	83 84 85	Passive components connected to the channel #2 recovery loop filter (LF2+, LF2- and LFO2) pins determine the dynamics of the channel #2 clock recovery unit. Refer to the Operation section for details.

Pin Name	Type	Pin No.	Function
CSB	Input	67	The active low chip select (CSB) signal is low during S/UNI-DUAL register accesses. If CSB is not required (i.e. register accesses are controlled by using the RDB and WRB signals only), CSB must be connected to an inverted version of the RSTB input.
RDB	Input	65	The active low read enable (RDB) signal is low during S/UNI-DUAL register read accesses. The S/UNI-DUAL drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are low.
WRB	Input	66	The active low write strobe (WRB) signal is low during a S/UNI-DUAL register write accesses. The D[7:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	I/O	126 127 128 130 131 132 133 134	The bidirectional data bus D[7:0] is used during S/UNI-DUAL register read and write accesses.

Pin Name	Type	Pin No.	Function
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7]	Input	77 76 75 74 73 72 71 70	The address bus A[8:0] selects specific registers during S/UNI-DUAL register accesses.
A[8]/TRS		69	The test register select (TRS) signal selects between normal and test mode register accesses. TRS is high during test mode register accesses, and is low during normal mode register accesses.
RSTB	Input	78	The active low reset (RSTB) signal provides an asynchronous S/UNI-DUAL reset. RSTB is a Schmitt triggered input with an integral pull up resistor.
ALE	Input	68	The address latch enable (ALE) is active high and latches the address bus A[8:0] when low. When ALE is high, the internal address latches are transparent. It allows the S/UNI-DUAL to interface to a multiplexed address/data bus. ALE has an integral pull up resistor.
INTB	Open-Drain Output	125	The active low interrupt (INTB) signal goes low when a S/UNI-DUAL interrupt source is active, and that source is unmasked. The S/UNI-DUAL may be enabled to report many alarms or events via interrupts. INTB returns tristate when the interrupt is acknowledged via an appropriate register access.

Pin Name	Type	Pin No.	Function
TCK	Input	152	The test clock (TCK) signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port.
TMS	Input	150	The test mode select (TMS) signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor.
TDI	Input	151	The test data input (TDI) signal carries test data into the S/UNI-DUAL via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.
TDO	Tristate	148	The test data output (TDO) signal carries test data out of the S/UNI-DUAL via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is tristate except when scanning of data is in progress.
TRSTB	Input	149	The active low test reset (TRSTB) signal provides an asynchronous S/UNI-DUAL test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull up resistor. TRSTB must be asserted during the power up sequence.

Pin Name	Type	Pin No.	Function
VDD_DC1 VDD_DC2 VDD_DC3 VDD_DC4 VDD_DC5 VDD_DC6 VDD_DC7 VDD_DC8 VDD_DC9 VDD_DC10	Power	8 20 29 42 51 63 100 124 142 154	The DC power (VDD_DC1 - VDD_DC10) pins should be connected to a well decoupled +5 V DC in common with VDD_AC.
VSS_DC1 VSS_DC2 VSS_DC3 VSS_DC4 VSS_DC5 VSS_DC6 VSS_DC7 VSS_DC8 VSS_DC9 VSS_DC10	Ground	10 21 30 41 50 64 101 123 141 155	The DC ground (VSS_DC1 - VSS_DC10) pins should be connected to GND in common with VSS_AC.
VDD_AC1 VDD_AC2 VDD_AC3 VDD_AC4 VDD_AC5	Power	24 34 45 55 135	The pad ring power (VDD_AC1 - VDD_AC5) pins should be connected to a well decoupled +5 V DC in common with VDD_DC.

Pin Name	Type	Pin No.	Function
VSS_AC1 VSS_AC2 VSS_AC3 VSS_AC4 VSS_AC5	Ground	26 35 46 56 129	The pad ring ground (VSS_AC1 - VSS_AC5) pins should be connected to GND in common with VSS_DC.
TAVD1	Power	103	The power (TAVD1) pin for the transmit clock synthesizer reference circuitry. TAVD1 should be connected to analog +5V.
TAVD2	Power	104	The power (TAVD2) pin for the transmit clock synthesizer oscillator. TAVD2 should be connected to analog +5V.
TAVS1	Ground	102	The ground (TAVS1) pin for the transmit clock synthesizer reference circuitry. TAVS1 should be connected to analog GND.
TAVS2	Ground	105	The ground (TAVS2) pin for the transmit clock synthesizer oscillator. TAVS2 should be connected to analog GND.
TXVD_AC	Power	92	The transmit pad ring power (TXVD_AC) supplies the TXD1+/- and TXD2+/- outputs. TXVD_AC is physically isolated from the other device power pins and should be a clean, well decoupled +5 V supply to minimize the noise coupled into the transmit stream.
TXVS_AC	Ground	97	The transmit pad ring ground (TXVS_AC) is the return path for the TXD1+/- and TXD2+/- outputs. TXVS_AC is physically isolated from the other device ground pins and should be clean to minimize the noise coupled into the transmit stream.
R1AVD1	Power	114	The power (R1AVD1) pin for the RXD1+/- and ALOS1+/- PECL inputs and for channel #1 receive clock and data recovery block reference circuitry. R1AVD1 should be connected to analog +5V.

Pin Name	Type	Pin No.	Function
R1AVD2	Power	120	The power (R1AVD2) pin for channel #1 receive clock and data recovery block active loop filter and oscillator. R1AVD2 should be connected to analog +5V.
R1AVDQ3	Power	106	R1AVDQ3 acts as a shield and should be connected to analog +5V.
R1AVS1	Ground	115	The ground (R1AVS1) pin for the RXD1+/- and ALOS1+/- PECL inputs and for channel #1 receive clock and data recovery block reference circuitry. R1AVS1 should be connected to analog GND.
R1AVS2	Ground	122	The ground (R1AVS2) pin for channel #1 receive clock and data recovery block active loop filter and oscillator. R1AVS2 should be connected to analog GND.
R1AVSQ3	Ground	109	R1AVSQ3 acts as a shield and should be connected to analog GND.
R2AVD1	Power	87	The power (R2AVD1) pin for the RXD2+/- and ALOS2+/- PECL inputs and for channel #2 receive clock and data recovery block reference circuitry. R2AVD1 should be connected to analog +5V.
R2AVD2	Power	81	The power (R2AVD2) pin for channel #2 receive clock and data recovery block active loop filter and oscillator. R2AVD2 should be connected to analog +5V.
R2AVDQ3	Power	93	R2AVDQ3 acts as a shield and should be connected to analog +5V.
R2AVS1	Ground	86	The ground (R2AVS1) pin for the RXD2+/- and ALOS2+/- PECL inputs and for channel #2 receive clock and data recovery block reference circuitry. R2AVS1 should be connected to analog GND.

Pin Name	Type	Pin No.	Function
R2AVS2	Ground	79	The ground (R2AVS2) pin for channel #2 receive clock and data recovery block active loop filter and oscillator. R2AVS2 should be connected to analog GND.
R2AVSQ3	Ground	96	R2AVSQ3 acts as a shield and should be connected to analog GND.
REFAVD	Power	110	The power (REFAVD) pin for the REFCLK+/- PECL inputs. REFAVD should be connected to analog +5V.
REFAVS	Ground	113	The ground (REFAVS) pin for the REFCLK+/- PECL inputs. REFAVS should be connected to analog GND.
NC	Ground	89	The no connection (NC) pin should be connected to analog GND.

Notes on Pin Description:

1. All S/UNI-DUAL inputs and bidirectionals present minimum capacitive loading and operate at TTL logic levels except for the REFCLK+/-, ALOS1+/-, ALOS2+/-, RXD1+/- and RXD2+/- differential inputs which operate at pseudo ECL (PECL) logic levels.

2. The TXD1+/-, and TXD2+/- outputs have a 6 mA drive capability. The RDAT[15:0], RXPRTY[1:0], RSOC1, RSOC2, RCA1, RCA2, TCA1, TCA2, TCLK, RCLK1, and RCLK2 outputs have a 4 mA drive capability. All other S/UNI-DUAL digital outputs and bidirectionals have 2 mA drive capability.

3. Inputs RSTB, ALE, TSEN, TMS, TDI and TRSTB have internal pull-up resistors.

4. The VSS_DC, VSS_AC, TXVS_AC and AVS ground pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the S/UNI-DUAL.

5. The VDD_DC, VDD_AC, TXVD_AC, and AVD power pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the S/UNI-DUAL.

6. All analog power and ground pins are sensitive to noise. They must be isolated from the digital power and ground. The TAVD2, R1AVD2 and R2AVD2 pins power oscillators; therefore, they generate significant switching noise. Care must be taken to decouple these pins from each other and all other analog power and ground pins.

7. Do not exceed 100 mA of current on any pin during the power-up or power-down sequence. Refer to the Power Sequencing description in the Operations section.

8. Before any input activity occurs, ensure that the device power supplies are within their nominal voltage range.

9. Hold the device in the reset condition until the device power supplies are within their nominal voltage range.

10. Ensure that all digital power is applied simultaneously, and it is applied before the analog power is applied. Refer to the Power Sequencing description in the Operations section.

11. Please refer to the Operation section for a discussion of PECL interfacing issues.

12. Please refer the Functional Timing Section for a discussion of the Drop Side Receive Interface.

13. Please refer to the Functional Timing section for a discussion of the Drop Side Transmit Interface.

9 FUNCTIONAL DESCRIPTION

9.1 Clock Recovery

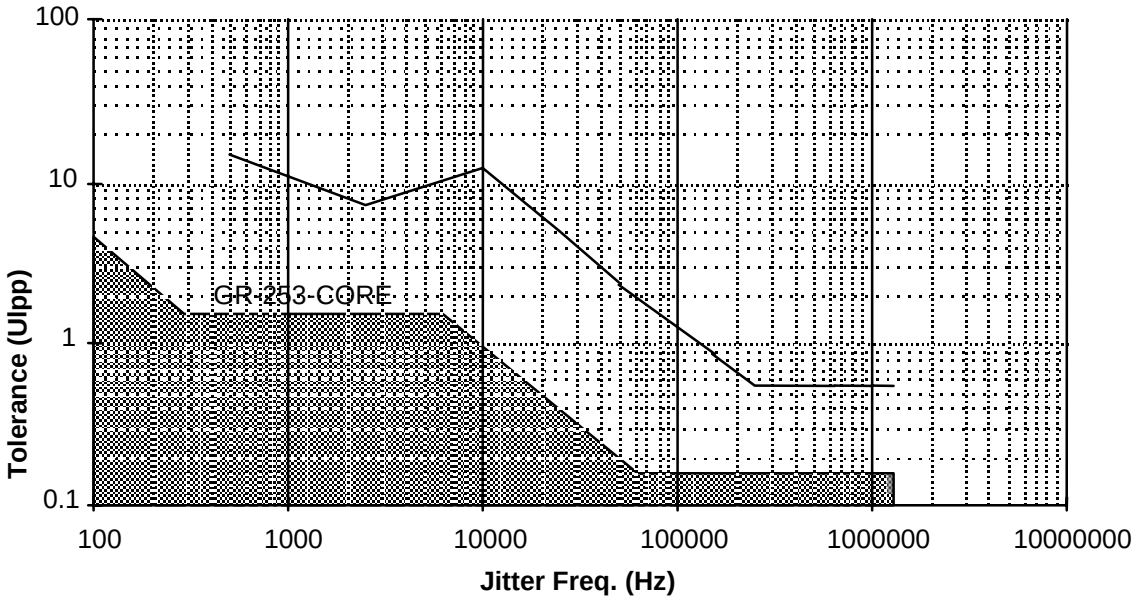
The clock recovery unit recovers the clock from the incoming bit serial data stream. The clock recovery unit is fully compliant with SONET and SDH jitter tolerance requirements. The clock recovery unit utilizes a low frequency reference clock to train and monitor its clock recovery PLL. Under loss of signal conditions, the clock recovery unit will continue to output a line rate clock that is locked to this reference for "keep alive" purposes. The clock recovery unit can be configured to utilize reference clocks at 6.48 or 19.44 MHz. The clock recovery unit provides status bits that indicate whether it is locked to the data or to the reference. The clock recovery unit also supports diagnostic loopback and a loss of signal input that squelches normal input data.

Initially, the PLL locks to the reference clock, REFCLK+/-. When the frequency of the recovered clock is within 488 ppm of the reference clock, the PLL attempts to lock to the data. Once in data lock, the PLL reverts to the reference clock if no data transitions occur in 80 bit periods or if the recovered clock drifts beyond 488 ppm of the reference clock.

When the transmit clock is derived from the recovered clock (loop timing), the accuracy of the transmit clock is directly related to the REFCLK+/- reference accuracy in the case of a loss of signal condition. To meet the GR-253-CORE SONET Network Element free-run accuracy specification, the reference must be within +/-20ppm. When not loop timed, the REFCLK+/- accuracy may be relaxed to +/-50ppm.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal. The total loop dynamics of the clock recovery PLL yield a jitter tolerance which exceeds the minimum tolerance required for SONET equipment by GR-253-CORE (Figure 3).

Figure 3 - STS-3c/STM-1Jitter Tolerance



Note that for frequencies below 300 Hz the jitter tolerance is greater than 15 UIpp; 15 UIpp is the maximum jitter tolerance of the test equipment. Also note that the dip in the tolerance curve between 300 Hz and 10 kHz is due to the S/UNI-DUAL's internal clock difference detector. If the recovered clock drifts beyond 488 ppm of the reference, the PLL locks to the reference clock.

The typical jitter tolerance illustrated in Figure 3 is associated with the external loop filter components illustrated in Figure 19.

9.2 Serial to Parallel Converter

The Serial to Parallel Converter (SIPO) converts the received bit serial SONET stream to a byte serial stream. The SIPO searches for the SONET/SDH framing pattern (A1, A2) in the incoming stream, and performs serial to parallel conversion on octet boundaries.

9.3 Receive Section Overhead Processor

The Receive Section Overhead Processor (RSOP) provides frame synchronization, descrambling, section level alarm and performance monitoring.

9.3.1 Framer

The Framer Block determines the in-frame/out-of-frame status of the STS-3c or STS-1 data stream. Output RALM2 or RALM1 can be configured to reflect this status with its timing aligned to RCLK2 and RCLK1, respectively.

While in-frame, the framing bytes (A1, A2) in each frame are compared against the expected pattern. Out-of-frame is declared when four consecutive frames containing one or more framing pattern errors have been received.

While out-of-frame, the SIPO block monitors the bit serial data stream for an occurrence of the framing pattern. When a framing pattern has been recognized, the Framer Block verifies that an error free framing pattern is present in the next frame before declaring in-frame.

9.3.2 Descramble

The Descramble Block utilizes a frame synchronous descrambler to process the received byte serial stream. The generating polynomial is $x^7 + x^6 + 1$ and the sequence length is 127. Details of the descrambling operation are provided in the references. Note that the framing bytes (A1 and A2) and the section trace/section growth bytes (J0/Z0) are not descrambled. A register bit is provided to disable the descrambling operation.

9.3.3 Error Monitor

The Error Monitor Block calculates the received section BIP-8 error detection code (B1) based on the scrambled data of the complete STS-3c or STS-1 frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-8 code is compared with the BIP-8 code extracted from the B1 byte of the following frame. Differences indicate that a section level bit error has occurred. Up to 64000 (8 x 8000) bit errors can be detected per second. The Error Monitor Block accumulates these section level bit errors in a 16 bit saturating counter that can be read via the microprocessor interface. Circuitry is provided to latch this counter so that its value can be read while simultaneously resetting the internal counter to 0 or 1, if appropriate, so that a new period of accumulation can begin without loss of any events. It is intended that this counter be polled at least once per second so as not to miss bit error events.

9.3.4 Loss of Signal

The Loss of Signal Block monitors the scrambled data of the complete STS-3c or STS-1 stream for the absence of 1's. When 20 ± 3 µs of all-zeros pattern is detected, a loss of signal (LOS) is declared. Loss of signal is cleared when two valid framing words are detected and during the intervening time, no loss of signal condition is detected. If configured, a loss of signal condition can assert the corresponding port's RALM output with timing aligned to its respective RCLK.

9.3.5 Loss of Frame

The Loss of Frame Block monitors the in-frame / out-of-frame status of the Framer Block. A loss of frame (LOF) is declared when an out-of-frame (OOF) condition persists for 3 ms. To provide for intermittent out-of-frame conditions, the 3 ms timer is not reset to zero until an in-frame condition persists for 3 ms. The loss of frame is cleared when an in frame condition persists for a period of 3 ms. If configured, a loss of frame condition can assert the corresponding port's RALM output with timing aligned to its respective RCLK.

9.4 Receive Line Overhead Processor

The Receive Line Overhead Processor (RLOP) provides line level alarm and performance monitoring.

9.4.1 Line Remote Defect Indication Detect

The Line RDI Detect Block detects the presence of Line remote defect indication (RDI) in the data stream. Line RDI is declared when a 110 binary pattern is detected in bits 6, 7, and 8 of the K2 byte, for five consecutive frames. Line RDI is removed when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for five consecutive frames. The line RDI status is available through a maskable interrupt and register bits.

9.4.2 Line AIS Detect

The Line AIS Block detects the presence of a Line Alarm Indication Signal (AIS) in the data stream. Line AIS is declared when a 111 binary pattern is detected in bits 6,7,8 of the K2 byte, for five consecutive frames. LAIS is removed when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for five consecutive frames. If configured, a line AIS detection can assert the corresponding port's RALM output with timing aligned to its respective RCLK.

9.4.3 Automatic Protection Switch Control Block

The Automatic Protection Switch Control (APSC) Block filters and captures the receive automatic protection switch channel bytes (K1 and K2) allowing them to be read via the RASE APS K1 Register and the RASE APS K2 Register. The bytes are filtered for three frames before being written to these registers. A protection switching byte failure alarm is declared when twelve successive frames have been received, where no three consecutive frames contain identical K1 bytes. The protection switching byte failure alarm is removed upon detection of three consecutive frames containing identical K1 bytes. The detection of invalid APS codes is done in software by polling the RASE APS K1 Register and the RASE APS K2 Register.

9.4.4 Error Monitor

The Error Monitor Block calculates the received line BIP-8/24 error detection code (B2) based on the line overhead and synchronous payload envelope of the receive data stream. The line BIP-8/24 code is a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP code is compared with the BIP-8/24 code extracted from the B2 byte(s) of the following frame. Any differences indicate that a line layer bit error has occurred. Up to 192000 (24 BIP/frame x 8000 frames/seconde) bit errors can be detected per second for STS-3 rate and 64000 (8 BIP/frame x 8000 frames/seconde) for STS-1 rate.

The Error Monitor Block accumulates these line layer bit errors in a 20 bit saturating counter that can be read via the microprocessor interface. During a read, the counter value is latched and the counter is reset to 0 (or 1, if there is an outstanding event). Note, this counter should be polled at least once per second to avoid saturation which in turn may result in missed bit error events.

Signal fail (SF) or signal degrade (SD) threshold crossing alarms can be detected and indicated in the Error Monitor Block. The bit error rates associated with the SF or SD alarms are programmable over a range of 10^{-3} to 10^{-9}. Details are provided in the Operations section.

The Error Monitor Block also accumulates line far end block error indications (contained in the M0/M1 byte) in a similar manner.

9.5 Receive Path Overhead Processor

The Receive Path Overhead Processor (RPOP) provides pointer interpretation, extraction of path overhead, extraction of the synchronous payload envelope, and path level alarm and performance monitoring.

9.5.1 Pointer Interpreter

The Pointer Interpreter interprets the incoming pointer (H1, H2) as specified in the references. The pointer value is used to determine the location of the path overhead (the J1 byte) in the incoming STS-3c (AU4) or STS-1 (AU3) stream.

The Pointer Interpreter Block detects loss of pointer (LOP) in the incoming STS-1 or STS-3c. LOP is declared as a result of eight consecutive invalid pointers or eight consecutive NDF enabled indications. LOP is removed when the same valid pointer with normal NDF is detected for three consecutive frames.

The Pointer Interpreter Block detects path AIS in the incoming STS-1 or STS-3c stream. PAIS is declared on entry to the AIS_state after three consecutive AIS indications. PAIS is removed when the same valid pointer with normal NDF is detected for three consecutive frames or when a valid with NDF enabled is detected.

The pointer value is used to extract the path overhead from the incoming stream.

Note that due to anomalies in the standard pointer interpretation rules, certain illegal pointers may not cause the device to declare a loss of pointer (LOP) state. In this situation, however, the device will declare a loss of cell delineation state and return to normal operation when presented with legal pointer values. Such illegal pointers typically can only be generated continuously by test equipment and will not normally occur during live-traffic operation.

9.5.2 Error Monitor

The Error Monitor Block contains two 16-bit counters that are used to accumulate path BIP-8 errors (B3), and far end block errors (FEBE). The contents of the two counters may be transferred to holding registers, and the counters reset under microprocessor control.

Path BIP-8 errors are detected by comparing the path BIP-8 byte (B3) extracted from the current frame, to the path BIP-8 computed for the previous frame.

FEBEs are detected by extracting the 4-bit FEBE field from the path status byte (G1). The legal range for the 4-bit field is between 0000 and 1000, representing zero to eight errors. Any other value is interpreted as zero errors.

Path remote defect indication (RDI) is detected by extracting bit 5 of the path status byte. Path RDI is declared when bit 5 is set high for five consecutive frames and is cleared when bit 5 is low for five consecutive frames.

9.6 Receive ATM Cell Processor

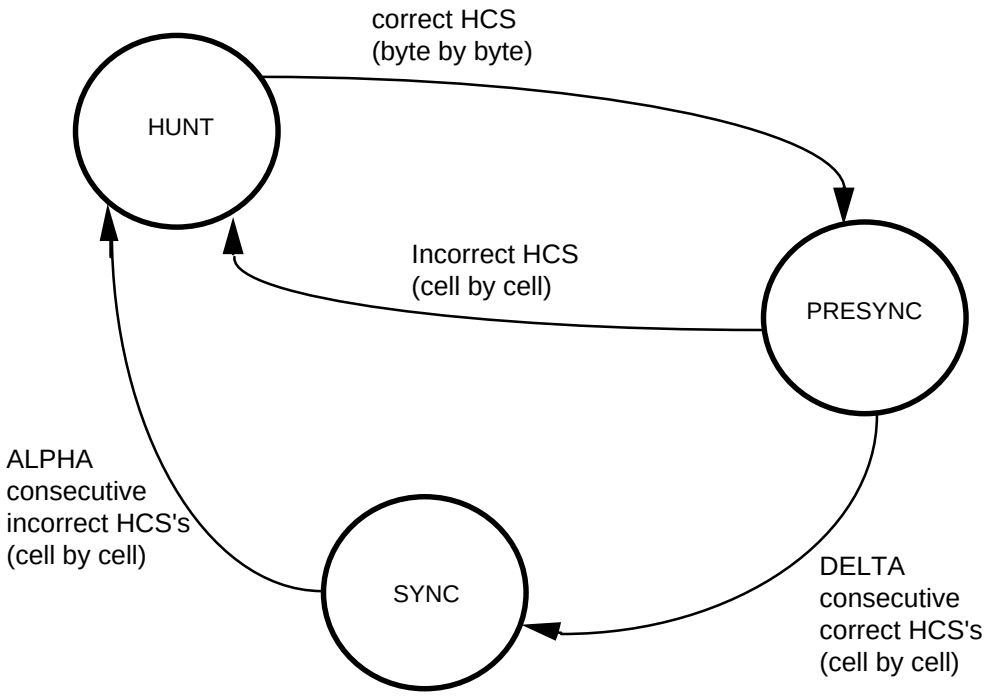
The Receive ATM Cell Processor (RACP) performs ATM cell delineation, provides cell filtering based on idle/unassigned cell detection and HCS error detection, and performs ATM cell payload descrambling. The RACP also provides a four cell deep receive FIFO. This FIFO passes a 53 byte data structure and is used to separate the line timing from the higher layer ATM system timing.

9.6.1 Cell Delineation

Cell Delineation is the process of framing to ATM cell boundaries using the header check sequence (HCS) field found in the cell header. The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. When performing delineation, correct HCS calculations are assumed to indicate cell boundaries. Cells must be byte aligned before insertion in the synchronous payload envelope.

The cell delineation algorithm searches the 53 possible cell boundary candidates one at a time to determine the valid cell boundary location. While searching for the cell boundary location, the cell delineation circuit is in the HUNT state. When a correct HCS is found, the cell delineation state machine locks on the particular cell boundary and enters the PRESYNC state. This state validates the cell boundary location. If the cell boundary is invalid then an incorrect HCS will be received within the next DELTA cells, at which point a transition back to the HUNT state is executed. If no HCS errors are detected in this PRESYNC period then the SYNC state is entered. While in the SYNC state, synchronization is maintained until ALPHA consecutive incorrect HCS patterns are detected. In such an event a transition is made back to the HUNT state. The state diagram of the delineation process is shown in Figure 4.

Figure 4 - Cell Delineation State Diagram



The values of ALPHA and DELTA determine the robustness of the delineation method. ALPHA determines the robustness against false misalignments due to bit errors. DELTA determines the robustness against false delineation in the synchronization process. ALPHA is chosen to be 7 and DELTA is chosen to be 6. These values result in a maximum average time to delineate of 31 µs for STS-3c and 93 µs for STS-1.

9.6.2 Descrambler

The self synchronous descrambler operates on the 48 byte cell payload only. The circuitry descrambles the information field using the '$x^{43} + 1$' polynomial. The descrambler is disabled for the duration of the header and HCS fields, and may optionally be disabled.

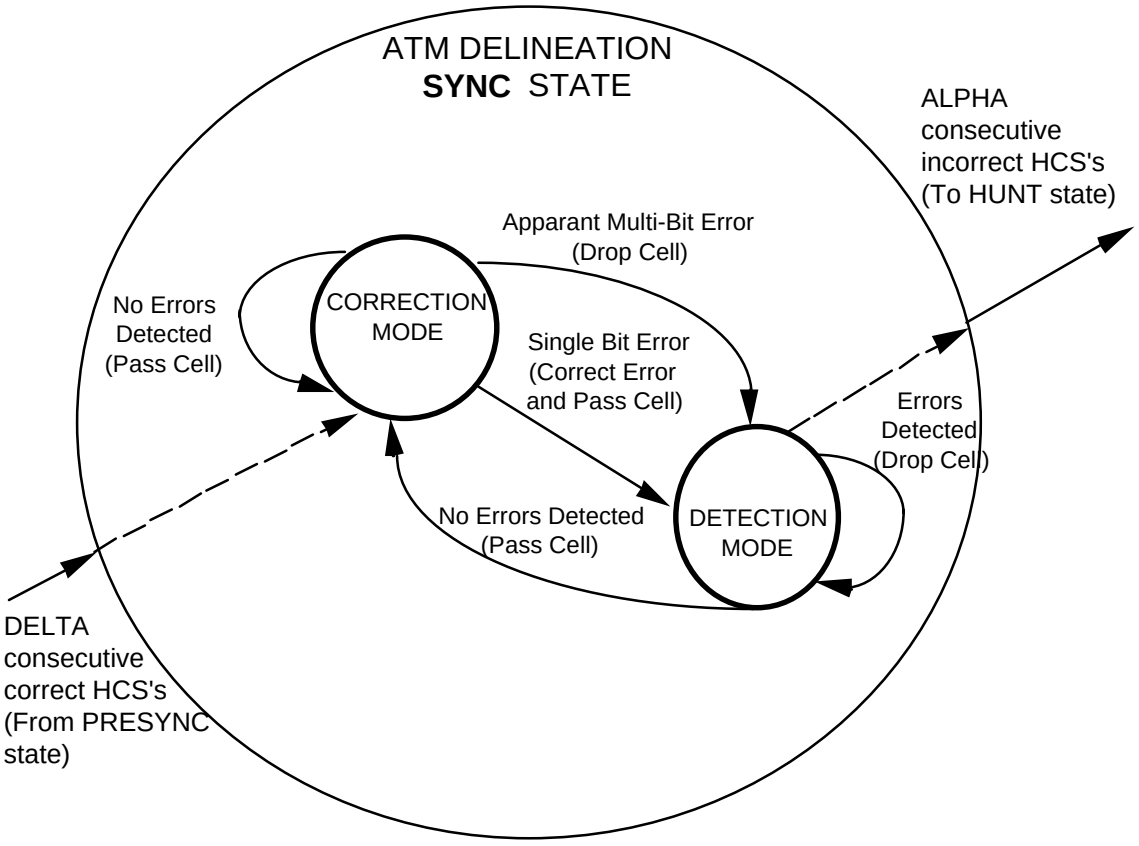
9.6.3 Cell Filter and HCS Verification

Cells are filtered (or dropped) based on HCS errors and/or a cell header pattern. Cell filtering is optional and is enabled through the RACP registers. Cells are passed to the receive FIFO while the cell delineation state machine is in the SYNC state as described above. When both filtering and HCS checking are

enabled, cells are dropped if uncorrectable HCS errors are detected, or if the corrected header contents match the pattern contained in the 'Match Header Pattern' and 'Match Header Mask' registers. Idle or unassigned cell filtering is accomplished by writing the appropriate cell header pattern into the 'Match Header Pattern' and 'Match Header Mask' registers. Idle/Unassigned cells are assumed to contain the all zeros pattern in the VCI and VPI fields. The 'Match Header Pattern' and 'Match Header Mask' registers allow filtering control over the contents of the GFC, PTI, and CLP fields of the header.

The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. The RACP block verifies the received HCS using the polynomial, $x^8 + x^2 + x + 1$. The coset polynomial, $x^6 + x^4 + x^2 + 1$, is added (modulo 2) to the received HCS octet before comparison with the calculated result. While the cell delineation state machine (described above) is in the SYNC state, the HCS verification circuit implements the state machine shown in Figure 5.

Figure 5 - HCS Verification State Diagram



In normal operation, the HCS verification state machine remains in the 'Correction Mode' state. Incoming cells containing no HCS errors are passed to the receive FIFO. Incoming single bit errors are corrected, and the resulting cell is passed to the FIFO. Upon detection of a single bit error or a multi bit error, the state machine transitions to the 'Detection Mode' state. In this state, the detection of any HCS error causes the corresponding cell to be dropped. Cells containing an error-free HCS are passed, and the state machine transitions back to the 'Correction Mode' state.

9.6.4 Performance Monitor

The Performance Monitor consists of two 8-bit saturating HCS error event counters and a 19-bit cell counter. One of the counters accumulates correctable HCS errors (i.e. single HCS bit errors detected while the HCS Verification state machine is in the 'Correction Mode' state described above). The second counter accumulates uncorrectable HCS errors (i.e. HCS bit errors detected while the HCS Verification state machine is in the 'Detection Mode' state or multiple HCS bit errors detected while the state machine is in the 'Correction Mode' state as described above). The cell counter accumulates the number of received assigned cells. All counters are enabled only when the RACP is in the SYNC state.

Each counter may be read through the microprocessor interface. Circuitry is provided to latch these counters so that their values can be read while simultaneously resetting the internal counters to 0 or 1, if appropriate, so that a new period of accumulation can begin without loss of any events. It is intended that the counters be polled at least once per second so HCS error events or cell counts will not be missed.

9.6.5 Receive FIFO

The Receive FIFO provides FIFO management and the asynchronous interface between the RACP block and chip pads to the external environment. The receive FIFO can accommodate four cells. The receive FIFO provides for the separation of the STS-1 or STS-3c line or physical layer timing from the ATM layer timing.

Management functions include filling the receive FIFO, indicating when cells are available to be read from the receive FIFO, maintaining the receive FIFO read and write pointers, and detecting FIFO overrun and underrun conditions. Upon detection of an overrun condition, the FIFO will drop all incoming cells until at least one cell has been read from the FIFO. At least one cell will be lost during

the FIFO drop operation. Upon detection of an underrun, the offending read is ignored. FIFO overruns are indicated through a maskable interrupt and register bit. The interface provided indicates the start of a cell (RSOC) when data is read from the receive FIFO (using RFCLK) and indicates the cell available status (RCA). The cell available status may be configured to change from available to unavailable on read cell boundaries or four reads before the cell boundary.

When the RCA signal is configured to be deasserted with zero octets (as opposed to four) in the FIFO, it is not an error condition to hold the read enable (RRDENB) active. In this situation, the RCA signal identifies the valid octets.

9.7 Clock Synthesis

The transmit clock is synthesized from a 19.44 MHz or 6.48 MHz reference. The transfer function yields a typical low pass corner of 500 kHz with a 19.44 MHz reference and 170 kHz with a 6.48 MHz reference, above which reference jitter is attenuated at 12dB per octave. The intrinsic jitter is minimised when the reference frequency is 19.44 MHz. With a jitter free 19.44 MHz differential reference input and a low noise board layout, the intrinsic jitter is typically 0.01 UI RMS when measured using a high pass filter with a 12 kHz cutoff frequency.

The REFCLK+/- reference should be within ±20 ppm to meet the SONET free-run accuracy requirements specified in GR-253-CORE.

9.8 Parallel to Serial Converter

The Parallel to Serial Converter (PISO) converts the internal byte serial stream to a bit serial stream.

9.9 Transmit Section Overhead Processor

The Transmit Section Overhead Processor (TSOP) provides frame pattern insertion (A1, A2), scrambling, section level alarm signal insertion, and section BIP-8 (B1) insertion.

9.9.1 Line AIS Insert

Line AIS insertion results in all bits of the SONET/SDH frame being set to 1 before scrambling except for the section overhead. The Line AIS Insert Block substitutes all ones as described when enabled through an internal register accessed through the microprocessor interface. Activation or deactivation of line AIS insertion is synchronized to frame boundaries.

9.9.2 BIP-8 Insert

The BIP-8 Insert Block calculates and inserts the BIP-8 error detection code (B1) into the unscrambled data stream.

The BIP-8 calculation is based on the scrambled data of the complete STS-3c or STS-1 frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-8 code is then inserted into the B1 byte of the following frame before scrambling. BIP-8 errors may be continuously inserted under register control for diagnostic purposes.

9.9.3 Framing and Section Trace

The Framing and Section Trace Block inserts the framing bytes (A1, A2) and section trace/section growth bytes (J0/Z0) into the STS-3c or STS-1 frame. Framing bit errors may be continuously inserted under register control for diagnostic purposes.

9.9.4 Generation of TFP

The TSOP generates a Transmit Framing Pulse (TFP) which is high for one TCLK cycle every 2430 TCLK cycles for STS-3c TC mode (STS-1 mode) or every 810 cycles for STS-1 TC mode.

Each channel of the S/UNI Dual contains a TSOP block and each of the channels may have independent transmit line rates depending on the source of the transmit clock. The source of the transmit clock may be obtained from the REFCLK+/- inputs or it may be derived from the received data (loop timed or line looped back modes). As a result, the two halves of the S/UNI Dual may generate different TFPs derived from different transmit clocks.

The S/UNI Dual selects the TCLK and TFP outputs depending whether the device is loop timed or in line loop back mode according to the following table:

Table 1 -

CH #1 Loop timed or Line Looped back	CH #2 Loop timed or Line Looped back	TFP Output Source	TCLK Output Source
NO	NO	Channel 1	Channel 1
NO	YES	Channel 1	Channel 1
YES	NO	Channel 2	Channel 2
YES	YES	Forced Low	Force Low

To summarize the table above, TFP and TCLK are taken from the channel which is not looped timed or in line loop back mode. In the case where neither is, then TFP and TCLK are taken from channel 1. In the case were both are, TFP and TCLK are forced low.

Looped timed mode or line loop back mode is selected using registers 0x05 and 0x085.

9.9.5 Scrambler

The Scrambler Block utilizes a frame synchronous scrambler to process the transmit serial stream when enabled through an internal register accessed via the microprocessor interface. The generating polynomial is $x^7 + x^6 + 1$. Precise details of the scrambling operation are provided in the references. Note that the framing bytes and the identity bytes are not scrambled. All zeros may be continuously inserted (after scrambling) under register control for diagnostic purposes.

9.10 Transmit Line Overhead Processor

The Transmit Line Overhead Processor (TLOP) provides line level alarm signal insertion, synchronization status insertion (S1), and line BIP-8/24 insertion (B2).

9.10.1 APS Insert

The APS Insert Block inserts the two automatic protection switch (APS) channel bytes in the Line Overhead (K1 and K2) into the transmit stream when enabled by an internal register.

9.10.2 BIP Calculate

The BIP Calculate Block calculates the line BIP error detection code (B2) based on the line overhead and synchronous payload envelope of the STS-3c or STS-1 stream. The line BIP code is a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP code is inserted into the B2 byte positions of the following frame. BIP errors may be continuously inserted under register control for diagnostic purposes.

9.10.3 Line Remote Defect Indication Insert

The Line RDI Insert Block multiplexes the line overhead bytes into the output stream and optionally inserts line RDI. Line RDI is inserted by this block when enabled via register control. Line RDI is inserted by transmitting the code 110 (binary) in bit positions 6, 7, and 8 of the K2 byte contained in the STS-3c or STS-1 stream.

9.10.4 Line FEBE Insert

The Line FEBE Insert Block accumulates line BIP errors (M0/M1) detected by the Receive Line Overhead Processor and encodes far end block error indications in the transmit M0/M1 byte.

Figure 6 - STS-3c/STM-1 Default Transport Overhead Values

A1 (0xF6)	A1 (0xF6)	A1 (0xF6)	A2 (0x28)	A2 (0x28)	A2 (0x28)	J0 (0x01)	Z0 (0x02)	Z0 (0x03)
B1 (*)	(0x00)	(0x00)	E1 (0x00)	(0x00)	(0x00)	F1 (0x00)	(0x00)	(0x00)
D1 (0x00)	(0x00)	(0x00)	D2 (0x00)	(0x00)	(0x00)	D3 (0x00)	(0x00)	(0x00)
H1 (0x62)	H1 (0x93)	H1 (0x93)	H2 (0x0A)	H2 (0xFF)	H2 (0xFF)	H3 (0x00)	H3 (0x00)	H3 (0x00)
B2 (*)	B2 (*)	B2 (*)	K1 (0x00)	(0x00)	(0x00)	K2 (0x00)	(0x00)	(0x00)
D4 (0x00)	(0x00)	(0x00)	D5 (0x00)	(0x00)	(0x00)	D6 (0x00)	(0x00)	(0x00)
D7 (0x00)	(0x00)	(0x00)	D8 (0x00)	(0x00)	(0x00)	D9 (0x00)	(0x00)	(0x00)
D10 (0x00)	(0x00)	(0x00)	D11 (0x00)	(0x00)	(0x00)	D12 (0x00)	(0x00)	(0x00)
S1 (0x00)	Z1 (0x00)	Z1 (0x00)	Z2 (0x00)	Z2 (0x00)	M1 (*)	E2 (0x00)	(0x00)	(0x00)

*** : B1, B2 values depend on payload contents**
M1 value depends on incoming line bit errors

Figure 7 - STS-1 Default Transport Overhead Values

A1 (0xF6)	A2 (0x28)	J0 (0x01)
B1 (*)	E1 (0x00)	F1 (0x00)
D1 (0x00)	D2 (0x00)	D3 (0x00)
H1 (0x62)	H2 (0x0A)	H3 (0x00)
B2 (*)	K1 (0x00)	K2 (0x00)
D4 (0x00)	D5 (0x00)	D6 (0x00)
D7 (0x00)	D8 (0x00)	D9 (0x00)
D10 (0x00)	D11 (0x00)	D12 (0x00)
S1 (0x00)	M0 (*)	E2 (0x00)

*** : B1, B2 values depend on payload contents**
M0 value depends on incoming line bit errors

9.11 Transmit Path Overhead Processor

The Transmit Path Overhead Processor (TPOP) provides transport frame alignment generation, pointer generation (H1, H2), path overhead insertion, insertion of the synchronous payload envelope, insertion of path level alarm signals and path BIP-8 (B3) insertion.

9.11.1 Pointer Generator

The Pointer Generator Block generates the outgoing payload pointer (H1, H2). The block contains a free running timeslot counter that locates the start of the

synchronous payload envelope based on the generated pointer value and the SONET/SDH frame alignment.

The Pointer Generator Block generates the outgoing pointer as specified in the references. The concatenation indication (the NDF field set to 1001, I-bits and D-bits set to all ones, and unused bits set to all zeros) is inserted in the second and third pointer bytes.

9.11.2 BIP-8 Calculate

The BIP-8 Calculate Block performs a path bit interleaved parity calculation on the SPE of the outgoing stream. The resulting parity byte is inserted in the path BIP-8 (B3) byte position of the subsequent frame. BIP-8 errors may be continuously inserted under register control for diagnostic purposes.

9.11.3 FEBE Calculate

The FEBE Calculate Block accumulates far end block errors on a per frame basis, and inserts the accumulated value (up to maximum value of eight) in the FEBE bit positions of the path status (G1) byte. The FEBE information is derived from path BIP-8 errors detected by the receive path overhead processor, RPOP. The asynchronous nature of these signals implies that more than eight FEBE events may be accumulated between transmit G1 bytes. If more than eight receive Path BIP-8 errors are accumulated between transmit G1 bytes, the accumulation counter is decremented by eight, and the remaining FEBEs are transmitted at the next opportunity. Far end block errors may be inserted under register control for diagnostic purposes.

9.11.4 SPE Multiplexer

The SPE Multiplexer Block multiplexes the payload pointer bytes, the SPE stream, and the path overhead bytes into the STS-3c or STS-1 stream.

Figure 8 - Default Path Overhead Values

J1 (0x00)
B3 (*)
C2 (0x13)
G1 (*)
F2 (0x00)
H4 (*)
Z3 (0x00)
Z4 (0x00)
Z5 (0x00)

*** : B3 value depend on payload contents**
G1 value depends on incoming path bit errors
H4 value depends on cell boundary offset

9.12 Transmit ATM Cell Processor

The Transmit ATM Cell Processor (TACP) inserts H4 framing, provides rate adaptation via idle/unassigned cell insertion, provides HCS generation and insertion, and performs ATM cell scrambling. The TACP contains a four cell transmit FIFO. An idle or unassigned cell is transmitted if a complete ATM cell has not been written into the FIFO.

9.12.1 Idle/Unassigned Cell Generator

The Idle/Unassigned Cell Generator inserts idle or unassigned cells into the cell stream when enabled. Registers are provided to program the GFC, PTI, and CLP fields of the idle cell header and the idle cell payload. An all zeros pattern is inserted into the VCI/VPI bit locations. The idle cell HCS is automatically calculated and inserted.

9.12.2 Scrambler

The Scrambler scrambles the 48 octet information field. Scrambling is performed using a parallel implementation of the self synchronous scrambler described in the references. The cell headers are transmitted unscrambled, and the scrambler may optionally be completely disabled.

9.12.3 HCS Generator

The HCS Generator performs a CRC-8 calculation over the first four header octets. A parallel implementation of the polynomial, x^8+x^2+x+1, is used. The coset polynomial, $x^6+x^4+x^2+1$, is added (modulo 2) to the residue. The HCS Generator inserts the result into the fifth octet of the header.

9.12.4 Transmit FIFO

The Transmit FIFO provides FIFO management and a synchronous interface between the S/UNI-DUAL device and the external environment. The transmit FIFO can accommodate four cells. It provides for the separation of the physical layer timing from the ATM layer timing.

Management functions include filling the transmit FIFO, indicating when cells are available to be written to the transmit FIFO, maintaining the transmit FIFO read and write pointers, and detecting a FIFO overrun condition. The synchronous interface provided to an external device expects the start of a cell (TSOC) when the first byte of the cell is written to the FIFO (using TFCLK in conjunction with TWRENB) and indicates the cell available status (TCA). The FIFO status changes from cell unavailable to cell available on read cell boundaries. The FIFO status can be configured to change from cell available to cell unavailable on write cell boundaries or four octets before the end of the cell.

The latency through the transmit FIFO can be controlled by setting the fill level at which the cell available (TCA) signal is deasserted. Although all four cell buffers

are always accessible, TCA may be programmed to indicate when the FIFO contains one, two, three or four cells. (The current cell being read out of the FIFO is included in the count. Be aware that setting a depth of one may limit throughput.) If a cell write is started immediately after TCA transitions from deasserted to asserted, the latency through the device for the cell being written in STS-3c/STM-1 is:

latency = depth*(53 line byte periods) + 16 line byte periods (min.)
= depth*(53 line byte periods) + 26 line byte periods (max.).

The latency for the cell being written in STS-1 is:

latency = depth*(53 line byte periods) + 10 line byte periods (min.)
= depth*(53 line byte periods) + 14 line byte periods (max.).

The presence of the SONET/SDH overhead accounts for the difference between the minimum and maximum latencies.

When the FIFO contains four cells and the upstream device writes into the FIFO, the TACP indicates a FIFO overrun condition using a maskable interrupt and register bits. The offending write and all subsequent writes are ignored until there is room in the FIFO.

9.13 Saturn Compliant Split-Bus PHY Interface (SPHY)

The Saturn Compliant Split-Bus PHY Interface block (SPHY) permits the two receive cell FIFOs (RXFF) and the two transmit cell FIFOs (TXFF) to share a single cell interface on the S/UNI-DUAL.

Two interface modes are supported: 1) Split-Bus Direct-PHY addressing (when the SPLIT bit in S/UNI-DUAL Interface Control register is logic 1), and 2) Multi-PHY selection (when the SPLIT bit is logic 0).

When Split-Bus addressing is enabled, both transmit/receive FIFOs are accessible. The FIFOs are limited to 8-bit mode. The transmit FIFO for channel #1 uses TDAT[7:0], TSOC[1], TWRENB[1], TCA[1] and TXPRTY[0]. The transmit FIFO for channel #2 uses TDAT[15:8], TSOC[2], TWRENB[2], TCA[2] and TXPRTY[1]. The receive FIFO for channel #1 uses RDAT[7:0], RSOC[1], RRDENB[1], RCA[1] and RXPRTY[0]. The receive FIFO for channel #2 uses RDAT[15:8], RSOC[2], RRDENB[2], RCA[2] and RXPRTY[1].

When Multi-PHY selection is enabled, one of two possible transmit/receive FIFOs is selected by the corresponding TWRENB[2:1]/RRDENB[2:1] signal respectively. The cell available status for each of the transmit and receive FIFOs is directly available on RCA[2:1] and TCA[2:1]. The transmit/receive FIFOs can operate in 8-bit mode (BUS8 bit in S/UNI-DUAL is logic 1) or in 16-bit mode (BUS8 bit is logic 0). With Multi-PHY selected, TSOC[2] and RSOC[2] are not used.

9.14 Microprocessor Interface

The microprocessor interface block provides normal and test mode registers, and the logic required to connect to the microprocessor interface. The normal mode registers are required for normal operation, and test mode registers are used to enhance the testability of the S/UNI-DUAL.

10 REGISTER MEMORY MAP

Address		Register
#1	#2	
0x000		S/UNI-DUAL Master Reset and Identity / Channel #1 Monitoring Update
0x080		S/UNI-DUAL Channel #2 Monitoring Update
0x001	0x081	S/UNI-DUAL Configuration
0x002	0x082	S/UNI-DUAL Interrupt Status
0x003		S/UNI-DUAL Master Mode Control
0x083		Reserved
0x004		S/UNI-DUAL Master Clock Monitor
0x084		Reserved
0x005	0x085	S/UNI-DUAL Control
0x006		S/UNI-DUAL Clock Synthesis Control and Status
0x086		Reserved
0x007	0x087	S/UNI-DUAL Clock Recovery Control and Status
0x008		S/UNI-DUAL Interface Control
0x009		S/UNI-DUAL Output Port Control
0x00A		S/UNI-DUAL POP[0] Strobe Rate
0x00B		S/UNI-DUAL POP[1] Strobe Rate
0x00C		S/UNI-DUAL POP[2] Strobe Rate
0x00D		S/UNI-DUAL POP[3] Strobe Rate
0x088-0x08D		Reserved
0x00E	0x08E	Transmit Synchronization Status
0x00F	0x08F	Reserved
0x010	0x090	RSOP Control/Interrupt Enable
0x011	0x091	RSOP Status/Interrupt Status
0x012	0x092	RSOP Section BIP-8 LSB

Address		Register
#1	#2	
0x013	0x093	RSOP Section BIP-8 MSB
0x014	0x094	TSOP Control
0x015	0x095	TSOP Diagnostic
0x016-0x017	0x096-0x097	TSOP Reserved
0x018	0x098	RLOP Control/Status
0x019	0x099	RLOP Interrupt Enable/Status
0x01A	0x09A	RLOP Line BIP-8/24 LSB
0x01B	0x09B	RLOP Line BIP-8/24
0x01C	0x09C	RLOP Line BIP-8/24 MSB
0x01D	0x09D	RLOP Line FEBE LSB
0x01E	0x09E	RLOP Line FEBE
0x01F	0x09F	RLOP Line FEBE MSB
0x020	0x0A0	TLOP Control
0x021	0x0A1	TLOP Diagnostic
0x022	0x0A2	TLOP Transmit K1
0x023	0x0A3	TLOP Transmit K2
0x024-0x02F	0x0A4-0x0AF	Reserved
0x030	0x0B0	RPOP Status/Control
0x031	0x0B1	RPOP Interrupt Status
0x032	0x0B2	RPOP Reserved
0x033	0x0B3	RPOP Interrupt Enable
0x034	0x0B4	RPOP Reserved
0x035	0x0B5	RPOP Reserved
0x036	0x0B6	RPOP Reserved
0x037	0x0B7	RPOP Path Signal Label

Address		Register
#1	#2	
0x038	0x0B8	RPOP Path BIP-8 LSB
0x039	0x0B9	RPOP Path BIP-8 MSB
0x03A	0x0BA	RPOP Path FEBE LSB
0x03B	0x0BB	RPOP Path FEBE MSB
0x03C	0x0BC	RPOP Reserved
0x03D	0x0BD	RPOP Path BIP-8 Configuration
0x03E-0x03F	0x0BE-0x0BF	RPOP Reserved
0x040	0x0C0	TPOP Control/Diagnostic
0x041	0x0C1	TPOP Pointer Control
0x042	0x0C2	TPOP Reserved
0x043	0x0C3	TPOP Reserved
0x044	0x0C4	TPOP Reserved
0x045	0x0C5	TPOP Arbitrary Pointer LSB
0x046	0x0C6	TPOP Arbitrary Pointer MSB
0x047	0x0C7	TPOP Reserved
0x048	0x0C8	TPOP Path Signal Label
0x049	0x0C9	TPOP Path Status
0x04A	0x0CA	TPOP Reserved
0x04B-0x04F	0x0CB-0x0CF	TPOP Reserved
0x050	0x0D0	RACP Control/Status
0x051	0x0D1	RACP Interrupt Enable/Status
0x052	0x0D2	RACP Match Header Pattern
0x053	0x0D3	RACP Match Header Mask
0x054	0x0D4	RACP Correctable HCS Error Count
0x055	0x0D5	RACP Uncorrectable HCS Error Count

Address		Register
#1	#2	
0x056	0x0D6	RACP Receive Cell Counter (LSB)
0x057	0x0D7	RACP Receive Cell Counter
0x058	0x0D8	RACP Receive Cell Counter (MSB)
0x059	0x0D9	RACP Configuration
0x05A-0x05F	0x0DA-0x0DF	RACP Reserved
0x060	0x0E0	TACP Control/Status
0x061	0x0E1	TACP Idle/Unassigned Cell Header Pattern
0x062	0x0E2	TACP Idle/Unassigned Cell Payload Octet Pattern
0x063	0x0E3	TACP FIFO Configuration
0x064	0x0E4	TACP Transmit Cell Counter (LSB)
0x065	0x0E5	TACP Transmit Cell Counter
0x066	0x0E6	TACP Transmit Cell Counter (MSB)
0x067	0x0E7	TACP Configuration
0x068	0x0E8	RASE Interrupt Enable
0x069	0x0E9	RASE Interrupt Status
0x06A	0x0EA	RASE Configuration/Control
0x06B	0x0EB	RASE SF Accumulation Period (LSB)
0x06C	0x0EC	RASE SF Accumulation Period
0x06D	0x0ED	RASE SF Accumulation Period (MSB)
0x06E	0x0EE	RASE SF Saturation Threshold (LSB)
0x06F	0x0EF	RASE SF Saturation Threshold (MSB)
0x070	0x0F0	RASE SF Declaring Threshold (LSB)
0x071	0x0F1	RASE SF Declaring Threshold (MSB)
0x072	0x0F2	RASE SF Clearing Threshold (LSB)
0x073	0x0F3	RASE SF Clearing Threshold (MSB)
0x074	0x0F4	RASE Reserved

Address		Register
#1	#2	
0x075	0x0F5	RASE Reserved
0x076	0x0F6	RASE Reserved
0x077	0x0F7	RASE Reserved
0x078	0x0F8	RASE Reserved
0x079	0x0F9	RASE Reserved
0x07A	0x0FA	RASE Reserved
0x07B	0x0FB	RASE Reserved
0x07C	0x0FC	RASE Reserved
0x07D	0x0FD	RASE Receive K1
0x07E	0x0FE	RASE Receive K2
0x07F	0x0FF	RASE Receive S1
0x100		S/UNI-DUAL Master Test
0x101-0x1FF		Reserved for Test

11 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the S/UNI-DUAL. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[8]) is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the S/UNI-DUAL to determine the programming state of the block. The master test register is an exception.

3. Writable normal mode register bits are cleared to logic zero upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect S/UNI-DUAL operation unless otherwise noted.

5. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the S/UNI-DUAL operates as intended, reserved register bits must only be written with logic zero. Similarly, writing to reserved registers should be avoided.

Register 0x000: S/UNI-DUAL Master Reset and Identity / Channel #1 Monitoring Update

Bit	Type	Function	Default
Bit 7	R/W	RESET	0
Bit 6	R	TYPE[2]	1
Bit 5	R	TYPE[1]	1
Bit 4	R	TYPE[0]	0
Bit 3	R	TIP	X
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	0
Bit 0	R	ID[0]	1

This register allows the revision of the S/UNI-DUAL to be read by software permitting graceful migration to support for newer, feature enhanced versions of the S/UNI-DUAL. It also provides software reset capability.

Writing this register loads all the error counters in the RSOP, RLOP, RPOP, RACP and TACP blocks in channel #1.

ID[3:0]:

The ID bits can be read to provide a binary S/UNI-DUAL revision number.

TIP:

The TIP bit is set to a logic one when any value with the RESET bit set to logic 0 is written to this register. Such a write initiates an accumulation interval transfer and loads all the performance meter registers in the RSOP, RLOP, RPOP, RACP, and TACP blocks for channel #1. TIP remains high while the transfer is in progress, and is set to a logic zero when the transfer is complete. TIP can be polled by a microprocessor to determine when the accumulation interval transfer is complete.

TYPE[2:0]:

The TYPE bits distinguish the S/UNI-DUAL from the other members of the S/UNI family of devices.

RESET:

The RESET bit allows the S/UNI-DUAL to be reset under software control. If the RESET bit is a logic one, the entire S/UNI-DUAL is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the S/UNI-DUAL out of reset. Holding the S/UNI-DUAL in a reset state places it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus negating the software reset. Otherwise, the effect of a software reset is equivalent to that of a hardware reset.

Register 0x080: S/UNI-DUAL Channel #2 Monitoring Update

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	TIP	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

Writing this register loads all the error counters in the RSOP, RLOP, RPOP, RACP and TACP blocks in channel #2.

TIP:

The TIP bit is set to a logic one when any value is written to this register. Such a write initiates an accumulation interval transfer and loads all the performance meter registers in the RSOP, RLOP, RPOP, RACP, and TACP blocks for channel #2. TIP remains high while the transfer is in progress, and is set to a logic zero when the transfer is complete. TIP can be polled by a microprocessor to determine when the accumulation interval transfer is complete.

Register 0x001, 0x081: S/UNI-DUAL Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	AUTOFEBE	1
Bit 5	R/W	AUTOLRDI	1
Bit 4	R/W	AUTOPRDI	1
Bit 3	R/W	TCAINV	0
Bit 2	R/W	RCAINV	0
Bit 1	R/W	RXDINV	0
Bit 0		Unused	X

RXDINV:

The RXDINV bit selects the active polarity of the RXD+/- signals. The default configuration selects RXD+ to be active high and RXD- to be active low. When RXDINV is set to logic one, RXD+ to be active low and RXD- to be active high.

RCAINV:

The RCAINV bit selects the active polarity of the RCA signal. The default configuration selects RCA to be active high, indicating that a received cell is available when high. When RCAINV is set to logic one, the RCA signal becomes active low.

TCAINV:

The TCAINV bit selects the active polarity of the TCA signal. The default configuration selects TCA to be active high, indicating that a cell is available in the transmit FIFO when high. When TCAINV is set to logic one, the TCA signal becomes active low.

AUTOPRDI

The AUTOPRDI bit determines whether STS path remote defect indication (RDI) is sent immediately upon detection of an incoming alarm. When AUTOPRDI is set to logic one, STS path RDI is inserted immediately upon declaration of loss of signal (LOS), loss of frame (LOF), line AIS, loss of pointer (LOP) or STS path AIS.

AUTOLRDI

The AUTOLRDI bit determines whether line remote defect indication (RDI) is sent immediately upon detection of an incoming alarm. When AUTOLRDI is set to logic one, line RDI is inserted immediately upon declaration of loss of signal (LOS), loss of frame (LOF) or line AIS.

AUTOFEBE

The AUTOFEBE bit determines whether line and path far end block errors are sent upon detection of an incoming line and path BIP error events. When AUTOFEBE is set to logic one, one line or path FEBE is inserted for each line or path BIP error event, respectively. When AUTOFEBE is set to logic zero, incoming line or path BIP error events do not generate FEBE events.

Register 0x002, 0x082: S/UNI-DUAL Interrupt Status

Bit	Type	Function	Default
Bit 7	R	TROOLI	X
Bit 6	R	LCDI	X
Bit 5	R	RDOOLI	X
Bit 4	R	TACPI	X
Bit 3	R	RACPI	X
Bit 2	R	RPOPI	X
Bit 1	R	RLOPI	X
Bit 0	R	RSOPI	X

This register allows the source of an active interrupt to be identified down to the block level. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RSOPI:

The RSOPI bit is high when an interrupt request is active from the RSOP block. The RSOP interrupt sources are enabled in the RSOP Control/Interrupt Enable Register.

RLOPI:

The RLOPI bit is high when an interrupt request is active from the RLOP or RASE block. The RLOP interrupt sources are enabled in the RLOP Interrupt Enable/Status Register and in the RASE Interrupt Enable Register.

RPOPI:

The RPOPI bit is high when an interrupt request is active from the RPOP block. The RPOP interrupt sources are enabled in the RPOP Interrupt Enable Register.

RACPI:

The RACPI bit is high when an interrupt request is active from the RACP block. The RACP interrupt sources are enabled in the RACP Interrupt Enable/Status Register.

TACPI:

The TACPI bit is high when an interrupt request is active from the TACP block. The TACP interrupt sources are enabled in the TACP Interrupt Control/Status Register.

RDOOLI:

The RDOOLI bit is the receive data out of lock interrupt status bit. RDOOLI is set high when the RDOOLV bit of the S/UNI-DUAL Clock Recovery Control and Status register changes state. RDOOLV is a logic one if the divided down recovered clock frequency not within 488 ppm of the REFCLK+/- frequency or if no transitions have occurred on the RXD+/- inputs for more than 80 bit periods. RDOOLI is cleared when this register is read.

LCDI:

The LCDI interrupt bit is set high when entering and exiting loss of cell delineation. This bit is reset immediately after a read to this register. The LCD interrupt is enabled in the S/UNI-DUAL Master Control Register.

TROOLI:

The TROOLI bit is the transmit reference out of lock interrupt status bit. TROOLI is set high when the TROOLV bit of the S/UNI-DUAL Clock Synthesis Control and Status register changes state. TROOLV indicates the clock synthesis phase locked loop is unable to lock to the reference on REFCLK+/- and is a logic one if the divided down synthesized clock frequency not within 488 ppm of the REFCLK+/- frequency. TROOLI is cleared when this register is read.

Register 0x003: S/UNI-DUAL Master Mode Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	RATE[1]	1
Bit 0	R/W	RATE[0]	1

RATE[1:0]:

The RATE[1:0] bits select the operation rate of the S/UNI-DUAL. The default configuration selects STS-3c rate operation. The S/UNI-DUAL will not operate correctly if a Reserved mode is selected.

RATE[1:0]	MODE
00	Reserved
01	Reserved
10	51.84 Mbit/s, STS-1
11	155.52 Mbit/s, STS-3c/STM-1

Register 0x004: S/UNI-DUAL Master Clock Monitor

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	REFCLKA	X
Bit 1	R	RFCLKA	X
Bit 0	R	TFCLKA	X

This register provides activity monitoring on S/UNI-DUAL input clocks. When a monitored clock signal makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read at periodic intervals to detect clock failures.

TFCLKA:

The TFCLK active (TFCLKA) bit monitors for low to high transitions on the TFCLK output. TFCLKA is set high on a rising edge of TFCLK, and is set low when this register is read.

RFCLKA:

The RFCLK active (RFCLKA) bit monitors for low to high transitions on the RFCLK output. RFCLKA is set high on a rising edge of RFCLK, and is set low when this register is read.

REFCLKA:

The REFCLK active (REFCLKA) bit monitors for low to high transitions on the REFCLK+ and REFCLK- inputs. REFCLKA is set high on a rising edge of REFCLK+, and is set low when this register is read.

Register 0x005, 0x085: S/UNI-DUAL Control

Bit	Type	Function	Default
Bit 7	R/W	LCDE	0
Bit 6	R	LCDV	X
Bit 5	R/W	FIXPTR	1
Bit 4		Unused	X
Bit 3	R/W	PDLE	0
Bit 2	R/W	LLE	0
Bit 1	R/W	SDLE	0
Bit 0	R/W	LOOPT	0

This register controls the timing and high speed loopback features of the S/UNI-DUAL.

LOOPT:

The LOOPT bit selects the source of timing for the transmit section of the S/UNI-DUAL. When LOOPT is a logic zero, the transmitter timing is derived from inputs REFCLK+ and REFCLK-. When LOOPT is a logic one, the transmitter timing is derived from the receiver inputs RXD+ and RXD-.

SDLE:

The SDLE bit enables the serial diagnostic loopback. When SDLE is a logic one, the transmit serial stream is connected to the receive stream. The SDLE and the LLE bits should not be set high simultaneously.

LLE:

The LLE bit enables the S/UNI-DUAL line loopback. When LLE is a logic one, the value on RXD+/- differential inputs is mapped to the TXD+/- differential outputs. The SDLE and the LLE bits should not be set high simultaneously.

PDLE:

The PDLE bit enables the parallel diagnostic loopback. When PDLE is a logic one, the transmit parallel stream is connected to the receive stream. The loopback point is between the TPOP and the RPOP blocks. Blocks upstream of the loopback point continue to operate normally. For example line AIS may

be inserted in the transmit stream upstream of the loopback point using the TSOP Control register.

FIXPTR:

The FIXPTR bit disables transmit payload pointer adjustments. If the FIXPTR bit is a logic 1, the transmit payload pointer is set at 522. If FIXPTR is a logic zero, the payload pointer is controlled by the contents of the TPOP Pointer Control register.

LCDV:

The LCDV bit reflects the current loss of cell delineation state. LCDV becomes a logic 1 when an out of cell delineation state has persisted for 4ms without any lower level alarms (LOS, LOP, Path AIS, Line AIS) occurring. LCDV becomes logic 0 when the SYNC state has been maintained for 4ms.

LCDE:

The LCDE bit enables the loss of cell delineation (LCD) interrupt. When logic one, the S/UNI-DUAL INTB output is asserted when there is a change in the LCD state. When logic zero, the S/UNI-DUAL INTB output is not affected by the change in LCD state.

Register 0x006: S/UNI-DUAL Clock Synthesis Control and Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	TROOLV	X
Bit 2		Unused	X
Bit 1	R/W	TROOLE	0
Bit 0	R/W	REFSEL	0

This register controls the clock synthesis and reports the state of the transmit phase locked loop.

REFSEL:

The reference select (REFSEL) bit determines the expected frequency of REFCLK+/-. If REFSEL is a logic 0, the correct line clock frequency is synthesized if the reference frequency is 19.44 MHz. If REFSEL is a logic 1, the reference frequency must be 6.48 MHz.

TROOLE:

The TROOLE bit is an interrupt enable for the transmit reference out of lock status. When TROOLE is set to logic one, an interrupt is generated when the TROOLV bit changes state.

TROOLV:

The transmit reference out of lock status indicates the clock synthesis phase locked loop is unable to lock to the reference on REFCLK+/-. TROOLV is a logic one if the divided down synthesized clock frequency not within 488 ppm of the REFCLK+/- frequency. While the PLL is locking onto the reference clock, the TROOLV status will make numerous transitions before stabilizing low. To correctly interpret that the divided down transmit and reference (REFCLK+/-) frequencies are within 488 ppm, TROOLV and TROOLI should be polled at 100 ms intervals. When TROOLV and TROOLI are both polled at logic 0 then the divided down transmit clock and the reference clock are within 488 ppm.

Register 0x007, 0x087: S/UNI-DUAL Clock Recovery Control and Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RDOOLV	X
Bit 2		Unused	X
Bit 1	R/W	RDOOLE	0
Bit 0		Unused	X

This register controls the clock recovery and reports the state of the receive phase locked loop.

RDOOLE:

The RDOOLE bit is an interrupt enable for the receive data out of lock status. When RDOOLE is set to logic one, an interrupt is generated when the RDOOLV bit changes state.

RDOOLV:

The receive data out of lock status indicates the clock recovery phase locked loop is unable to lock to the incoming data stream. RDOOLV is a logic one if the divided down recovered clock frequency not within 488 ppm of the REFCLK+/- frequency or if no transitions have occurred on the RXD+/- inputs for more than 80 bit periods. While the PLL is locking onto the incoming data, the RDOOLV status will make numerous transitions before stabilizing low. To correctly interpret that the divided down PLL and reference (REFCLK+/-) frequencies are within 488 ppm, RDOOLV and RDOOLI should be polled at 100 ms intervals. When RDOOLV and RDOOLI are both polled at logic 0 then the divided down recovered clock and the reference clock are within 488 ppm.

Register 0x008: S/UNI-DUAL Interface Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	CELL_PULSE	0
Bit 4	R/W	RFP_CH1	1
Bit 3	R/W	TFP_TS	1
Bit 2	R/W	ALARM	1
Bit 1	R/W	BUS8	1
Bit 0	R/W	SPLIT	1

SPLIT:

The Split-Bus PHY interface (SPLIT) bit selects the PHY interface mode. If SPLIT is a logic 0, the Multi-PHY interface mode is used. If SPLIT is a logic 1, the Split-Bus Direct-PHY FIFO interface mode is used.

BUS8:

The 8-bit FIFO interface (BUS8) bit selects between 8-bit and 16-bit data bus in the Multi-PHY interface mode. If BUS8 is a logic 0, the Multi-PHY interface uses the 16-bit data bus. If BUS8 is a logic 1, the Multi-PHY interface uses the 8-bit data bus. If SPLIT is a logic 1, the BUS8 setting is ignored.

ALARM:

The receive alarm interface (ALARM) bit determines whether the RALM2 and RALM1 outputs are controlled by the internal alarm conditions or by the POP[3:2] bits of the S/UNI-DUAL Output Port Control register. If ALARM is a logic 0, the activity on RALM2 and RALM1 are controlled by POP[3:2], respectively. If ALARM is a logic 1, the activity on RALM2 and RALM1 is controlled by the receive alarms for each corresponding channel.

TFP_TS:

The transmit frame pulse tri-state (TFP_TS) bit determines whether the TFP pin is used as an output or held in tri-state mode. When TFP_TS is a logic 0, TFP outputs the transmit overhead frame pulse for external use (see transmit section overhead processor section of the functional description). If TFP_TS is a logic 1, TFP is held in tri-state.

RFP_CH1:

The channel #1 receive frame pulse output interface (RFP_CH1) bit determines whether the RFP output source is channel #1 or channel #2. If RFP_CH1 is a logic 0, RFP outputs the receive frame pulse from channel #2. If RFP_CH1 is a logic 1, RFP outputs the receive frame pulse from channel #1.

CELL_PULSE:

The receive/transmit cell pulse selection (CELL_PULSE) bit decides whether the pulse generator or the strobe rate generator is used when toggling for the corresponding port is enabled. If CELL_PULSE is a logic 1 and toggling is enabled for the corresponding output, a 100ms pulse is generated on that output when its corresponding cell event occurs. RALM2 corresponds to a transmit cell event on channel #2, RALM1 corresponds to a receive cell event on channel #2, OUT[1] corresponds to a transmit cell event on channel #1, and OUT[0] corresponds to a receive cell event on channel #1. If CELL_PULSE is a logic 0 and toggling is enabled, the strobe rate for the corresponding output is used. The CELL_PULSE bit and the ALARM bit should not be asserted at the same time as it will defeat the purpose of both bits.

Register 0x009: S/UNI-DUAL Output Port Control

Bit	Type	Function	Default
Bit 7	R/W	POP[3]	0
Bit 6	R/W	POP[2]	0
Bit 5	R/W	POP[1]	0
Bit 4	R/W	POP[0]	0
Bit 3	R/W	TOGL[3]	0
Bit 2	R/W	TOGL[2]	0
Bit 1	R/W	TOGL[1]	0
Bit 0	R/W	TOGL[0]	0

TOGL[3:0]:

The output pin toggle (TOGL[3:0]) bits determine whether the corresponding output port is held at a constant value or toggles. If TOGL is a logic 0, the corresponding output is a steady state signal. If TOGL is a logic 1, the corresponding output is a pulse generated signal or a strobe rate generated signal, as selected by CELL_PULSE.

POP[3:0]:

The values written to the POP[3:0] bits either directly correspond to the states set on the corresponding output pins or enable the corresponding pin to strobe at a selectable rate. POP[3:2] corresponds to outputs RALM2 and RALM1, when the ALARM bit is set to logic 0; POP[1:0] corresponds to outputs OUT[1:0]. This provides a generic port useful for controlling an external PMD device or supplying external LED drivers.

Register 0x00A: S/UNI-DUAL POP[0] Strobe Rate

Bit	Type	Function	Default
Bit 7	R/W	RATE0[7]	0
Bit 6	R/W	RATE0[6]	0
Bit 5	R/W	RATE0[5]	1
Bit 4	R/W	RATE0[4]	1
Bit 3	R/W	RATE0[3]	1
Bit 2	R/W	RATE0[2]	1
Bit 1	R/W	RATE0[1]	1
Bit 0	R/W	RATE0[0]	0

RATE0[7:0]:

The POP[0] strobe rate (RATE0[7:0]) bits determine the period (in milliseconds increasing in 8 ms increments) of the OUT[0] output pin. The default setting is for a strobe period of 496 ms, resulting in a 2.0 Hz strobe. If enabled and the strobe rate value is set to 0x00, then the output pin will be held at logic 0.

Register 0x00B: S/UNI-DUAL POP[1] Strobe Rate

Bit	Type	Function	Default
Bit 7	R/W	RATE1[7]	0
Bit 6	R/W	RATE1[6]	0
Bit 5	R/W	RATE1[5]	0
Bit 4	R/W	RATE1[4]	0
Bit 3	R/W	RATE1[3]	0
Bit 2	R/W	RATE1[2]	1
Bit 1	R/W	RATE1[1]	1
Bit 0	R/W	RATE1[0]	0

RATE1[7:0]:

The POP[1] strobe rate (RATE1[7:0]) bits determine the period (in milliseconds increasing in 8 ms increments) of the OUT[1] output pin. The default setting is for a strobe period of 48 ms, resulting in a 20.8 Hz strobe. If enabled and the strobe rate value is set to 0x00, then the output pin will be held at logic 0.

Register 0x00C: S/UNI-DUAL POP[2] Strobe Rate

Bit	Type	Function	Default
Bit 7	R/W	RATE2[7]	0
Bit 6	R/W	RATE2[6]	0
Bit 5	R/W	RATE2[5]	1
Bit 4	R/W	RATE2[4]	1
Bit 3	R/W	RATE2[3]	1
Bit 2	R/W	RATE2[2]	1
Bit 1	R/W	RATE2[1]	1
Bit 0	R/W	RATE2[0]	0

RATE2[7:0]:

The POP[2] strobe rate (RATE2[7:0]) bits determine the period (in milliseconds increasing in 8 ms increments) of the RALM1 output pin. The default setting is for a strobe period of 496 ms, resulting in a 2.0 Hz strobe. If enabled and the strobe rate value is set to 0x00, then the output pin will be held at logic 0.

Register 0x00D: S/UNI-DUAL POP[3] Strobe Rate

Bit	Type	Function	Default
Bit 7	R/W	RATE3[7]	0
Bit 6	R/W	RATE3[6]	0
Bit 5	R/W	RATE3[5]	0
Bit 4	R/W	RATE3[4]	0
Bit 3	R/W	RATE3[3]	0
Bit 2	R/W	RATE3[2]	1
Bit 1	R/W	RATE3[1]	1
Bit 0	R/W	RATE3[0]	0

RATE3[7:0]:

The POP[3] strobe rate (RATE3[7:0]) bits determine the period (in milliseconds increasing in 8 ms increments) of the RALM2 output pin. The default setting is for a strobe period of 48 ms, resulting in a 20.8 Hz strobe. If enabled and the strobe rate value is set to 0x00, then the output pin will be held at logic 0.

Register 0x00E, 0x08E: Transmit Synchronization Status

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	TS1[3]	0
Bit 2	R/W	TS1[2]	0
Bit 1	R/W	TS1[1]	0
Bit 0	R/W	TS1[0]	0

TS1[3:0]:

The value written to these bit positions is inserted in the first S1 byte position of the transmit stream. The S1 byte is used to carry synchronization status messages between line terminating network elements. TS1[3] is the most significant bit, corresponding to the first synchronization status bit (bit 5 of the S1 byte) transmitted. TS1[0] is the least significant bit, corresponding to the last synchronization status bit (bit 8 of the S1 byte) transmitted.

Reserved:

The reserved bits must be programmed to logic 0 for proper operation.

Register 0x010, 0x090: RSOP Control/Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	DDS	0
Bit 5	W	FOOF	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	BIPEE	0
Bit 2	R/W	LOSE	0
Bit 1	R/W	LOFE	0
Bit 0	R/W	OOFE	0

OOFE:

The OOFE bit is an interrupt enable for the out of frame alarm. When OOFE is set to logic one, an interrupt is generated when the out of frame alarm changes state.

LOFE:

The LOFE bit is an interrupt enable for the loss of frame alarm. When LOFE is set to logic one, an interrupt is generated when the loss of frame alarm changes state.

LOSE:

The LOSE bit is an interrupt enable for the loss of signal alarm. When LOSE is set to logic one, an interrupt is generated when the loss of signal alarm changes state.

BIPEE:

The BIPEE bit is an interrupt enable for the section BIP-8 errors. When BIPEE is set to logic one, an interrupt is generated when a section BIP-8 error (B1) is detected.

FOOF:

The FOOF bit controls the framing of the RSOP. When a logic one is written to FOOF, the RSOP is forced out of frame at the next frame boundary. The FOOF bit is a write only bit, register reads may yield a logic one or a logic zero.

DDS:

The DDS bit is set to logic one to disable the descrambling of the STS-3c (STM-1) stream. When DDS is a logic zero, descrambling is enabled.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x011, 0x091: RSOP Status/Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	BIPEI	X
Bit 5	R	LOSI	X
Bit 4	R	LOFI	X
Bit 3	R	OOFI	X
Bit 2	R	LOSV	X
Bit 1	R	LOFV	X
Bit 0	R	OOFV	X

OOFV:

The OOFV bit is read to determine the out of frame state of the RSOP. When OOFV is high, the RSOP is out of frame. When OOFV is low, the RSOP is in-frame.

LOFV:

The LOFV bit is read to determine the loss of frame state of the RSOP. When LOFV is high, the RSOP has declared loss of frame.

LOSV:

The LOSV bit is read to determine the loss of signal state of the RSOP. When LOSV is high, the RSOP has declared loss of signal.

OOFI:

The OOFI bit is the out of frame interrupt status bit. OOFI is set high when a change in the out of frame state occurs. This bit is cleared when this register is read.

LOFI:

The LOFI bit is the loss of frame interrupt status bit. LOFI is set high when a change in the loss of frame state occurs. This bit is cleared when this register is read.

LOSI:

The LOSI bit is the loss of signal interrupt status bit. LOSI is set high when a change in the loss of signal state occurs. This bit is cleared when this register is read.

BIPEI:

The BIPEI bit is the section BIP-8 interrupt status bit. BIPEI is set high when a section layer (B1) bit error is detected. This bit is cleared when this register is read.

Register 0x012, 0x092: RSOP Section BIP-8 LSB

Bit	Type	Function	Default
Bit 7	R	SBE[7]	X
Bit 6	R	SBE[6]	X
Bit 5	R	SBE[5]	X
Bit 4	R	SBE[4]	X
Bit 3	R	SBE[3]	X
Bit 2	R	SBE[2]	X
Bit 1	R	SBE[1]	X
Bit 0	R	SBE[0]	X

Register 0x013, 0x093: RSOP Section BIP-8 MSB

Bit	Type	Function	Default
Bit 7	R	SBE[15]	X
Bit 6	R	SBE[14]	X
Bit 5	R	SBE[13]	X
Bit 4	R	SBE[12]	X
Bit 3	R	SBE[11]	X
Bit 2	R	SBE[10]	X
Bit 1	R	SBE[9]	X
Bit 0	R	SBE[8]	X

SBE[15:0]:

Bits SBE[15:0] represent the number of section BIP-8 errors (B1) that have been detected since the last time the error count was polled. The error count is polled by writing to either of the RSOP Section BIP-8 Register addresses. Such a write transfers the internally accumulated error count to the Section BIP-8 registers within approximately 1µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

The error count can also be polled by writing to the S/UNI-DUAL Master Reset and Identity / Channel #1 Monitoring Update register (0x000) or the S/UNI-DUAL Channel #2 Monitoring Update register (0x080). Writing to register address 0x000 loads all the error counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks of channel #1. Writing to register address 0x080 loads all the error counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks of channel #2.

Register 0x014, 0x094: TSOP Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DS	0
Bit 5	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	LAIS	0

LAIS:

The LAIS bit controls the insertion of line alarm indication signal (AIS). When LAIS is set to logic one, the TSOP inserts AIS into the transmit SONET stream. Activation or deactivation of line AIS insertion is synchronized to frame boundaries. Line AIS insertion results in all bits of the SONET frame being set to 1 prior to scrambling except for the section overhead. The LAIS bit is logically ORed with the external TLAIS input.

DS:

The DS bit is set to logic one to disable the scrambling of the STS-3c or STS-1 stream. When DS is a logic zero, scrambling is enabled.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x015, 0x095: TSOP Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	DLOS	0
Bit 1	R/W	DBIP8	0
Bit 0	R/W	DFP	0

DFP:

The DFP bit controls the insertion of a single bit error continuously in the most significant bit (bit 1) of the A1 section overhead framing byte. When DFP is set to logic one, the A1 bytes are set to 0x76 instead of 0xF6.

DBIP8:

The DBIP8 bit controls the insertion of bit errors continuously in the section BIP-8 byte (B1). When DBIP8 is set to logic one, the B1 byte is inverted.

DLOS:

The DLOS bit controls the insertion of all zeros in the transmit stream. When DLOS is set to logic one, the transmit stream is forced to 0x00.

Register 0x018, 0x098: RLOP Control/Status

Bit	Type	Function	Default
Bit 7	R/W	BIPWORD	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2		Unused	X
Bit 1	R	LAISV	0
Bit 0	R	RDIV	0

RDIV:

The RDIV bit is read to determine the remote defect indication state of the RLOP. When RDIV is high, the RLOP has declared line RDI.

LAISV:

The LAISV bit is read to determine the line AIS state of the RLOP. When LAISV is high, the RLOP has declared line AIS.

BIPWORD:

The BIPWORD bit controls the accumulation of B2 errors. When BIPWORD is logic one, the B2 error event counter is incremented only once per frame whenever one or more B2 bit errors occur during that frame. When BIPWORD is logic zero, the B2 error event counter is incremented for each B2 bit error that occurs during that frame (the counter can be incremented up to 8 times per frame for STS-1 and 24 times per frame for STS-3c).

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x019, 0x099: RLOP Interrupt Enable/Interrupt Status

Bit	Type	Function	Default
Bit 7	R/W	FEBEE	0
Bit 6	R/W	BIPEE	0
Bit 5	R/W	LAISE	0
Bit 4	R/W	RDIE	0
Bit 3	R	FEBEI	X
Bit 2	R	BIPEI	X
Bit 1	R	LAISI	X
Bit 0	R	RDII	X

RDII:

The RDII bit is the far end receive failure interrupt status bit. RDII is set high when a change in the line RDI state occurs. This bit is cleared when this register is read.

LAISI:

The LAISI bit is the line AIS interrupt status bit. LAISI is set high when a change in the line AIS state occurs. This bit is cleared when this register is read.

BIPEI:

The BIPEI bit is the line BIP interrupt status bit. BIPEI is set high when a line layer (B2) bit error is detected. This bit is cleared when this register is read.

FEBEI:

The FEBEI bit is the line far end block error interrupt status bit. FEBEI is set high when a line layer FEBE (Z2) is detected. This bit is cleared when this register is read.

RDIE:

The RDIE bit is an interrupt enable for the far end receive failure alarm. When RDIE is set to logic one, an interrupt is generated when RDI changes state.

LAISE:

The LAISE bit is an interrupt enable for line AIS. When LAISE is set to logic one, an interrupt is generated when line AIS changes state.

BIPEE:

The BIPEE bit is an interrupt enable for the line BIP-24 errors. When BIPEE is set to logic one, an interrupt is generated when a line BIP-24 error (B2) is detected.

FEBEE:

The FEBEE bit is an interrupt enable for the line far end block errors. When FEBE (Z2) is detected.

Register 0x01A, 0x09A: RLOP Line BIP-8/24 LSB

Bit	Type	Function	Default
Bit 7	R	LBE[7]	X
Bit 6	R	LBE[6]	X
Bit 5	R	LBE[5]	X
Bit 4	R	LBE[4]	X
Bit 3	R	LBE[3]	X
Bit 2	R	LBE[2]	X
Bit 1	R	LBE[1]	X
Bit 0	R	LBE[0]	X

Register 0x01B, 0x09B: RLOP Line BIP-8/24

Bit	Type	Function	Default
Bit 7	R	LBE[15]	X
Bit 6	R	LBE[14]	X
Bit 5	R	LBE[13]	X
Bit 4	R	LBE[12]	X
Bit 3	R	LBE[11]	X
Bit 2	R	LBE[10]	X
Bit 1	R	LBE[9]	X
Bit 0	R	LBE[8]	X

Register 0x01C, 0x09C: RLOP Line BIP-8/24 MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	LBE[19]	X
Bit 2	R	LBE[18]	X
Bit 1	R	LBE[17]	X
Bit 0	R	LBE[16]	X

LBE[19:0]

Bits LBE[19:0] represent the number of line BIP-8/24 errors (B2) that have been detected since the last time the error count was polled. The error count is polled by writing to any of the RLOP Line BIP Register or Line FEBE Register addresses. Such a write transfers the internally accumulated error count to the Line BIP Registers within approximately 1µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

The error count can also be polled by writing to the S/UNI-DUAL Master Reset and Identity / Channel #1 Monitoring Update register (0x000) or the S/UNI-DUAL Channel #2 Monitoring Update register (0x080). Writing to register address 0x000 loads all the error counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks of channel #1. Writing to register address 0x080 loads all the error counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks of channel #2.

Register 0x01D, 0x09D: RLOP Line FEBE LSB

Bit	Type	Function	Default
Bit 7	R	LFE[7]	X
Bit 6	R	LFE[6]	X
Bit 5	R	LFE[5]	X
Bit 4	R	LFE[4]	X
Bit 3	R	LFE[3]	X
Bit 2	R	LFE[2]	X
Bit 1	R	LFE[1]	X
Bit 0	R	LFE[0]	X

Register 0x01E, 0x09E: RLOP Line FEBE

Bit	Type	Function	Default
Bit 7	R	LFE[15]	X
Bit 6	R	LFE[14]	X
Bit 5	R	LFE[13]	X
Bit 4	R	LFE[12]	X
Bit 3	R	LFE[11]	X
Bit 2	R	LFE[10]	X
Bit 1	R	LFE[9]	X
Bit 0	R	LFE[8]	X

Register 0x01F, 0x09F: RLOP Line FEBE MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	LFE[19]	X
Bit 2	R	LFE[18]	X
Bit 1	R	LFE[17]	X
Bit 0	R	LFE[16]	X

LFE[19:0]

Bits LFE[19:0] represent the number of line FEBE errors (Z2) that have been detected since the last time the error count was polled. The error count is polled by writing to any of the RLOP Line BIP Register or Line FEBE Register addresses. Such a write transfers the internally accumulated error count to the Line FEBE Registers within approximately 1µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

The error count can also be polled by writing to the S/UNI-DUAL Master Reset and Identity / Channel #1 Monitoring Update register (0x000) or the S/UNI-DUAL Channel #2 Monitoring Update register (0x080). Writing to register address 0x000 loads all the error counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks of channel #1. Writing to register address 0x080 loads all the error counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks of channel #2.

Register 0x020, 0x0A0: TLOP Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	APSREG	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	RDI	0

RDI:

The RDI bit controls the insertion of line far end receive failure (RDI). When RDI is set to logic one, the TLOP inserts line RDI into the transmit SONET stream. Line RDI is inserted by transmitting the code 110 in bit positions 6, 7, and 8 of the K2 byte of the transmit stream.

APSREG:

The APSREG bit selects the source for the transmit APS channel. When APSREG is a logic zero, 0x0000 hexadecimal is inserted in the transmit APS channel. When APSREG is a logic one, the transmit APS channel is inserted from the TLOP Transmit K1 Register and the TLOP Transmit K2 Register.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x021, 0x0A1: TLOP Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	DBIP	0

DBIP24:

The DBIP bit controls the insertion of bit errors continuously in the line BIP byte(s) (B2). When DBIP is set to logic one, the B2 byte(s) are inverted.

Register 0x022, 0x0A2: TLOP Transmit K1

Bit	Type	Function	Default
Bit 7	R/W	K1[7]	0
Bit 6	R/W	K1[6]	0
Bit 5	R/W	K1[5]	0
Bit 4	R/W	K1[4]	0
Bit 3	R/W	K1[3]	0
Bit 2	R/W	K1[2]	0
Bit 1	R/W	K1[1]	0
Bit 0	R/W	K1[0]	0

K1[7:0]:

The K1[7:0] bits contain the value inserted in the K1 byte when the APSREG bit in the TLOP Control Register is a logic one. K1[7] is the most significant bit, corresponding to the first bit (bit 1) transmitted. K1[0] is the least significant bit, corresponding to the last bit (bit 8) transmitted. The bits in this register are double buffered so that register writes do not need to be synchronized to SONET/SDH frame boundaries. The insertion of a new APS code value is initiated by a write to this register. The contents of this register, and the TLOP Transmit K2 Register are inserted in the transmit stream starting at the next frame boundary. Successive writes to this register must be spaced at least two frames (250 µs) apart.

Register 0x023, 0x0A3: TLOP Transmit K2

Bit	Type	Function	Default
Bit 7	R/W	K2[7]	0
Bit 6	R/W	K2[6]	0
Bit 5	R/W	K2[5]	0
Bit 4	R/W	K2[4]	0
Bit 3	R/W	K2[3]	0
Bit 2	R/W	K2[2]	0
Bit 1	R/W	K2[1]	0
Bit 0	R/W	K2[0]	0

K2[7:0]:

The K2[7:0] bits contain the value inserted in the K2 byte when the APSREG bit in the TLOP Control Register is a logic one. K2[7] is the most significant bit, corresponding to the first bit (bit 1) transmitted. K2[0] is the least significant bit, corresponding to the last bit (bit 8) transmitted. The bits in this register are double buffered so that register writes do not need to be synchronized to SONET/SDH frame boundaries. The insertion of a new APS code value is initiated by a write to the TLOP Transmit K1 Register. A coherent APS code value is ensured by writing the desired K2 APS code value to this register before writing the TLOP Transmit K1 Register.

Register 0x030, 0x0B0: RPOP Status/Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5	R	LOP	X
Bit 4		Unused	X
Bit 3	R	PAIS	X
Bit 2	R	PRDI	X
Bit 1		Unused	X
Bit 0	R/W	Reserved	0

This register allows the status of path level alarms to be monitored.

PRDI, PAIS, LOP:

The PRDI, PAIS, and LOP bits reflect the current state of the corresponding path level alarms.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x031, 0x0B1: RPOP Interrupt Status

Bit	Type	Function	Default
Bit 7	R	PSLI	X
Bit 6		Unused	X
Bit 5	R	LOPI	X
Bit 4		Unused	X
Bit 3	R	PAISI	X
Bit 2	R	PRDII	X
Bit 1	R	BIPEI	X
Bit 0	R	FEBEI	X

This register allows identification and acknowledgment of path level alarm and error event interrupts.

FEBEI, BIPEI:

The BIPEI and FEBEI bits are set to logic one when the corresponding event, a path BIP-8 error or path FEBE is detected.

PRDII, PAISI, LOPI:

The PRDII, PAISI, and LOPI bits are set to logic one when a transition occurs in the corresponding alarm state.

PSLI:

The PSLI bit is set to logic one when a change is detected in the path signal label register. The current path signal label can be read from the RPOP Path Signal Label register.

These bits (and the interrupt) are cleared when this register is read.

Register 0x033, 0x0B3: RPOP Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	PSLE	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	LOPE	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	PAISE	0
Bit 2	R/W	PRDIE	0
Bit 1	R/W	BIPEE	0
Bit 0	R/W	FEBEE	0

This register allows interrupt generation to be enabled for path level alarm and error events.

FEBEE:

When a 1 is written to the FEBEE interrupt enable bit position, the reception of one or more FEBEs will activate the interrupt output.

BIPEE:

When a 1 is written to the BIPEE interrupt enable bit position, the detection of one or more path BIP-8 errors will activate the interrupt output.

PRDIE, PAISE:

When a 1 is written to the PRDIE interrupt enable bit position, a change in the path remote defect indication state will activate the interrupt output. When a 1 is written to the PAISE interrupt enable bit position, a change in the path AIS state will activate the interrupt output.

LOPE:

When a 1 is written to the LOPE interrupt enable bit position, a change in the loss of pointer state will activate the interrupt output.

PSLE:

When a 1 is written to the PSLE interrupt enable bit position, a change in the path signal label will activate the interrupt output.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x037, 0x0B7: RPOP Path Signal Label

Bit	Type	Function	Default
Bit 7	R	PSL[7]	X
Bit 6	R	PSL[6]	X
Bit 5	R	PSL[5]	X
Bit 4	R	PSL[4]	X
Bit 3	R	PSL[3]	X
Bit 2	R	PSL[2]	X
Bit 1	R	PSL[1]	X
Bit 0	R	PSL[0]	X

This register allows the received path signal label byte to be read.

PSL[7:0]:

The PSL7 - PSL0 bits contain the path signal label byte (C2). The value in this register is updated to a new path signal label value if the same new value is observed for three consecutive frames.

Register 0x038, 0x0B8: RPOP Path BIP-8 LSB

Bit	Type	Function	Default
Bit 7	R	PBE[7]	X
Bit 6	R	PBE[6]	X
Bit 5	R	PBE[5]	X
Bit 4	R	PBE[4]	X
Bit 3	R	PBE[3]	X
Bit 2	R	PBE[2]	X
Bit 1	R	PBE[1]	X
Bit 0	R	PBE[0]	X

Register 0x039, 0x0B9: RPOP Path BIP-8 MSB

Bit	Type	Function	Default
Bit 7	R	PBE[15]	X
Bit 6	R	PBE[14]	X
Bit 5	R	PBE[13]	X
Bit 4	R	PBE[12]	X
Bit 3	R	PBE[11]	X
Bit 2	R	PBE[10]	X
Bit 1	R	PBE[9]	X
Bit 0	R	PBE[8]	X

These registers allow path BIP-8 errors to be accumulated.

PBE[15:0]:

Bits PBE[15:0] represent the number of path BIP-8 errors (B3) that have been detected since the last time the error count was polled. The error count is polled by writing to either of the RPOP Path BIP-8 Register addresses or to either of the RPOP Path FEBE Register addresses. Such a write transfers the internally accumulated error count to the Path BIP-8 Registers within a maximum of 7µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

The error count can also be polled by writing to the S/UNI-DUAL Master Reset and Identity / Channel #1 Monitoring Update register (0x000) or the S/UNI-DUAL Channel #2 Monitoring Update register (0x080). Writing to register address 0x000 loads all the error counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks of channel #1. Writing to register address 0x080 loads all the error counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks of channel #2.

Register 0x03A, 0x0BA: RPOP Path FEBE LSB

Bit	Type	Function	Default
Bit 7	R	PFE7	X
Bit 6	R	PFE6	X
Bit 5	R	PFE5	X
Bit 4	R	PFE4	X
Bit 3	R	PFE3	X
Bit 2	R	PFE2	X
Bit 1	R	PFE1	X
Bit 0	R	PFE0	X

Register 0x03B, 0x0BB: RPOP Path FEBE MSB

Bit	Type	Function	Default
Bit 7	R	PFE15	X
Bit 6	R	PFE14	X
Bit 5	R	PFE13	X
Bit 4	R	PFE12	X
Bit 3	R	PFE11	X
Bit 2	R	PFE10	X
Bit 1	R	PFE9	X
Bit 0	R	PFE8	X

These registers allow path FEBEs to be accumulated.

PFE[15:0]:

Bits PFE[15:0] represent the number of path FEBE errors (G1) that have been detected since the last time the error count was polled. The error count is polled by writing to either of the RPOP Path BIP-8 Register addresses or to either of the RPOP Path FEBE Register addresses. Such a write transfers the internally accumulated error count to the Path FEBE Registers within a maximum of 7µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

The error count can also be polled by writing to the S/UNI-DUAL Master Reset and Identity / Channel #1 Monitoring Update register (0x000) or the S/UNI-DUAL Channel #2 Monitoring Update register (0x080). Writing to register address 0x000 loads all the error counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks of channel #1. Writing to register address 0x080 loads all the error counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks of channel #2.

Register 0x03D, 0x0BD: RPOP Path BIP-8 Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	BLKBIP	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

BLKBIP:

When set high, the block BIP-8 bit (BLKBIP) indicates that path BIP-8 errors are to be reported and accumulated on a block basis. A single BIP error is accumulated and reported to the return transmit path overhead processor if one or more of the BIP-8 results indicates a mismatch. When BLKBIP is set low, BIP-8 errors are accumulated and reported on a bit basis.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x040, 0x0C0: TPOP Control/Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	DB3	0
Bit 0	R/W	PAIS	0

This register allows insertion of path level alarms and diagnostic signals.

PAIS:

The PAIS bit controls the insertion of STS path alarm indication signal. When a logic one is written to this bit position, the complete SPE, and the pointer bytes (H1, H2, and H3) are overwritten with the all ones pattern. When a logic zero is written to this bit position, the pointer bytes and the SPE are processed normally.

DB3:

The DB3 bit controls the inversion of the B3 byte value. When a logic one is written to this bit position, the B3 byte is inverted, causing the insertion of eight path BIP-8 errors per frame. When a logic zero is written to this bit position, the B3 byte is transmitted uncorrupted.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x041, 0x0C1: TPOP Pointer Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	FTPTR	0
Bit 5	R/W	SOS	0
Bit 4	R/W	PLD	0
Bit 3	R/W	NDF	0
Bit 2	R/W	NSE	0
Bit 1	R/W	PSE	0
Bit 0	R/W	Reserved	0

This register allows control over the transmitted payload pointer for diagnostic purposes.

PSE:

The PSE bit controls the insertion of positive pointer movements. A zero to one transition on this bit enables the insertion of a single positive pointer justification in the outgoing stream. This register bit is automatically cleared when the pointer movement is inserted. This bit has no effect if the FIXPTR bit of the Master Control register is a logic 1.

NSE:

The NSE bit controls the insertion of negative pointer movements. A zero to one transition on this bit enables the insertion of a single negative pointer justification in the outgoing stream. This register bit is automatically cleared when the pointer movement is inserted. This bit has no effect if the FIXPTR bit of the Master Control register is a logic 1.

NDF:

The NDF bit controls the insertion of new data flags in the inserted payload pointer. When a logic one is written to this bit position, the pattern contained in the NDF[3:0] bit positions in the Arbitrary Pointer MSB Register is inserted continuously in the payload pointer. When a logic zero is written to this bit position, the normal pattern (0110) is inserted in the payload pointer.

PLD:

The PLD bit controls the loading of the pointer value contained in the Arbitrary Pointer Registers. Normally, the Arbitrary Pointer Registers are written to set up the arbitrary new pointer value and a logic one is then written to this bit position to load the new pointer value.

If a legal value (i.e. $0 \leq$ pointer value ≤ 782) is transferred from the Arbitrary Pointer Registers, the transmit payload pointer will immediately change to the corresponding byte position. If a value greater than 782 is transferred, the payload pointer remains unchanged.

This bit is automatically cleared after the new payload pointer has been loaded. This bit has no effect if the FIXPTR bit of the Master Control register is a logic 1.

SOS:

The SOS bit controls the stuff opportunity spacing between consecutive SPE positive or negative stuff events. When SOS is a logic zero, stuff events may be generated every frame as controlled by the PSE and NSE register bits described above. When SOS is a logic one, stuff events may be generated at a maximum rate of once every four frames.

FTPTR:

The force transmit pointer bit (FTPTR) enables the insertion of the pointer value contained in the Arbitrary Pointer Registers into the transmit stream for diagnostic purposes. This allows upstream payload mapping circuitry to continue functioning normally and a valid SPE to continue to be generated, although it is unlikely to be extracted by far end circuitry. If FTPTR is set to logic 1, the APTR[9:0] bits of the Arbitrary Pointer Registers are inserted into the H1 and H2 bytes of the transmit stream. At least one corrupted pointer is guaranteed to be sent. If FTPTR is a logic 0, a valid pointer is inserted.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x045, 0x0C5: TPOP Arbitrary Pointer LSB

Bit	Type	Function	Default
Bit 7	R/W	APTR[7]	0
Bit 6	R/W	APTR[6]	0
Bit 5	R/W	APTR[5]	0
Bit 4	R/W	APTR[4]	0
Bit 3	R/W	APTR[3]	0
Bit 2	R/W	APTR[2]	0
Bit 1	R/W	APTR[1]	0
Bit 0	R/W	APTR[0]	0

This register allows an arbitrary pointer to be inserted for diagnostic purposes.

APTR[7], APTR[6], APTR[5], APTR[4], APTR[3], APTR[2], APTR[1], APTR[0]:

The APTR[7:0] bits, along with the APTR[9:8] bits in the Arbitrary Pointer MSB Register are used to set an arbitrary payload pointer value. The arbitrary pointer value is transferred by writing a logic one to the PLD bit in the Pointer Control Register. A legal value (i.e. $0 \leq$ pointer value ≤ 782) results in the transmit payload pointer immediately changing to the corresponding byte position. If a value greater than 782 is transferred, the payload pointer remains unchanged.

If the FTPTR bit in the Pointer Control register is a logic 1, the current APTR[9:0] value is inserted into the payload pointer bytes (H1 and H2) in the transmit stream.

Register 0x046, 0x0C6: TPOP Arbitrary Pointer MSB

Bit	Type	Function	Default
Bit 7	R/W	NDF[3]	1
Bit 6	R/W	NDF[2]	0
Bit 5	R/W	NDF[1]	0
Bit 4	R/W	NDF[0]	1
Bit 3	R/W	S[1]	0
Bit 2	R/W	S[0]	0
Bit 1	R/W	APTR[9]	0
Bit 0	R/W	APTR[8]	0

This register allows an arbitrary pointer to be inserted for diagnostic purposes.

APTR[9], APTR[8]:

The APTR[9:8] bits, along with the APTR[7:0] bits in the TPOP Arbitrary Pointer LSB Register are used to set an arbitrary payload pointer value. The arbitrary pointer value is inserted in the outgoing stream by writing a logic one to the PLD bit in the TPOP Pointer Control Register.

S[1], S[0]:

The S[1:0] bits contain the value inserted in the S[1:0] bit positions (also referred to as the unused bits) in the payload pointer.

NDF[3], NDF[2], NDF[1], NDF[0]:

The NDF[3:0] bits contain the value inserted in the NDF bit positions when an arbitrary new payload pointer value is inserted (using the PLD bit in the Pointer Control Register) or when new data flag generation is enabled using the NDF bit in the TPOP Pointer Control Register.

Register 0x048, 0x0C8: TPOP Path Signal Label

Bit	Type	Function	Default
Bit 7	R/W	C2[7]	0
Bit 6	R/W	C2[6]	0
Bit 5	R/W	C2[5]	0
Bit 4	R/W	C2[4]	1
Bit 3	R/W	C2[3]	0
Bit 2	R/W	C2[2]	0
Bit 1	R/W	C2[1]	1
Bit 0	R/W	C2[0]	1

This register allows control over the path signal label.

C2[7], C2[6], C2[5], C2[4], C2[3], C2[2], C2[1], C2[0]:

The C2[7:0] bits are inserted in the C2 byte position in the transmit stream.

Register 0x049, 0x0C9: TPOP Path Status

Bit	Type	Function	Default
Bit 7	R/W	FEBE[3]	0
Bit 6	R/W	FEBE[2]	0
Bit 5	R/W	FEBE[1]	0
Bit 4	R/W	FEBE[0]	0
Bit 3	R/W	PRDI	0
Bit 2	R/W	G1[2]	0
Bit 1	R/W	G1[1]	0
Bit 0	R/W	G1[0]	0

This register allows control over the path status byte.

FEBE[3], FEBE[2], FEBE[1], FEBE[0]:

The FEBE[3:0] bits are inserted in the FEBE bit positions in the path status byte. The value contained in FEBE[3:0] is cleared after being inserted in the path status byte. Any non-zero FEBE[3:0] value overwrites the value that would normally have been inserted based on the number of FEBEs accumulated during the last frame. When reading this register, a non-zero value in these bit positions indicates that the insertion of this value is still pending.

PRDI:

The PRDI bit controls the insertion of the path remote defect indication (RDI). When a logic one is written to this bit position, the PRDI bit position in the path status byte (G1) is set high. If the AUTORDI bit is a logic one, an alarm state also sets the PRDI bit high. When a logic zero is written to this bit position, the PRDI bit position in the path status byte is set low provided AUTORDI is low or no alarms are currently active.

G1[2], G1[1], G1[0]:

The G1[2:0] bits are inserted in the unused bit positions in the path status byte.

Register 0x050, 0x0D0: RACP Control/Status

Bit	Type	Function	Default
Bit 7	R	OOCDV	X
Bit 6	R/W	RXPTYP	0
Bit 5	R/W	PASS	0
Bit 4	R/W	DISCOR	0
Bit 3	R/W	HCSPASS	0
Bit 2	R/W	HCSADD	1
Bit 1	R/W	DDSCR	0
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset the four cell receive FIFO. When FIFORST is set to logic zero, the FIFO operates normally. When FIFORST is set to logic one, the FIFO is immediately emptied and ignores writes. The FIFO remains empty and continues to ignore writes until a logic zero is written to FIFORST.

DDSCR:

The DDSCR bit controls the descrambling of the cell payload. When DDSCR is a logic one, cell payload descrambling is disabled. When DDSCR is a logic zero, payload descrambling is enabled.

HCSADD:

The HCSADD bit controls the addition of the coset polynomial, $x^6+x^4+x^2+1$, to the HCS octet prior to comparison. When HCSADD is a logic one, the polynomial is added, and the resulting HCS is compared. When HCSADD is a logic zero, the polynomial is not added, and the unmodified HCS is compared.

HCSPASS:

The HCSPASS bit controls the dropping of cells based on the detection of an uncorrectable HCS error. When HCSPASS is a logic zero, cells containing an uncorrectable HCS error are dropped. When HCSPASS is a logic one, cells are passed to the receive FIFO regardless of errors detected in the HCS. In addition, the HCS verification finite state machine never exits the correction

mode. Regardless of the programming of this bit, cells are always dropped while the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states.

DISCOR:

The DISCOR bit disables the HCS error correction algorithm. When DISCOR is a logic zero, the error correction algorithm is enabled, and single bit errors detected in the cell header are corrected. When DISCOR is a logic one, the error correction algorithm is disabled, and any error detected in the cell header is treated as an uncorrectable HCS error.

PASS:

The PASS bit controls the function of the cell filter. When PASS is written with a logic zero, all cells matching the cell filter are dropped. When PASS is a logic one, the match header pattern registers are ignored and filtering of cells with VPI and VCI fields set to 0 is not performed. The default state of this bit together with the default states of the bits in the Match Mask and Match Pattern Registers enable the dropping of cells containing all zero VCI and VPI fields.

RXPTYP:

The RXPTYP bit selects even or odd parity for outputs RXPRTY[1:0]. When operating in split bus mode and when RXPTRYP is set to logic one, output RXPRTY[0] is the even parity bit for outputs RDAT[7:0], and output RXPRTY[1] is the even parity bit for outputs RDAT[15:8]. When it is set to logic zero, RXPRTY[0] is the odd parity bit for outputs RDAT[7:0], and RXPRTY[1] is the odd parity bit for outputs RDAT[15:8].

When the SCI-PHY bus is configured for 8 bit FIFO mode and when RXPTRYP is set to logic one, output RXPRTY[0] is the even parity bit for outputs RDAT[7:0]. When it is set to logic zero, RXPRTY[0] is the odd parity bit for outputs RDAT[7:0]. In 8 bit FIFO mode, RXPRTY[1] is undefined.

When the SCI-PHY bus is configured for 16 bit FIFO mode and when RXPTRYP is set to logic one, output RXPRTY[1] is the even parity bit for outputs RDAT[15:0]. When it is set to logic zero, RXPRTY[1] is the odd parity bit for outputs RDAT[15:0]. In 16 bit FIFO mode RXPRTY[0] is held low.

OOCDV:

The OOCDV bit indicates the cell delineation state. When OOCDV is set high, the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states, and is hunting for the cell boundaries in the synchronous payload envelope.

When OOCDV is set low, the cell delineation state machine is in the 'SYNC' state and cells are passed through the receive FIFO.

Register 0x051, 0x0D1: RACP Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R/W	OOCDE	0
Bit 6	R/W	HCSE	0
Bit 5	R/W	FIFOE	0
Bit 4	R	OOCDI	X
Bit 3	R	CHCSI	X
Bit 2	R	UHCSI	X
Bit 1	R	FOVRI	X
Bit 0		Unused	X

FOVRI:

The FOVRI bit is set high when a FIFO overrun occurs. This bit is reset immediately after a read to this register.

UHCSI:

The UHCSI bit is set high when an uncorrectable HCS error is detected. This bit is reset immediately after a read to this register.

CHCSI:

The CHCSI bit is set high when a correctable HCS error is detected. This bit is reset immediately after a read to this register.

OOCDI:

The OOCDI bit is set high when a change of cell delineation state has occurred. The OOCDI bit is set high when the RACP block transitions from the PRESYNC state to the SYNC state and from the SYNC state to the HUNT state. This bit is reset immediately after a read to this register.

FIFOE:

The FIFOE bit enables the generation of an interrupt due to a FIFO overrun error condition. When FIFOE is set to logic one, the interrupt is enabled.

HCSE:

The HCSE bit enables the generation of an interrupt due to the detection of a correctable or an uncorrectable HCS error. When HCSE is set to logic one, the interrupt is enabled.

OOCDE:

The OOCDE bit enables the generation of an interrupt due to a change of cell delineation state. When OOCDE is set to logic one, the interrupt is enabled.

Register 0x052, 0x0D2: RACP Match Header Pattern

Bit	Type	Function	Default
Bit 7	R/W	GFC[3]	0
Bit 6	R/W	GFC[2]	0
Bit 5	R/W	GFC[1]	0
Bit 4	R/W	GFC[0]	0
Bit 3	R/W	PTI[2]	0
Bit 2	R/W	PTI[1]	0
Bit 1	R/W	PTI[0]	0
Bit 0	R/W	CLP	0

This register extends the cell filtering criteria beyond the all zeros pattern that must be present in the VPI and VCI fields of the idle or unassigned cell. The PASS bit in the RACP Control/Status Register must be set to logic zero to enable dropping of idle/unassigned cells matching the pattern defined by the contents of this register and the RACP Match Header Mask Register.

GFC[3:0]:

The GFC[3:0] bits contain the pattern to match in the first, second, third and fourth bits of the first octet of the 53 octet cell, in conjunction with the RACP Match Header Mask Register.

PTI[2:0]:

The PTI[2:0] bits contain the pattern to match in the fifth, sixth and seventh bits of the fourth octet of the 53 octet cell, in conjunction with the RACP Match Header Mask Register.

CLP:

The CLP bit contains the pattern to match in the eighth bit of the fourth octet of the 53 octet cell, in conjunction with the RACP Match Header Mask Register.

Register 0x053, 0x0D3: RACP Match Header Mask

Bit	Type	Function	Default
Bit 7	R/W	MGFC[3]	0
Bit 6	R/W	MGFC[2]	0
Bit 5	R/W	MGFC[1]	0
Bit 4	R/W	MGFC[0]	0
Bit 3	R/W	MPTI2]	0
Bit 2	R/W	MPTI[1]	0
Bit 1	R/W	MPTI[0]	0
Bit 0	R/W	MCLP	0

The mask contained in this register is applied to the RACP Match Header Pattern Register to select the bits included in the cell filter. A logic one in any bit position enables the corresponding bit in the pattern register to be compared. A logic zero causes the masking of the corresponding bit.

MGFC[3:0]:

The MGFC[3:0] bits contain the mask pattern for the first, second, third and fourth bits of the first octet of the 53 octet cell.

MPTI3:0]:

The MPTI[3:0] bits contain the mask pattern for the fifth, sixth and seventh bits of the fourth octet of the 53 octet cell.

MCLP:

The MCLP bit contains the mask pattern for the eighth bit of the fourth octet of the 53 octet cell.

Register 0x054, 0x0D4: RACP Correctable HCS Error Count

Bit	Type	Function	Default
Bit 7	R	CHCS[7]	X
Bit 6	R	CHCS[6]	X
Bit 5	R	CHCS[5]	X
Bit 4	R	CHCS[4]	X
Bit 3	R	CHCS[3]	X
Bit 2	R	CHCS[2]	X
Bit 1	R	CHCS[1]	X
Bit 0	R	CHCS[0]	X

CHCS[7:0]:

The CHCS[7:0] bits indicate the number of correctable HCS error events that occurred during the last accumulation interval. The contents of these registers are valid 200 ns after a transfer is triggered by a write to the correctable HCS error count register address, or to the uncorrectable HCS error count register address.

The error count can also be polled by writing to the S/UNI-DUAL Master Reset and Identity / Channel #1 Monitoring Update register (0x000) or the S/UNI-DUAL Channel #2 Monitoring Update register (0x080). Writing to register address 0x000 loads all the error counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks of channel #1. Writing to register address 0x080 loads all the error counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks of channel #2.

Register 0x055, 0x0D5: RACP Uncorrectable HCS Error Count

Bit	Type	Function	Default
Bit 7	R	UHCS[7]	X
Bit 6	R	UHCS[6]	X
Bit 5	R	UHCS[5]	X
Bit 4	R	UHCS[4]	X
Bit 3	R	UHCS[3]	X
Bit 2	R	UHCS[2]	X
Bit 1	R	UHCS[1]	X
Bit 0	R	UHCS[0]	X

UHCS[7:0]:

The UHCS[7:0] bits indicate the number of uncorrectable HCS error events that occurred during the last accumulation interval. The contents of these registers are valid 200 ns after a transfer is triggered by a write to the correctable HCS error count register address, or to the uncorrectable HCS error count register address.

The error count can also be polled by writing to the S/UNI-DUAL Master Reset and Identity / Channel #1 Monitoring Update register (0x000) or the S/UNI-DUAL Channel #2 Monitoring Update register (0x080). Writing to register address 0x000 loads all the error counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks of channel #1. Writing to register address 0x080 loads all the error counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks of channel #2.

Register 0x056, 0x0D6: RACP Receive Cell Counter (LSB)

Bit	Type	Function	Default
Bit 7	R	RCELL[7]	X
Bit 6	R	RCELL[6]	X
Bit 5	R	RCELL[5]	X
Bit 4	R	RCELL[4]	X
Bit 3	R	RCELL[3]	X
Bit 2	R	RCELL[2]	X
Bit 1	R	RCELL[1]	X
Bit 0	R	RCELL[0]	X

Register 0x057, 0x0D7: RACP Receive Cell Counter

Bit	Type	Function	Default
Bit 7	R	RCELL[15]	X
Bit 6	R	RCELL[14]	X
Bit 5	R	RCELL[13]	X
Bit 4	R	RCELL[12]	X
Bit 3	R	RCELL[11]	X
Bit 2	R	RCELL[10]	X
Bit 1	R	RCELL[9]	X
Bit 0	R	RCELL[8]	X

Register 0x058, 0x0D8: RACP Receive Cell Counter (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	RCELL[18]	X
Bit 1	R	RCELL[17]	X
Bit 0	R	RCELL[16]	X

RCELL[18:0]:

The RCELL[18:0] bits indicate the number of cells received and written into the receive FIFO during the last accumulation interval. Cells received and filtered due to HCS errors or Idle/Unassigned cell matches are not counted. The counter should be polled every second to avoid saturating. The contents of these registers are valid 200 ns after a transfer is triggered by a write to the correctable HCS error count register addresses, the uncorrectable HCS error count register addresses or the receive cell counter register addresses. The cell count can also be polled by writing to the S/UNI-DUAL Master Reset and Identity / Channel #1 Monitoring Update register (0x000) or the S/UNI-DUAL Channel #2 Monitoring Update register (0x080). Writing to register address 0x000 loads all the error counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks of channel #1. Writing to register address 0x080 loads all the error counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks of channel #2.

Register 0x059, 0x0D9: RACP Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	Reserved	1
Bit 5	R/W	Reserved	1
Bit 4	R/W	Reserved	1
Bit 3	R/W	FSEN	1
Bit 2	R/W	RCALEVEL0	1
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

RCALEVEL0:

The RCA level 0 bit, RCALEVEL0, determines what output RCA indicates when it transitions low. When RCALEVEL0 is set to logic one, a high to low transition on output RCA indicates that the receive FIFO is empty. When RCALEVEL0 is set to logic zero, a high to low transition on output RCA indicates that the receive FIFO is near empty and contains four only bytes.

FSEN:

The active high fix stuff control enable bit FSEN selects the expected payload mapping of ATM cells when STS-1 mapping is selected. When FSEN is set to logic one, it is assumed columns 30 and 59 of the Synchronous Payload Envelope (SPE) contain fixed stuff bytes. When FSEN is set to logic zero, it is assumed ATM payload fills the entire SPE except the path overhead column.

Reserved:

The reserved bits must be programmed to logic one for proper operation.

Register 0x060, 0x0E0: TACP Control/Status

Bit	Type	Function	Default
Bit 7	R/W	FIFOE	0
Bit 6	R	TSOCI	X
Bit 5	R	FOVRI	X
Bit 4	R/W	DHCS	0
Bit 3	R/W	HCSB	0
Bit 2	R/W	HCSADD	1
Bit 1	R/W	DSCR	0
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset the four cell transmit FIFO. When FIFORST is set to logic zero, the FIFO operates normally. When FIFORST is set to logic one, the FIFO is immediately emptied and ignores writes. The FIFO remains empty and continues to ignore writes until a logic zero is written to FIFORST.

DSCR:

The DSCR bit controls the scrambling of the cell payload. When DSCR is a logic one, cell payload scrambling is disabled. When DSCR is a logic zero, payload scrambling is enabled.

HCSADD:

The HCSADD bit controls the addition of the coset polynomial, $x^6+x^4+x^2+1$, to the HCS octet prior to insertion in the synchronous payload envelope. When HCSADD is a logic one, the polynomial is added, and the resulting HCS is inserted. When HCSADD is a logic zero, the polynomial is not added, and the unmodified HCS is inserted.

HCSB:

The active low HCS bit enables the internal generation and insertion of the HCS octet into the transmit cell stream. When HCSB is a logic zero, the HCS is generated and inserted internally. When HCSB is a logic one, the HCS octet read from the FIFO is inserted transparently into the transmit cell stream.

DHCS:

The DHCS bit controls the insertion of HCS errors for diagnostic purposes. When DHCS is set to logic one, the HCS octet is inverted prior to insertion in the synchronous payload envelope.

FOVRI:

The FOVRI bit is set high when a FIFO overrun occurs. This bit is reset immediately after a read to this register

TSOCI:

The TSOCI bit is set high when the TSOC input is sampled high during any position other than the first byte. The write address counter is reset to the first byte of the cell when TSOC is sampled high. This bit is reset immediately after a read to this register.

FIFOE:

The FIFOE bit enables the generation of an interrupt due to a FIFO overrun error condition, or when the TSOC input is sampled high during any position other than the first byte. When FIFOE is set to logic one, the interrupt is enabled.

Register 0x061, 0x0E1: TACP Idle/Unassigned Cell Header Pattern

Bit	Type	Function	Default
Bit 7	R/W	GFC[3]	0
Bit 6	R/W	GFC[2]	0
Bit 5	R/W	GFC[1]	0
Bit 4	R/W	GFC[0]	0
Bit 3	R/W	PTI[2]	0
Bit 2	R/W	PTI[1]	0
Bit 1	R/W	PTI[0]	0
Bit 0	R/W	CLP	0

GFC[3:0]:

The GFC[3:0] bits contain the first, second, third, and fourth bit positions of the first octet of the idle/unassigned cell pattern. Cell rate decoupling is accomplished by transmitting idle/unassigned cells when the TACP detects that no outstanding cells exist in the transmit FIFO. The all zeros pattern is transmitted in the VCI and VPI fields of the idle cell.

PTI[3:0]:

The PTI[3:0] bits contain the fifth, sixth, and seventh bit positions of the fourth octet of the idle/unassigned cell pattern. Idle cells are transmitted when the TACP detects that no outstanding cells exist in the transmit FIFO.

CLP:

The CLP bit contains the eighth bit position of the fourth octet of the idle/unassigned cell pattern. Idle cells are transmitted when the TACP detects that no outstanding cells exist in the transmit FIFO.

Register 0x062, 0x0E2: TACP Idle/Unassigned Cell Payload Octet Pattern

Bit	Type	Function	Default
Bit 7	R/W	ICP[7]	0
Bit 6	R/W	ICP[6]	1
Bit 5	R/W	ICP[5]	1
Bit 4	R/W	ICP[4]	0
Bit 3	R/W	ICP[3]	1
Bit 2	R/W	ICP[2]	0
Bit 1	R/W	ICP[1]	1
Bit 0	R/W	ICP[0]	0

ICP[7:0]:

The ICP[7:0] bits contain the pattern inserted in the payload octets of the idle or unassigned cell. Cell rate decoupling is accomplished by transmitting idle/unassigned cells when the TACP detects that no outstanding cells exist in the transmit FIFO. Bit ICP[7] corresponds to the most significant bit of the octet, the first bit transmitted.

Register 0x063, 0x0E3: TACP FIFO Control

Bit	Type	Function	Default
Bit 7	R/W	TXPTYP	0
Bit 6	R/W	TXPRTYE	0
Bit 5	R	TXPRTY[1]	X
Bit 4	R	TXPRTY[0]	X
Bit 3	R/W	FIFODP[1]	0
Bit 2	R/W	FIFODP[0]	0
Bit 1	R/W	TCALEVEL0	0
Bit 0	R/W	HCSCTLEB	0

HCSCTLEB:

The active low HCS control enable, HCSCTLEB bit enables the XORing of the HCS Control byte with the generated HCS before insertion into the SPE stream. When set to logic zero, the HCS Control byte provided in the third word of the 27 word data structure is XORed with the generated HCS. When set to logic one, XORing is disabled and the HCS Control byte is ignored.

Please note, most users of the S/UNI DUAL require this bit to be set to a logic 1.

TCALEVEL0:

The active high TCA level 0 bit, TCALEVEL0 determines what output TCA indicates when it transitions low. When TCALEVEL0 is set to logic one, output TCA indicates that the transmit FIFO is full and can accept no more writes. When TCALEVEL0 is set to logic zero, output TCA indicates that the transmit FIFO is near full and can accept no more than four additional writes.

FIFODP[1:0]:

The FIFODP[1:0] bits determine the transmit FIFO cell depth. FIFO depth control may be important in systems where the cell latency through the TACP must be minimized. When the FIFO is filled to the specified depth, the transmit cell available signal, TCA is deasserted. TCA is asserted only after a complete cell has been read out; therefore, the current cell being read is included in the count. The selectable FIFO cell depths are shown below:

FIFODP[1]	FIFODP[0]	FIFO DEPTH
0	0	4 cells
0	1	3 cells
1	0	2 cells
1	1	1 cell

Note that FIFODP[1:0] only affects when TCA is asserted. All four cells of the FIFO may be filled before an over flow is declared.

It is not recommended that the FIFO depth be set to 1 cell. If a cell write is initiated only when TCA is asserted, half the bandwidth is lost to idle/unassigned cells. For minimum latency and maximum throughput, set the FIFO depth to 2 cells.

TXPRTYI[1:0]:

The TXPRTYI[1:0] bits indicate if a parity error was detected on the TDAT bus. These bits are cleared when this register is read. Odd or even parity is selected using the TXPTYP bit.

If in 8 bit bus mode or split bit mode, a parity error detected on the inputs TDAT[7:0] and TXPRTY[0] sets TXPRTYI[0] to a logic 1. If in split bus mode a parity error detected on TDAT[15:8] and TXPRTY[1] sets TXPRTY[1] to a logic 1.

If in 16 bit bus mode, a parity error detected on the inputs TDAT[15:0] and TXPRTY[1] sets TXPRTYI[1] to a logic 1. The TXPRTY[0] input is ignored.

TXPRTYE:

The TXPRTYE bit enables transmit parity interrupts. When set to logic one, parity errors on inputs TDAT[15:0] and TXPTRY[1:0] are indicated by the TXPRTYI[1:0] bits and the INTB output. When set to logic zero, parity errors are indicated by the TXPRTYI bit but are not indicated on the INTB output.

TXPTYP:

The TXPTYP bit selects even or odd parity for inputs TXPRTY[1:0]. When set to logic one even parity is checked and when set to a logic 0 odd parity is checked.

In split bus mode two parity checks are performed: the parity over TDAT[7:0] and TXPTRY[0]; and the parity over TDAT[15:8] and TXPRTY[1]. In 16 bit bus

mode, the parity of TDAT[15:0] and input TXPRTY[1] is checked. In 8 bit bus mode, the parity of TDAT[7:0] and input TXPRTY[0] is checked.

Register 0x064, 0x0E4: TACP Transmit Cell Counter (LSB)

Bit	Type	Function	Default
Bit 7	R	TCELL[7]	X
Bit 6	R	TCELL[6]	X
Bit 5	R	TCELL[5]	X
Bit 4	R	TCELL[4]	X
Bit 3	R	TCELL[3]	X
Bit 2	R	TCELL[2]	X
Bit 1	R	TCELL[1]	X
Bit 0	R	TCELL[0]	X

Register 0x065, 0x0E5: TACP Transmit Cell Counter

Bit	Type	Function	Default
Bit 7	R	TCELL[15]	X
Bit 6	R	TCELL[14]	X
Bit 5	R	TCELL[13]	X
Bit 4	R	TCELL[12]	X
Bit 3	R	TCELL[11]	X
Bit 2	R	TCELL[10]	X
Bit 1	R	TCELL[9]	X
Bit 0	R	TCELL[8]	X

Register 0x066, 0x0E6: TACP Transmit Cell Counter (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	TCELL[18]	X
Bit 1	R	TCELL[17]	X
Bit 0	R	TCELL[16]	X

TCELL[15:0]:

The TCELL[18:0] bits indicate the number of cells read from the transmit FIFO and inserted into the SPE during the last accumulation interval. Idle/Unassigned cells inserted into the SPE are not counted.

A write to any one of the Transmit Cell Counter registers loads the registers with the current counter value and resets the internal 19 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Transmit Cell Counter registers. The counter should be polled every second to avoid saturating. The contents of these registers are valid 200 ns after a transfer is triggered by a write to the transmit cell count register space.

The cell count can also be polled by writing to the S/UNI-DUAL Master Reset and Identity / Channel #1 Monitoring Update register (0x000) or the S/UNI-DUAL Channel #2 Monitoring Update register (0x080). Writing to register address 0x000 loads all the error counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks of channel #1. Writing to register address 0x080 loads all the error counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks of channel #2.

Register 0x067, 0x0E7: TACP Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	FSEN	1
Bit 2	R/W	H4INSB	0
Bit 1	R/W	FIXBYTE[1]	0
Bit 0	R/W	FIXBYTE[0]	0

FIXBYTE[1:0]:

The FIXBYTE[1:0] bits identify the byte pattern inserted into fixed byte columns of the synchronous payload envelope.

FIXBYTE[1]	FIXBYTE[0]	BYTE
0	0	00H
0	1	55H
1	0	AAH
1	1	FFH

H4INSB:

The active low H4 insert enable, H4INSB bit determines the contents of the H4 byte in the outgoing SPE. If H4INSB is set to logic one, the H4 byte is set to the value of 00 hexadecimal. If H4INSB is set to logic zero, the H4 byte is set to the cell indicator offset value.

FSEN:

The active high fix stuff control enable, FSEN bit determines the payload mapping of ATM cells for STS-1 mapping. When FSEN is set to logic one, a fixed pattern is inserted into columns 30 and 59 of the Synchronous Payload Envelope (SPE). When FSEN is set to logic zero, ATM payload fills the entire SPE except the path overhead column.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Registers 0x068, 0x0E8: RASE Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	PSBFE	0
Bit 6	R/W	COAPSE	0
Bit 5	R/W	S1E	0
Bit 4	R/W	SFBERE	0
Bit 3	R/W	Unused	X
Bit 2	R/W	Unused	X
Bit 1	R/W	Unused	X
Bit 0	R/W	Unused	X

PSBFE:

The PSBF interrupt enable is an interrupt mask for protection switch byte failure alarms. When PSBFE is a logic one, an interrupt is generated when PSBF is declared or removed.

COAPSE:

The COAPS interrupt enable is an interrupt mask for changes in the received APS code. When COAPSE is a logic one, an interrupt is generated when a new K1/K2 code value is extracted into the Receive K1 and Receive K2 registers.

S1E:

The S1 interrupt enable is an interrupt mask for changes in the received synchronization status. When S1E is a logic one, an interrupt is generated when a new synchronization status message is extracted into the Receive S1 register.

SFBERE:

The SFBERE bit is the interrupt enable for the signal fail threshold alarm. When SFBERE is a logic one, an interrupt is generated when the SF alarm is declared or removed.

Registers 0x069, 0x0E9: RASE Interrupt Status

Bit	Type	Function	Default
Bit 7	R	PSBFI	X
Bit 6	R	COAPSI	X
Bit 5	R	S1I	X
Bit 4	R	SFBERI	X
Bit 3	R	Unused	X
Bit 2	R	SFBERV	X
Bit 1	R	Unused	X
Bit 0	R	PSBFV	X

PSBFI:

The PSBFI bit is set high when the protection switching byte failure alarm is declared or removed. This bit is cleared when the RASE Interrupt Status register is read.

COAPSI:

The COAPSI bit is set high when a new APS code value has been extracted into the Receive K1 and Receive K2 registers. This bit is cleared when the RASE Interrupt Status register is read.

S1I:

The S1I bit is set high when a new synchronization status message has been extracted into the Receive S1 register. This bit is cleared when the RASE Interrupt Status register is read.

SFBERI:

The SFBERI bit is set high when the signal failure threshold crossing alarm is declared or removed. This bit is cleared when the RASE Interrupt Status register is read.

SFBERV:

The SFBERV bit indicates the signal failure threshold crossing alarm state. The alarm is declared (SFBERV is set high) when the bit error rate exceeds the threshold programmed in the SF Declaring Threshold registers. The

alarm is removed (SFBERV is set low) when the bit error rate is below the threshold programmed in the SF Clearing Threshold registers.

PSBFV:

The PSBFV bit indicates the protection switching byte failure alarm state. The alarm is declared (PSBFV is set high) when twelve successive frames, where no three consecutive frames contain identical K1 bytes, have been received. The alarm is removed (PSBFV is set low) when three consecutive frames containing identical K1 bytes have been received. This bit position is reserved when the ENH bit in the Mode Select register is a logic 1.

Registers 0x06A, 0x0EA: RASE Configuration/Control Register

Bit	Type	Function	Default
Bit 7	R/W	S1_CAP3	0
Bit 6	R/W	SFBERTEN	0
Bit 5	R/W	SFSMODE	0
Bit 4	R/W	SFCMODE	0
Bit 3	R/W	Unused	X
Bit 2	R/W	Unused	X
Bit 1	R/W	Unused	X
Bit 0	R/W	Unused	X

S1_CAP3:

The S1_CAP3 bit enables the S1 Capture algorithm. When S1_CAP3 is a logic one, the S1 nibble must have the same value for three consecutive frames before writing the new value into the Receive S1 register. When S1_CAP3 is logic zero, the S1 nibble value is written directly into the Receive S1 register.

SFBERTEN:

The SFBERTEN bit enables automatic monitoring of line bit error rate threshold events by the Signal Failure Bit Error Rate Monitor (SF BERM). When SFBERTEN is a logic one, the SF BERM continuously monitors line BIP errors over a period defined in the BERM configuration registers. When SFBERTEN is a logic zero, the SF BERM BIP accumulation logic is disabled, and the BERM logic is reset to restart in the declaration monitoring state.

All SF BERM accumulation period and threshold registers should be set up before the monitoring is enabled.

SFSMODE:

The SFSMODE bit selects the SF BERM saturation mode. When SFSMODE is a logic 0, the SF BERM limits the number of B2 errors accumulated in one frame period to the SF Saturation Threshold register value. When SFSMODE is a logic 1, the SF BERM limits the number of B2 errors accumulated in one window subtotal accumulation period to the SF Saturation Threshold register

value. Note that the number of frames in a window subtotal accumulation period is determined by the SF Accumulation Period register value.

SFCMODE:

The SFCMODE alarm bit selects the SF BERM window size to use for clearing the SF alarm. When SFCMODE is a logic 0, the SF BERM clears the SF alarm using the same window size used for declaration. When SFCMODE is a logic 1, the SF BERM clears the SF alarm using a window size that is 8 times longer than the alarm declaration window size. The declaration window size is determined by the SF BERM Accumulation Period registers.

Registers 0x06B, 0x0EB: RASE SF Accumulation Period (LSB)

Bit	Type	Function	Default
Bit 7	R/W	SFSAP[7]	0
Bit 6	R/W	SFSAP[6]	0
Bit 5	R/W	SFSAP[5]	0
Bit 4	R/W	SFSAP[4]	0
Bit 3	R/W	SFSAP[3]	0
Bit 2	R/W	SFSAP[2]	0
Bit 1	R/W	SFSAP[1]	0
Bit 0	R/W	SFSAP[0]	0

Registers 0x06C, 0x0EC: RASE SF Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SFSAP[15]	0
Bit 6	R/W	SFSAP[14]	0
Bit 5	R/W	SFSAP[13]	0
Bit 4	R/W	SFSAP[12]	0
Bit 3	R/W	SFSAP[11]	0
Bit 2	R/W	SFSAP[10]	0
Bit 1	R/W	SFSAP[9]	0
Bit 0	R/W	SFSAP[8]	0

Registers 0x06D, 0x0ED: RASE SF Accumulation Period (MSB)

Bit	Type	Function	Default
Bit 7	R/W	SFSAP[23]	0
Bit 6	R/W	SFSAP[22]	0
Bit 5	R/W	SFSAP[21]	0
Bit 4	R/W	SFSAP[20]	0
Bit 3	R/W	SFSAP[19]	0
Bit 2	R/W	SFSAP[18]	0
Bit 1	R/W	SFSAP[17]	0
Bit 0	R/W	SFSAP[16]	0

SFSAP[23:0]:

The SFSAP[23:0] bits represent the number of 8 kHz frames used to accumulate the B2 error subtotal. The total evaluation window to declare the SF alarm is broken into 8 subtotals, so this register value represents 1/8 of the total sliding window size. Refer to the Operations section for recommended settings.

Registers 0x06E, 0x0EE: RASE SF Saturation Threshold (LSB)

Bit	Type	Function	Default
Bit 7	R/W	SFSTH[7]	0
Bit 6	R/W	SFSTH[6]	0
Bit 5	R/W	SFSTH[5]	0
Bit 4	R/W	SFSTH[4]	0
Bit 3	R/W	SFSTH[3]	0
Bit 2	R/W	SFSTH[2]	0
Bit 1	R/W	SFSTH[1]	0
Bit 0	R/W	SFSTH[0]	0

Registers 0x06F, 0x0EF: RASE SF Saturation Threshold (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SFSTH[11]	0
Bit 2	R/W	SFSTH[10]	0
Bit 1	R/W	SFSTH[9]	0
Bit 0	R/W	SFSTH[8]	0

SFSTH[11:0]:

The SFSTH[11:0] value represents the allowable number of B2 errors that can be accumulated during an evaluation window before an SF threshold event is declared. Setting this threshold to 0xFFF disables the saturation functionality. Refer to the Operations section for the recommended settings.

Registers 0x070, 0x0F0: RASE SF Declaring Threshold (LSB)

Bit	Type	Function	Default
Bit 7	R/W	SFDTH[7]	0
Bit 6	R/W	SFDTH[6]	0
Bit 5	R/W	SFDTH[5]	0
Bit 4	R/W	SFDTH[4]	0
Bit 3	R/W	SFDTH[3]	0
Bit 2	R/W	SFDTH[2]	0
Bit 1	R/W	SFDTH[1]	0
Bit 0	R/W	SFDTH[0]	0

Registers 0x071, 0x0F1: RASE SF Declaring Threshold (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SFDTH[11]	0
Bit 2	R/W	SFDTH[10]	0
Bit 1	R/W	SFDTH[9]	0
Bit 0	R/W	SFDTH[8]	0

SFDTH[11:0]:

The SFDTH[11:0] value determines the threshold for the declaration of the SF alarm. The SF alarm is declared when the number of B2 errors accumulated during an evaluation window is greater than or equal to the SFDTH[11:0] value. Refer to the Operations section for the recommended settings.

Registers 0x072, 0x0F2: RASE SF Clearing Threshold (LSB)

Bit	Type	Function	Default
Bit 7	R/W	SFCTH[7]	0
Bit 6	R/W	SFCTH[6]	0
Bit 5	R/W	SFCTH[5]	0
Bit 4	R/W	SFCTH[4]	0
Bit 3	R/W	SFCTH[3]	0
Bit 2	R/W	SFCTH[2]	0
Bit 1	R/W	SFCTH[1]	0
Bit 0	R/W	SFCTH[0]	0

Registers 0x073, 0x0F3: RASE SF Clearing Threshold (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SFCTH[11]	0
Bit 2	R/W	SFCTH[10]	0
Bit 1	R/W	SFCTH[9]	0
Bit 0	R/W	SFCTH[8]	0

SFCTH[11:0]:

The SFCTH[11:0] value determines the threshold for the removal of the SF alarm. The SF alarm is removed when the number of B2 errors accumulated during an evaluation window is less than the SFCTH[11:0] value. Refer to the Operations section for the recommended settings.

Registers 0x07D, 0x0FD: RASE Receive K1

Bit	Type	Function	Default
Bit 7	R	K1[7]	X
Bit 6	R	K1[6]	X
Bit 5	R	K1[5]	X
Bit 4	R	K1[4]	X
Bit 3	R	K1[3]	X
Bit 2	R	K1[2]	X
Bit 1	R	K1[1]	X
Bit 0	R	K1[0]	X

K1[7:0]:

The K1[7:0] bits contain the current K1 code value. The contents of this register are updated when a new K1 code value (different from the current K1 code value) has been received for three consecutive frames. An interrupt may be generated when a new code value is received (using the COAPSE bit in the RASE Interrupt Enable Register). K1[7] is the most significant bit corresponding to bit 1, the first bit received. K1[0] is the least significant bit, corresponding to bit 8, the last bit received.

Registers 0x07E, 0x0FE: RASE Receive K2

Bit	Type	Function	Default
Bit 7	R	K2[7]	X
Bit 6	R	K2[6]	X
Bit 5	R	K2[5]	X
Bit 4	R	K2[4]	X
Bit 3	R	K2[3]	X
Bit 2	R	K2[2]	X
Bit 1	R	K2[1]	X
Bit 0	R	K2[0]	X

K2[7:0]:

The K2[7:0] bits contain the current K2 code value. The contents of this register are updated when a new K2 code value (different from the current K2 code value) has been received for three consecutive frames. An interrupt may be generated when a new code value is received (using the COAPSE bit in the RASE Interrupt Enable Register). K2[7] is the most significant bit corresponding to bit 1, the first bit received. K2[0] is the least significant bit, corresponding to bit 8, the last bit received.

Registers 0x07F, 0x0FF: RASE Receive S1

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	S1[3]	X
Bit 2	R	S1[2]	X
Bit 1	R	S1[1]	X
Bit 0	R	S1[0]	X

S1[3:0]:

The lower nibble of the S1 byte contained in the receive stream is extracted into this register. The S1 byte is used to carry synchronization status messages between line terminating network elements. S1[3] is the most significant bit corresponding to bit 5, the first bit received. S1[0] is the least significant bit, corresponding to bit 8, the last bit received. When enabled by the S1E bit in the RASE Interrupt Enable Register, an interrupt will be generated when the S1 nibble value received differs from the value extracted in the previous frame.

12 TEST FEATURES DESCRIPTION

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the S/UNI-DUAL. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[8]) is high.

Test mode registers may also be used for board testing. When all of the TSBs within the S/UNI-DUAL are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

Table 2 - Test Mode Register Memory Map

Address	Register
0x000-0x08F	Normal Mode Registers
0x100	Master Test
0x101-0xFFF	Reserved For Test

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence unused register bits should be masked off by software when read.

2. Writable test mode register bits are not initialized upon reset unless otherwise noted.

Register 0x100: Master Test

Bit	Type	Function	Default
Bit 7	R/W	CHNL_TM	X
Bit 6	R/W	BYPASS	X
Bit 5	W	PMCATST	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	X
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	X
Bit 0	R/W	HIZIO	0

This register is used to enable S/UNI-DUAL test features. All bits, except CHNL_TM, BYPASS, PMCTST and PMCATST, are reset to zero by a hardware reset of the S/UNI-DUAL.

HIZIO,HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the S/UNI-DUAL . While the HIZIO bit is a logic one, all output pins of the S/UNI-DUAL except the data bus are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each TSB block in the S/UNI-DUAL for board level testing. When IOTST is a logic one, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequentially the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic one, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the S/UNI-DUAL to drive the data bus and holding the CSB pin

low tri-states the data bus. The DBCTRL bit only has effect if either the IOTST bit, the PMCTST bit or the PMCATST bit is a logic one. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

PMCTST:

The PMCTST bit is used to configure the S/UNI-DUAL for PMC's manufacturing tests. When PMCTST is set to logic one, the S/UNI-DUAL microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

PMCATST:

The PMCATST bit is used to configure the analog portion of the S/UNI-DUAL for PMC's manufacturing tests. When PMCATST is set to logic one, the S/UNI-DUAL microprocessor port becomes the test access port used to run the PMC manufacturing analog test vectors. The PMCATST bit is logically "ORed" with the IOTST bit. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

BYPASS:

The BYPASS bit is used to permit the input data and clock to feed directly into the serial-to-parallel converter. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

CHNL_TM:

The CHNL_TM bit is used to select which channel of the S/UNI-DUAL is under test. When CHNL_TM is set to logic 0, channel #1 (master) is under test. When CHNL_TM is set to logic 1, channel #2 (slave) is under test. The CHNL_TM bit is not cleared by RSTB or CSB; therefore, it must be written to prior to testing.

12.1 Test Mode 0 Details

In test mode 0, the S/UNI-DUAL allows the logic levels on the device inputs to be read through the microprocessor interface, and allows the device outputs to be forced to either logic level through the microprocessor interface. The IOTST bit in the Master Test register should be set to logic one.

To enable test mode 0, the IOTST bit in the Master Test register is set to logic one and the following addresses must be written with 0x00: 0x111, 0x115,

0x119, 0x121, 0x131, 0x141, 0x151, 0x161, 0x169, 0x191, 0x195, 0x199, 0x1A1, 0x1B1, 0x1C1, 0x1D1, 0x1E1, 0x1E9.

The following inputs can not be read using the IOTST feature: REFCLK+/-, RXD1+/-, ALOS1+/-, RXD2+/-, ALOS2+/-, TXPRTY[1:0], TDAT[15:0], TSOC1, TSOC2, TWRENB1, TWRENB2, RRDENB1, RRDENB2, TSEN, D[7:0], A[8:0], ALE, CSB, WRB, RDB and RSTB.

Writing the following address locations forces the outputs to the value in the corresponding bit position:

Table 3 -

0x009					RALM2[1]	RALM1[1]	OUT[1][1]	OUT[0][1]
0x110						RFP		
0x116								TFP[2]
0x150	RSOC1		RCA1				RXPRTY[0]	
0x152	RDAT[7]	RDAT[6]	RDAT[5]	RDAT[4]	RDAT[3]	RDAT[2]	RDAT[1]	RDAT[0]
0x160								INT[3]
0x1D0	RSOC2		RCA2				RXPRTY[1]	
0x1D2	RDAT[15]	RDAT[14]	RDAT[13]	RDAT[12]	RDAT[11]	RDAT[10]	RDAT[9]	RDAT[8]

Notes:

1. ALARM bit in the S/UNI-DUAL Interface Control register must be set to logic 0.

2. TFP_TS bit in the S/UNI-DUAL Interface Control register must be set to logic 0. The test clock, TCK, must toggle high for the value to become valid.

3. Bit INT corresponds to output INTB. The following address locations should be written with the value 0x00: 0x112, 0x11A, 0x132, 0x150, 0x16A, 0x192, 0x19A, 0x1B2, 0x1D0, 0x1E0, and 0x1EA. INTB is an open drain output and should be pulled high for proper operation. Writing a logic one to the INT bit allows the S/UNI-DUAL to drive INTB low. Writing a logic zero to the INT bit tristates the INTB output.

The following outputs can not be controlled using the IOTST feature: TXD1+/-, TXD2+/-, TCLK, RCLK1, RCLK2, TCA1, TCA2, and D[7:0].

12.2 JTAG Test Port

The S/UNI-DUAL JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device boundary scan path can be bypassed. For more details on the JTAG port, please refer to the Operation section.

13 OPERATION

13.1 Overhead Byte Usage

Under normal operating conditions, the S/UNI-DUAL processes a subset of the complete transport overhead present in an STS-3c/STM-1 stream. The byte positions processed by the S/UNI-DUAL are indicated in Figure 9 and Figure 10.

Figure 9 - STS-3c (STM-1) Overhead

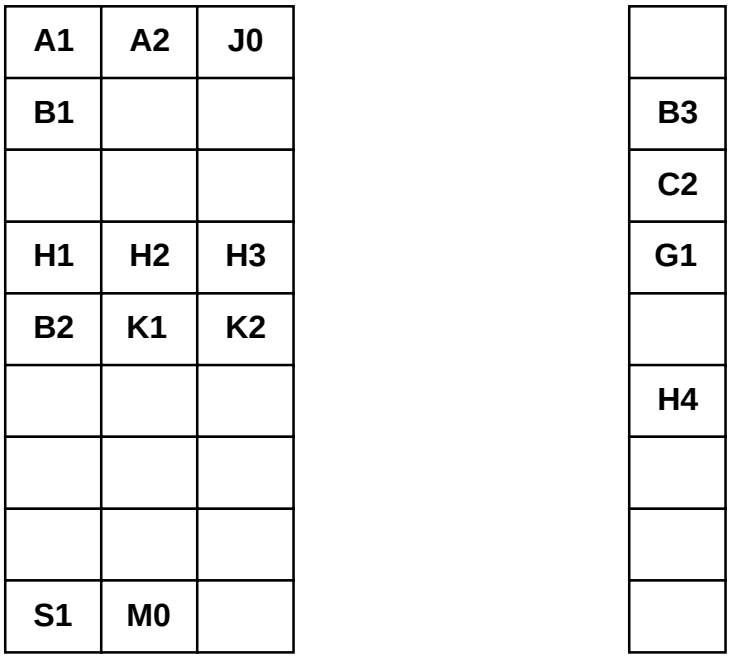
A1	A1	A1	A2	A2	A2	J0	Z0	Z0
B1								
H1	H1	H1	H2	H2	H2	H3	H3	H3
B2	B2	B2	K1			K2		
S1					M1			

TRANSPORT OVERHEAD SOH

B3
C2
G1
H4

PATH OVERHEAD POH

Figure 10 - STS-1 Overhead



A1, A2: The frame alignment bytes (A1, A2) locate the SONET frame in the data stream. The transmitter inserts these bytes in the outgoing stream. The receiver searches for the A1, A2 bit sequence in the incoming stream. A1 and A2 are not scrambled by the frame synchronous SONET scrambler.

J0: The J0 byte is currently defined as the STS-1/STM-1 section trace byte for SONET/SDH. J0 byte is not scrambled by the frame synchronous scrambler.

Z0: The Z0 bytes are currently defined as the STM-1 section growth bytes for SONET/SDH. Z0 bytes are not scrambled by the frame synchronous scrambler.

B1: The section bit interleaved parity byte provides a section error monitoring function. B1 is calculated over all bits of the previous frame after scrambling. B1 is placed in the current frame before scrambling. Receive B1 errors are accumulated in an error event counter.

H1, H2: The pointer value bytes locate the start of the synchronous payload envelope (SPE) in the SONET/SDH frame. In the transmit direction, a fixed pointer value of 522 decimal, with a normal new data flag indication, is inserted in the first H1-H2 pair. The concatenation indication is inserted in the remaining two H1-H2 pairs in STS-3c mode. In the receive direction, the pointer is interpreted to locate the SPE. The loss of pointer state is entered when a valid pointer cannot be found. Path AIS is detected when H1, H2 contain an all ones pattern.

H3: The pointer action bytes contain synchronous payload envelope data when a negative stuff event occurs. The all zeros pattern is inserted in the transmit direction. This byte is ignored in the receive direction unless a negative stuff event is detected.

B2: The line bit interleaved parity bytes provide a line error monitoring function. B2 is calculated over all bits of the line overhead, and the SPE capacity of the previous frame before scrambling. B2 is placed in the current frame before scrambling. Receive B2 errors are accumulated in an error event counter.

K1, K2: The K1 and K2 bytes provide the automatic protection switching channel. The K2 byte is used to identify line layer maintenance signals. Line RDI is indicated when bits 6, 7, and 8 of the K2 byte are set to the pattern '110'. Line AIS is indicated when bits 6, 7, and 8 of the K2 byte are set to the pattern '111'.

S1: The S1 byte provides the synchronization status byte. Bits 5 through 8 of the synchronization status byte identifies the synchronization source of the STS-3c (STM-1) or STS-1 signal. Bits 1 through 4 are currently undefined.

M0: The M0 byte is defined only for STS-1, and bits 5 through 8 provide a line far end block error function for remote performance monitoring. Bits 1 through 4 are currently undefined.

M1: The M1 byte is located in the third STS-1 of a STS-3c (STM-1) and provides a line far end block error function for remote performance monitoring.

B3: The path bit interleaved parity byte provides a path error monitoring function. B3 is calculated over all bits of the SPE capacity of the previous frame before scrambling. B3 is placed in the current frame before scrambling. Receive B3 errors are accumulated in an error event counter.

C2: The path signal label byte indicates the content of the SPE. A hexadecimal value of 13 is transmitted, which indicates "Mapping for ATM."

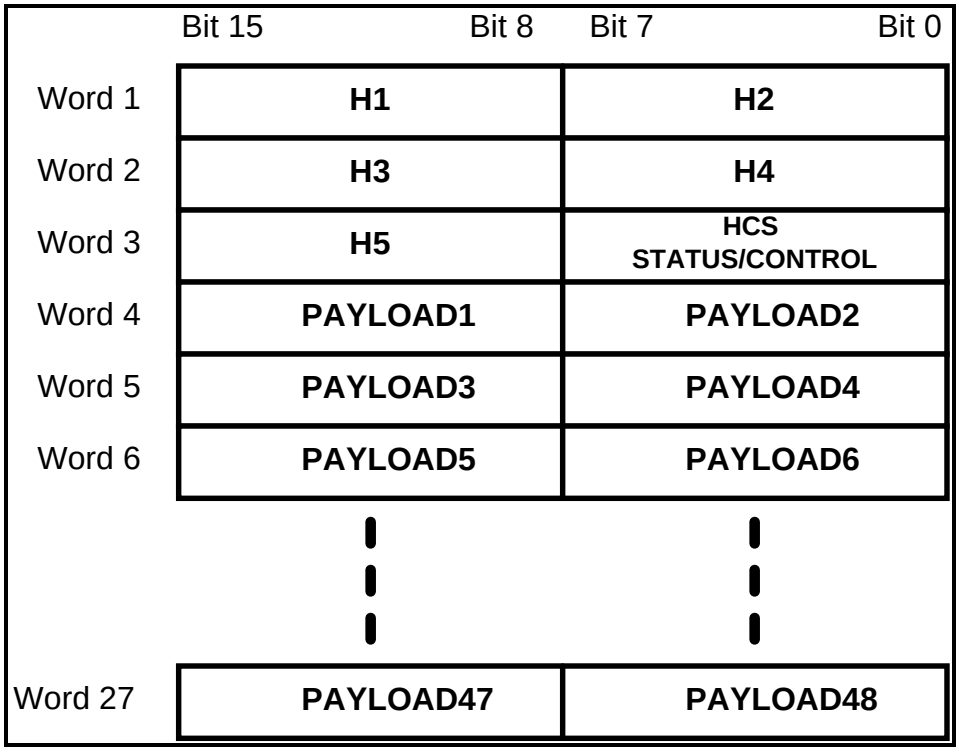
G1: The path status byte provides a path far end block error function, and provides control over the path remote defect indication maintenance signal. In the transmit direction, path remote alarm indication (RDI) and the number of B3 errors detected in the previous interval are inserted. This number has 9 legal values, namely 0 to 8 errors. In the receive direction, a legal G1 byte value is added to the path FEBE event counter. In addition, the path remote defect indication is detected.

H4: The cell offset indicator byte indicates the offset in bytes between itself, and the first cell boundary following the H4 byte. This byte is inserted correctly in the transmit direction, and is ignored in the receive direction.

13.2 Cell Data Structure

ATM cells may be passed to/from the S/UNI-DUAL using a twenty-seven word data structure or a fifty-three word data structure. These data structures are shown in Figure 11 and Figure 12.

Figure 11 - 16-bit Wide, 27 Word Structure



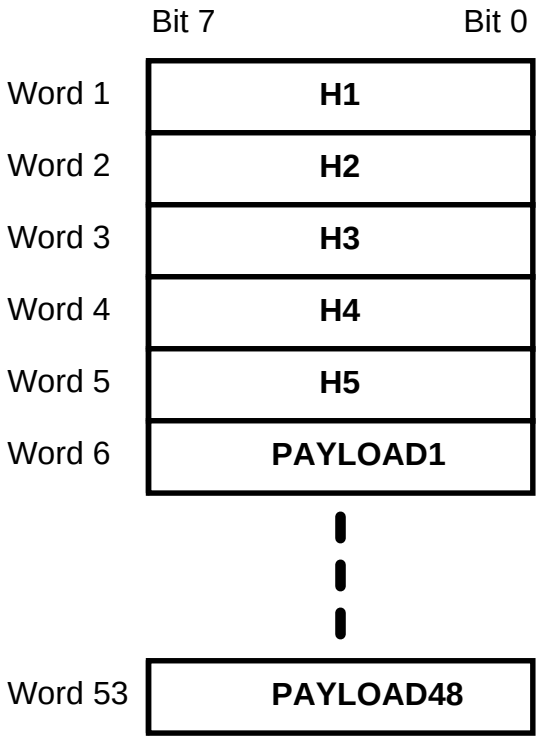
The 16-bit SCI-PHY compliant data structure is selected when the BUS8 bit of the S/UNI-DUAL Interface Control register is set low. Bit 15 of each word is the most significant bit (which corresponds to the first bit transmitted or received). The header check sequence octet (HCS) is passed through this structure. The start of cell indication input and output (TSOC[1] and RSOC[1]) are coincident with Word 1 (containing the first two header octets). Word 3 of this structure contains the HCS octet in bits 15 to 8.

In the receive direction, the lower 8 bits of Word 3 contain the HCS status octet. An all-zeros pattern in these 8 bits indicates that the associated header is error free. An all-ones pattern indicates that the header contains an uncorrectable error (if the HCSPASS bit in the RACP Control Register is set to logic zero, the all-ones pattern will never be passed in this structure). An alternating ones and zeros pattern (0xAA) indicates that the header contained a correctable error. In this case the header passed through the structure is the "corrected" header.

In the transmit direction, the HCS bit in the TACP Control register determines whether the HCS is calculated internally or is inserted directly from the upper 8 bits of Word 3. The lower 8 bits of Word 3 contain the HCS control octet. The

HCS control octet is an error mask that allows the insertion of one or more errors in the HCS octet. A logic one in a given bit position causes the inversion of the corresponding HCS bit position (for example a logic one in bit 7 causes the most significant bit of the HCS to be inverted). This feature may be disabled by setting the HCSCTLEB bit of registers 0x063 and 0x0E3 to a level 1.

Figure 12 - 8-bit Wide, 53 Word Structure



The 8-bit SCI-PHY compliant data structure is selected when the BUS8 bit or the SPLIT bit of the S/UNI-DUAL Interface Control register is set high. Bit 7 of each word is the most significant bit (which corresponds to the first bit transmitted or received). The header check sequence octet (HCS) is passed through this structure. The start of cell indication input and output (TSOC[2:1] and RSOC[2:1]) are coincident with Word 1 (containing the first cell header octet). Word 5 of this structure contains the HCS octet.

In the receive direction, cells containing "detected and uncorrected" header errors are dropped when the HCSPASS bit in the RACP Control/Status Register is set to logic zero. No HCS status information is passed within this data structure. Error free headers and "detected and corrected" headers are passed when HCSPASS is a logic zero. Error free headers, "detected and corrected"

headers, and "detected and uncorrected" headers are passed when HCSPASS is a logic one.

In the transmit direction, the HCS bit in the TACP Control Register determines whether the HCS is calculated internally or is inserted directly from Word 5.

13.3 Loopback Operation

The S/UNI-DUAL supports three loopback functions: line loopback, parallel diagnostic loopback and serial diagnostic loopback. Each channel's loopback modes operate almost independently. The exception is that channel #1 provides the transmit frame alignment signal for channel #2. The line loopback connects the high speed receive data and clock to the transmit data and clock, see Figure 13. The serial diagnostic loopback connects the high speed transmit data and clock to the high speed receive data and clock, see Figure 14. The parallel diagnostic loopback connects the byte wide transmit data and clock to the byte wide receive data and clock, see Figure 15. The loopback modes are activated by bits contained in the S/UNI-DUAL Control Register.

Figure 13 - Line Loopback Mode

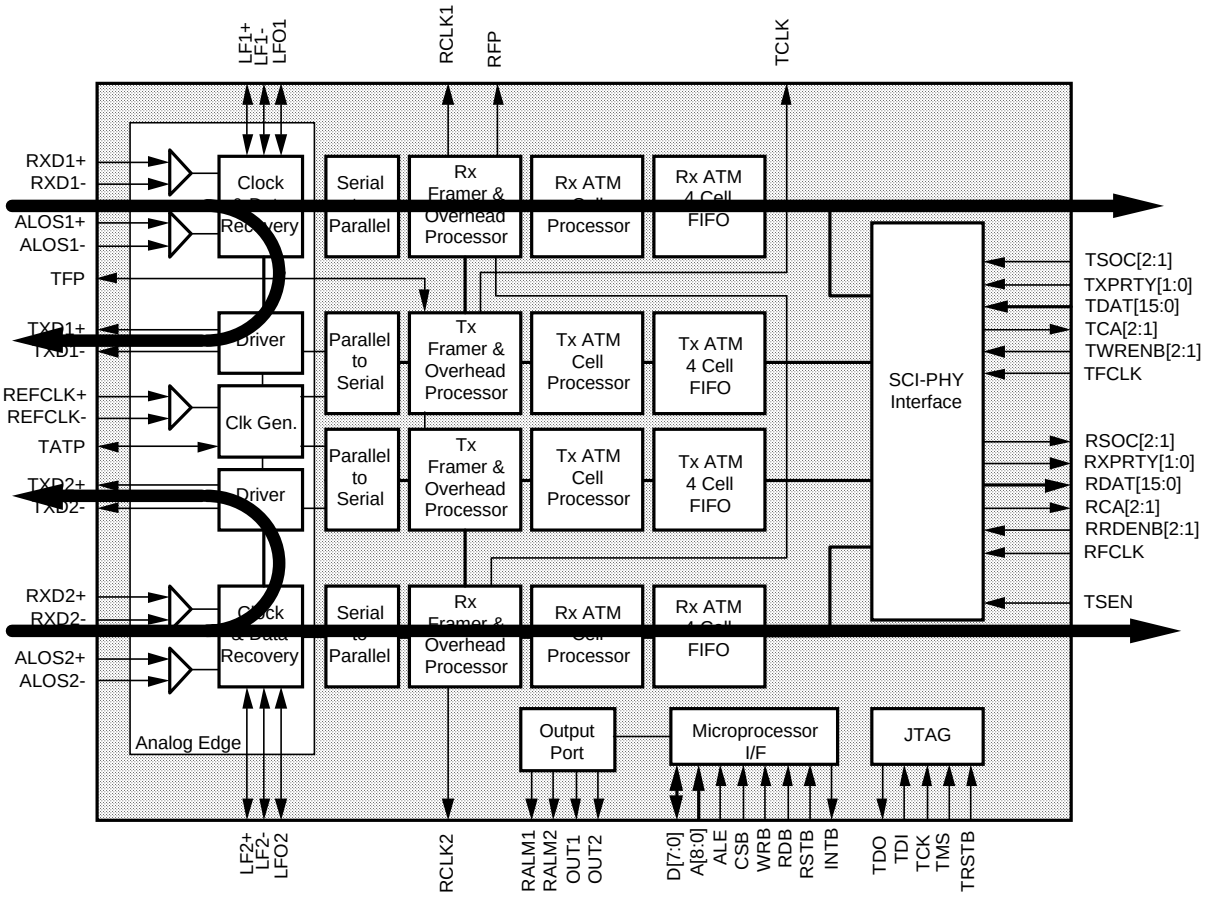


Figure 14 - Serial Diagnostic Loopback Mode

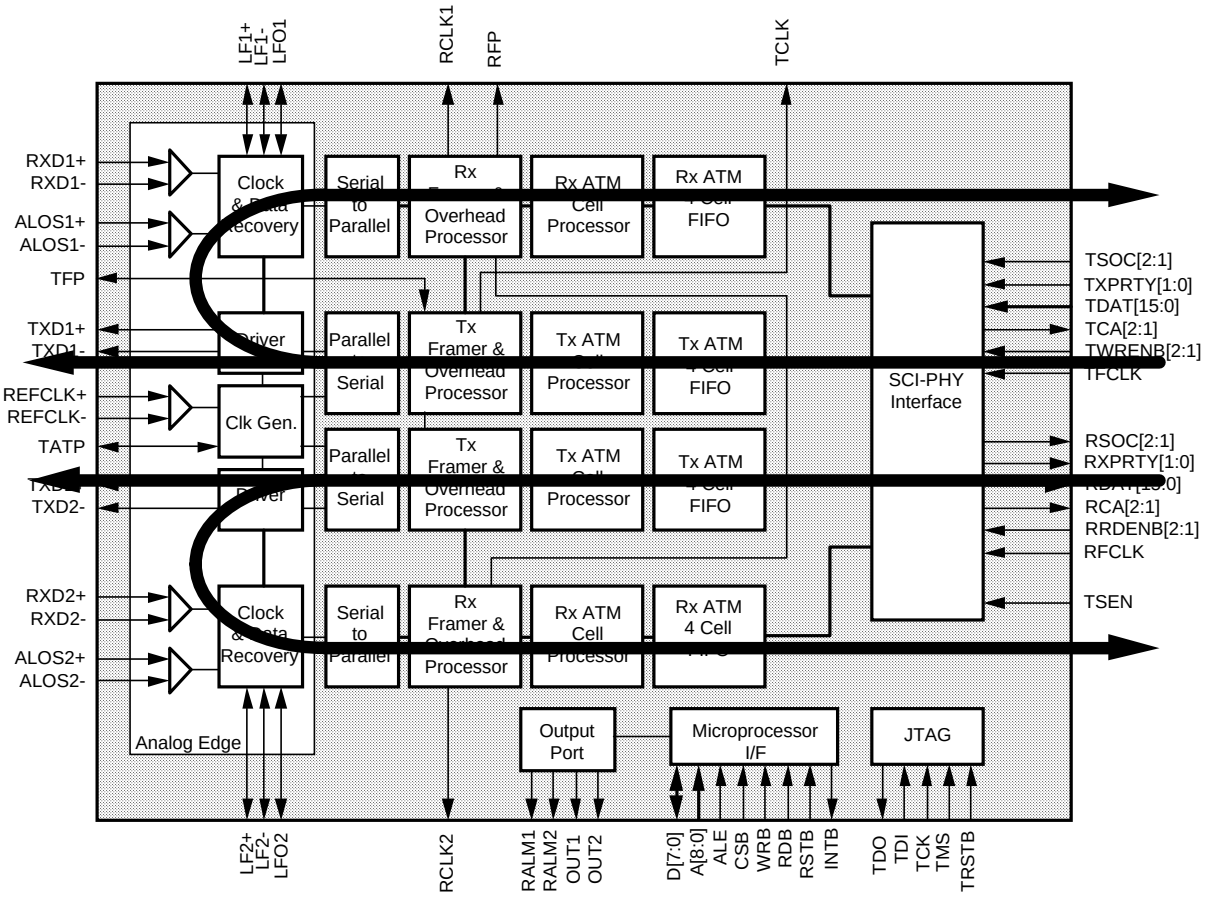
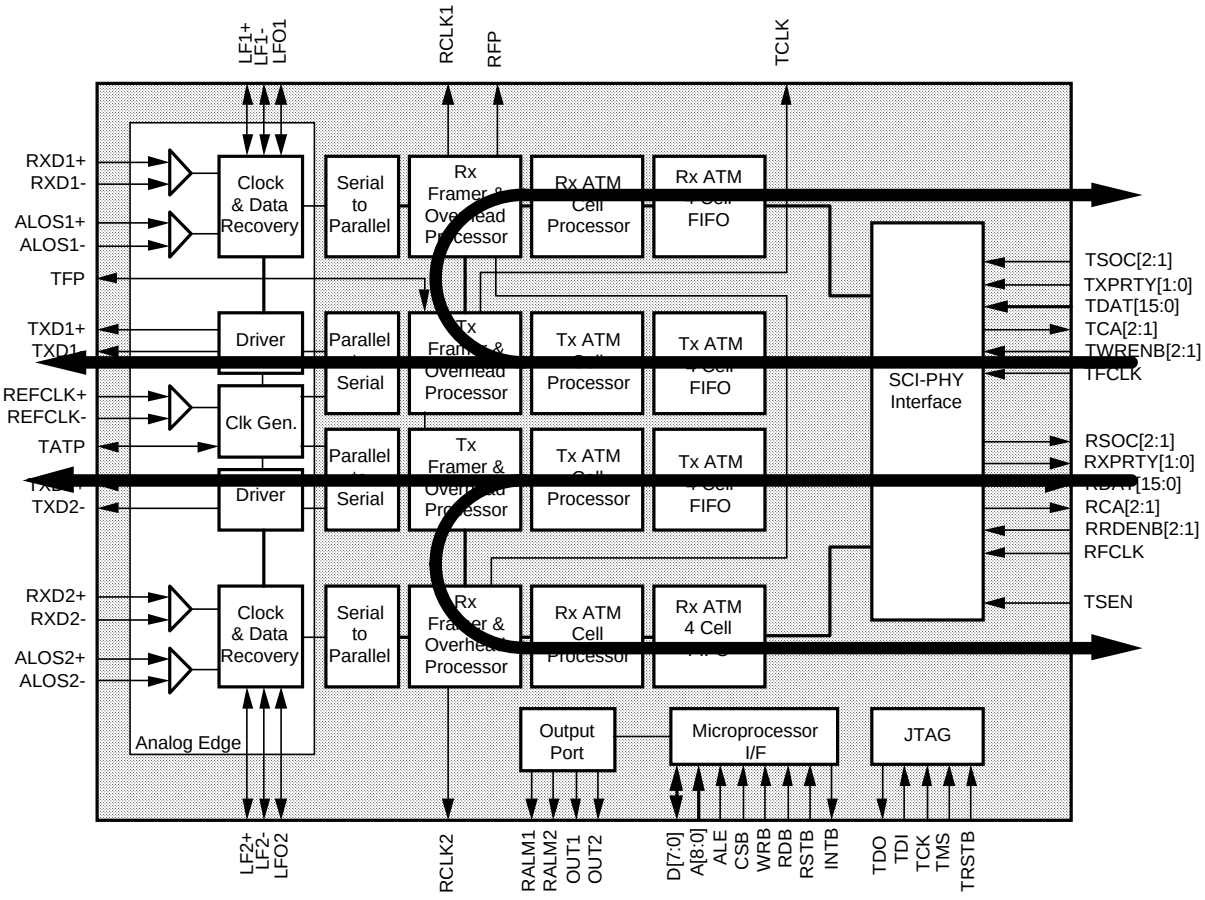


Figure 15 - Parallel Diagnostic Loopback Mode



13.4 Board Design Recommendations

The noise environment and signal integrity are often the limiting factors in system performance. Therefore, the following board design guidelines *must* be followed in order to ensure proper operation:

1. Connect digital and analog grounds together at only one point close to the connector where ground is brought into the card.

2. Provide separate +5 volt analog transmit, +5 volt analog receive, and +5 volt digital supplies, but otherwise connect the supply voltages together at one point close to the connector where +5 volts is brought to the card.

3. Ferrite beads are not advisable in digital switching circuits because inductive spiking (di/dt noise) is introduced into the power rail. Simple RC filtering is

probably the best approach provided care is taken to ensure the IR drop in the resistance does not lower the supply voltage below the recommended operating voltage.

4. Ferrite beads are recommended for TAVD1, TAVD2, R1AVD1, R1AVD2, R2AVD1 and R2AVD2.

5. Separate high-frequency decoupling capacitors are recommended for each analog power (TAVD1, TAVD2, R1AVD1, R1AVD2, R2AVD1 and R2AVD2) pin as close to the package pin as possible. Separate decoupling is required to prevent the transmitter from coupling noise into the receiver and to prevent transients from coupling into the reference circuitry powered by TAVD1, R1AVD1 and R2AVD1.

6. The high speed serial streams (TXD+/- and RXD+/) must be routed with controlled impedance circuit board traces and must be terminated with a matched load. Normal TTL-type design rules are not recommended and will reduce the performance of the device.

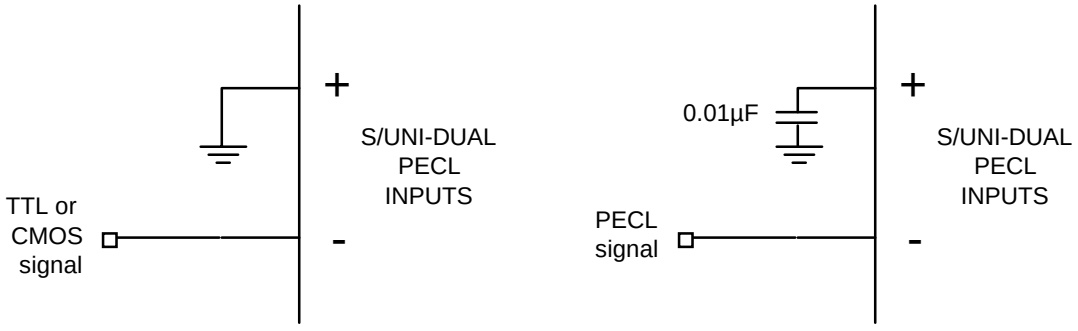
13.5 Driving Differential Inputs Single Ended

In some applications it may be more cost effective or technically desirable to drive the ALOS1+/- or ALOS2+/- inputs with a single ended PECL, TTL or CMOS signal. Figure 16 illustrates the suggested configuration to achieve this.

Note:

RXD1+/-, RXD2+/- inputs do not support single ended operation and must always be driven by a differential source.

Figure 16 - Single Ended Driving Differential Inputs



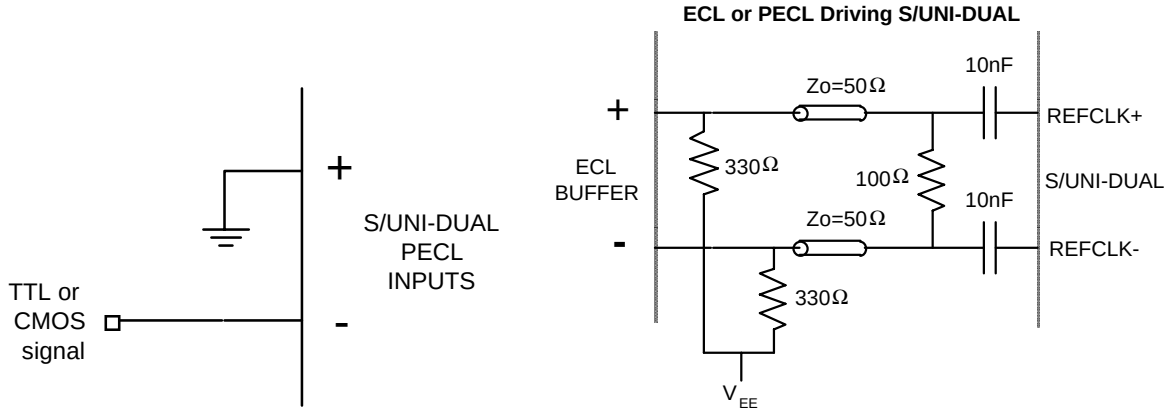
For TTL or CMOS signals, the positive input must be grounded. The negative input should be connected directly to a TTL or CMOS signal. In the case where a single ended PECL source is used, the positive input should be decoupled to ground through a 0.01µF capacitor.

These configurations logically invert the input signal.

13.6 Driving the Differential Reference Clock

In some applications it may be more cost effective or technically desirable to drive the REFCLK+/- inputs with a single ended TTL or CMOS signal, as illustrated in Figure 17. Similarly, the REFCLK+/- inputs to the S/UNI-DUAL may be driven differentially and would be AC coupled as shown in Figure 17.

Figure 17 - Driving REFCLK Inputs



For TTL or CMOS signals, the positive input must be grounded. The negative input should be connected directly to a TTL or CMOS signal. This configuration logically inverts the input signal.

For differential PECL signals, the REFCLK+/- inputs are self-biasing to improve operating speed and waveform symmetry. For this reason, the DC blocking capacitors are always required, even when interfacing to PECL drivers. Ceramic capacitors are recommended.

13.7 Interfacing to ECL or PECL Devices

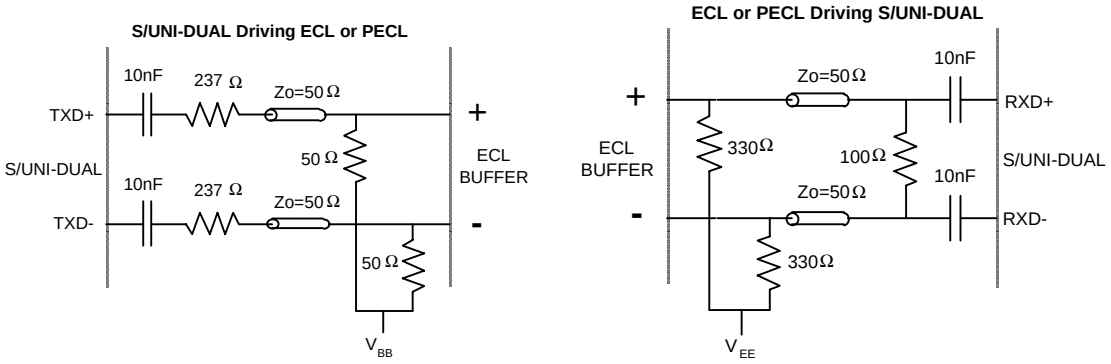
Although the TXD+/- outputs are TTL compatible, only a few passive components are required to convert the signals to ECL (or PECL) logic levels. Figure 18 illustrates the recommended configuration. The capacitors AC couple the

outputs so that the ECL inputs are free to swing around the ECL bias voltage (V_{BB}). The combination of the 237 Ω and 50 Ω resistors divides the voltage down to a nominally 800mV swing. The 50 Ω resistors also terminate the signals.

Similarly, the RXD+/- inputs to the S/UNI-DUAL are AC coupled as shown in Figure 18. The S/UNI-DUAL inputs are self-biasing to improve operating speed and waveform symmetry. For this reason, the DC blocking capacitors are always required, even when interfacing to PECL drivers. The only exception are the ALOS+/- inputs which must be DC coupled because of their low frequency content.

Ceramic capacitors are recommended.

Figure 18 - Interfacing S/UNI-DUAL to ECL or PECL



13.8 Clock Recovery

Figure 19 is an abstraction of the clock recovery phase lock loop illustrating the connections to external components. The figure illustrates the unity gain buffer loop filter application where the integral op-amp output is buffered through a unity gain amplifier to minimize the effect of its finite output impedance on the transfer function of the PLL. The unity gain buffer loop filter circuit exceeds SONET/SDH jitter tolerance specifications.

Additional analysis of jitter transfer and jitter tolerance issues for the S/UNI-DUAL can be found in PMC's ATM Design Notes "Meeting SONET/SDH WAN Interface Jitter Transfer Requirements with the S/UNI-DUAL", PMC-950139

The internal op-amp in the S/UNI-DUAL's clock recovery unit (CRU) regenerates a 155.52 MHz clock from the incoming SONET data. The op-amp has a frequency-dependent output resistance. All amplifiers exhibit this, but the CRU's op-amp displays a significant output resistance (approximately 200Ω) in a frequency band that affects some signal components which feed through the PLL.

This increase in output resistance is seen in series with the external loop filter passive components which set the jitter tolerance and transfer characteristics of the CRU. This effectively unbalances the loop filter signal paths, decreasing jitter tolerance.

To balance the signal paths, R_2 has to be equal to $R_1 + R_{out}$, where R_{out} is the output resistance of the op-amp. If the output resistance of the op-amp is approximately 200Ω, R_2 would have to be at least 200Ω.

Figure 19 - Clock Recovery Circuit - Unity Gain Buffer Loop Filter

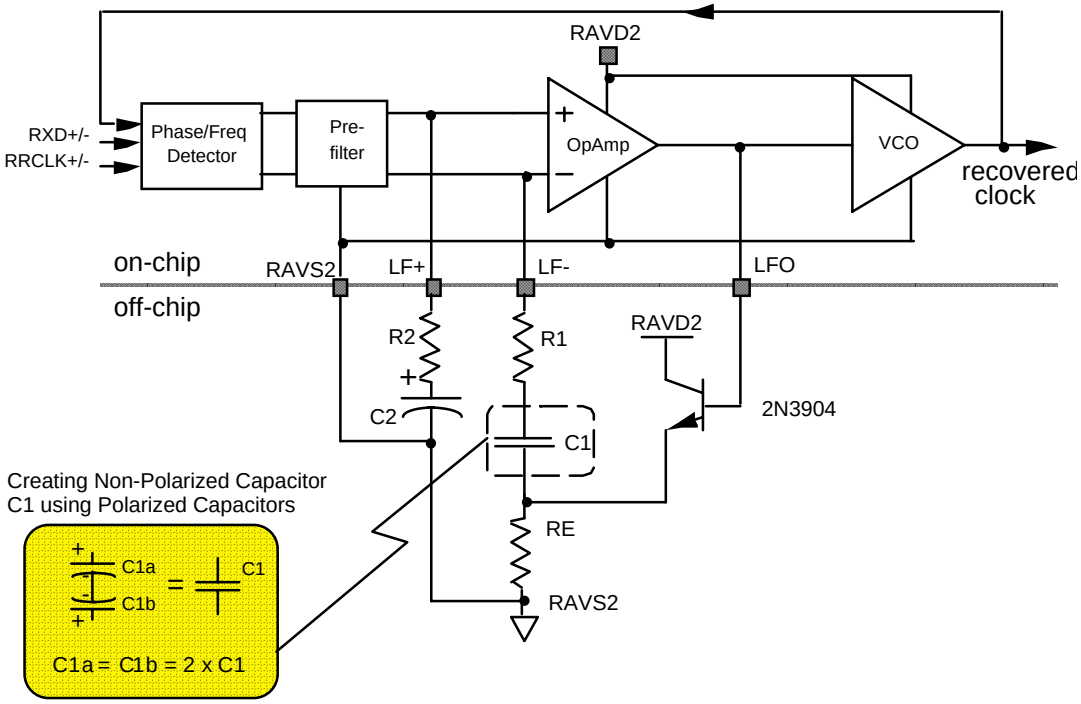


Table 4 -

Line Rate (Mbit/s)	R1 (Ω±1%)	R2 (Ω±1%)	C1, C2 (µF±20%)	RE (Ω±1%)
155.52	68.1	200	4.7	100
51.84	68.1	200	15	100

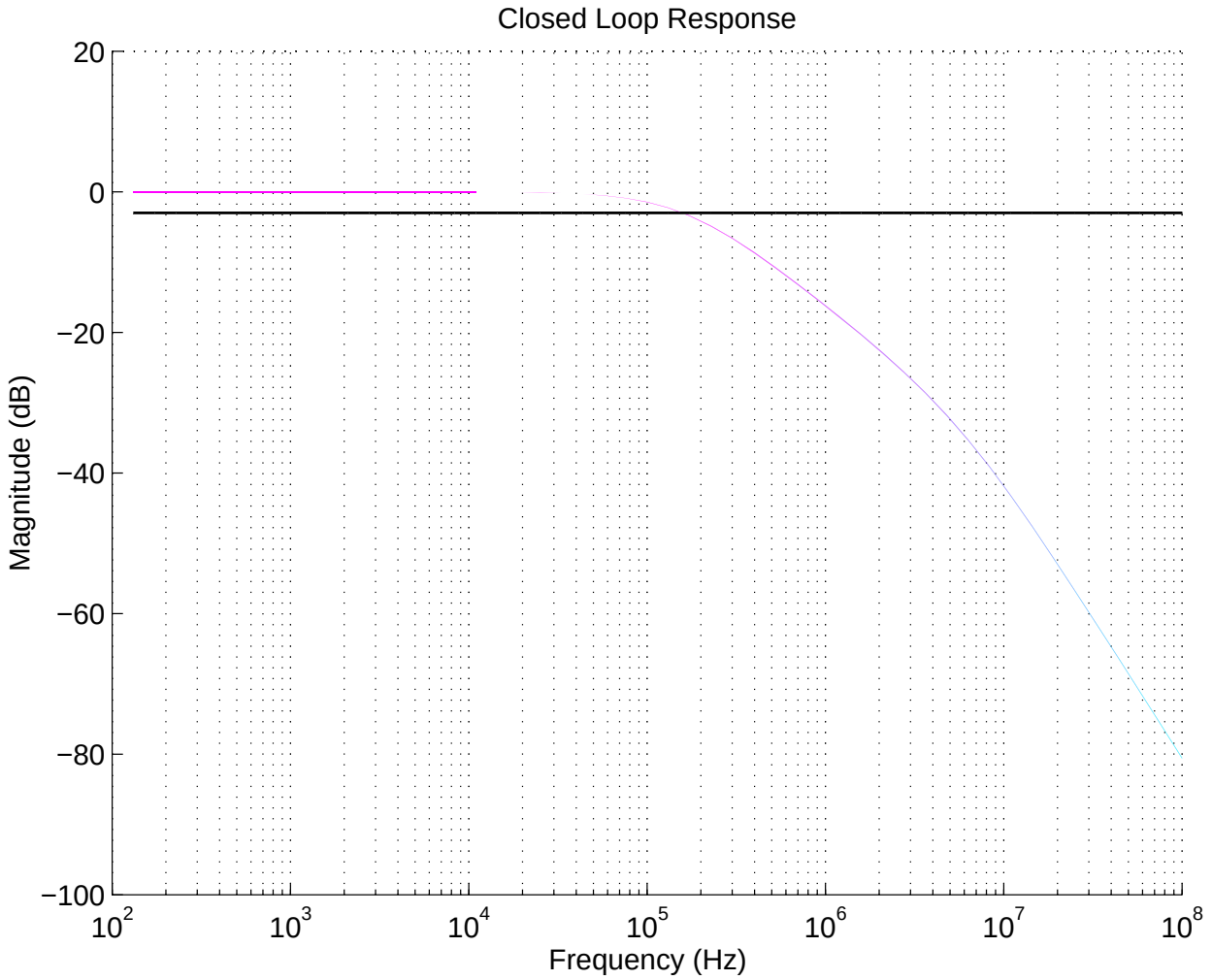
Note:

The above component values are provisional. The capacitors (C1, C2) determine the amount of "peaking" in the jitter transfer curve. Capacitor C1 should be non-polarized because when the S/UNI-DUAL is held in reset, the capacitor is reverse-biased at approximately 2.0V. Also, for some process extremes, the capacitor may operate with a D.C. reverse-bias of up to 1.0V.

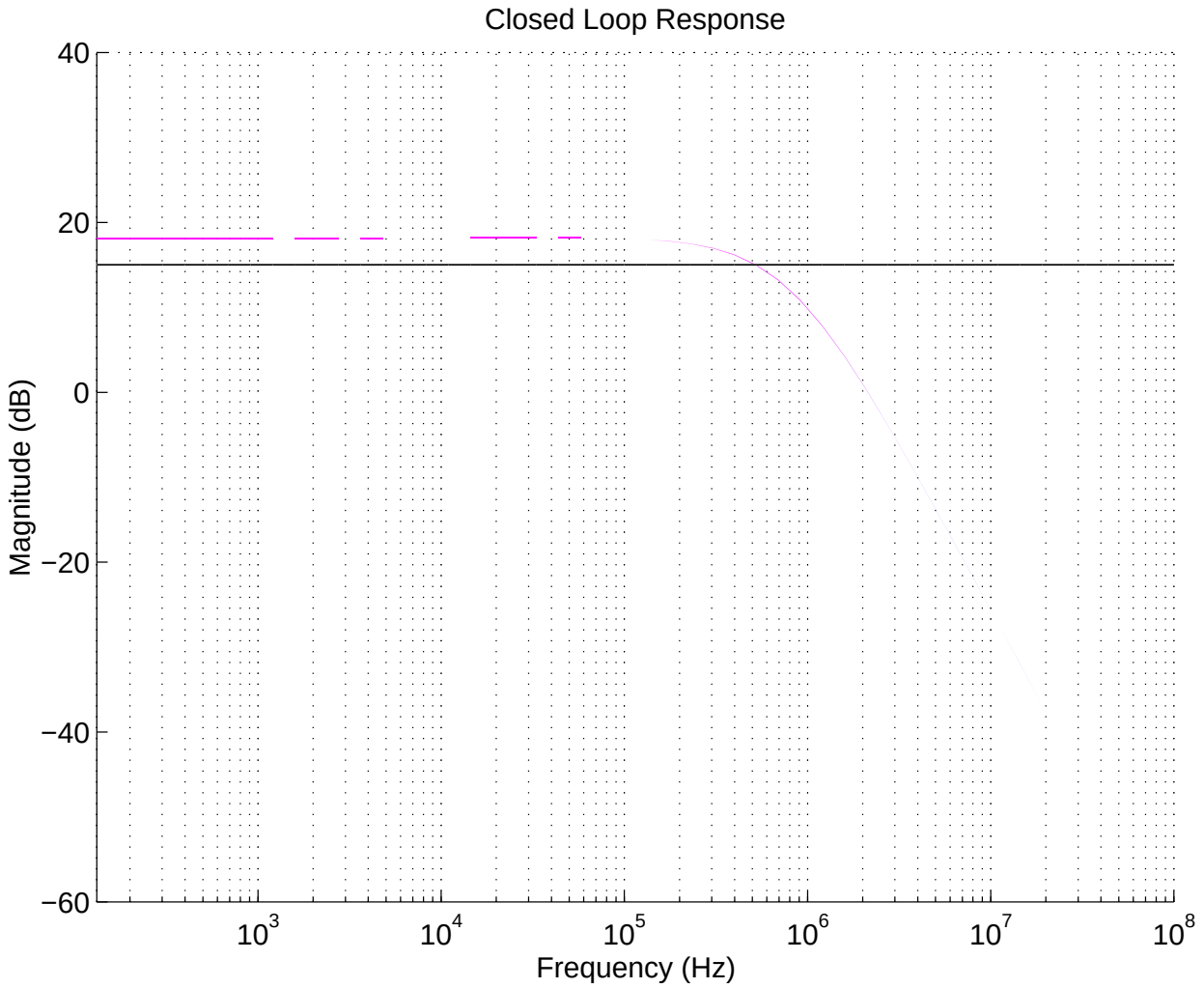
In STS-1 mode (51.84 Mbit/s), the recommended value for C1 may not be readily available in non-polarized versions. Therefore, two polarized capacitors can be connected "back-to-back" (in series, anode-to-anode or cathode to cathode) to implement the capacitance in Figure 19. Since these back-to-back capacitors will be in series, they should be of twice the value of the desired capacitance. Please see insert of Figure 19. This back-to-back configuration effectively creates a "bi-polar" capacitor. AVX Corporation has published several application notes on this issue.

4.7µF non-polarized ceramic surface mount capacitors are available from Taiyo Yuden Inc. (part No. EMK325BJ475MN-B), TDK (part No. CC1206JX5R475K), and PHILIPS (Part No. 2220RR475K8AB0C).

The following graph shows the typical closed loop response for the CRU using the recommended loop filter components:



The following graph shows the typical closed loop response for the CSU:



13.9 Bit Error Rate Monitor

The S/UNI-DUAL Bit Error Rate Monitor (BERM) block counts and monitors line BIP errors over programmable periods of time (window size). It can monitor to declare an alarm or to clear it if the alarm is already set. A different threshold and accumulation period is used to declare or clear the alarm since those two operations are not performed at the same bit error rate (BER). The following table lists the recommended content of the BERM registers for different speeds (STS-N) and BERs.

The Saturation threshold is not listed in the table, and should be programmed with the value 0xFFF by default, deactivating saturation. Saturation capabilities are provided to allow the user to address issues associated with error bursts.

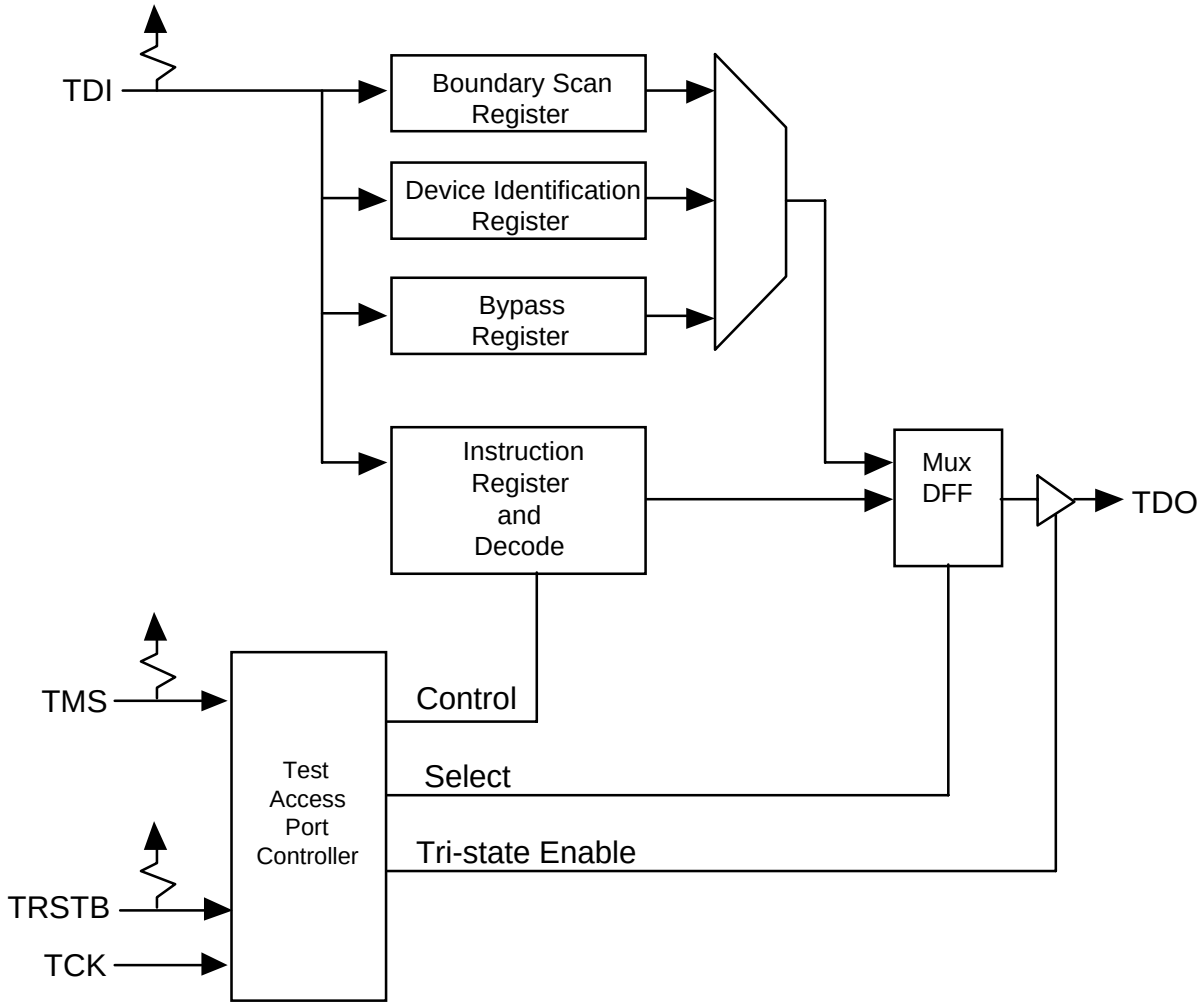
Table 5 -

STS-n	Bit Error Rate	SMODE bit	CMODE bit	Sample Accumulation Period	Declare Threshold	Clear Threshold
1	10^{-3}	0	0	0x000008	0x0BA	0x0DF
1	10^{-4}	0	0	0x000028	0x0A7	0x0D4
1	10^{-5}	0	0	0x00012C	0x084	0x0AD
1	10^{-6}	0	0	0x000BB8	0x085	0x0AF
1	10^{-7}	0	0	0x007530	0x085	0x0AF
1	10^{-8}	0	0	0x03D090	0x06D	0x093
1	10^{-9}	0	0	0x1E8480	0x055	0x078
3	10^{-3}	0	0	0x000008	0x245	0x286
3	10^{-4}	0	0	0x00000D	0x0A3	0x0CF
3	10^{-5}	0	0	0x000064	0x084	0x0AD
3	10^{-6}	0	0	0x0003E8	0x085	0x0AF
3	10^{-7}	0	0	0x002710	0x085	0x0AF
3	10^{-8}	0	0	0x014438	0x06D	0x093
3	10^{-9}	0	0	0x0A2D78	0x055	0x078

13.10 JTAG Support

The S/UNI-DUAL supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO, used to control the TAP controller and the boundary scan registers. The TRSTB input is the active low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown in Figure 20.

Figure 20 - Boundary Scan Architecture



The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single bit delay from primary input, TDI to primary output , TDO. The device identification register contains the device identification code.

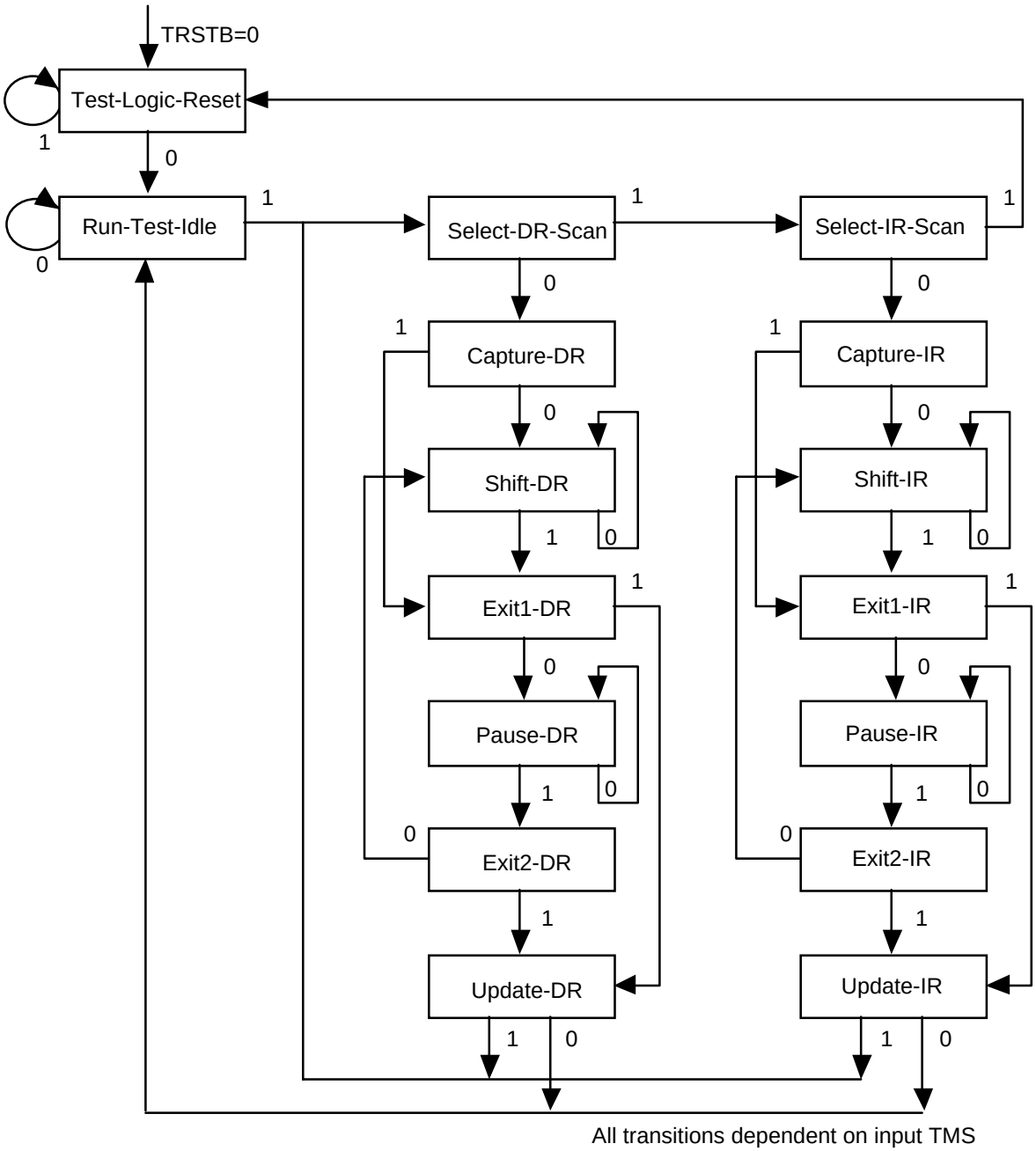
The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be

sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described in Figure 21.

Figure 21 - TAP Controller Finite State Machine



Test-Logic-Reset:

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input,

TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle:

The run test/idle state is used to execute tests.

Capture-DR:

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR:

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR:

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR:

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR:

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR:

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

The TDO output is enabled during states Shift-DR and Shift-IR. Otherwise, it is tri-stated.

Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects an serial test data register path between input, TDI, and output, TDO.

BYPASS

The bypass instruction shifts data from input TDI to output TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input TDI and output TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out on output TDO using the Shift-DR state.

Table 6 - Instruction Register

Length - 3 bits

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Identification Register

Length - 32 bits

Version number - 0x0

Part Number - 0x5348

Manufacturer's identification code - 0x0CD

Device identification - 0x053480CD

Boundary Scan Register

The boundary scan register is made up of 96 boundary scan cells, divided into input observation (in_cell), output (out_cell), and bidirectional (io_cell) cells. These cells are detailed in the Figures 22, 23, 24 and 25. The first 32 cells form the ID code register, and carry the code 0x053480CD. The cells are arranged as follows:

Table 7 -

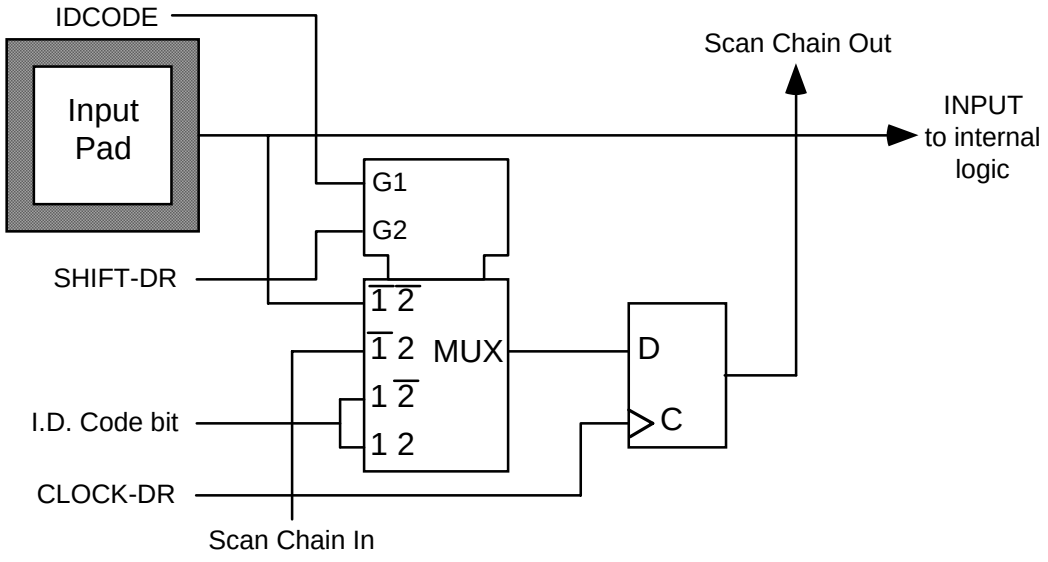
Pin/ Enable	Register Bit	Cell Type	I.D. Bit(s)	Pin/ Enable	Register Bit	Cell Type	I.D Bit(s).
hiz[1]	95	OUT_CELL	0	txprty[0:1]	29 - 28	in_CELL	-
RDLENB[3]	94	OUT_CELL	0	ralm2	27	OUT_CELL	-
RDHENB[4]	93	OUT_CELL	0	ralm1	26	OUT_CELL	-
RSCO2_ENB[5]	92	OUT_CELL	0	out[1:0]	25 - 24	OUT_CELL	-
a[0:8]	91 - 83	IN_CELL	010100110	tsen	23	in_CELL	-
ale	82	IN_CELL	1	rfp	22	OUT_CELL	-
rstb	81	IN_CELL	0	rclk2	21	OUT_CELL	-
csb	80	IN_CELL	0	rclk1	20	out_CELL	-
wrb	79	IN_CELL	1	tfp	19	IO_CELL	-
rdb	78	IN_CELL	0	tfp_input_en	18	OUT_CELL	-
rrdenb1	77	IN_CELL	0	tclk	17	out_CELL	-
rrdenb2	76	IN_CELL	0	d[7]	16	io_CELL	-
rca1	75	out_CELL	0	oenb[7][2]	15	OUT_CELL	-
rca2	74	out_CELL	0	d[6]	14	io_CELL	-
rsoc1	73	out_CELL	0	oenb[6][2]	13	OUT_CELL	-
rsoc2	72	out_CELL	0	d[5]	12	io_CELL	-
rdat[0:7]	71 - 64	out_CELL	11001101	oenb[5][2]	11	OUT_CELL	-
rdat[8:15]	63 - 56	out_CELL	-	d[4]	10	io_CELL	-
rxprty[0:1]	55 - 54	out_CELL	-	oenb[4][2]	9	OUT_CELL	-
rfclk	53	IN_CELL	0	d[3]	8	io_CELL	-
twrenb1	52	IN_CELL	1	oenb[3][2]	7	OUT_CELL	-
twrenb2	51	IN_CELL	1	d[2]	6	io_CELL	-
tca1	50	OUT_CELL	0	oenb[2][2]	5	OUT_CELL	

Pin/ Enable	Register Bit	Cell Type	I.D. Bit(s)	Pin/ Enable	Register Bit	Cell Type	I.D Bit(s).
tca2	49	OUT_CELL	1	d[1]	4	io_CELL	-
tsoc1	48	in_CELL	-	oenb[1][2]	3	OUT_CELL	-
tsoc2	47	in_CELL	-	d[0]	2	io_CELL	-
tdat[0:4]	46 - 42	IN_CELL	-	oenb[0][2]	1	OUT_CELL	-
tfclk	41	IN_cell	-	intb	0	OUT_CELL	-
tdat[5:15]	40 - 30	in_celL	-				

Notes:

1. HIZ is the first bit of the boundary scan chain, and when set high, TCA1, TCA2, RALM2, RALM1, OUT[1:0], RFP, RCLK1, RCLK2, TCLK, TXD1+/-, TXD2+/-, RCA1 and RCA2 will be set to high impedance.
2. All OENB signals will set the corresponding bidirectional pin to an output when set low.
3. When set high, RDAT[7:0], RXPRTY[0] and RSOC1 will be set to high impedance.
4. When set high, RDAT[15:8] and RXPRTY[1] will be set to high impedance.
5. When set high, RSOC2 will be set to high impedance.

Figure 22 - Input Observation Cell (IN_CELL)



In this diagram and those that follow, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the centre of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the table above.

Figure 23 - Output Cell (OUT_CELL)

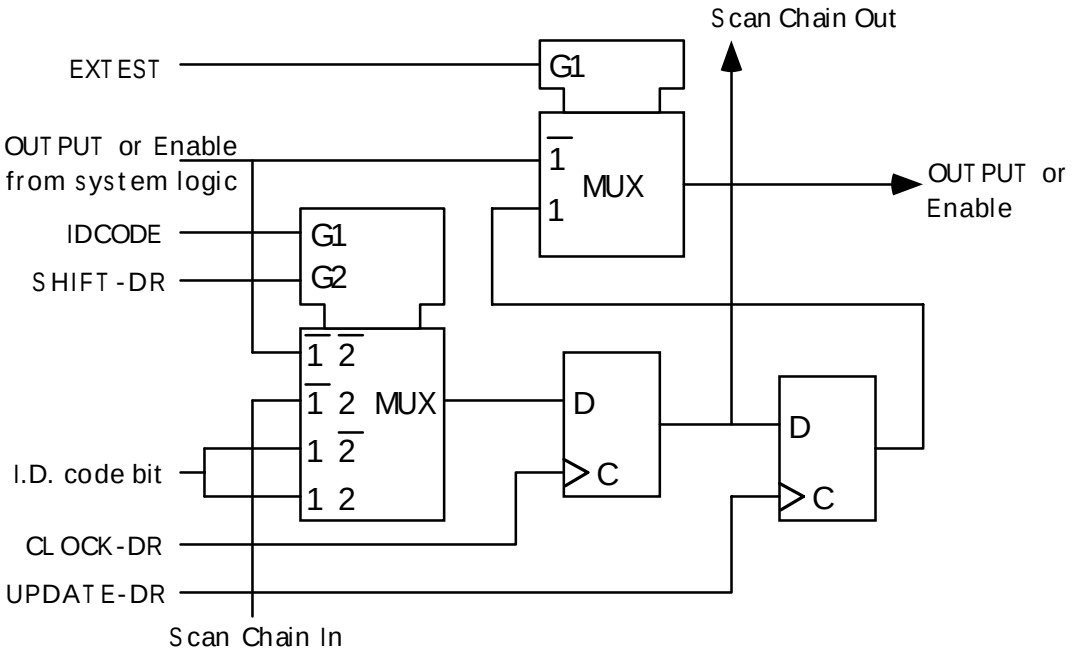


Figure 24 - Bidirectional Cell (IO_CELL)

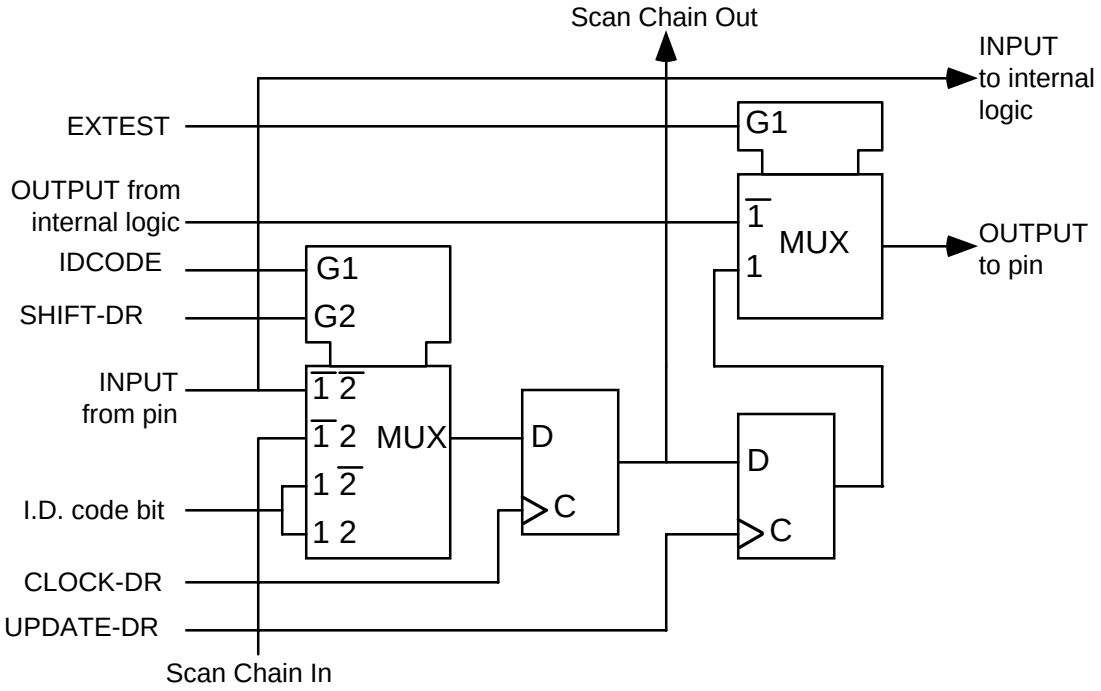
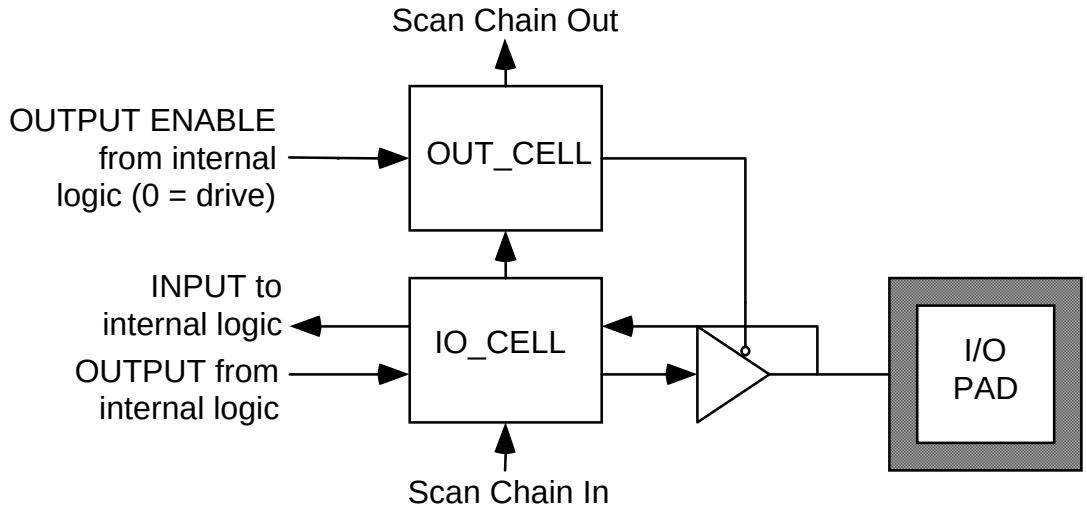


Figure 25 - Layout of Output Enable and Bidirectional Cells



13.11 Power Sequencing

Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions it is possible to damage these ESD protection devices or trigger latch up. The recommended power supply sequencing is as follows:

1. VDD_DC power must be supplied either before VDD_AC or simultaneously with VDD_AC to prevent current flow through the ESD protection devices which exist between VDD_DC and VDD_AC power supplies. Connection to a common VDD power plane is the recommended standard practice for customer applications.

2. To prevent damage to the ESD protection on the device inputs the maximum DC input current specification must be respected. This is accomplished by either ensuring that the VDD_DC power is applied before input pins are driven or by increasing the source impedance of the driver so that the maximum driver short circuit current is less than the maximum DC input current specification (20 mA).

3. Analog power supplies must be applied after both VDD_DC and VDD_AC have been applied or they must be current limited to the maximum latchup current specification (100 mA). To prevent forward biasing the ESD protection diode between AVD supplies and VDD_DC, the differential voltage measured between these power supplies must be less than 0.5 volt. This recommended differential voltage is to include peak to peak noise on the VDD_DC power supply as digital noise will otherwise be coupled into the analog circuitry. Current limiting can be accomplished by using an off chip three terminal voltage regulator supplied by a quiet high voltage supply. If the VDD power supply is relatively quiet, VDD can be filtered using a ferrite bead and a high frequency decoupling capacitor to supply AVD. The relative power sequencing of the multiple AVD power supplies is not important.

4. Power down the device in the reverse sequence. Use the above current limiting technique for the analog power supplies. Small offsets in VDD and AVD discharge times will not damage the device.

14 FUNCTIONAL TIMING

14.1 Drop Side Receive Interface

The Receive FIFO can operates in two different modes: Multi-PHY and Split-Bus Direct-PHY. Each mode of operation has various options available: FIFO empty indication, data bus width and bus tristating. In the Split-Bus mode of operation, the interface operates as two independent 8-bit PHY interfaces; therefore, the bus width is fixed at 8 bits. Figure 26 illustrates the Split-Bus mode. Figure 27 and Figure 28 illustrate the Multi-PHY mode.

Figure 26 - Split-Bus Mode, Receive FIFO Empty Option

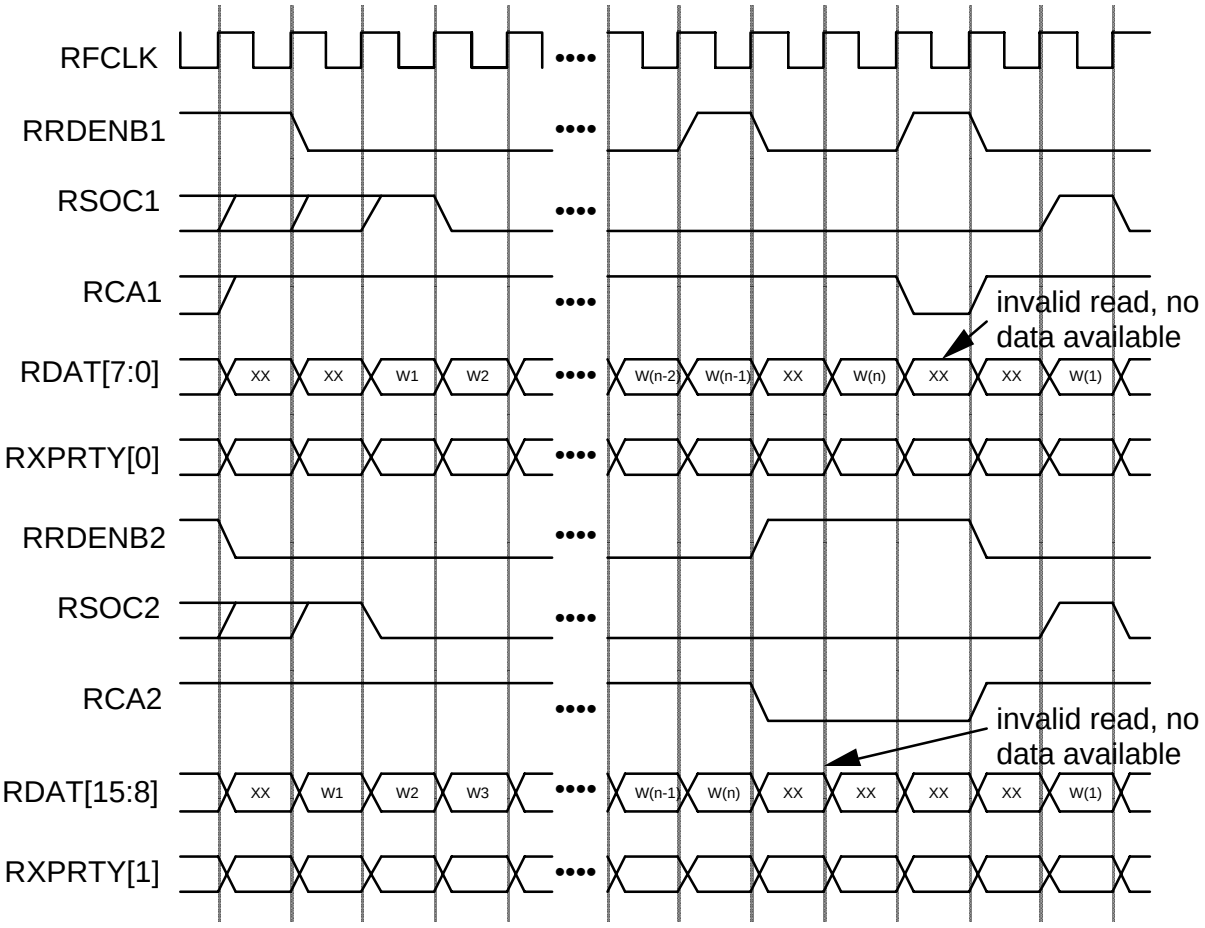


Figure 27 - 16-bit Multi-PHY Mode, Receive FIFO Empty and Tristate Options

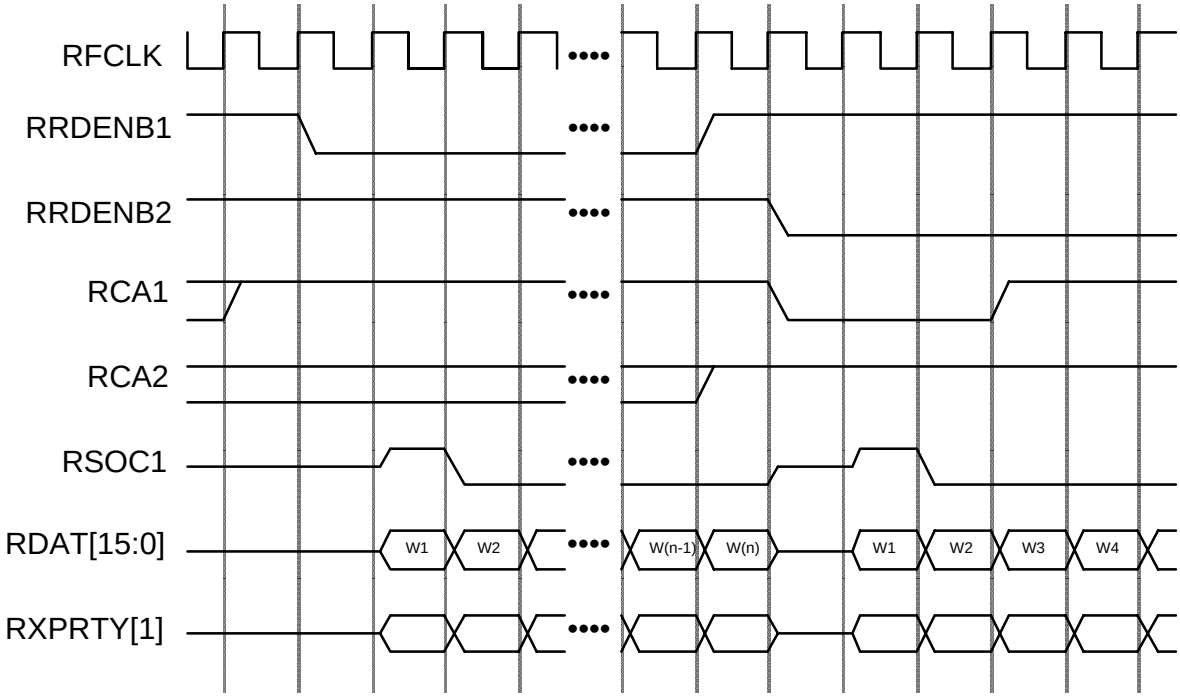
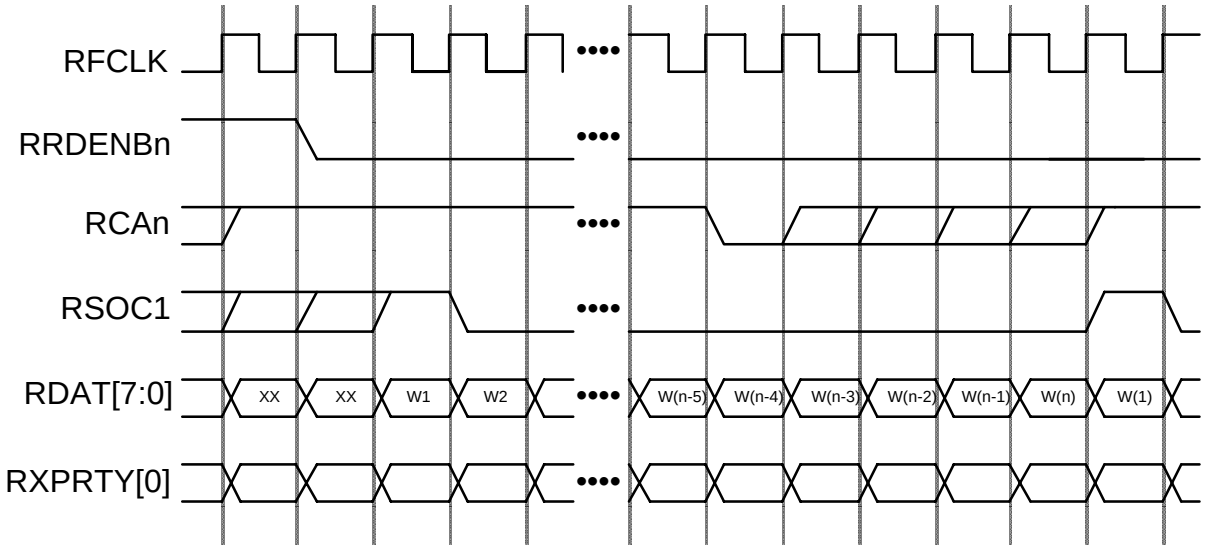


Figure 28 - 8-bit Multi-PHY Mode, Receive FIFO Near Empty Option



The S/UNI-DUAL indicates that a cell is available by asserting the corresponding receive cell available signal, RCA. RCA remains high until the internal FIFO is near empty or empty. Near empty implies that the ATM Layer device, after sampling RCA deasserted, can initiate at most four additional reads. Empty implies that the ATM Layer device, after sampling RCA deasserted, can initiate no more additional reads. The ATM Layer device indicates, by asserting the corresponding RRDENB signal, that the data on the receive FIFO data bus, during the next RFCLK cycle, will be read from the S/UNI-DUAL.

Figure 26 illustrates the Receive FIFO empty option in Split-Bus mode. RCA1 transitions low when the last word of the last cell is available on the RDAT[7:0] bus. RCA2 transitions low when the last word of the last cell is available on the RDAT[15:8] bus. The RDAT[7:0] bus, RXPRTY[0] and RSOC1 are valid in cycles for which RCA1 is high and RRDENB1 was low is the previous cycle. The RDAT[15:8] bus, RXPRTY[1] and RSOC2 are valid in cycles for which RCA2 is high and RRDENB2 was low is the previous cycle. If the ATM Layer device requests a read while either RCA1 or RCA2 is deasserted, then the PHY layer device will ignore the additional reads. In Figure 26, TSEN is set to logic 0, RDAT[15:0], RXPRTY[1:0], RSOC2 and RSOC1 always drive a valid logic level. If TSEN is set to a logic 1, RRDENB1 controls the tristating of RDAT[7:0], RXPRTY[0] and RSOC1, and RRDENB2 controls the tristating of RDAT[15:8], RXPRTY[1] and RSOC2.

Figure 27 illustrates the Receive FIFO empty and tri-state options in 16-bit Multi-PHY mode. The RCA performance is the same as that described for the Split-Bus Mode in Figure 26. The exception is that only one PHY channel can be accessed at a time; therefore, only one RRDENB signal may be active at a time. The RSOC2 output is not used in Multi-PHY mode and is tristated. In Figure 27, TSEN is set to logic 1, and if neither RRDENB1 or RRDENB2 is active then RDAT[15:0], RXPRTY[1:0] and RSOC1 are tristated. If TSEN is set to a logic 0, then RDAT[15:0], RXPRTY[1:0] and RSOC1 always drive a valid logic level.

Figure 28 illustrates the Receive FIFO near empty option in 8-bit Multi-PHY mode. The near empty option is selected by setting the RCALEVEL0 bit to logic 0 in the RACP Configuration register. RCAn transitions low four words before the last word of the last cell is read from corresponding channel of the S/UNI-DUAL. RCAn remains low for a minimum of one RFCLK clock cycle and then can transition high to indicate that there are additional cells available from the corresponding channel's PHY layer device. Once RCAn is deasserted and has been sampled, the ATM Layer device can issue no more than four reads to the corresponding channel. If the ATM Layer device issues more reads than the allowable number, and RCAn remains deasserted throughout, the corresponding channel of the PHY layer device will ignore the additional reads.

The following table indicates which inputs and outputs are used depending on the settings of the SPLIT and BUS8 bits in the S/UNI-DUAL Interface Control register:

Table 8 -

SPLIT	BUS8	Common Signals	Channel #1 Signals	Channel #2 Signals	Unused Signals
0	0	RDAT[15:0], RXPRTY[1], RSOC1	RCA1, RRDENB1	RCA2, RRDENB2	RSOC2 RXPRTY[0]
0	1	RDAT[7:0], RXPRTY[0], RSOC1	RCA1, RRDENB1	RCA2, RRDENB2	RSOC2 RDAT[15:8] RXPRTY[1]
1	X		RDAT[7:0], RXPRTY[0], RSOC1, RCA1, RRDENB1	RDAT[15:8], RXPRTY[1], RSOC2, RCA2, RRDENB2	

14.2 Drop Side Transmit Interface

The Transmit FIFO can operates in two different modes: Multi-PHY and Split-Bus Direct-PHY. Each mode of operation has various options available: FIFO empty indication and data bus width. In the Split-Bus mode of operation, the interface operates as two independent 8-bit PHY interfaces; therefore, the bus width is fixed at 8 bits. Figure 29 illustrates the Split-Bus mode, and Figure 30 illustrates the Multi-PHY mode.

Figure 29 - Split-Bus Mode, Transmit FIFO Empty Option

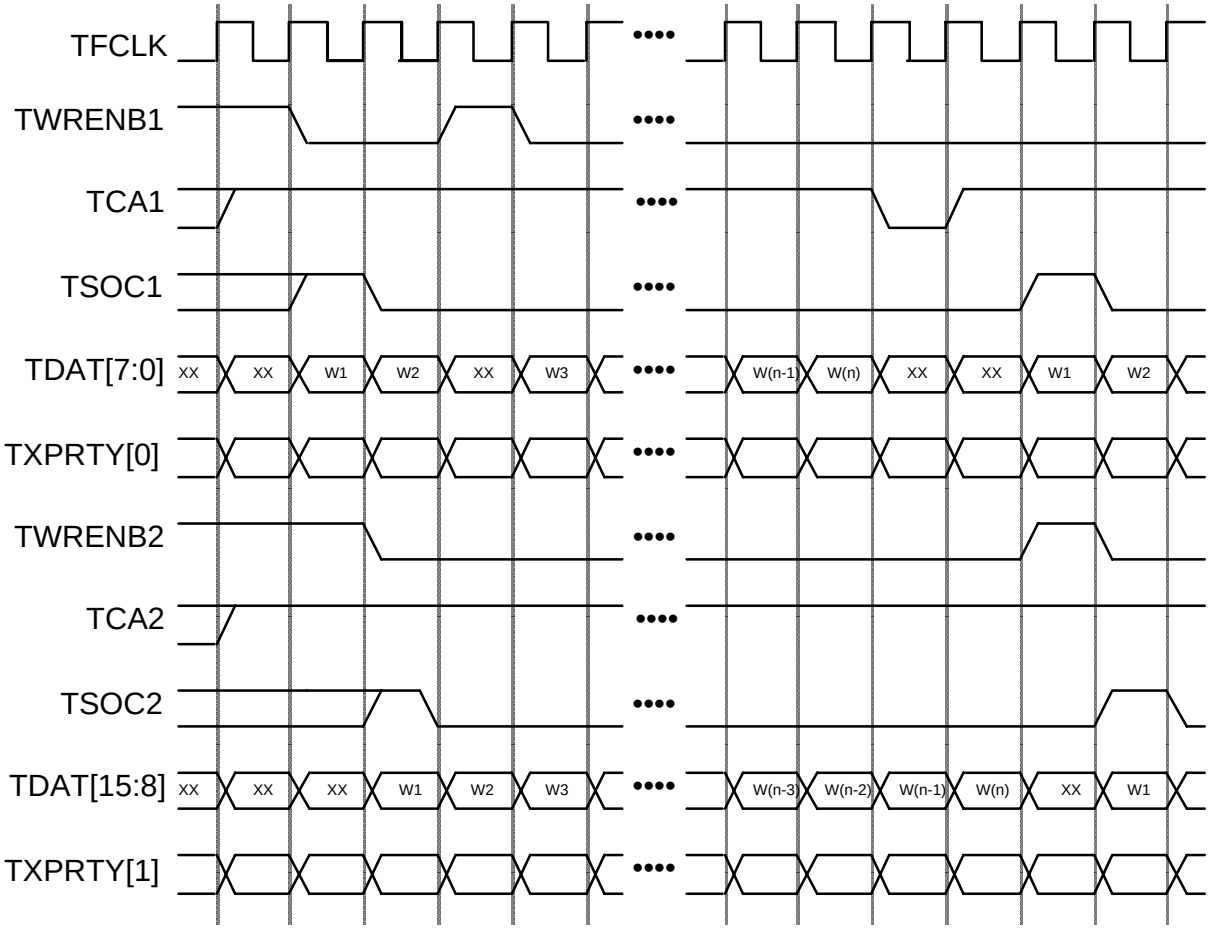
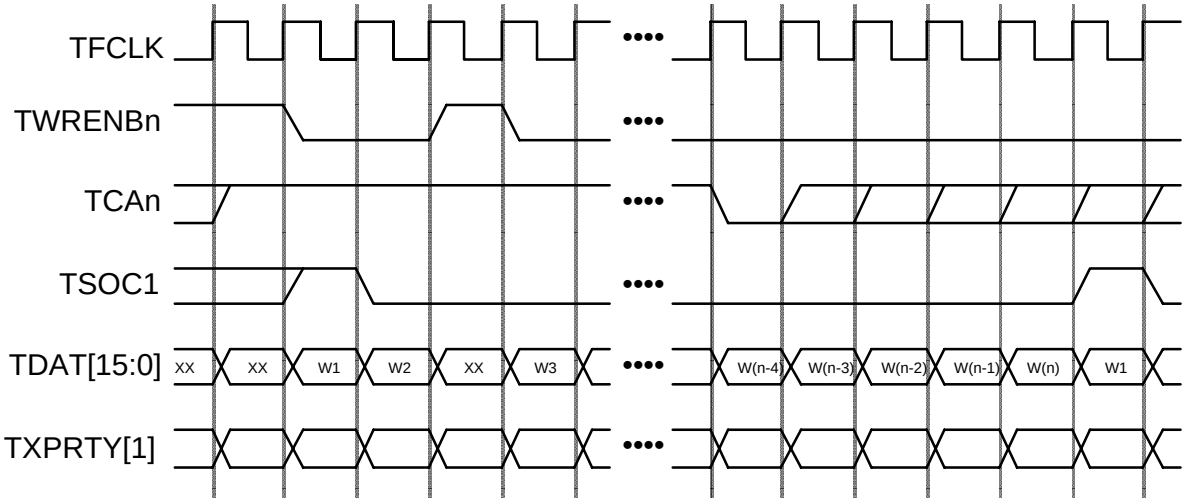


Figure 30 - 16-bit Multi-PHY Mode, Transmit FIFO Near Empty Option



The S/UNI-DUAL indicates that there is space available for a full cell in its internal FIFO by asserting the transmit cell available signal, TCA. TCA remains asserted until the transmit FIFO is full or almost full. Full implies that the ATM Layer device, after sampling TCA deasserted, can initiate no more additional writes. Almost full implies that the ATM Layer device, after sampling TCA deasserted, can initiate at most four additional writes. The ATM Layer device indicates, by asserting the corresponding TWRENB signal, that the data on the transmit FIFO data bus, during the current RFCLK cycle, will be written to the S/UNI-DUAL.

Figure 29 illustrates the transmit FIFO full option in Split-Bus mode. The full option is selected by setting the TCALEVEL0 bit to logic 1 in the TACP FIFO Control register. If TCA1 is asserted and the ATM Layer device is ready to write a byte into channel #1, it should assert TWRENB1 low and present the byte on the TDAT[7:0] bus. If the presented byte is the first byte of a cell, the ATM Layer device should also assert signal TSOC1. If TCA2 is asserted and the ATM Layer device is ready to write a byte into channel #2, it should assert TWRENB2 low and present the byte on the TDAT[15:8] bus. If the presented byte is the first byte of a cell, the ATM Layer device should also assert signal TSOC2. At any time, if the ATM Layer device does not have a byte to write on either channel, it can deassert the corresponding TWRENB.

Figure 30 illustrates the transmit FIFO almost full option in 16-bit Multi-PHY mode. If TCAn is asserted and the ATM Layer device is ready to write a byte to the corresponding channel, it should assert TWRENBn low and present the byte on the TDAT[15:0] bus. If the presented byte is the first byte of a cell, the ATM

Layer device should also assert signal TSOC1. At any time, if the ATM Layer device does not have a byte to write, it can deassert TWRENBn. When TCAn is deasserted and it has been sampled, the ATM Layer device can write no more than four bytes to the corresponding PHY layer device. If the ATM Layer writes more than four bytes and TCAn remains deasserted throughout, the corresponding channel of the S/UNI-DUAL will indicate an error condition and ignore additional writes until it asserts TCAn again.

The following table indicates which inputs and outputs are used depending on the settings of the SPLIT and BUS8 bits in the S/UNI-DUAL Interface Control register:

Table 9 -

SPLIT	BUS8	Common Signals	Channel #1 Signals	Channel #2 Signals	Unused Signals
0	0	TDAT[15:0], TXPRTY[1], TSOC1	TCA1, TWRENB1	TCA2, TWRENB2	TSOC2, TXPRTY[0]
0	1	TDAT[7:0], TXPRTY[0], TSOC1	TCA1, TWRENB1	TCA2, TWRENB2	TSOC2, TXPRTY[1], TDAT[15:8]
1	X		TDAT[7:0], TXPRTY[0], TSOC1, TCA1, TWRENB1	TDAT[15:8], TXPRTY[1], TSOC2, TCA2, TWRENB2	

15 ABSOLUTE MAXIMUM RATINGS

Table 10 - S/UNI-DUAL Absolute Maximum Ratings

Ambient Temperature under Bias	0°C to +70°C
Storage Temperature	-40°C to +125°C
Supply Voltage	-0.5V to +6.0V
Voltage on Any Pin	-0.5V to V_{DD}+0.5V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+300°C
Absolute Maximum Junction Temperature	+150°C

16 D.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{DD} = 5 V ±10%, A_{VD} = 5V ±10%)

Table 11 - S/UNI-DUAL D.C. Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{IL}	Input Low Voltage (TTL Only)	-0.5		0.8	Volts	Guaranteed Input LOW Voltage
V_{PIL}	Input Low Voltage (ALOS1+/-, ALOS2+/- Only)	A_{VD} -1.8		A_{VD} -1.6	Volts	Guaranteed Input LOW Voltage referenced to R1AVD3 or R2AVD3. With input in PECL mode. See Figure 16.
V_{TPIL}	Input Low Voltage (ALOS1-, ALOS2- REFCLK- Only)	-0.5		0.8	Volts	Guaranteed Input LOW Voltage of inputs while in TTL/CMOS mode. See Figure 17.
V_{IH}	Input High Voltage (TTL Only)	2.0		V_{DD} +0.5	Volts	Guaranteed Input HIGH Voltage
V_{PIH}	Input High Voltage (ALOS1+/-, ALOS2+/- Only)	A_{VD} -1.0		A_{VD} -0.8	Volts	Guaranteed Input HIGH Voltage referenced to R1AVD3 or R2AVD3. With input in PECL mode. See Figure 16.

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{TPIH}	Input High Voltage (ALOS1-, ALOS2-, REFCLK-Only)	2.2		V_{DD} +0.5	Volts	Guaranteed Input HIGH Voltage of inputs while in TTL/CMOS mode. See Figure 17.
V_{PSWG}	Input Voltage Swing (RXD1+/-, RXD2+/-, REFCLK+/-Only)	600		1000	mV	Input swing assuming ECL/PECL signal AC coupled as illustrated in Figures 17 and 18.
V_{OL}	Output or Bidirectional Low Voltage		0.1	0.4	Volts	I_{OL} = -4 mA for outputs RDAT[15:0], RSOC[2:1], RXPRTY[1:0], RCA[2:1], TCA[2:1], TCLK, RCLK1, and RCLK2. I_{OL} = -2 mA for all others, Note 3
V_{TXOL}	Output Low Voltage (TXD1+/-, TXD2+/-only)			0.4	Volts	I_{OL} = -6 mA for outputs TXD1+/- and TXD2+/-, Note 5
V_{OH}	Output or Bidirectional High Voltage	2.4	4.7		Volts	I_{OH} = 4 mA for outputs RDAT[15:0], RSOC[2:1], RXPRTY[1:0], RCA[2:1], TCA[2:1], TCLK, RCLK1, and RCLK2. I_{OH} = 2 mA for all others, Note 3

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{TXOH}	Output High Voltage (TXD1+/-, TXD2+/- only)	3.9			Volts	I_{OL} = 6 mA for outputs TXD1+/- and TXD2+/-, Note 5
V_{T+}	Reset Input High Voltage	3.5			Volts	
V_{T-}	Reset Input Low Voltage			0.8	Volts	
V_{TH}	Reset Input Hysteresis Voltage		1.0		Volts	
I_{ILPU}	Input Low Current	175	330	525	µA	V_{IL} = GND, Notes 1, 3
I_{IHPU}	Input High Current	-10		+10	µA	$V_{IH} = V_{DD}$, Notes 1, 3
I_{IL}	Input Low Current	-10		+10	µA	V_{IL} = GND, Notes 2, 3
I_{IH}	Input High Current	-10		+10	µA	$V_{IH} = V_{DD}$, Notes 2, 3
C_{IN}	Input Capacitance		5		pF	Excluding Package, Package Typically 2 pF
C_{OUT}	Output Capacitance		5		pF	Excluding Package, Package Typically 2 pF
C_{IO}	Bidirectional Capacitance		5		pF	Excluding Package, Package Typically 2 pF

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{DDOP}	Operating Current Processing Cells (Split-Bus mode operating at 50 MHz)			295 280 175 160	mA mA mA mA	Outputs Unloaded V_{DD} = 5.5V, STS-3 V_{DD} = 5.25V, STS-3 V_{DD} = 5.5V, STS-1 V_{DD} = 5.25V, STS-1

Notes on D.C. Characteristics:

1. Input pin or bidirectional pin with internal pull-up resistor.
2. Input pin or bidirectional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. Input pin or bidirectional pin with internal pull-down resistor.
5. The values for VTXOL and VTXOH ensure a minimum 600 mV swing at the ECL buffer input when the circuit shown in Figure 18 is used to attenuate TXD1+/- and TXD2+/-.
6. Typical values are not production tested.

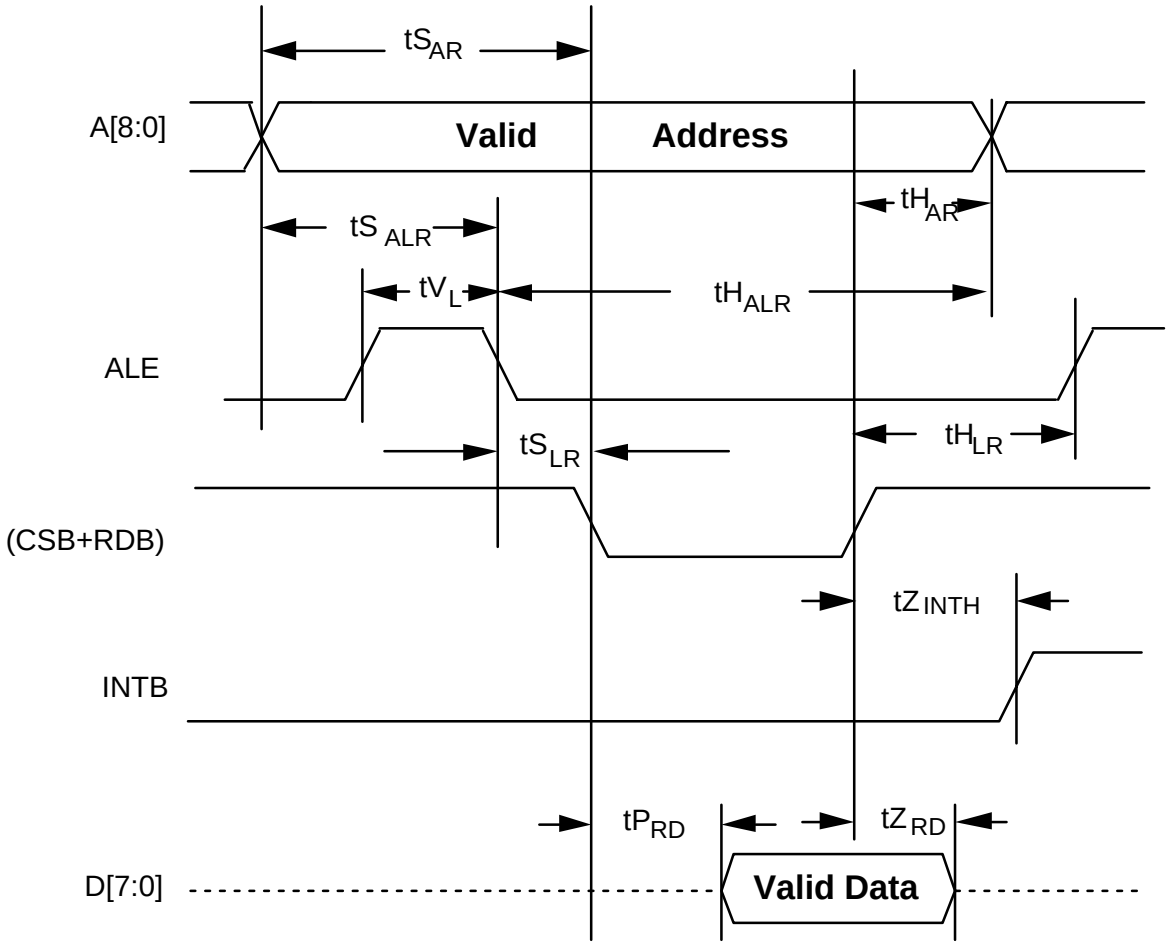
17 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T_A = 0°C to +70°C, V_{DD} = 5 V ±10%)

Table 12 - Microprocessor Interface Read Access (Figure 31)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	25		ns
tH_{AR}	Address to Valid Read Hold Time	5		ns
tS_{ALR}	Address to Latch Set-up Time	20		ns
tH_{ALR}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	5		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		80	ns
tZ_{RD}	Valid Read Negated to Output Tri-state		20	ns
tZ_{INTH}	Valid Read Negated to Output Tri-state		50	ns

Figure 31 - Microprocessor Interface Read Timing



Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. Microprocessor Interface timing applies to normal mode register accesses only.

5. In non-multiplexed address/data bus architectures, ALE should be held high, parameters tS_{ALR}, tH_{ALR}, tV_L, and tS_{LR} are not applicable.

6. Parameters tH_{AR} and tS_{AR} are not applicable if address latching is used.

7. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

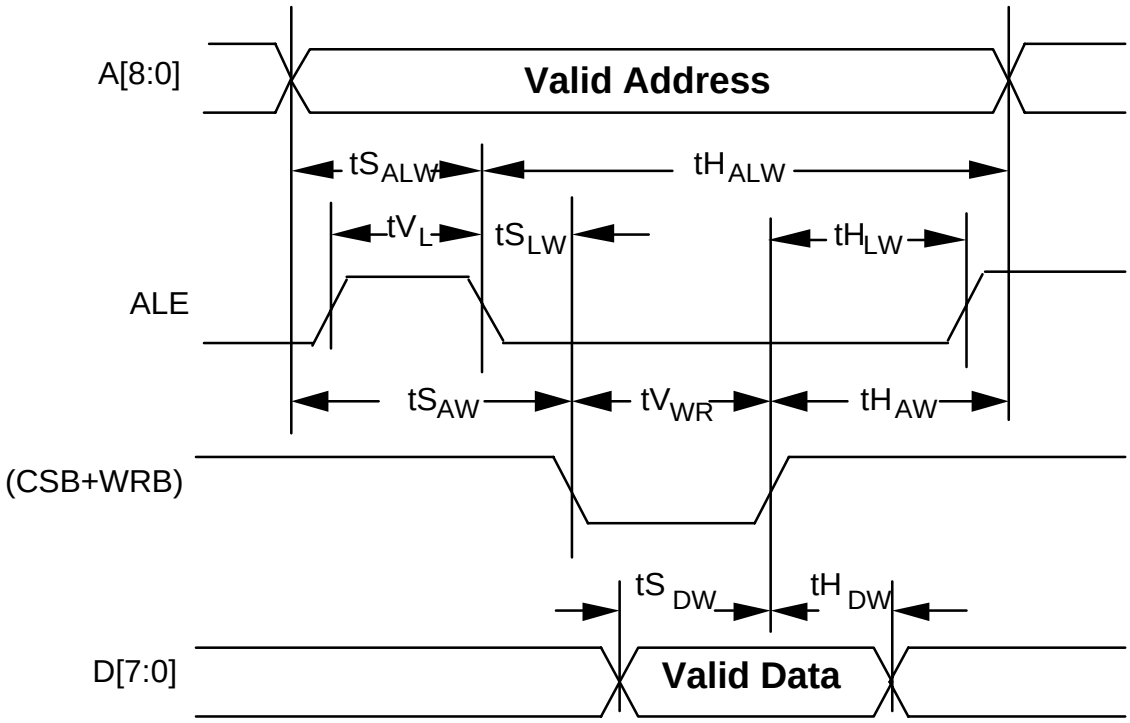
8. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

9. Output tristate delay is the time in nanoseconds from the 1.4 Volt point of the reference signal to ±300mV of the termination voltage on the output. The test load is 50Ω to 1.4V in parallel with 10 pf to GND.

Table 13 - Microprocessor Interface Write Access (Figure 32)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	25		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	20		ns
tH_{ALW}	Address to Latch Hold Time	10		ns
tV_L	Valid Latch Pulse Width	20		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	5		ns
tH_{DW}	Data to Valid Write Hold Time	5		ns
tH_{AW}	Address to Valid Write Hold Time	5		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Figure 32 - Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.

2. Microprocessor Interface timing applies to normal mode register accesses only.

3. In non-multiplexed address/data bus architectures, ALE should be held high, parameters tS_{ALW}, tH_{ALW}, tV_L, and tS_{LW} are not applicable.

4. Parameters tH_{AW} and tS_{AW} are not applicable if address latching is used.

5. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

6. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

18 S/UNI-DUAL TIMING CHARACTERISTICS

(T_A = 0°C to +70°C, V_{DD} = 5 V ±10%)

Table 14 - Line Side Reference Clock

Symbol	Description	Min	Max	Units
	REFCLK+/REFCLK- Duty Cycle 19.44 or 6.48 MHz	30	70	%
	REFCLK+/REFCLK- Frequency Tolerance†	-20	+20	ppm

† The specification may be relaxed to +/- 50 ppm if the S/UNI-DUAL is not loop timed, or for LAN applications that do not require this timing accuracy. If loop timing is enabled, the tighter tolerance is required to meet the SONET free run accuracy specification under loss of signal conditions.

Table 15 - Receive Frame Pulse Output (Figure 33)

Symbol	Description	Min	Max	Units
tP_{RFP}	**RCLK2 High to RFP Valid**	**2**	**20**	**ns**
	RCLK1 High to RFP Valid	**2**	**20**	**ns**

Figure 33 - Receive Frame Pulse Output Timing

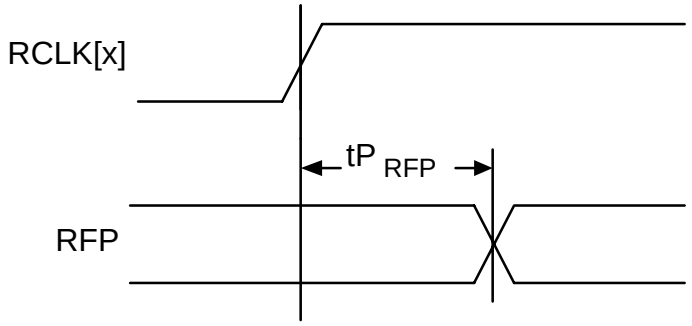


Table 16 - Transmit Frame Pulse (Figure 34)

Symbol	Description	Min	Max	Units
tP_{TFP}	TCLK High to TFP Valid (TFP_TS bit is logic 0)	-3	10	ns

Figure 34 - Transmit Frame Pulse Output Timing

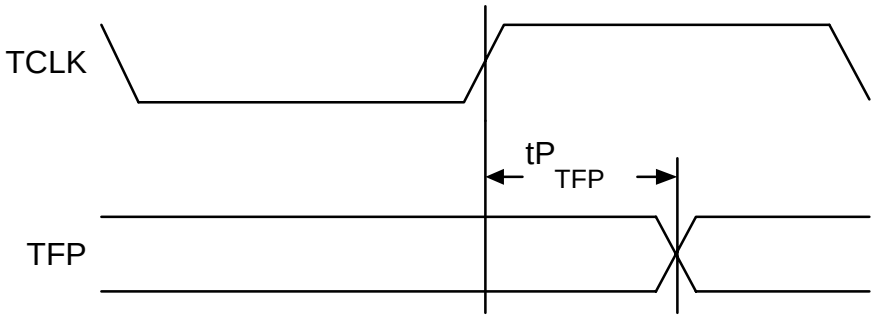


Table 17 - Drop Side Receive Synchronous Interface (Figure 35)

Symbol	Description	Min	Max	Units
	RFCLK Frequency		52	MHz
	RFCLK Duty Cycle	40	60	%
tS_{RRDENB}	RRDENB[2:1] to RFCLK High Setup	4		ns
tH_{RRDENB}	RFCLK High to RRDENB[2:1] Hold	1		ns
tP_{RDAT}	RFCLK High to RDAT[15:0] Valid	2	14	ns
tP_{RXP}	RFCLK High to RXPRTY[1:0] Valid	2	14	ns
tP_{RCA}	RFCLK High to RCA[2:1] Valid	2	14	ns
tP_{RSOC}	RFCLK High to RSOC[2:1] Valid	2	14	ns

Figure 35 - Drop Side Receive Synchronous Interface Timing (TSEN = 0)

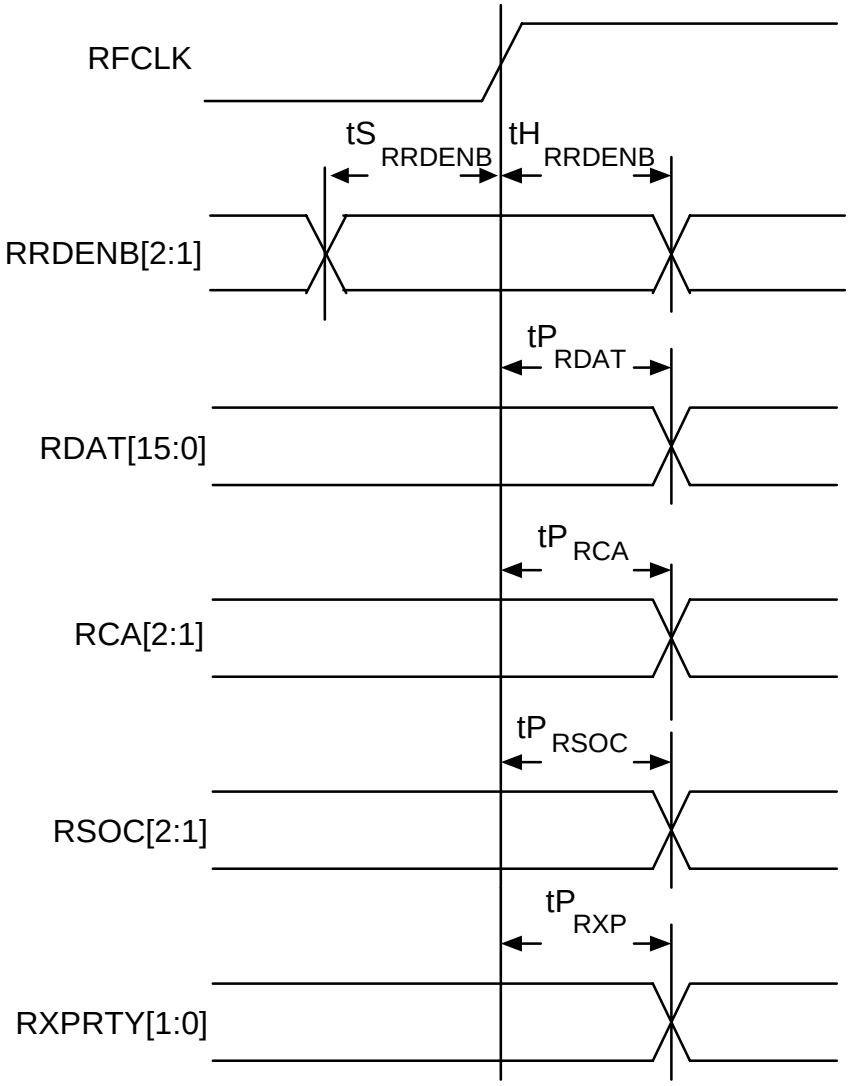


Table 18 - Drop Side Receive Synchronous Interface (Figure 36)

Symbol	Description	Min	Max	Units
	RFCLK Frequency		52	MHz
	RFCLK Duty Cycle	40	60	%
tS_{RRDENB}	RRDENB[2:1] to RFCLK High Setup	4		ns

Symbol	Description	Min	Max	Units
tH_{RRDENB}	RFCLK High to RRDENB[2:1] Hold	1		ns
tP_{RDAT}	RFCLK High to RDAT[15:0] Valid	2	14	ns
tZ_{RDAT}	RFCLK High to RDAT[15:0] Tristate	2	14	ns
tP_{RXP}	RFCLK High to RXPRTY[1:0] Valid	2	14	ns
tZ_{RXP}	RFCLK High to RXPRTY[1:0] Tristate	2	14	ns
tP_{RCA}	RFCLK High to RCA[2:1] Valid	2	14	ns
tP_{RSOC}	RFCLK High to RSOC[2:1] Valid	2	14	ns
tZ_{RSOC}	RFCLK High to RSOC[2:1] Tristate	2	14	ns

Figure 36 - Drop Side Receive Synchronous Interface Timing (TSEN = 1)

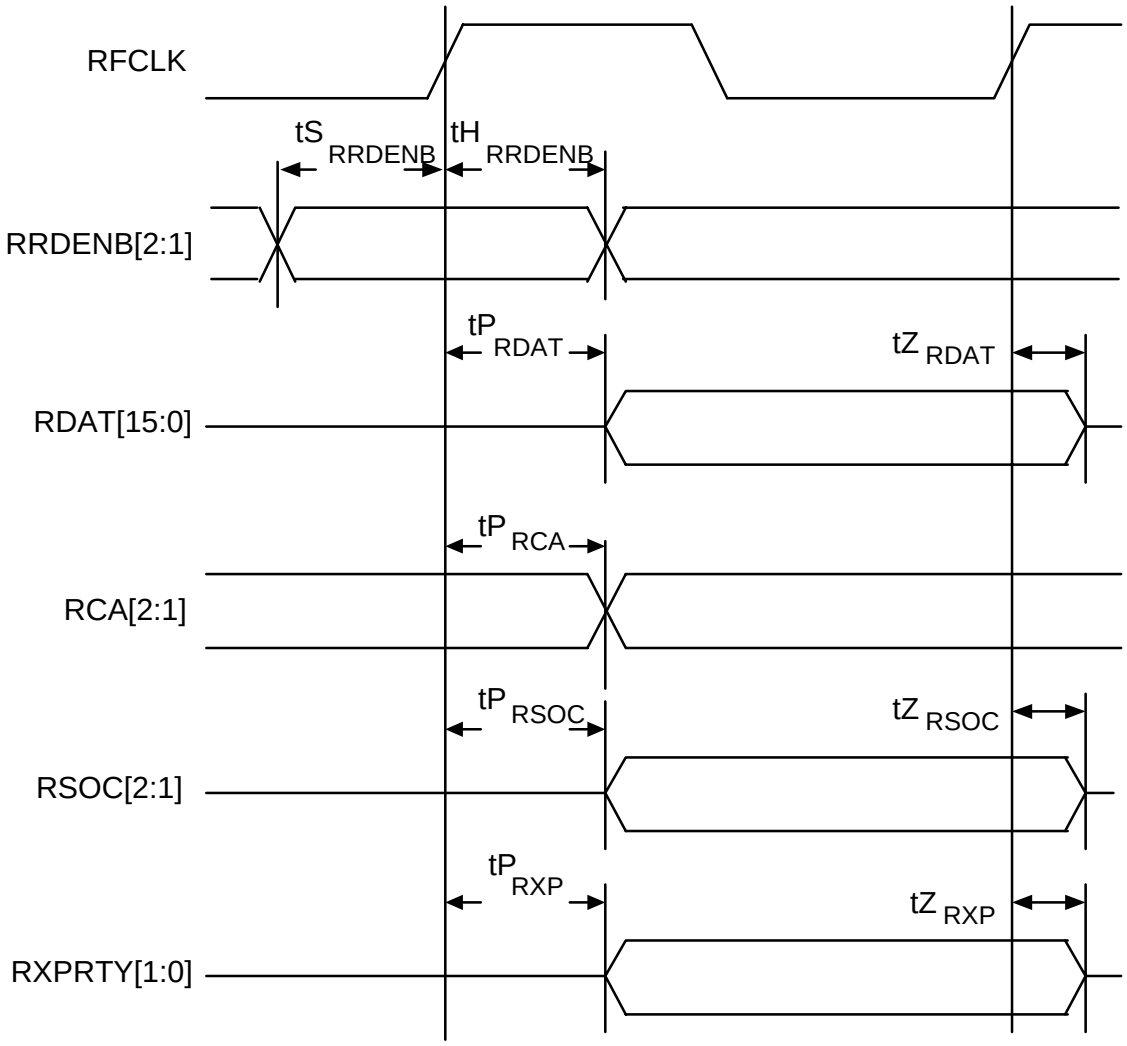
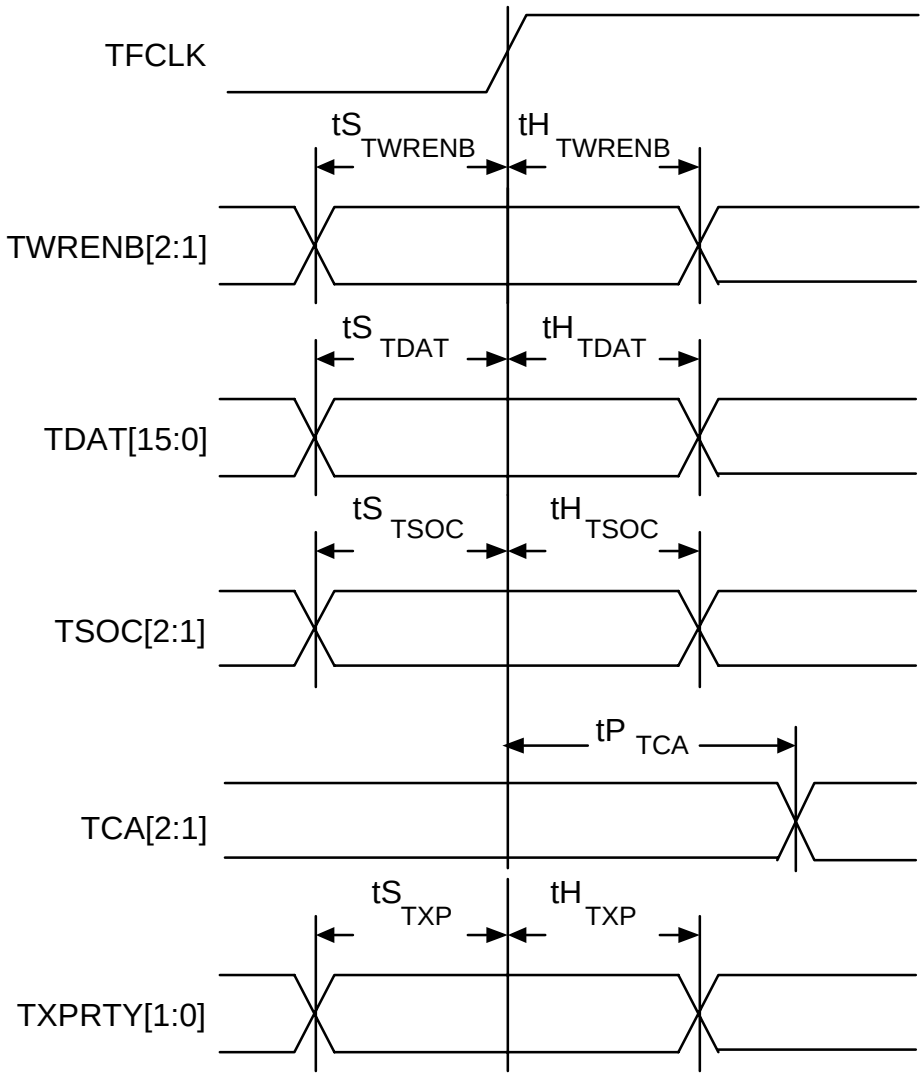


Table 19 - Drop Side Transmit Synchronous Interface (Figure 37)

Symbol	Description	Min	Max	Units
	TFCLK Frequency		52	MHz
	TFCLK Duty Cycle	40	60	%
tS_{TWRENB}	TWRENB Set-up time to TFCLK	4		ns
tH_{TWRENB}	TWRENB Hold time to TFCLK	1		ns
tS_{TDAT}	TDAT[7:0] Set-up time to TFCLK	4		ns
tH_{TDAT}	TDAT[7:0] Hold time to TFCLK	1		ns
tS_{TXP}	TXPRTY Set-up time to TFCLK	4		ns
tH_{TXP}	TXPRTY Hold time to TFCLK	1		ns
tS_{TSOC}	TSOC Set-up time to TFCLK	4		ns
tH_{TSOC}	TSOC Hold time to TFCLK	1		ns
tP_{TCA}	TFCLK to TCA Valid	2	14	ns

Figure 37 - Drop Side Transmit Synchronous Interface



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. The drop side transmit and receive synchronous FIFO interface output propagation delays are measured with a 30 pF load. All other output propagation delays are measured with a 50 pF load.

3. Output tristate delay is the time in nanoseconds from the 1.4 Volt point of the reference signal to ±300mV of the termination voltage on the output. The test load is 50Ω to 1.4V in parallel with 10 pf to GND.

19 ORDERING AND THERMAL INFORMATION

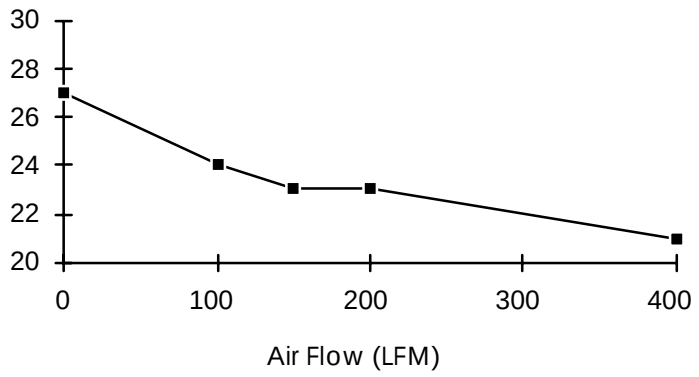
Table 20 - S/UNI-DUAL Ordering Information

PART NO	DESCRIPTION
PM5348-RI	160 Pin Metric Quad Flat Pack (MQFP)

Table 21 - S/UNI-DUAL Thermal Information

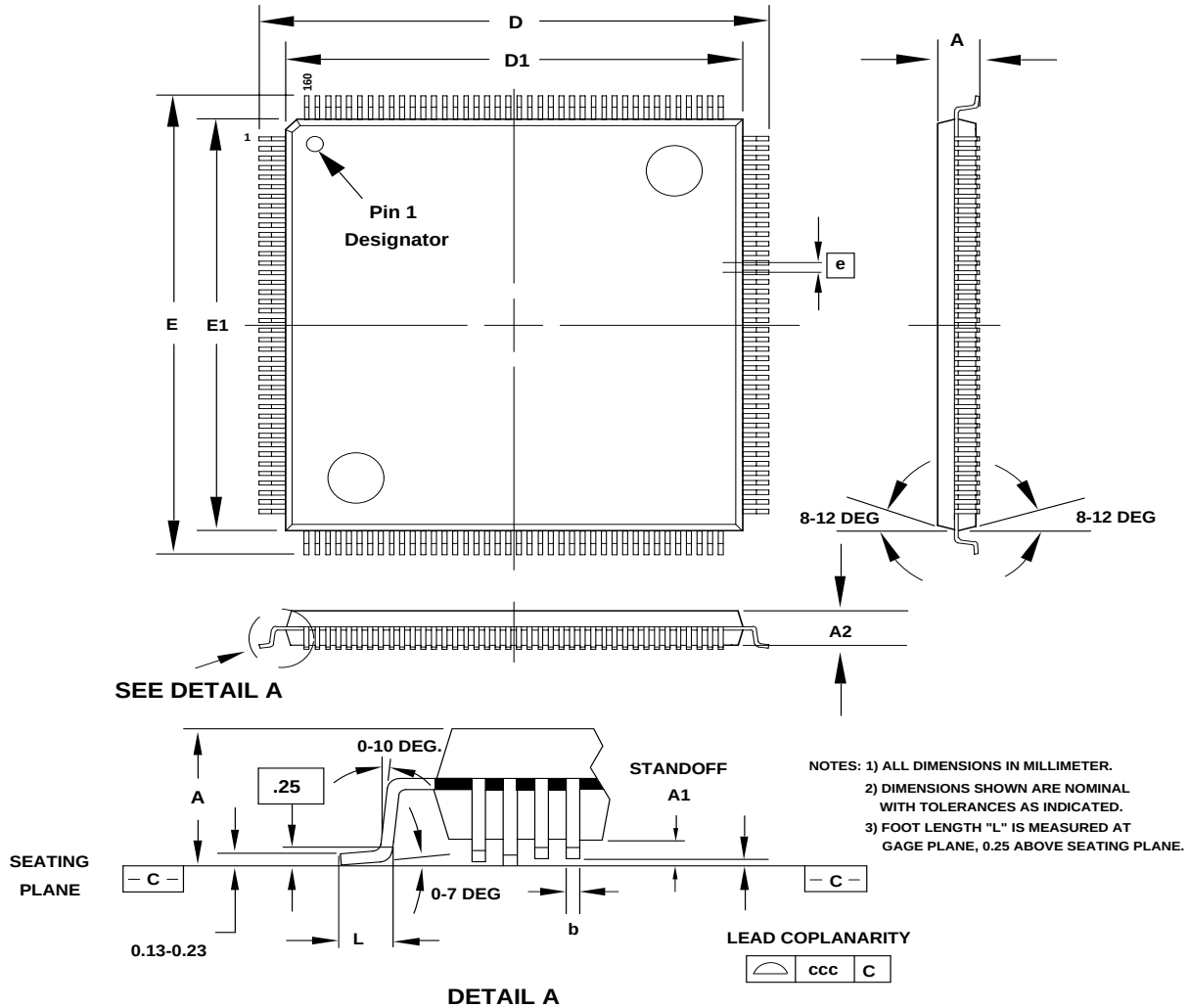
PART NO.	AMBIENT TEMPERATURE	Theta Ja	Theta Jc
PM5348-RI	0°C to 70°C	27 °C/W	11 °C/W

Figure 38 - Theta Ja vs. Air Flow



20 MECHANICAL INFORMATION

Figure 39 - 160 Pin Metric Plastic Quad Flat Pack (R Suffix):



PACKAGE TYPE: 160 PIN METRIC PLASTIC QUAD FLATPACK-MQFP											
BODY SIZE: 28 x 28 x 3.49 MM											
Dim.	A	A1	A2	D	D1	E	E1	L	e	b	ccc
Min.	3.42	0.25	3.17	30.95	27.85	30.95	27.85	0.73		0.22	
Nom.			3.42	31.20	28.00	31.20	28.00	0.88	0.65		
Max.	4.07	0.39	3.68	31.45	28.10	31.45	28.10	1.03		0.38	0.10

NOTES

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