PM5349

S/UNI-® 155-QUAD

S/UNI-QUAD

SATURN USER NETWORK INTERFACE (155-QUAD)

DATASHEET

ISSUE 6: JULY 1999

REVISION HISTORY

Issue No.	Issue Date	Details of Change
6	July, 1999	General Update: • Section 4: Augmented the DEFINITIONS table • Section 9.6: Changed TDO output drive from 2mA to 1mA, changed other DC currents from 16mA to 4mA and 4mA to 2mA • Section 11: Added RPOP PAISCONV and LOPCONV status bits in Register 0x30 • Section 11: Clarified EPRDIEN register bit description in Register 0x40 • Section 11: Added H4INSB register bit to Register 0x82 • Section 11: Fixed logic level specification in Register 0x91 • Section 11: Changed Z1/S1_CAP bit description in Register 0xE2 • Section 13.8: Enhanced Power Supply Sequencing information • Section 13.9: Analog Power Supply Filtering new recommendations • Section 16: DC Characteristics updated into include IDDOP values • Section 19: Maximum temperature changed from TC = +85°C to TA = +85°C. Added Airflow versus Theta JA chart.
5	January, 1999	General update
4	September, 1998	General Update

CONTENTS

1 FEATURES

1.1 General

- Single chip QUAD ATM User-Network Interface operating at 155.52 Mbit/s.
- Implements the ATM Forum User Network Interface Specification and the ATM physical layer for Broadband ISDN according to CCITT Recommendation I.432.
- Processes duplex 155.52 Mbit/s STS-3c (STM-1) data streams with on-chip clock and data recovery and clock synthesis.
- Exceeds Bellcore GR-253-CORE jitter tolerance and intrinsic jitter criteria.
- Fully implements the ATM Forum's Utopia Level 2 Specification with Multi-PHY addressing and parity support.
- Provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.
- Provides a generic 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power 3.3V CMOS with PECL and TTL compatible inputs and CMOS/TTL outputs, with 5V tolerance inputs (system side interface is 3.3V only).
- Industrial temperature range (-40°C to +85°C).
- 304 pin Super BGA package.

1.2 The SONET Receiver

- Provides a serial interface at 155.52 Mbit/s.
- Recovers the clock and data.
- Frames to and de-scrambles the recovered stream.
- Detects signal degrade (SD) and signal fail (SF) threshold crossing alarms based on received B2 errors.

- Captures and debounces the synchronization status (S1) byte in a readable register.
- Filters and captures the automatic protection switch channel (K1, K2) bytes in readable registers and detects APS byte failure.
- Counts received section BIP-8 (B1) errors, received line BIP-24 (B2) errors, line far end block errors (FEBE), received path BIP-8 (B3) errors and path far end block errors (FEBE).
- Detects loss of signal (LOS), out of frame (OOF), loss of frame (LOF), line alarm indication signal (LAIS), line remote defect indication (LRDI), loss of pointer (LOP), path alarm indication signal (PAIS), path remote defect indication (PRDI) and path extended remote defect indicator (PERDI).
- Interprets the received payload pointer (H1, H2) and extracts the STS-3c (STM-1) synchronous payload envelope and path overhead.
- Provides individual divide by 8 recovered clocks (19.44 MHz) for each channel.
- Provides individual 8KHz receive frame pulses for each channel.

1.3 The Receive ATM Processor

- Extracts ATM cells from the received STS-3c (STM-1) synchronous payload envelope using ATM cell delineation.
- Provides ATM cell payload de-scrambling.
- Performs header check sequence (HCS) error detection and correction, and idle/unassigned cell filtering.
- Detects Out of Cell Delineation (OCD) and Loss of Cell Delineation (LCD).
- Counts number of received cells, idle cells, errored cells and dropped cells.
- Provides a synchronous 8-bit wide, four-cell FIFO buffer.

1.4 The SONET Transmitter

- Synthesizes the 155.52 MHz transmit clock from a 19.44 MHz reference.

- Provides a differential TTL serial interface (can be adapted to PECL levels) at 155.52 Mbit/s.
- Provides a single transmit frame pulse input across the four channels to align the transport frames to a system reference.
- Provides a single transmit byte clock (divide by eight of the synthesized line rate clock) to provide a timing reference for the transmit outputs.
- Optionally inserts register programmable APS (K1, K2) and synchronization status (S1) bytes.
- Optionally inserts path alarm indication signal (PAIS), path remote defect indication (PRDI), line alarm indication signal (LAIS) and line remote defect indication (LRDI).
- Inserts path BIP-8 codes (B3), path far end block error (G1) indications, line BIP-24 codes (B2), line far end block error (M1) indications, and section BIP-8 codes (B1) to allow performance monitoring at the far end.
- Scrambles the transmitted STS-3c (STM-1) stream and inserts the framing bytes (A1, A2).
- Inserts ATM cells into the transmitted STS-3c (STM-1) synchronous payload envelope.

1.5 The Transmit ATM Processor

- Provides idle/unassigned cell insertion.
- Provides HCS generation/insertion, and ATM cell payload scrambling.
- Counts number of transmitted and idle cells.
- Provides a synchronous 8-bit wide, four cell FIFO buffer.

2 APPLICATIONS

- LAN switches and hubs.
- Layer 3 switches.
- Multiservice switches (FR, ATM, IP, etc..).
- Gibabit and terabit routers.

3 REFERENCES

- Bell Communications Research - GR-253-CORE “SONET Transport Systems: Common Generic Criteria”, Issue 2, December 1995.
- Bell Communications Research - GR-436-CORE “Digital Network Synchronization Plan”, Issue 1 Revision 1, June 1996..
- ITU-T Recommendation G.703 - "Physical/Electrical Characteristics of Hierarchical Digital Interfaces", 1991.
- ITU-T Recommendation G.704 - "General Aspects of Digital Transmission Systems; Terminal Equipment - Synchronous Frame Structures Used At 1544, 6312, 2048, 8488 and 44 736 kbit/s Hierarchical Levels", July, 1995.
- ITU, Recommendation G.707 - "Network Node Interface For The Synchronous Digital Hierarchy", 1996.
- ITU Recommendation G781, “Structure of Recommendations on Equipment for the Synchronous Design Hierarchy (SDH)”, January 1994.
- ITU, Recommendation G.783 - "Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks", 1996.
- ITU Recommendation I.432, “ISDN User Network Interfaces”, March 93.
- ATM Forum - ATM User-Network Interface Specification, V3.1, October, 1995.
- ATM Forum - “UTOPIA, An ATM PHY Interface Specification, Level 2, Version 1”, June, 1995.
- PMC-950820 “SONET/SDH Bit Error Threshold Monitoring Application Note”, Issue 2, September 1998.

4 DEFINITIONS

The following table defines the abbreviations for the S/UNI-QUAD.

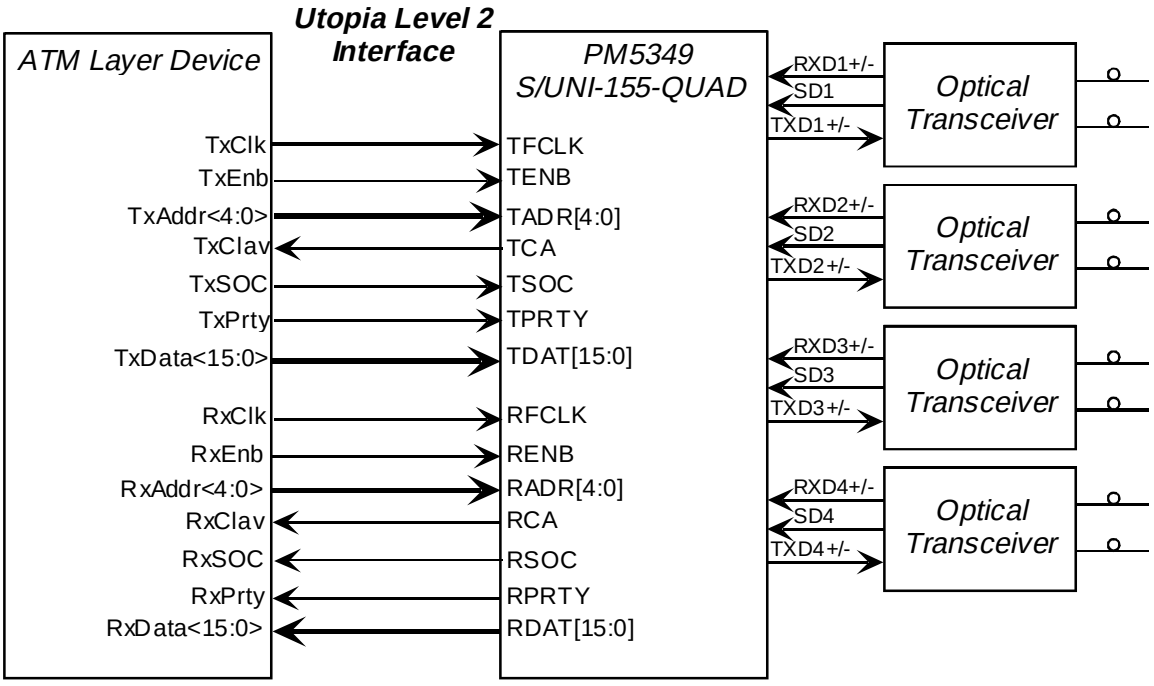
CRSI	CRU and SIPO
CRU	Clock Recovery Unit
CSPI	CSU and PISO
CSU	Clock Synthesis Unit
RASE	Receive APS, Synchronization Extractor and Bit Error Monitor
RLOP	Receive Line Overhead Processor
RPOP	Receive Path Overhead Processor
RSOP	Receive Section Overhead Processor
RXCP	Receive ATM Cell Processor
TLOP	Transmit Line Overhead Processor
TPOP	Transmit Path Overhead Processor
TSOP	Transmit Section Overhead Processor
TXCP	Transmit ATM Cell Processor

5 APPLICATION EXAMPLES

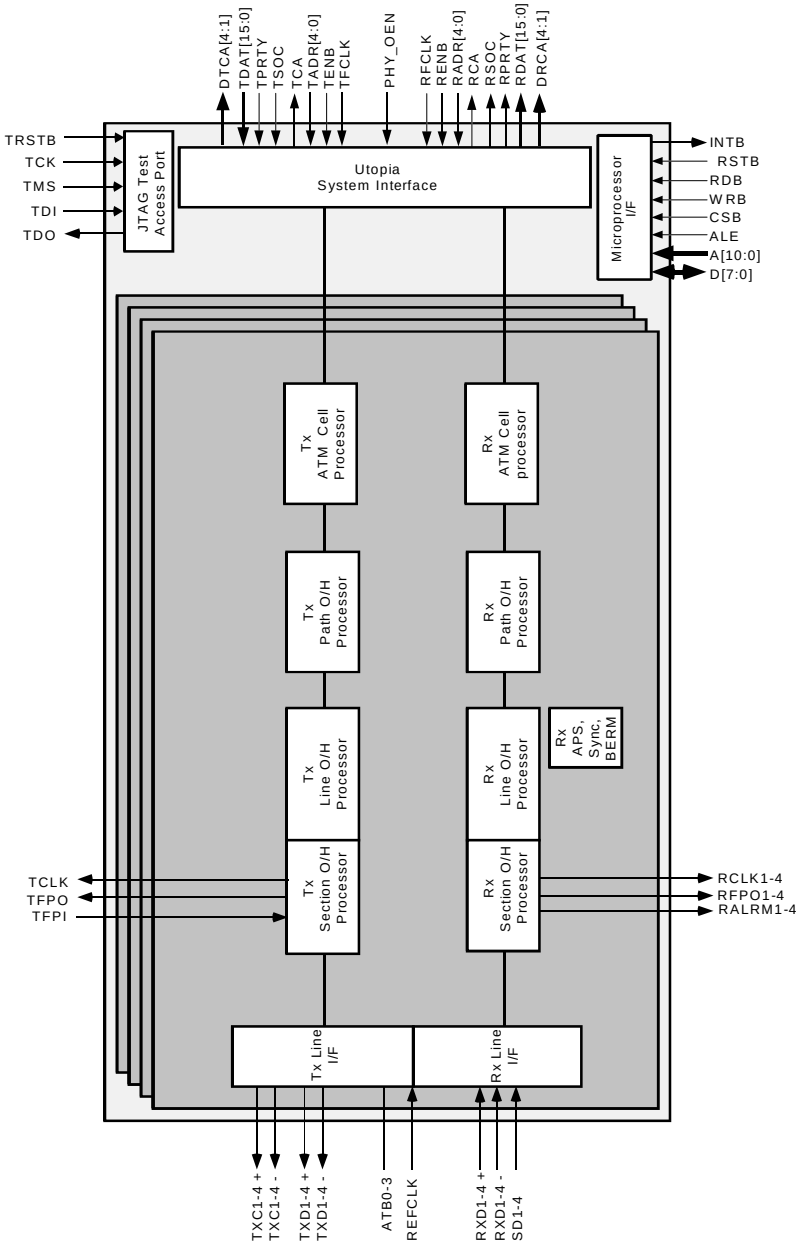
The PM5349 S/UNI-QUAD is intended for use in equipment implementing Asynchronous Transfer Mode (ATM) User-Network Interfaces (UNI). The S/UNI-QUAD may find application at either end of switch-to-switch links or switch-to-terminal links. The S/UNI-QUAD performs the mapping of ATM cells into the SONET/SDH STS-3c (STM-1) synchronous payload envelope (SPE) and processes applicable SONET/SDH section, line and path overhead.

In a typical STS-3c (STM-1) ATM application, the S/UNI-QUAD performs clock and data recovery for the receive direction and clock synthesis for the transmit direction of the line interface. On the system side, the S/UNI-QUAD interfaces directly with ATM layer processors and switching or adaptation functions using a Utopia Level 2 compliant synchronous FIFO style interface. The initial configuration and ongoing control and monitoring of the S/UNI-QUAD are normally provided via a generic microprocessor interface. This application is shown in Figure 1.

Figure 1: Typical STS-3c (STM-1) ATM Switch Port Application



6 BLOCK DIAGRAM



7 DESCRIPTION

The PM5349 S/UNI-QUAD SATURN User Network Interface is a monolithic integrated circuit that implements four channel SONET/SDH processing and ATM mapping functions at the STS-3c (STM-1) 155.52 Mbit/s rate.

The S/UNI-QUAD receives SONET/SDH streams using a bit serial interface, recovers the clock and data and processes section, line, and path overhead. It performs framing (A1, A2), de-scrambling, detects alarm conditions, and monitors section, line, and path bit interleaved parity (B1, B2, B3), accumulating error counts at each level for performance monitoring purposes. Line and path far end block error indications (M1, G1) are also accumulated. The S/UNI-QUAD interprets the received payload pointers (H1, H2) and extracts the synchronous payload envelope which carries the received ATM cell payload.

The S/UNI-QUAD frames to the ATM payload using cell delineation. HCS error correction is provided. Idle/unassigned cells may be dropped according to a programmable filter. Cells are also dropped upon detection of an uncorrectable header check sequence error. The ATM cell payloads are descrambled. The ATM cells that are passed are written to a four cell FIFO buffer. The received cells are read from the FIFO using a 16-bit wide Utopia level 2 compliant datapath interface. Counts of received ATM cell headers that are errored and uncorrectable and also those that are errored and correctable are accumulated independently for performance monitoring purposes.

The S/UNI-QUAD transmits SONET/SDH streams using a bit serial interface and formats section, line, and path overhead appropriately. It synthesizes the transmit clock from a lower frequency reference and performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and creates section, line, and path bit interleaved parity (B1, B2, B3) as required to allow performance monitoring at the far end. Line and path far end block error indications (M1, G1) are also inserted. The S/UNI-QUAD generates the payload pointer (H1, H2) and inserts the synchronous payload envelope which carries the ATM cell payload. The S/UNI-QUAD also supports the insertion of a large variety of errors into the transmit stream, such as framing pattern errors, bit interleaved parity errors, and illegal pointers, which are useful for system diagnostics and tester applications.

ATM cells are written to an internal four cell FIFO using a 16-bit wide Utopia Level 2 datapath interface. Idle/unassigned cells are automatically inserted when the internal FIFO contains less than one cell. The S/UNI-QUAD provides generation of the header check sequence and scrambles the payload of the ATM cells. Each of these transmit ATM cell processing functions can be enabled or bypassed.

No line rate clocks are required directly by the S/UNI-QUAD as it synthesizes the transmit clock and recovers the receive clock using a 19.44 MHz reference clock. The S/UNI-QUAD outputs a differential TTL (externally coverted to PECL) line data (TXD+/-).

The S/UNI-QUAD is configured, controlled and monitored via a generic 8-bit microprocessor bus interface. The S/UNI-QUAD also provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.

The S/UNI-QUAD is implemented in low power, +3.3 Volt, CMOS technology. It has TTL and pseudo-ECL (PECL) compatible inputs and TTL/CMOS compatible outputs and is packaged in a 304 pin SBGA package.

8 PIN DIAGRAM

The S/UNI-QUAD is available in a 304 pin SBGA package having a body size of 31 mm by 31 mm and a ball pitch of 1.27 mm.

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	VDD	VSS	TDAT[12]	TDAT[15]	PHY_OEN	VSS	D[2]	VSS	A[0]	A[3]	A[7]	VSS	A[10]	WRB	TDO	VSS	N/C	VSS	N/C	RAVD1_B	RAVS1_B	VSS	VDD
B	VSS	VDD	VSS	TDAT[13]	N/C	N/C	D[1]	D[4]	D[6]	A[2]	A[6]	A[9]	CSB	RSTB	TMS	TCK	N/C	N/C	QAVS_5	N/C	VSS	VDD	VSS
C	TDAT[7]	VSS	VDD	TDAT[10]	TDAT[14]	N/C	BIAS	D[3]	D[5]	A[1]	A[5]	A[8]	ALE	INTB	TRSTB	N/C	N/C	QAVD_5	N/C	RAVD1_C	VDD	VSS	TXD1P
D	TDAT[4]	TDAT[6]	TDAT[9]	VDD	TDAT[11]	VDD	N/C	D[0]	VDD	D[7]	A[4]	VDD	RDB	TDI	VDD	N/C	N/C	VDD	RAVS1_C	VDD	N/C	TXD1N	RX1-
E	TDAT[0]	TDAT[3]	TDAT[5]	TDAT[8]																N/C	SD1	RX1+	TXD2P
F	VSS	N/C	TDAT[2]	VDD																VDD	RAVS1_A	TXD2N	VSS
G	TADR[0]	TADR[2]	TADR[4]	TDAT[1]																RAVD1_A	N/C	RX2-	RX2+
H	VSS	TPRTY	TADR[1]	TADR[3]																N/C	RAVS2_A	RAVD2_A	VSS
J	TCA	TENB	TSOC	VDD																VDD	SD2	N/C	RAVD2_C
K	DTCA[3]	DTCA[4]	BIAS	TFCLK																RAVS2_C	RAVS2_B	N/C	N/C
L	N/C	N/C	DTCA[1]	DTCA[2]																RAVD2_B	TAVD1_A	TAVS1_A	TAVD1_B
M	VSS	N/C	DRCA[4]	VDD																VDD	TAVS1_B	RAVD3_B	VSS
N	DRCA[3]	DRCA[2]	DRCA[1]	RCA																RAVD3_C	RAVS3_B	N/C	N/C
P	RSOC	RENB	RFCLK	RADR[3]																ATB2	ATB1	ATB0	RAVS3_C
R	RADR[4]	RADR[2]	RADR[1]	VDD																VDD	N/C	N/C	ATB3
T	VSS	RADR[0]	RPRTY	RDAT[13]																RAVS3_A	N/C	TXD3P	VSS
U	RDAT[15]	RDAT[14]	RDAT[12]	RDAT[9]																N/C	SD3	RAVD3_A	TXD3N
V	VSS	RDAT[11]	RDAT[8]	VDD																VDD	N/C	RX3-	VSS
W	RDAT[10]	RDAT[7]	RDAT[5]	RDAT[2]																RAVS4_A	SD4	TXD4P	RX3+
Y	RDAT[6]	RDAT[4]	RDAT[1]	VDD	N/C	VDD	N/C	N/C	VDD	RALRM3	RCLK2	VDD	N/C	N/C	VDD	N/C	TFPI	VDD	RAVS4_C	VDD	RAVD4_A	RX4-	TXD4N
AA	RDAT[3]	VSS	VDD	RDAT[0]	N/C	N/C	N/C	N/C	N/C	RALRM1	RCLK1	RFPO1	N/C	N/C	N/C	N/C	N/C	QAVD_1	N/C	RAVD4_C	VDD	VSS	RX4+
AB	VSS	VDD	VSS	N/C	N/C	N/C	N/C	N/C	RALRM4	RCLK4	RFPO4	RFPO2	TFPO	N/C	N/C	N/C	N/C	N/C	QAVS_1	N/C	VSS	VDD	VSS
AC	VDD	VSS	N/C	N/C	N/C	VSS	N/C	VSS	RALRM2	RCLK3	RFPO3	VSS	TCLK	N/C	N/C	VSS	N/C	VSS	REFCLK	RAVD4_B	RAVS4_B	VSS	VDD

BOTTOM VIEW

9 PIN DESCRIPTION

9.1 Line Side Interface Signals

Pin Name	Type	Pin No.	Function
REFCLK	Input	AC5	The reference clock input (REFCLK) must provide a jitter-free 19.44 MHz reference clock. It is used as the reference clock by both clock recovery and clock synthesis circuits. This pin is shared by all channels.
RXD1+ RXD1- RXD2+ RXD2- RXD3+ RXD3- RXD4+ RXD4-	Differential PECL inputs	E2 D1 G1 G2 W1 V2 AA1 Y2	The receive differential data inputs (RXD+, RXD-) contain the NRZ bit serial receive stream. The receive clock is recovered from the RXD+/- bit stream. Please refer to the Operation section for a discussion of PECL interfacing issues. This pin is available independently for each channel.
SD1 SD2 SD3 SD4	Single-Ended PECL Input	E3 J3 U3 W3	The Signal Detect pin (SD) indicates the presence of valid receive signal power from the Optical Physical Medium Dependent Device. A PECL high indicates the presence of valid data and a PECL low indicates a loss of signal. It is mandatory that SD be terminated into the equivalent network that RXD+/- is terminated into. This pin is available independently for each channel.
RCLK1 RCLK2 RCLK3 RCLK4	Output	AA13 Y13 AC14 AB14	The receive byte clock (RCLK) provides a timing reference for the S/UNI-QUAD receive outputs. RCLK is a divide by eight of the recovered line rate clock (19.44 MHz). This pin is available independently for each channel.

Pin Name	Type	Pin No.	Function
RFPO1 RFPO2 RFPO3 RFPO4	Output	AA12 AB12 AC13 AB13	The Receive Frame Pulse Output (RFPO), when the framing alignment is found (the OOF register bit is logic zero), is an 8 kHz signal derived from the receive line clock. RFPO pulses high for one RCLK cycle every 2430 RCLK cycles (STS-3c (STM-1)). RFPO is updated on the rising edge of RCLK. This pin is available independently for each channel.
RALRM1 RALRM2 RALRM3 RALRM4	Output	AA14 AC15 Y14 AB15	The Receive Alarm (RALRM) output indicates the state of the receive framing. RALRM is low if no receive alarms are active. RALRM is high if line AIS (LAIS), path AIS (PAIS), line RDI (LRDI), path RDI (PRDI), enhanced path RDI (PERDI), loss of signal (LOS), loss of frame (LOF), out of frame (OOF), loss of pointer (LOP), loss of cell delineation (LCD), signal fail BER (SFBER), signal degrade BER (SDBER), or path signal label mismatch (PSLM) is detected in the associated channel. Each alarm can be individually enabled using bits in the S/UNI-QUAD Channel Alarm Control registers #1 and #2. RALRM is updated on the rising edge of RCLK. This pin is available independently for each channel.
TXD1+ TXD1- TXD2+ TXD2- TXD3+ TXD3- TXD4+ TXD4-	Differential TTL output (externally converted to PECL)	C1 D2 E1 F2 T2 U1 W2 Y1	The transmit differential data outputs (TXD+, TXD-) contain the 155.52 Mbit/s transmit stream. This pin is available independently for each channel.

Pin Name	Type	Pin No.	Function
TFPI	Input	Y7	The active high framing position (TFPI) signal is an 8 kHz timing marker for the transmitter. TFPI is used to align the SONET/SDH transport frame generated by the S/UNI-QUAD device to a system reference. TFPI is internally used to align a master frame pulse counter. When TFPI is not used, this counter is free-running. TFPI should be brought high for a single TCLK period every 2430 (STS-3c (STM-1)) TCLK cycles, or a multiple thereof. TFPI shall be tied low if such synchronization is not required. TFPI cannot be used as an input to a loop-timed channel. For TFPI to operate correctly it is required that the TCLK/TFPO output be configured to output the CSU byte clock. The TFPI_EN register bits allow to individually configure each channel to use the global framing pulse counter and TFPI for framing alignment. TFPI is sampled on the rising edge of TCLK, but only when the TTSEL register bit is set to logic zero. When TTSEL is set to logic one, TFPI is unused. This pin is shared by all channels.
TCLK	Output	AC11	The transmit byte clock (TCLK) output provides a timing reference for the S/UNI-QUAD self-timed channels. TCLK always provide a divide by eight of the synthesized line rate clock and thus has a nominal frequency of 19.44 MHz. TFPI is sampled on the rising edge of TCLK. TCLK does not apply to internally loop-timed channels, in which case the channel's RCLK provides transmit timing information.

Pin Name	Type	Pin No.	Function
TFPO	Output	AB11	The Transmit Frame Pulse Output (TFPO) pulses high for one TCLK cycle every 2430 TCLK cycles and provides an 8 KHz timing reference. TFPO can be assigned to any of the four channels using TFPO_CH[1:0] configuration register bits, with the restriction that the selected channel must be self-timed (not in loop-timed or line-loopback modes). TFPO is updated on the rising edge of TCLK.

9.2 UTOPIA Level 2 System Interface

Pin Name	Type	Pin No.	Function
TDAT[15] TDAT[14] TDAT[13] TDAT[12] TDAT[11] TDAT[10] TDAT[9] TDAT[8] TDAT[7] TDAT[6] TDAT[5] TDAT[4] TDAT[3] TDAT[2] TDAT[1] TDAT[0]	Input	A20 C19 B20 A21 D19 C20 D21 E20 C23 D22 E21 D23 E22 F21 G20 E23	UTOPIA Transmit Cell Data Bus (TDAT[15:0]). This data bus carries the ATM cell octets that are written to the selected transmit FIFO. TDAT[15:0] is considered valid only when TENB is simultaneously asserted and the S/UNI-QUAD is selected via TADR[4:0]. TDAT[15:0] is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TPRTY	Input	H22	UTOPIA Transmit bus parity (TPRTY) signal. The transmit parity (TPRTY) signal indicates the parity of the TDAT[15:0] bus. A parity error is indicated by a status bit and a maskable interrupt. Cells with parity errors are inserted in the transmit stream, so the TPRTY input may be unused. Odd or even parity selection is made independently for each channel using the RXPTYP register bit. TPRTY is considered valid only when TENB is simultaneously asserted and the S/UNI-QUAD is selected via TADR[4:0]. TPRTY is sampled on the rising edge of TFCLK.
TSOC	Input	J21	UTOPIA Transmit Start of Cell (TSOC) signal. The transmit start of cell (TSOC) signal marks the start of cell on the TDAT bus. When TSOC is high, the first word of the cell structure is present on the TDAT bus. It is not necessary for TSOC to be present for each cell. An interrupt may be generated if TSOC is high during any word other than the first word of the cell structure. TSOC is considered valid only when TENB is simultaneously asserted and the S/UNI-QUAD is selected via TADR[4:0]. TSOC is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TENB	Input	J22	UTOPIA Transmit Multi-PHY Write Enable (TENB) signal. The TENB signal is an active low input which is used along with the TADR[4:0] inputs to initiate writes to the transmit FIFO's. TENB works as follows. When sampled high, no write is performed, but the TADR[4:0] address is latched to identify the transmit FIFO to be accessed. When TENB is sampled low, the word on the TDAT bus is written into the transmit FIFO that is selected by the TADR[4:0] address bus. A complete 53 octet cell must be written to the transmit FIFO before it is inserted into the transmit stream. Idle cells are inserted when a complete cell is not available. While TENB is deasserted, TADR[4:0] can be used for polling TCA. TENB is sampled on the rising edge of TFCLK.
TADR[4] TADR[3] TADR[2] TADR[1] TADR[0]	Input	G21 H20 G22 H21 G23	UTOPIA Transmit Write Address (TADR[4:0]) signals. The TADR[4:0] bus is used to select the FIFO (and hence port) that is written to using the TENB signal and the FIFO's whose cell available signal is visible on the TCA polling output. Note that address 0x1F is the null-PHY address and cannot be assigned to any port on the S/UNI-QUAD. TADR[4:0] is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TCA	Output	J23	UTOPIA Transmit multi-PHY Cell Available (TCA) The TCA signal indicates when a cell is available in the transmit FIFO for the port polled by TADR[4:0] when TENB is asserted. When high, TCA indicates that the corresponding transmit FIFO is not full and a complete cell may be written. When TCA goes low, it can be configured to indicate either that the corresponding transmit FIFO is near full or that the corresponding transmit FIFO is full. TCA will transition low on the rising edge of TFCLK after the Payload word 19 (TCALEVEL0=0) or 23 (TCALEVEL0=1) is sampled if the PHY being polled is the same as the PHY in use. To reduce FIFO latency, the FIFO depth at which TCA indicates "full" can be set to one, two, three or four cells. Note that regardless of what fill level TCA is set to indicate "full" at, the transmit cell processor can store 4 complete cells. TCA is tri-stated when either the null-PHY address (0x1F) or an address not matching the address space set by PHY_ADR[2:0] is latched from the TADR[4:0] inputs when TENB is high. TCA is updated on the rising edge of TFCLK.
TFCLK	Input	K20	UTOPIA Transmit FIFO Write Clock (TFCLK). This signal is used to write ATM cells to the four cell transmit FIFOs. TFCLK cycles at a 50 MHz or lower instantaneous rate.

Pin Name	Type	Pin No.	Function
DTCA[4] DTCA[3] DTCA[2] DTCA[1]	Output	K22 K23 L20 L21	UTOPIA Direct Transmit Cell Available (DTCA[4:1]). These output signals provide direct status indication of when a cell is available in the transmit FIFO for the corresponding port. When high, DTCA indicates that the corresponding transmit FIFO is not full and a complete cell may be written. When DTCA goes low, it can be configured to indicate either that the corresponding transmit FIFO is near full or that the corresponding transmit FIFO is full. DTCA will transition low on the rising edge of TFCLK after the Payload word 19 (TCALEVEL0=0) or 23 (TCALEVEL0=1) is sampled if the PHY being polled is the same as the PHY in use. To reduce FIFO latency, the FIFO depth at which DTCA indicates "full" can be set to one, two, three or four cells. Note that regardless of what fill level DTCA is set to indicate "full" at, the transmit cell processor can store 4 complete cells DTCA[4:1] are updated on the rising edge of TFCLK.
RDAT[15] RDAT[14] RDAT[13] RDAT[12] RDAT[11] RDAT[10] RDAT[9] RDAT[8] RDAT[7] RDAT[6] RDAT[5] RDAT[4] RDAT[3] RDAT[2] RDAT[1] RDAT[0]	Output	U23 U22 T20 U21 V22 W23 U20 V21 W22 Y23 W21 Y22 AA23 W20 Y21 AA20	UTOPIA Receive Cell Data Bus (RDAT[15:0]). This data bus carries the ATM cells that are read from the receive FIFO selected by RADR[4:0]. RDAT[15:0] is tri-stated when RENB is high. RDAT[15:0] is tristated when RENB is high. RDAT[15:0] is also tristated when either the null-PHY address (0x1F) or an address not matching the address space is latched from the RADR[4:0] inputs when RENB is high. RDAT[15:0] is updated on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
RPRTY	Output	T21	UTOPIA Receive Parity (RPRTY). The receive parity (RPRTY) signal indicates the parity of the RDAT bus. RPRTY reflects the parity of RDAT[15:0]. Odd or even parity selection is made independently for every channel by using the RXPTYP register bit (in ATM cell processors, the four RXCP shall be programmed with the same parity setting).RPRTY is tristated when RENB is high. RPRTY is also tristated when either the null-PHY address (0x1F) or an address not matching the address space is latched from the RADR[4:0] inputs when RENB is high. RPRTY is updated on the rising edge of RFCLK.
RSOC	Output	P23	UTOPIA Receive Start of Cell (RSOC). RSOC marks the start of cell on the RDAT bus. RSOC is tristated when RENB is deasserted. RSOC is also tristated when either the null-PHY address (0x1F) or an address not matching the address space is latched from the RADR[4:0] inputs when RENB is high. RSOC is sampled on the rising edge of RFCLK.
RENB	Input	P22	UTOPIA Receive multi-PHY Read Enable (RENB). The RENB signal is used to initiate reads from the receive FIFO's. RENB works as follows. When RENB is sampled high, no read is performed and RDAT[15:0], RPRTY and RSOC are tristated, and the address on RADR[4:0] is latched to select the device or port for the next FIFO access. When RENB is sampled low, the word on the RDAT bus is read from the selected receive FIFO. RENB must operate in conjunction with RFCLK to access the FIFO's at a high enough rate to prevent FIFO overflows. The system may de-assert RENB at anytime it is unable to accept another byte. RENB is sampled on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
RADR[4] RADR[3] RADR[2] RADR[1] RADR[0]	Input	R23 P20 R22 R21 T22	UTOPIA Receive Read Address (RADR[4:0]). The RADR[4:] signal is used to select the FIFO (and hence port) that is read from using the RENB signal and the FIFO whose cell available signal is visible on the RCA output. Note that address 0x1F is the null-PHY address and will not be identified to any port on the S/UNI-QUAD. RADR[4:0] is sampled on the rising edge of RFCLK.
RCA	Output	N20	UTOPIA Receive multi-PHY Cell Available (RCA). RCA indicates when a cell is available in the receive FIFO for the port selected by RADR[4:0]. RCA can be configured to be de-asserted when either zero or four bytes remain in the selected/addressed FIFO. RCA will thus transition low on the rising edge of RFCLK after Payload word 24 (RCALEVEL0=1) or 19 (RCALEVEL0=0) is output if the PHY being polled is the same as the PHY in use. RCA is tristated when either the null-PHY address (0x1F) or an address not matching the address space is latched from the RADR[4:0] inputs when RENB is high. RCA is updated on the rising edge of RFCLK.
RFCLK	Input	P21	UTOPIA Receive FIFO Read Clock (RFCLK). RFCLK is used to read ATM cells from the receive FIFO's. RFCLK must cycle at a 50 MHz or lower instantaneous rate, but at a high enough rate to avoid FIFO overflows.

Pin Name	Type	Pin No.	Function
DRCA[4] DRCA[3] DRCA[2] DRCA[1]	Output	M21 N23 N22 N21	UTOPIA Direct Receive Cell Available (DRCA[4:1]). These output signals provides direct status indication of when a cell is available in the receive FIFO for the corresponding port. DRCA can be configured to be de-asserted when either zero or four bytes remain in the selected/addressed FIFO. DRCA will thus transition low on the rising edge of RFCLK after Payload word 24 (RCALEVEL0=1) or 19 (RCALEVEL0=0) is output if the PHY being polled is the same as the PHY in use. DRCA[x] is updated on the rising edge of RFCLK.
PHY_OEN	Input	A19	The PHY Output Enable (PHY_OEN) signal controls the operation of the system interface. When set to logic zero, all System Interface outputs are held tristate. When PHY_OEN is set to logic one, the interface is enabled. PHY_OEN can be overwritten by the PHY_EN Master System Interface Configuration register bit. PHY_OEN and PHY_EN are OR'ed together to enable the interface. When the S/UNI-QUAD is the only PHY layer device on the bus, PHY_OEN can safely be tied to logic one. When the S/UNI-QUAD shares the bus with other devices, then PHY_OEN must be tied to logic zero, and the PHY_EN register bit used to enable the bus once its PHY_ADR[2:0] is programmed in order to avoid conflicts.

9.3 Microprocessor Interface Signals

Pin Name	Type	Pin No.	Function
CSB	Input	B11	The active-low chip select (CSB) signal is low during S/UNI-QUAD register accesses. Note that when not being used, CSB must be tied high. If CSB is not required (i.e., registers accesses are controlled using the RDB and WRB signals only), CSB must be connected to an inverted version of the RSTB input.
RDB	Input	D11	The active-low read enable (RDB) signal is low during S/UNI-QUAD register read accesses. The S/UNI-QUAD drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are low.
WRB	Input	A10	The active-low write strobe (WRB) signal is low during a S/UNI-QUAD register write accesses. The D[7:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	I/O	D16 B17 A17 C16 B16 C15 B15 D14	The bi-directional data bus D[7:0] is used during S/UNI-QUAD register read and write accesses.
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7] A[8] A[9]	Input	A15 C14 B14 A14 D13 C13 B13 A13 C12 B12	The address bus A[9:0] selects specific registers during S/UNI-QUAD register accesses. Except for S/UNI-QUAD global registers, the A[9:8] bits allow to select which channel is being accessed. The A[7:0] bits allow to select which register is being access within a given channel address space.

Pin Name	Type	Pin No.	Function
A[10]/TRS	Input	A11	The test register select (TRS) signal selects between normal and test mode register accesses. TRS is high during test mode register accesses, and is low during normal mode register accesses.
RSTB	Input pull-up	B10	The active-low reset (RSTB) signal provides an asynchronous S/UNI-QUAD reset. RSTB is a Schmitt triggered input with an integral pull-up resistor.
ALE	Input pull-up	C11	The address latch enable (ALE) is active-high and latches the address bus A[7:0] when low. When ALE is high, the internal address latches are transparent. It allows the S/UNI-QUAD to interface to a multiplexed address/data bus. ALE has an integral pull-up resistor.
INTB	Output Open-drain	C10	The active-low interrupt (INTB) signal goes low when a S/UNI-QUAD interrupt source is active and that source is unmasked. The S/UNI-QUAD may be enabled to report many alarms or events via interrupts. Examples of interrupt sources are loss of signal (LOS), loss of frame (LOF), line AIS, line remote defect indication (LRDI) detect, loss of pointer (LOP), path AIS, path remote defect indication detect and others. INTB is tristated when the interrupt is acknowledged via an appropriate register access. INTB is an open drain output.

9.4 JTAG Test Access Port (TAP) Signals

Pin Name	Type	Pin No.	Function
TCK	Input	B8	The test clock (TCK) signal provides timing for test operations that are carried out using the IEEE P1149.1 test access port.
TMS	Input pull-up	B9	The test mode select (TMS) signal controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull-up resistor.
TDI	Input pull-up	D10	The test data input (TDI) signal carries test data into the S/UNI-QUAD via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull-up resistor.
TDO	Tristate	A9	The test data output (TDO) signal carries test data out of the S/UNI-QUAD via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tristate output which is inactive except when scanning of data is in progress.
TRSTB	Input pull-up	C9	The active-low test reset (TRSTB) signal provides an asynchronous S/UNI-QUAD test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull-up resistor. Note that when not being used, TRSTB must be connected to the RSTB input.

9.5 Analog Signals

Pin Name	Type	Pin No.	Function
ATB0 ATB1 ATB2 ATB3	Analog I/O	P2 P3 P4 R1	The Analog Test Bus (ATB). These pins are used for manufacturing testing only and should be connected ground.

9.6 Power and Ground

Pin Name	Type	Pin No.	Function
BIAS	Bias Voltage	K21 C17	I/O Bias (BIAS). When tied to +5V via a 1 KΩ resistor, the BIAS input is used to bias the wells in the input and I/O pads so that the pads can tolerate 5V on their inputs without forward biasing internal ESD protection devices. When BIAS is tied to +3.3V, the inputs and bi-directional inputs will only tolerate 3.3V level inputs.

Pin Name	Type	Pin No.	Function
VDD	Power	A1 A23 B2 B22 C3 C21 D4 D6 D9 D12 D15 D18 D20 F4 F20 J4 J20 M4 M20 R4 R20 V4 V20 Y4 Y6 Y9 Y12 Y15 Y18 Y20 AA3 AA21 AB2 AB22 AC1 AC23	The digital power (VDD) pins should be connected to a well-decoupled +3.3 V DC supply.

Pin Name	Type	Pin No.	Function
VSS	Ground	A2 A6 A8 A12 A16 A18 A22 B1 B3 B21 B23 C2 C22 F1 F23 H1 H23 M1 M23 T1 T23 V1 V23 AA2 AA22 AB1 AB3 AB21 AB23 AC2 AC6 AC8 AC12 AC16 AC18 AC22	The digital ground (VSS) pins should be connected to ground.

Pin Name	Type	Pin No.	Function
QAVD	Analog Power	AA6 C6	QAVD1 QAVD2 The quiet analog power (QAVD) pins for the analog core. QAVD should be connected to analog +3.3V.
QAVS	Analog Ground	AB5 B5	QAVS1 QAVS2 The quiet analog ground (QAVS) pins for the analog core. QAVS should be connected to analog GND.
AVD	Analog Power	G4 A4 C4 H2 L4 J1 U2 M2 N4 Y3 AC4 AA4 L3 L1	RAVD1_A - Channel #1 PECL Input Buffer RAVD1_B - Channel #1 CRU RAVD1_C - Channel #1 CRU RAVD2_A - Channel #2 PECL Input Buffer RAVD2_B - Channel #2 CRU RAVD2_C - Channel #2 CRU RAVD3_A - Channel #3 PECL Input Buffer RAVD3_B - Channel #3 CRU RAVD3_C - Channel #3 CRU RAVD4_A - Channel #4 PECL Input Buffer RAVD4_B - Channel #4 CRU RAVD4_C - Channel #4 CRU TAVD1_A - CSU TAVD1_B - CSU The analog power (AVD) pins for the analog core. AVD should be connected to analog +3.3V.

Pin Name	Type	Pin No.	Function
AVS	Analog Ground	F3 A3 D5 H3 K3 K4 T4 N3 P1 W4 AC3 Y5 L2 M3	RAVS1_A - Channel #1 PECL Input Buffer RAVS1_B - Channel #1 CRU RAVS1_C - Channel #1 CRU RAVS2_A - Channel #2 PECL Input Buffer RAVS2_B - Channel #2 CRU RAVS2_C - Channel #2 CRU RAVS3_A - Channel #3 PECL Input Buffer RAVS3_B - Channel #3 CRU RAVS3_C - Channel #3 CRU RAVS4_A - Channel #4 PECL Input Buffer RAVS4_B - Channel #4 CRU RAVS4_C - Channel #4 CRU TAVS1_A - CSU TAVS1_B - CSU The analog ground (AVS) pins for the analog core. AVS should be connected to analog GND.

Notes on Pin Description:

1. All S/UNI-QUAD inputs and bi-directionals present minimum capacitive loading and operate at TTL logic levels except: the SD, RXD+ and RXD- inputs which operate at pseudo-ECL (PECL) logic levels

2. The RDAT[7:0], RPRTY, RSOC, DRCA4-1, RCA, DTCA4-1, TCA, TCLK and RCLK1-4 outputs have a 4 mA DC drive capability. The TDO output has a 1 mA drive capability. All the other outputs have a 2 mA DC drive capability. The TXD+ and TXD- outputs are met to be terminated in a passive network and interface at PECL levels.

3. It is mandatory that every ground pin (VSS) be connected to the printed circuit board ground plane to ensure a reliable device operation.

4. It is mandatory that every power pin (VDD) be connected to the printed circuit board power plane to ensure a reliable device operation.

5. All analog power and ground can be sensitive to noise. They must be isolated from the digital power and ground. Care must be taken to decouple these pins from each other and all other analog power and ground pins.

Power supply filtering recommendations are provided in the OPERATION section of this document.

6. Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions it is possible to blow these ESD protection devices or trigger latch up. **Please adhere to the recommended power supply sequencing as described in the OPERATION section of this document**.

7. If it is intended to substitute a S/UNI-QUAD in a S/UNI-TETRA socket, special attention must be given to the NC pins. The requirement is that no S/UNI-QUAD input pin is left floating when used in a S/UNI-QUAD socket. Please refer to the relevant PMC-Sierra, Inc. application note.

8. Some device pins can be made 5V tolerant by connecting the BIAS pins to a 5V power supply, while some other pins are 3.3V only. In summary, the system interface is 3.3V only while the microprocessor interface, SONET and line interfaces can be 5V tolerant.

   3.3V only I/O's:

   RDAT[15:0], RSOC, RPRTY, RENB,
   TDAT[15:0], TSOC, TPRTY, TENB,
   RCA, DRCA4-1, TCA, DTCA4-1,
   RADR[5:0], TADR[5:0], PHY_OEN

   5V tolerant I/O's:

   REFCLK, RXD
   RCLK4-1, RFPO4-1, RALRM4-1,
   TCLK, TFPO, TFPI,
   D[7:0], A[10:0], WRB, RDB, CSB, RSTB, INTB, ALE,
   TRSTB, TCK, TMS, TDI, TDO,

10 FUNCTIONAL DESCRIPTION

10.1 Receive Line Interface (CRSI)

The Receive Line Interface allows to directly interface the S/UNI-QUAD with optical modules (ODLs) or other medium interfaces. This block performs clock and data recovery and performs serial to parallel conversion on the incoming 155.52 Mbit/s data stream.

10.1.1 Clock Recovery

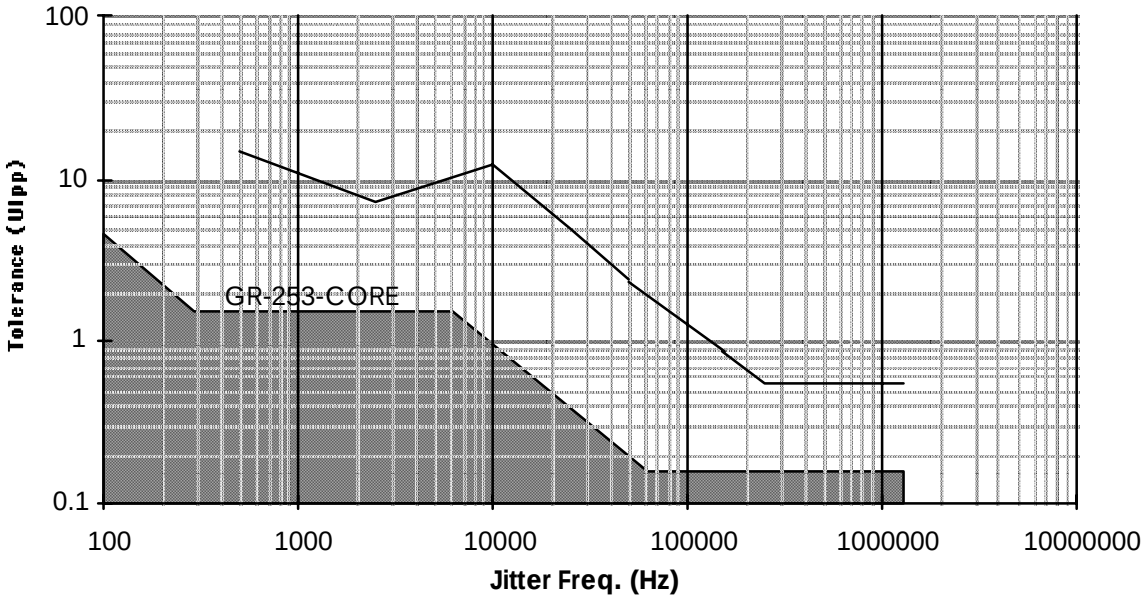
The clock recovery unit recovers the clock from the incoming bit serial data stream. The clock recovery unit is fully compliant with SONET and SDH jitter tolerance requirements. The clock recovery unit utilizes a low frequency reference clock to train and monitor its clock recovery PLL. Under loss of signal conditions, the clock recovery unit continues to output a line rate clock that is locked to this reference for keep alive purposes. The clock recovery unit utilizes a reference clocks at 19.44 MHz. The clock recovery unit provides status bits that indicate whether it is locked to data or the reference. The clock recovery unit also supports diagnostic loopback and a loss of signal input that squelches normal input data.

Initially, the PLL locks to the reference clock, REFCLK. When the frequency of the recovered clock is within 488 ppm of the reference clock, the PLL attempts to lock to the data. Once in data lock, the PLL reverts to the reference clock if no data transitions occur in 80 bit periods or if the recovered clock drifts beyond 488 ppm of the reference clock.

When the transmit clock is derived from the recovered clock (loop timing), the accuracy of the transmit clock is directly related to the REFCLK reference accuracy in the case of a loss of signal condition. To meet the Bellcore GR-253-CORE SONET Network Element free-run accuracy specification, the reference must be within +/-20ppm. When not loop timed, the REFCLK accuracy may be relaxed to +/-50ppm.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET/SDH data signal. The total loop dynamics of the clock recovery PLL yield a jitter tolerance that exceeds the minimum tolerance proposed for SONET equipment by GR-253-CORE (Figure 3).

Figure 2: Typical STS-3c (STM-1) Jitter Tolerance



Note that for frequencies below 300 Hz, the jitter tolerance is greater than 15 UIpp; 15 UIpp is the maximum jitter tolerance of the test equipment. Also note that the dip in the tolerance curve between 300 Hz and 10 kHz is due to the S/UNI-QUAD's internal clock difference detector: if the recovered clock drifts beyond 488 ppm of the reference, the PLL locks to the reference clock.

10.1.2 Serial to Parallel Converter

The Serial to Parallel Converter (SIPO) converts the received bit serial stream to a byte serial stream. The SIPO searches for the SONET/SDH framing pattern (A1, A2) in the receive stream, and performs serial to parallel conversion on octet boundaries.

10.2 Receive Section Overhead Processor (RSOP)

The Receive Section Overhead Processor (RSOP) provides frame synchronization, de-scrambling, section level alarm and performance monitoring.

10.2.1 Framer

The Framer Block determines the in-frame/out-of-frame status of the receive stream.

While in-frame, the framing bytes (A1, A2) in each frame are compared against the expected pattern. Out-of-frame is declared when four consecutive frames containing one or more framing pattern errors have been received.

While out-of-frame, the SIPO block monitors the receive stream for an occurrence of the framing pattern. When a framing pattern is recognized, the Framer block verifies that an error free framing pattern is present in the next frame before declaring in-frame.

10.2.2 Descramble

The Descramble Block utilizes a frame synchronous descrambler to process the receive stream. The generating polynomial is $x^7 + x^6 + 1$ and the sequence length is 127. Details of the de-scrambling operation are provided in the references. Note that the framing bytes (A1 and A2) and the trace/growth bytes (J0/Z0) are not descrambled. A register bit is provided to disable the de-scrambling operation.

10.2.3 Error Monitor

The Error Monitor Block calculates the received section BIP-8 error detection code (B1) based on the scrambled data of the complete STS-3c (STM-1) frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-8 code is compared with the BIP-8 code extracted from the B1 byte of the following frame. Differences indicate that a section level bit error has occurred. Up to 64000 (8 x 8000) bit errors can be detected per second. The Error Monitor Block accumulates these section level bit errors in a 16-bit saturating counter that can be read via the microprocessor interface. Circuitry is provided to latch this counter so that its value can be read while simultaneously resetting the internal counter to 0 or 1, if appropriate, so that a new period of accumulation can begin without loss of any events. It is intended that this counter be polled at least once per second so as not to miss bit error events.

10.2.4 Loss of Signal

The Loss of Signal Block monitors the scrambled data of the receive stream for the absence of 1's. When 20 ± 3 µs of all zeros patterns is detected, a loss of signal (LOS) is declared. Loss of signal is cleared when two valid framing words are detected and during the intervening time, no loss of signal condition is detected. The LOS signal is optionally reported on the RALRM output pin when enabled by the LOSEN Receive Alarm Control Register bit.

10.2.5 Loss of Frame

The Loss of Frame Block monitors the in-frame / out-of-frame status of the Framer Block. A loss of frame (LOF) is declared when an out-of-frame (OOF) condition persists for 3 ms. The LOF is cleared when an in-frame condition persists for a period of 3 ms. To provide for intermittent out-of-frame (or in-frame) conditions, the 3 ms timer is not reset to zero until an in-frame (or out-of-frame) condition persists for 3 ms. The LOF and OOF signals are optionally reported on the RALRM output pin when enabled by the LOFEB and OOFEN Receive Alarm Control Register bits.

10.3 Receive Line Overhead Processor (RLOP)

The Receive Line Overhead Processor (RLOP) provides line level alarm and performance monitoring.

10.3.1 Line RDI Detect

The Line RDI Detect Block detects the presence of Line Remote Defect Indication (LRDI) in the receive stream. Line RDI is declared when a 110 binary pattern is detected in bits 6, 7, and 8 of the K2 byte, for three or five consecutive frames. Line RDI is removed when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. The LRDI signal is optionally reported on the RALRM output pin when enabled by the LRDIEN Receive Alarm Control Register bit.

10.3.2 Line AIS Detect

The Line AIS Block detects the presence of a Line Alarm Indication Signal (LAIS) in the receive stream. Line AIS is declared when a 111 binary pattern is detected in bits 6, 7, and 8 of the K2 byte, for three or five consecutive frames. Line AIS is removed when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. The LAIS signal is optionally reported on the RALRM output pin when enabled by the LAISEN Receive Alarm Control Register bit.

10.3.3 Error Monitor Block

The Error Monitor Block calculates the received line BIP-8 error detection codes based on the Line Overhead bytes and synchronous payload envelopes of the STS-3c (STM-1) stream. The line BIP-8 code is a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-8

codes are compared with the BIP-8 codes extracted from the following frame. Any differences indicate that a line layer bit error has occurred. Optionally the RLOP can be configured to count a maximum of only one BIP error per frame.

This block also extracts the line FEBE code from the third Z2 byte. The FEBE code is contained in bits 2 to 8 of the Z2 byte, and represents the number of line BIP-8 errors that were detected in the last frame by the far end. The FEBE code value has 25 legal values (0 to 24) for an STS-3c (STM-1) stream. Illegal values are interpreted as zero errors.

The Error Monitor Block accumulates B2 error events and FEBE events in two 20 bit saturating counter that can be read via the microprocessor interface. The contents of these counters may be transferred to internal holding registers by writing to any one of the counter addresses, or by using the TIP register bit feature. During a transfer, the counter value is latched and the counter is reset to 0 (or 1, if there is an outstanding event). Note, these counters should be polled at least once per second to avoid saturation.

The B2 error events counters optionally can be configured to accumulate only "word" errors. A B2 word error is defined as the occurrence of one or more B2 bit error events during a frame. The B2 error counter is incremented by one for each frame in which a B2 word error occurs.

In addition the FEBE events counters optionally can be configured to accumulate only "word" events. In STS-3c (STM-1) framing a FEBE word event is defined as the occurrence of one or more FEBE bit events during a frame. The FEBE event counter is incremented by one for each frame in which a FEBE event occurs.

10.4 The Receive APS, Synchronization Extractor and Bit Error Monitor (RASE)

10.4.1 Automatic Protection Switch Control

The Automatic Protection Switch (APS) control block filters and captures the receive automatic protection switch channel bytes (K1 and K2) allowing them to be read via the RASE APS K1 Register and the RASE APS K2 Register. The bytes are filtered for three frames before being written to these registers. A protection switching byte failure alarm is declared when twelve successive frames have been received, where no three consecutive frames contain identical K1 bytes. The protection switching byte failure alarm is removed upon detection of three consecutive frames containing identical K1 bytes. The detection of invalid APS codes is done in software by polling the RASE APS K1 Register and the RASE APS K2 Register.

10.4.2 Bit Error Rate Monitor

The Bit Error Monitor Block (BERM) calculates the received line BIP-24 error detection code (B2) based on the line overhead and synchronous payload envelope of the receive data stream. The line BIP-24 code is a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP code is compared with the BIP-24 code extracted from the B2 byte(s) of the following frame. Any differences indicate that a line layer bit error has occurred. Up to 192000 (24 BIP/frame x 8000 frames/second) bit errors can be detected per second for STS-3c (STM-1) rate.

The BERM accumulates these line layer bit errors in a 20 bit saturating counter that can be read via the microprocessor interface. During a read, the counter value is latched and the counter is reset to 0 (or 1, if there is an outstanding event). Note, this counter should be polled at least once per second to avoid saturation which in turn may result in missed bit error events.

The BERM block is able to simultaneously monitor for signal fail (SF) or signal degrade (SD) threshold crossing and provide alarms through software interrupts. The bit error rates associated with the SF or SD alarms are programmable over a range of 10^{-3} to 10^{-9}. Details are provided in the Operations section.

In both declaring and clearing detection states, the accumulated BIP count is continuously compared against the threshold. This allows to rapidly declare in the presence of error bursts or error rates that significantly exceed the monitored BER. This behavior allows meeting the ITU-T G.783 detection requirements at various error rates (where the detection time is a function of the actual BER, for a given monitored BER.

10.4.3 Synchronization Status Extraction

The Synchronization Status Extraction (SSE) Block extracts the synchronization status (S1) byte from the line overhead. The SSE block can be configured to capture the S1 nibble after three or after eight frames with the same value (filtering turned on) or after any change in the value (filtering turned off). The S1 nibble can be read via the microprocessor interface.

Optionally, the SSE can be configured to perform filtering based on the whole S1 byte. Although this mode of operation is not standard, it might become useful in the future.

10.5 Receive Path Overhead Processor (RPOP)

The Receive Path Overhead Processor (RPOP) provides pointer interpretation, extraction of path overhead, extraction of the synchronous payload envelope, and path level alarm indication and performance monitoring.

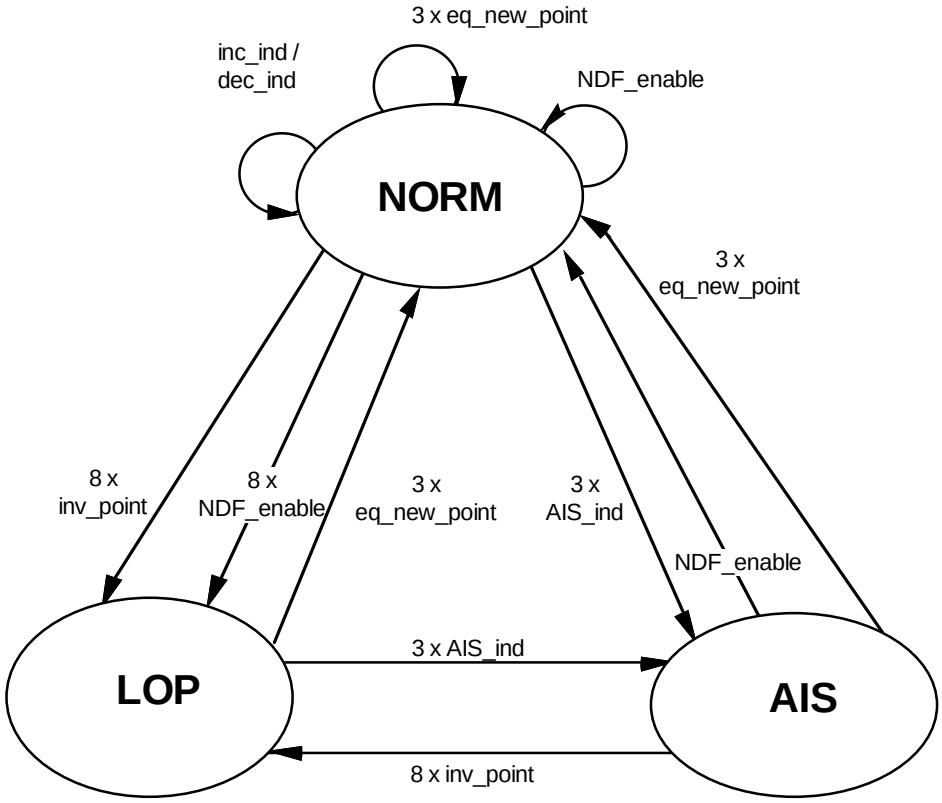
10.5.1 Pointer Interpreter

The Pointer Interpreter interprets the incoming pointer (H1, H2) as specified in the references. The pointer value is used to determine the location of the path overhead (the J1 byte) in the incoming STS-3c (STM-1) stream. The algorithm can be modeled by a finite state machine. Within the pointer interpretation algorithm three states are defined as shown below:

NORM_state (NORM)
AIS_state (AIS)
LOP_state (LOP)

The transition between states will be consecutive events (indications), e.g., three consecutive AIS indications to go from the NORM_state to the AIS_state. The kind and number of consecutive indications activating a transition is chosen such that the behavior is stable and insensitive to low BER. The only transition on a single event is the one from the AIS_state to the NORM_state after receiving a NDF enabled with a valid pointer value. It should be noted that, since the algorithm only contains transitions based on consecutive indications, this implies that, for example, non-consecutively received invalid indications do not activate the transitions to the LOP_state.

Figure 3: Pointer Interpretation State Diagram



The following table defines the events (indications) shown in the state diagram.

Table 1: Pointer Interpreter Event (Indications) Description

Event (Indication)	Description
norm_point	disabled NDF + ss + offset value equal to active offset
NDF_enable	enabled NDF + ss + offset value in range of 0 to 782 or enabled NDF + ss, if NDFPOR bit is set (Note that the current pointer is not updated by an enabled NDF if the pointer is out of range).
AIS_ind	H1 = 'hFF, H2 = 'hFF
inc_ind	disabled NDF + ss + majority of I bits inverted + no majority of D bits inverted + previous NDF_enable, inc_ind or dec_ind more than 3 frames ago
dec_ind	disabled NDF + ss + majority of D bits inverted + no

	majority of I bits inverted + previous NDF_enable, inc_ind or dec_ind more than 3 frames ago
inv_point	not any of above (i.e., not norm_point, and not NDF_enable, and not AIS_ind, and not inc_ind and not dec_ind)
new_point	disabled_NDF + ss + offset value in range of 0 to 782 but not equal to active offset
inc_req	majority of I bits inverted + no majority of D bits inverted
dec_req	majority of D bits inverted + no majority of I bits inverted

Note 1.- active offset is defined as the accepted current phase of the SPE (VC) in the NORM_state and is undefined in the other states.

Note 2 - enabled NDF is defined as the following bit patterns: 1001, 0001, 1101, 1011, 1000.

Note 3 - disabled NDF is defined as the following bit patterns: 0110, 1110, 0010, 0100, 0111.

Note 4 - the remaining six NDF codes (0000, 0011, 0101, 1010, 1100, 1111) result in an inv_point indication.

Note 5 - ss bits are unspecified in SONET and has bit pattern 10 in SDH

Note 6 - the use of ss bits in definition of indications may be optionally disabled.

Note 7 - the requirement for previous NDF_enable, inc_ind or dec_ind be more than 3 frames ago may be optionally disabled.

Note 8 - new_point is also an inv_point.

Note 9 - LOP is not declared if all the following conditions exist:
- the received pointer is out of range (>782),
- the received pointer is static,
- the received pointer can be interpreted, according to majority voting on the I and D bits, as a positive or negative justification indication,
- after making the requested justification, the received pointer continues to be interpretable as a pointer justification.

When the received pointer returns to an in-range value, the S/UNI/QUAD will interpret it correctly.

Note 10 - LOP will exit at the third frame of a three frame sequence consisting of one frame with NDF enabled followed by two frames with NDF disabled, if all three pointers have the same legal value.

The transitions indicated in the state diagram are defined in the following table.

Table 2: Pointer Interpreter Transition Description

Transition	Description
inc_ind/dec_ind	offset adjustment (increment or decrement indication)
3 x eq_new_point	three consecutive equal new_point indications
NDF_enable	single NDF_enable indication
3 x AIS_ind	three consecutive AIS indications
8 x inv_point	eight consecutive inv_point indications
8 x NDF_enable	eight consecutive NDF_enable indications

Note 1 - the transitions from NORM_state to NORM_state do not represent state changes but imply offset changes.

Note 2 - 3 x new_point takes precedence over other events and if the IINVCNT bit is set resets the inv_point count.

Note 3 - all three offset values received in 3 x eq_new_point must be identical.

Note 4 - "consecutive event counters" are reset to zero on a change of state except for consecutive NDF count.

The Pointer Interpreter detects loss of pointer (LOP) in the incoming STS-3c (STM-1) stream. LOP is declared on entry to the LOP_state as a result of eight consecutive invalid pointers or eight consecutive NDF enabled indications. The alarm condition is reported in the receive alarm port and is optionally returned to the source node by signaling the corresponding Transmit Path Overhead Processor in the local S/UNI-QUAD to insert a path RDI indication.

The Pointer Interpreter detects path AIS in the incoming STS-3c (STM-1) stream. PAIS is declared on entry to the AIS_state after three consecutive AIS indications. The alarm condition reported in the receive alarm port and is

optionally returned to the source node by signaling the corresponding Transmit Path Overhead Processor in the local SONET/SDH equipment to insert a path RDI indication.

Invalid pointer indications (inv_point), invalid NDF codes, new pointer indications (new_point), discontinuous change of pointer alignment, and illegal pointer changes are also detected and reported by the Pointer Interpreter block via register bits. An invalid NDF code is any NDF code that does not match the NDF enabled or NDF disabled definitions. The third occurrence of equal new_point indications (3 x eq_new_point) is reported as a discontinuous change of pointer alignment event (DISCOPA) instead of a new pointer event and the active offset is updated with the receive pointer value. An illegal pointer change is defined as a inc_ind or dec_ind indication that occurs within three frames of the previous inc_ind, dec_ind or NDF_enable indications. Illegal pointer changes may be optionally disabled via register bits.

The active offset value is used to extract the path overhead from the incoming stream and can be read from an internal register.

10.5.2 SPE Timing

The SPE Timing Block provides SPE timing information to the Error Monitor and the Extract blocks. The block contains a free running timeslot counter that is initialized by a J1 byte identifier (which identifies the first byte of the SPE). Control signals are provided to the Error Monitor and the Extract blocks to identify the Path Overhead bytes and to downstream circuitry to extract the ATM cell payload.

10.5.3 Error Monitor

The Error Monitor Block contains two 16-bit counters that are used to accumulate path BIP-8 errors (B3), and far end block errors (FEBEs). The contents of the two counters may be transferred to holding registers, and the counters reset under microprocessor control.

Path BIP-8 errors are detected by comparing the path BIP-8 byte (B3) extracted from the current frame, to the path BIP-8 computed for the previous frame.

FEBEs are detected by extracting the 4-bit FEBE field from the path status byte (G1). The legal range for the 4-bit field is between 0000 and 1000, representing zero to eight errors. Any other value is interpreted as zero errors.

Path RDI alarm is detected by extracting bit 5 of the path status byte. The PRDI signal is set high when bit 5 is set high for five/ten consecutive frames. PRDI is set low when bit 5 is low for five/ten consecutive frames. Auxiliary RDI alarm is detected by extracting bit 6 of the path status byte. The Auxiliary RDI alarm is indicated when bit 6 is set high for five/ten consecutive frames. The Auxiliary RDI alarm is removed when bit 6 is low for five/ten consecutive frames. The Enhanced RDI alarm is detected when the enhanced RDI code in bits 5,6,7 of the path status byte indicates the same error codepoint for five/ten consecutive frames. The Enhanced RDI alarm is removed when the enhanced RDI code in bits 5,6,7 of the path status byte indicates the same non error codepoint for five/ten consecutive frames. The ERDII maskable interrupt is set high when bits 5, 6 & 7 of the path status byte (G1) byte are set to a new codepoint for five or ten consecutive frames. The ERDIV[2:0] signal reflects the state of the filtered ERDI value (G1 byte bits 5, 6, & 7).

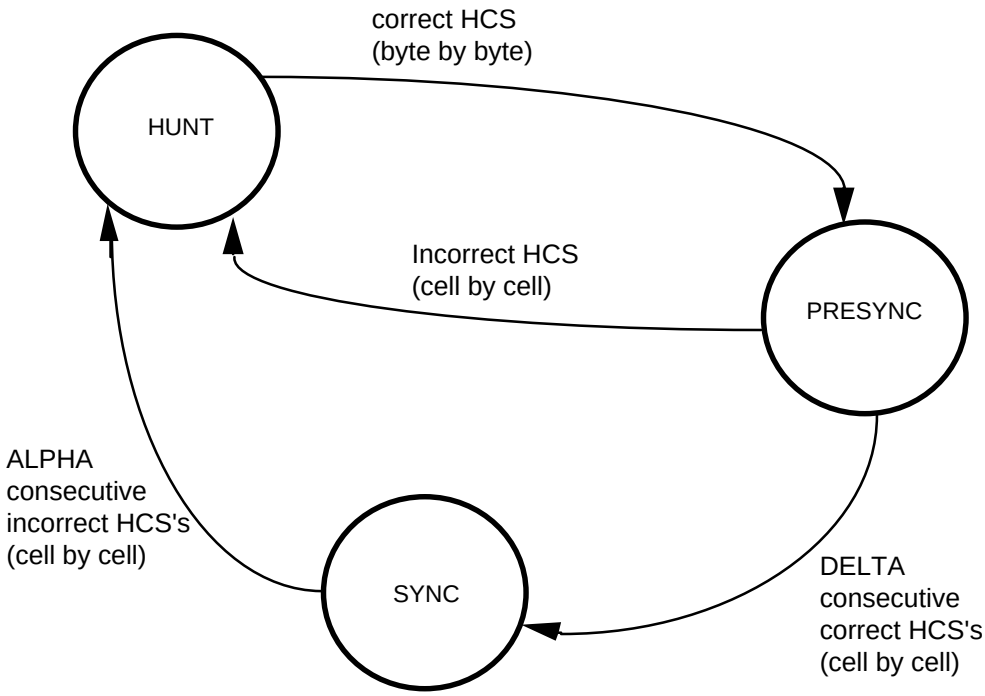
10.6 Receive ATM Cell Processor (RXCP)

The Receive ATM Cell Processor (RXCP) performs ATM cell delineation, provides cell filtering based on idle/unassigned cell detection and HCS error detection, and performs ATM cell payload de-scrambling. The RXCP also provides a four cell deep receive FIFO. This FIFO is used to separate the STS-3c (STM-1) line timing from the higher layer ATM system timing.

10.6.1 Cell Delineation

Cell Delineation is the process of framing to ATM cell boundaries using the header check sequence (HCS) field found in the cell header. The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. When performing delineation, correct HCS calculations are assumed to indicate cell boundaries. Cells are assumed to be byte-aligned to the synchronous payload envelope. The cell delineation algorithm searches the 53 possible cell boundary candidates individually to determine the valid cell boundary location. While searching for the cell boundary location, the cell delineation circuit is in the HUNT state. When a correct HCS is found, the cell delineation state machine locks on the particular cell boundary, corresponding to the correct HCS, and enters the PRESYNC state. The PRESYNC state validates the cell boundary location. If the cell boundary is invalid, an incorrect HCS will be received within the next DELTA cells, at which time a transition back to the HUNT state is executed. If no HCS errors are detected in this PRESYNC period, the SYNC state is entered. While in the SYNC state, synchronization is maintained until ALPHA consecutive incorrect HCS patterns are detected. In such an event a transition is made back to the HUNT state. The state diagram of the delineation process is shown in Figure 4.

Figure 4: Cell Delineation State Diagram



The values of ALPHA and DELTA determine the robustness of the delineation process. ALPHA determines the robustness against false misalignments due to bit errors. DELTA determines the robustness against false delineation in the synchronization process. ALPHA is chosen to be 7 and DELTA is chosen to be 6. These values result in an average time to delineation of 33.66 µs for the STS-3c (STM-1) rate.

10.6.2 Descrambler

The self synchronous descrambler operates on the 48 byte cell payload only. The circuitry descrambles the information field using the $x^{43} + 1$ polynomial. The descrambler is disabled for the duration of the header and HCS fields and may optionally be disabled for the payload.

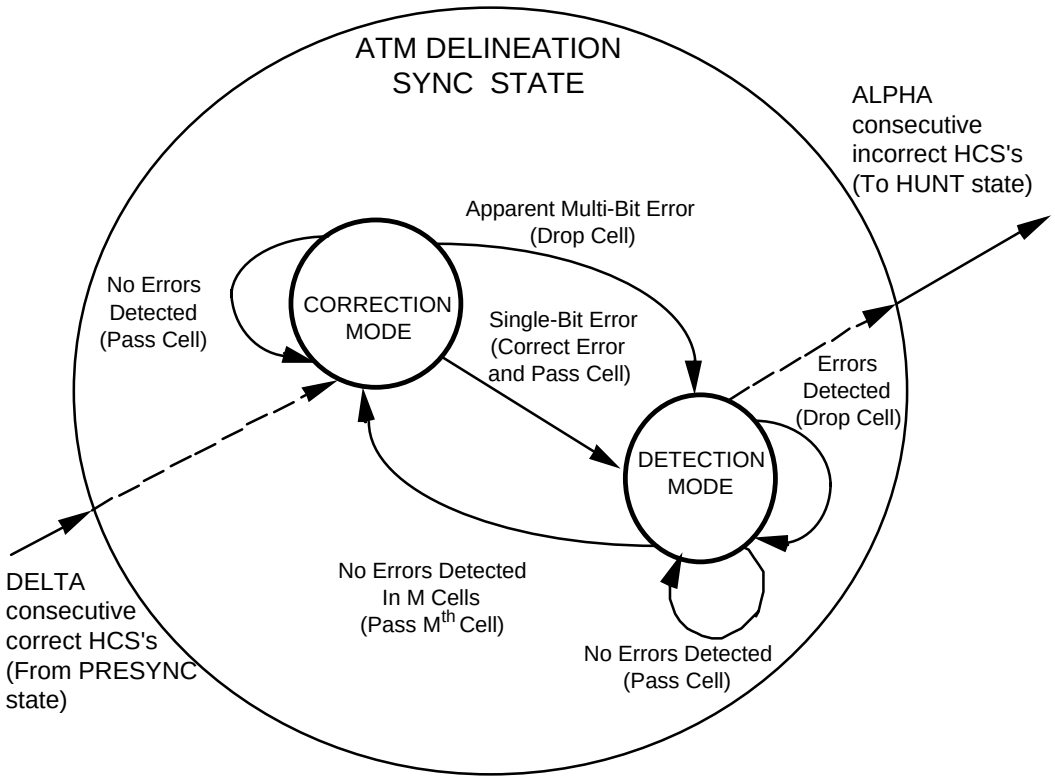
10.6.3 Cell Filter and HCS Verification

Cells are filtered (or dropped) based on HCS errors and/or a cell header pattern. Cell filtering is optional and is enabled through the RXCP registers. Cells are passed to the receive FIFO while the cell delineation state machine is in the SYNC state as described above. When both filtering and HCS checking are

enabled, cells are dropped if uncorrectable HCS errors are detected, or if the corrected header contents match the pattern contained in the RXCP Match Header Pattern and RXCP Match Header Mask registers. Idle or unassigned cell filtering is accomplished by writing the appropriate cell header pattern into the RXCP Match Header Pattern and RXCP Match Header Mask registers. Idle/Unassigned cells are assumed to contain the all zeros pattern in the VCI and VPI fields. The RXCP Match Header Pattern and RXCP Match Header Mask registers allow filtering control over the contents of the GFC, PTI, and CLP fields of the header.

The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. The RXCP block verifies the received HCS using the polynomial, $x^8 + x^2 + x + 1$. The coset polynomial, $x^6 + x^4 + x^2 + 1$, is added (modulo 2) to the received HCS octet before comparison with the calculated result. While the cell delineation state machine (described above) is in the SYNC state, the HCS verification circuit implements the state machine shown in Figure 5.

Figure 5: HCS Verification State Diagram



In normal operation, the HCS verification state machine remains in the 'Correction Mode' state. Incoming cells containing no HCS errors are passed to the receive FIFO. Incoming single-bit errors are corrected, and the resulting cell is passed to the FIFO. Upon detection of a single-bit error or a multi-bit error, the state machine transitions to the 'Detection Mode' state. In this state, programmable HCS error filtering is provided. The detection of any HCS error causes the corresponding cell to be dropped. The state machine transitions back to the 'Correction Mode' state when M (where M = 1, 2, 4, 8) cells are received with correct HCSs. The Mth cell is not discarded.

10.6.4 Performance Monitor

The Performance Monitor consists of two 12-bit saturating HCS error event counters and a 21-bit saturating receive cell counter. One of the counters accumulates correctable HCS errors which are HCS single-bit errors detected and corrected while the HCS Verification state machine is in the 'Correction Mode' state. The second counter accumulates uncorrectable HCS errors which are HCS bit errors detected while the HCS Verification state machine is in the 'Detection Mode' state or HCS bit errors detected but not corrected while the state machine is in the 'Correction Mode' state. The 21-bit receive cell counter counts all cells written into the receive FIFO. Filtered cells are not counted.

Each counter may be read through the microprocessor interface. Circuitry is provided to latch these counters so that their values can be read while simultaneously resetting the internal counters to 0 or 1, if appropriate, so that a new period of accumulation can begin without loss of any events. It is intended that the counter be polled at least once per second so as not to miss HCS error events.

10.7 Transmit Line Interface (CSPI)

The Transmit Line Interface allows to directly interface the S/UNI-QUAD with optical modules (ODLs) or other medium interfaces. This block performs clock synthesis and performs parallel to serial conversion of the incoming outgoing 155.52 Mbit/s data stream.

10.7.1 Clock Synthesis

The transmit clock is synthesized from a 19.44 MHz reference. The transfer function yields a typical low pass corner of 2.0 MHz above which reference jitter is attenuated at 12 dB per octave. The design of the loop filter and PLL is optimized for minimum intrinsic jitter. With a jitter free 19.44 MHz reference, the

intrinsic jitter is typically less than 0.01 UI RMS when measured using a high pass filter with a 12 kHz cutoff frequency.

The REFCLK reference should be within ±20 ppm to meet the SONET free-run accuracy requirements specified in GR-253-CORE.

10.7.2 Parallel to Serial Converter

The Parallel to Serial Converter (PISO) converts the transmit byte serial stream to a bit serial stream. Every self-timed channel (a self-timed channel is one that uses the CSU output clock) share a common line rate clock and byte clock, which can be output as TCLK. Only self-timed channels can be synchronized using the TFPI input. When a channel is loop-timed, TCLK, TFPI and TFPI are no more available and the receive signals shall be used instead to extract timing information.

10.8 Transmit Section Overhead Processor (TSOP)

The Transmit Section Overhead Processor (TSOP) provides frame pattern insertion (A1, A2), scrambling, section level alarm signal insertion, and section BIP-8 (B1) insertion.

10.8.1 Line AIS Insert

Line AIS insertion results in all bits of the SONET/SDH frame being set to 1 before scrambling except for the section overhead. The Line AIS Insert Block substitutes all ones as described when enabled through an internal register (Reg 0x14, TSOP) accessed through the microprocessor interface. Activation or deactivation of line AIS insertion is synchronized to frame boundaries.

10.8.2 BIP-8 Insert

The BIP-8 Insert Block calculates and inserts the BIP-8 error detection code (B1) into the transmit stream.

The BIP-8 calculation is based on the scrambled data of the complete STS-3c (STM-1) frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-8 code is then inserted into the B1 byte of the following frame before scrambling. BIP-8 errors may be continuously inserted under register control for diagnostic purposes.

10.8.3 Framing and Identity Insert

The Framing and Identity Insert Block inserts the framing bytes (A1, A2) into the STS-3c (STM-1) frame. Framing bit errors may be continuously inserted under register control for diagnostic purposes.

10.8.4 Scrambler

The Scrambler Block utilizes a frame synchronous scrambler to process the transmit stream when enabled through an internal register accessed via the microprocessor interface. The generating polynomial is $x^7 + x^6 + 1$. Precise details of the scrambling operation are provided in the references. Note that the framing bytes and the identity bytes are not scrambled. All zeros may be continuously inserted (after scrambling) under register control for diagnostic purposes.

10.9 Transmit Line Overhead Processor (TLOP)

The Transmit Line Overhead Processor (TLOP) provides line level alarm signal insertion, and line BIP-24 insertion (B2).

10.9.1 APS Insert

The APS Insert Block inserts the two automatic protection switch (APS) channel bytes in the Line Overhead (K1 and K2) into the transmit stream when enabled by an internal register.

10.9.2 Line BIP Calculate

The Line BIP Calculate Block calculates the line BIP-24 error detection code (B2) based on the line overhead and synchronous payload envelope of the transmit stream. The line BIP-24 code is a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-24 code is inserted into the B2 byte positions of the following frame. BIP-24 errors may be continuously inserted under register control for diagnostic purposes.

10.9.3 Line RDI Insert

The Line RDI Insert Block controls the insertion of line remote defect indication. Line RDI insertion is enabled using the TLRDI input, or register control. Line RDI is inserted by transmitting the code 110 (binary) in bit positions 6, 7, and 8 of the K2 byte contained in the transmit stream.

10.9.4 Line FEBE Insert

The Line FEBE Insert Block accumulates line BIP-24 errors (B2) detected by the Receive Line Overhead Processor and encodes far end block error indications in the transmit M1 byte.

10.10 Transmit Path Overhead Processor (TPOP)

The Transmit Path Overhead Processor (TPOP) provides transport frame alignment generation, pointer generation (H1, H2), path overhead insertion and the insertion of path level alarm signals.

10.10.1 Pointer Generator

The Pointer Generator Block generates the outgoing payload pointer (H1, H2) as specified in the references. The concatenation indication (the NDF field set to 1001, I-bits and D-bits set to all ones, and unused bits set to all zeros) is inserted in the second and third pointer byte locations in the transmit stream.

- (1) A "normal pointer value" locates the start of the SPE. Note: 0 ≤ "normal pointer value" ≤ 782, and the new data flag (NDF) field is set to 0110. Note that values greater than 782 may be inserted, using internal registers, to generate a loss of pointer alarm in downstream circuitry.

- (2) Arbitrary "pointer values" may be generated using internal registers. These new values may optionally be accompanied by a programmable new data flag. New data flags may also be generated independently using internal registers.

- (3) Positive pointer movements may be generated using a bit in an internal register. A positive pointer movement is generated by inverting the five I-bits of the pointer word. The SPE is not inserted during the positive stuff opportunity byte position, and the pointer value is incremented by one. Positive pointer movements may be inserted once per frame for diagnostic purposes.

- (4) Negative pointer movements may be generated using a bit in an internal register. A negative pointer movement is generated by inverting the five D-bits of the pointer word. The SPE is inserted during the negative stuff opportunity byte position, the H3 byte, and the pointer value is decremented by one. Negative pointer movements may be inserted once per frame for diagnostic purposes.

The pointer value is used to insert the path overhead into the transmit stream. The current pointer value may be read via internal registers.

10.10.2 BIP-8 Calculate

The BIP-8 Calculate Block performs a path bit interleaved parity calculation on the SPE of the transmit stream. Details are provided in the references. The resulting parity byte is inserted in the path BIP-8 (B3) byte position of the subsequent frame. BIP-8 errors may be continuously inserted under register control for diagnostic purposes.

10.10.3 FEBE Calculate

The FEBE Calculate Block accumulates far end block errors on a per frame basis, and inserts the accumulated value (up to maximum value of eight) in the FEBE bit positions of the path status (G1) byte. The FEBE information is derived from path BIP-8 errors detected by the receive path overhead processor, RPOP. Far end block errors may be inserted under register control for diagnostic purposes.

10.11 Transmit ATM Cell Processor (TXCP)

The Transmit ATM Cell Processor (TXCP) provides rate adaptation via idle/unassigned cell insertion, provides HCS generation and insertion, and performs ATM cell scrambling. The TXCP contains a four cell transmit FIFO. An idle or unassigned cell is transmitted if a complete ATM cell has not been written into the FIFO.

10.11.1 Idle/Unassigned Cell Generator

The Idle/Unassigned Cell Generator inserts idle or unassigned cells into the cell stream when enabled. Registers are provided to program the GFC, PTI, and CLP fields of the idle cell header and the idle cell payload. The idle cell HCS is automatically calculated and inserted.

10.11.2 Scrambler

The Scrambler scrambles the 48 octet information field. Scrambling is performed using a parallel implementation of the self synchronous scrambler ($x^{43} + 1$ polynomial) described in the references. The cell headers are transmitted unscrambled, and the scrambler may optionally be disabled.

10.11.3 HCS Generator

The HCS Generator performs a CRC-8 calculation over the first four header octets. A parallel implementation of the polynomial, x^8+x^2+x+1, is used. The coset polynomial, $x^6+x^4+x^2+1$, is added (modulo 2) to the residue. The HCS Generator optionally inserts the result into the fifth octet of the header.

10.12 UTOPIA Level 2 System Interface

The S/UNI-QUAD system interface provides a Utopia level 2 compliant bus to transfer ATM cells between the ATM layer device and the S/UNI-QUAD.

10.12.1 Receive ATM Interface

The Receive ATM FIFO (RXCP) provides FIFO management at the S/UNI-QUAD receive cell interface. The receive FIFO contains four cells. The FIFO provides the cell rate decoupling function between the transmission system physical layer and the ATM layer.

In general, the management functions include filling the receive FIFO, indicating when the receive FIFO contains cells, maintaining the receive FIFO read and write pointers, and detecting FIFO overrun and underrun conditions.

The FIFO interface is “UTOPIA Level 2" compliant and accepts a read clock (RFCLK) and read enable signal (RENB). The receive FIFO output bus (RDAT[15:0]) is tri-stated when RENB is logic one or if the PHY device address (RADR[4:0]) selected does not match this device's address. The interface indicates the start of a cell (RSOC) and the receive cell available status (RCA and DRCA[4:1]) when data is read from the receive FIFO (using the rising edges of RFCLK). The RCA (and DRCA[x]) status changes from available to unavailable when the FIFO is either empty (RCALEVEL0=1) or near empty (RCALEVEL0 is logic zero). This interface also indicates FIFO overruns via a maskable interrupt and register bits. Read accesses while RCA (or DRCA[x]) is a logic zero will output invalid data. The FIFO is reset on FIFO overrun, causing up to 4 cells to be lost.

10.12.2 Transmit ATM Interface

The ATM Transmit FIFO (TXCP) provides FIFO management at the S/UNI-QUAD transmit cell interface. The transmit FIFO contains four cells. The FIFO depth may be programmed to four, three, two, or one cells. The FIFO provides the cell

rate decoupling function between the transmission system physical layer and the ATM layer.

In general, the management functions include emptying cells from the transmit FIFO, indicating when the transmit FIFO is full, maintaining the transmit FIFO read and write pointers, and detecting a FIFO overrun condition.

The FIFO interface is “UTOPIA Level 2” compliant and accepts a write clock (TFCLK), a write enable signal (TENB), the start of a cell (TSOC) indication, the parity bit (TPRTY), and the ATM device address (TADR[4:0]) when data is written to the transmit FIFO (using the rising edges of TFCLK). The interface provides the transmit cell available status (TCA and DTCA[4:1]) which can transition from "available" to "unavailable" when the transmit FIFO is near full (when TCALEVEL0 is logic zero) or when the FIFO is full (when TCALEVEL0 is logic one) and can accept no more writes. To reduce FIFO latency, the FIFO depth at which TCA and DTCA[x] indicates "full" can be set to one, two, three or four cells by the FIFODP[1:0] bits of TXCP Configuration 2 register. If the programmed depth is less than four, more than one cell may be written after TCA or DTCA[x] is asserted as the TXCP still allows four cells to be stored in its FIFO. This interface also indicates FIFO overruns via a maskable interrupt and register bit, but write accesses while TCA or DTCA[x] is logic zero are not processed. The TXCP automatically transmits idle cells until a full cell is available to be transmitted.

10.13 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The S/UNI-QUAD identification code is 053490CD hexadecimal.

10.14 Microprocessor Interface

The microprocessor interface block provides normal and test mode registers, and the logic required to connect to the microprocessor interface. The normal mode registers are required for normal operation, and test mode registers are used to enhance the testability of the S/UNI-QUAD. The register set is accessed as shown in Table 3. In the following section every register is documented and identified using the register number (REG #). The corresponding memory map address for every channel (CH #1,2,3,4) is given in the table. Addresses that are not shown are not used and must be treated as Reserved.

Table 3: Register Memory Map

Address A[10:0]	Description

REG #	CH #1	CH #2	CH #3	CH #4	
00	000				S/UNI-QUAD Master Reset and Identity
01	001				S/UNI-QUAD Master Configuration
02	002				S/UNI-QUAD Master System Interface Config
03	003				S/UNI-QUAD Master Clock Monitor
04	004				S/UNI-QUAD Master Interrupt Status
05	005	105	205	305	S/UNI-QUAD Channel Reset and Performance Monitoring Update
06	006	106	206	206	S/UNI-QUAD Channel Configuration
07	007	107	207	307	S/UNI-QUAD Channel Control
08	008	108	208	308	S/UNI-QUAD Channel Control Extensions
09	009	109	209	309	Reserved
0A	00A	10A	20A	30A	S/UNI-QUAD Channel Interrupt Status 1
0B	00B	10B	20B	30B	Reserved
0C	00C				CSPI Control and Status (Clock Synthesis)
0D	00D				Reserved
0E	00E	10E	20E	30E	CRSI Control and Status (Clock Recovery)
0F	00F	10F	20F	30F	Reserved
10	010	110	210	310	RSOP Control/Interrupt Enable
11	011	111	211	311	RSOP Status/Interrupt Status
12	012	112	212	312	RSOP Section BIP-8 LSB
13	013	113	213	313	RSOP Section BIP-8 MSB
14	014	114	214	314	TSOP Control
15	015	115	215	315	TSOP Diagnostic
16	016	116	216	316	Reserved
17	017	117	217	317	Reserved
18	018	118	218	318	RLOP Control/Status
19	019	119	219	319	RLOP Interrupt Enable/Status
1A	01A	11A	21A	31A	RLOP Line BIP-24 LSB
1B	01B	11B	21B	31B	RLOP Line BIP-24
1C	01C	11C	21C	31C	RLOP Line BIP-24 MSB
1D	01D	11D	21D	31D	RLOP Line FEBE LSB
1E	01E	11E	21E	31E	RLOP Line FEBE
1F	01F	11F	21F	31F	RLOP Line FEBE MSB
20	020	120	220	320	TLOP Control
21	021	121	221	321	TLOP Diagnostic
22	022	122	222	322	TLOP Transmit K1
23	023	123	223	323	TLOP Transmit K2
24	024	124	224	324	S/UNI-QUAD Channel Transmit Synchronization Message (S1)

Address A[10:0]					Description
REG #	CH #1	CH #2	CH #3	CH #4	
25	025	125	225	325	Reserved
26	026	126	226	326	Reserved
27	027	127	227	327	Reserved
28	028	128	228	328	Reserved
29	029	129	229	329	Reserved
2A	02A	12A	22A	32A	Reserved
2B	02B	12B	22B	32B	Reserved
2C	02C	12C	22C	32C	Reserved
2D	02D	12D	22D	32D	Reserved
2E	02E	12E	22E	32E	Reserved
2F	02F	12F	22F	32F	Reserved
30	030	130	230	330	RPOP Status/Control (EXTD=0)
30	030	130	230	330	RPOP Status/Control (EXTD=1)
31	031	131	231	331	RPOP Interrupt Status (EXTD=0)
31	031	131	231	331	RPOP Interrupt Status (EXTD=1)
32	032	132	232	332	RPOP Pointer Interrupt Status
33	033	133	233	333	RPOP Interrupt Enable (EXTD=0)
33	033	133	233	333	RPOP Interrupt Enable (EXTD=1)
34	034	134	234	334	RPOP Pointer Interrupt Enable
35	035	135	235	335	RPOP Pointer LSB
36	036	136	236	336	RPOP Pointer MSB and RDI Filter Control
37	037	137	237	337	RPOP Path Signal Label
38	038	138	238	338	RPOP Path BIP-8 LSB
39	039	139	239	339	RPOP Path BIP-8 MSB
3A	03A	13A	23A	33A	RPOP Path FEBE LSB
3B	03B	13B	23B	33B	RPOP Path FEBE MSB
3C	03C	13C	23C	33C	RPOP Auxiliary RDI
3D	03D	13D	23D	33D	RPOP Path BIP-8 Configuration
3E	03E	13E	23E	33E	Reserved
3F	03F	13F	23F	33F	Reserved
40	040	140	240	340	TPOP Control/Diagnostic
41	041	141	241	341	TPOP Pointer Control
42	042	142	242	342	Reserved
43	043	143	243	343	TPOP Current Pointer LSB
44	044	144	244	344	TPOP Current Pointer MSB
45	045	145	245	345	TPOP Arbitrary Pointer LSB
46	046	146	246	346	TPOP Arbitrary Pointer MSB
47	047	147	247	347	Reserved

Address A[10:0]					Description
REG #	CH #1	CH #2	CH #3	CH #4	
48	048	148	248	348	TPOP Path Signal Label
49	049	149	249	349	TPOP Path Status
4A	04A	14A	24A	34A	Reserved
4B	04B	14B	24B	34B	Reserved
4C	04C	14C	24C	34C	Reserved
4D	04D	14D	24D	34D	Reserved
4E	04E	14E	24E	34E	Reserved
4F	04F	14F	24F	34F	Reserved
50	050	150	250	350	Reserved
51	051	151	251	351	Reserved
52	052	152	252	352	Reserved
53	053	153	253	353	Reserved
54	054	154	254	354	Reserved
55	055	155	255	355	Reserved
56	056	156	256	356	Reserved
57	057	157	257	357	Reserved
58	058	158	258	358	Reserved
59	059	159	259	359	Reserved
5A	05A	15A	25A	35A	Reserved
5B	05B	15B	25B	35B	Reserved
5C	05C	15C	25C	35C	Reserved
5D	05D	15D	25D	35D	Reserved
5E	05E	15E	25E	35E	Reserved
5F	05F	15F	25F	35F	Reserved
60	060	160	260	360	RXCP Configuration 1
61	061	161	261	361	RXCP Configuration 2
62	062	162	262	362	RXCP FIFO/UTOPIA Control & Config
63	063	163	263	363	RXCP Interrupt Enables and Counter Status
64	064	164	264	364	RXCP Status/Interrupt Status
65	065	165	265	365	RXCP LCD Count Threshold (MSB)
66	066	166	266	366	RXCP LCD Count Threshold (LSB)
67	067	167	267	367	RXCP Idle Cell Header Pattern
68	068	168	268	368	RXCP Idle Cell Header Mask
69	069	169	269	369	RXCP Corrected HCS Error Count
6A	06A	16A	26A	36A	RXCP Uncorrected HCS Error Count
6B	06B	16B	26B	36B	RXCP Received Cell Count LSB
6C	06C	16C	26C	36C	RXCP Received Cell Count
6D	06D	16D	26D	36D	RXCP Received Cell Count MSB

Address A[10:0]					Description
REG #	CH #1	CH #2	CH #3	CH #4	
6E	06E	16E	26E	36E	RXCP Idle Cell Count LSB
6F	06F	16F	26F	36F	RXCP Idle Cell Count
70	070	170	270	370	RXCP Idle Cell Count MSB
71	071	171	271	371	Reserved
72	072	172	272	372	Reserved
73	073	173	273	373	Reserved
74	074	174	274	374	Reserved
75	075	175	275	375	Reserved
76	076	176	276	376	Reserved
77	077	177	277	377	Reserved
78	078	178	278	378	Reserved
79	079	179	279	379	Reserved
7A	07A	17A	27A	37A	Reserved
7B	07B	17B	27B	37B	Reserved
7C	07C	17C	27C	37C	Reserved
7D	07D	17D	27D	37D	Reserved
7E	07E	17E	27E	37E	Reserved
7F	07F	17F	27F	37F	Reserved
80	080	180	280	380	TXCP Configuration 1
81	081	181	281	381	TXCP Configuration 2
82	082	182	282	382	TXCP Transmit Cell Status/Configuration Options
83	083	183	283	383	TXCP Interrupt Enable/Status
84	084	184	284	384	TXCP Idle Cell Header Control
85	085	185	285	385	TXCP Idle Cell Payload Control
86	086	186	286	386	TXCP Transmit Cell Counter LSB
87	087	187	287	387	TXCP Transmit Cell Counter
88	088	188	288	388	TXCP Transmit Cell Counter MSB
89	089	189	289	389	Reserved
8A	08A	18A	28A	38A	Reserved
8B	08B	18B	28B	38B	Reserved
8C	08C	18C	28C	38C	Reserved
8D	08D	18D	28D	38D	Reserved
8E	08E	18E	28E	38E	Reserved
8F	08F	18F	28F	38F	Reserved
90	090	190	290	390	S/UNI-QUAD Channel Auto Line RDI Control
91	091	191	291	391	S/UNI-QUAD Channel Auto Path RDI Control
92	092	192	292	392	S/UNI-QUAD Channel Auto Enhanced Path RDI Control

Address A[10:0]					Description
REG #	CH #1	CH #2	CH #3	CH #4	
93	093	193	293	393	S/UNI-QUAD Channel Receive RDI and Enhanced RDI Control Extensions
94	094	194	294	394	S/UNI-QUAD Channel Receive Line AIS Control
95	095	195	295	395	S/UNI-QUAD Channel Receive Path AIS Control
96	096	196	296	396	S/UNI-QUAD Channel Receive Alarm Control #1
97	097	197	297	397	S/UNI-QUAD Channel Receive Alarm Control #2
98 - DF	098 - 0DF	198 - 1DF	298 - 2DF	398 - 3DF	Reserved
E0	0E0	1E0	2E0	3E0	RASE Interrupt Enable
E1	0E1	1E1	2E1	3E1	RASE Interrupt Status
E2	0E2	1E2	2E2	3E2	RASE Configuration/Control
E3	0E3	1E3	2E3	3E3	RASE SF BERM Accumulation Period (LSB)
E4	0E4	1E4	2E4	3E4	RASE SF BERM Accumulation Period
E5	0E5	1E5	2E5	3E5	RASE SF BERM Accumulation Period (MSB)
E6	0E6	1E6	2E6	3E6	RASE SF BERM Saturation Threshold (LSB)
E7	0E7	1E7	2E7	3E7	RASE SF BERM Saturation Threshold (MSB)
E8	0E8	1E8	2E8	3E8	RASE SF BERM Declaring Threshold (LSB)
E9	0E9	1E9	2E9	3E9	RASE SF BERM Declaring Threshold (MSB)
EA	0EA	1EA	2EA	3EA	RASE SF BERM Clearing Threshold (LSB)
EB	0EB	1EB	2EB	3EB	RASE SF BERM Clearing Threshold (MSB)
EC	0EC	1EC	2EC	3EC	RASE SD BERM Accumulation Period (LSB)
ED	0ED	1ED	2ED	3ED	RASE SD BERM Accumulation Period
EE	0EE	1EE	2EE	3EE	RASE SD BERM Accumulation Period (MSB)
EF	0EF	1EF	2EF	3EF	RASE SD BERM Saturation Threshold (LSB)
F0	0F0	1F0	2F0	3F0	RASE SD BERM Saturation Threshold (MSB)
F1	0F1	1F1	2F1	3F1	RASE SD BERM Declaring Threshold (LSB)
F2	0F2	1F2	2F2	3F2	RASE SD BERM Declaring Threshold (MSB)
F3	0F3	1F3	2F3	3F3	RASE SD BERM Clearing Threshold (LSB)
F4	0F4	1F4	2F4	3F4	RASE SD BERM Clearing Threshold (MSB)
F5	0F5	1F5	2F5	3F5	RASE APS K1
F6	0F6	1F6	2F6	3F6	RASE APS K2
F7	0F7	1F7	2F7	3F7	RASE Synchronization Status S1
F8	0F8	1F8	2F8	3F8	Reserved
F9	0F9	1F9	2F9	3F9	Reserved
FA	0FA	1FA	2FA	3FA	Reserved
FB	0FB	1FB	2FB	3FB	Reserved
FC	0FC	1FC	2FC	3FC	Reserved
FD	0FD	1FD	2FD	3FD	Reserved

Address A[10:0]					Description
REG #	CH #1	CH #2	CH #3	CH #4	
FE	0FE	1FE	2FE	3FE	Reserved
FF	0FF	1FF	2FF	3FF	Reserved
	400				S/UNI-QUAD Master Test Register
	401 - 4FF	501 - 5FF	601 - 6FF	701 - 7FF	Reserved for Test

Notes on Register Memory Map:

- For all register accesses, CSB must be low.
- Addresses that are not shown must be treated as Reserved.
- A[10] is the test resister select (TRS) and should be set to logic zero for normal mode register access.

11 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the S/UNI-QUAD. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[10]) is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the S/UNI-QUAD to determine the programming state of the block.

3. Writable normal mode register bits are cleared to logic zero upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect S/UNI-QUAD operation unless otherwise noted. Performance monitoring counters registers are a common exception.

5. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the S/UNI-QUAD operates as intended, reserved register bits must be written with their default value as indicated by the register bit description.

Register 0x00: S/UNI-QUAD Master Reset and Identity

Bit	Type	Function	Default
Bit 7	R/W	RESET	0
Bit 6	R	TYPE[3]	1
Bit 5	R	TYPE[2]	1
Bit 4	R	TYPE[1]	1
Bit 3	R	TYPE[0]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	0
Bit 0	R	ID[0]	1

This register allows the revision of the S/UNI-QUAD to be read by software permitting graceful migration to support newer feature enhanced versions of the S/UNI-QUAD. It also provides software reset capability.

In addition, writing to this register simultaneously loads all the performance meter registers in the RSOP, RLOP, RPOP, RXCP and TXCP blocks.

ID[2:0]:

The ID bits can be read to provide a binary S/UNI-QUAD revision number.

TYPE[3:0]:

The TYPE bits distinguish the S/UNI-QUAD from the other members of the S/UNI family of devices.

RESET:

The RESET bit allows the S/UNI-QUAD to be reset under software control. If the RESET bit is a logic one, the entire S/UNI-QUAD is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the S/UNI-QUAD out of reset. Holding the S/UNI-QUAD in a reset state places it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus negating the software reset. Otherwise, the effect of a software reset is equivalent to that of a hardware reset.

Register 0x01: S/UNI-QUAD Master Configuration

Bit	Type	Function	Default
Bit 7	R/W	PECLV	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	TFPO_CH[1]	0
Bit 4	R/W	TFPO_CH[0]	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

TFPO_CH[1:0]:

The transmit frame pulse channel select (TFPO_CH[1:0]) bits selects which channel's transmit frame pulse is available on the TFPO output pin. Since the RFPO1-4 output pins are providing transmit timing information for loop-timed channels, it is suggested (but not mandatory) that a self-timed channel be selected. Self-timed channels all operate off the same clock synthesis unit and thus have a common timing reference (their frequency will be identical although their frame pulses might not be aligned).

Table 5: TFPO Channel Selection

TFPO_CH[1:0]	Selected Channel
00	Channel #1
01	Channel #2
10	Channel #3
11	Channel #4

PECLV:

The PECL reveiver input voltage (PECLV) bit configures the PECL receiver level shifter. When PECLV is set to logic zero, the PECL receivers are configured to operate with a 3.3V input voltage. When PECLV is set to logic one, the PECL receivers are configured to operate with a 5.0V input voltage.

Reserved:

The reserved bits must be programmed to their default value proper operation.

Register 0x02: S/UNI-QUAD Master System Interface Control

Bit	Type	Function	Default
Bit 7	R/W	PHY_ADR[2]	0
Bit 6	R/W	PHY_ADR[1]	0
Bit 5	R/W	PHY_ADR[0]	0
Bit 4	R/W	PHY_EN	0
Bit 3		Unused	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

PHY_EN:

The PHY_EN enables the System Interface (Utopia bus).

When set to logic zero, all the output signals of the System Interface are held in high impedance. When set to logic one, the System Interface is driven. This register bit must be set to logic one to start using the device. If the System Interface is shared by several PHY layer devices, they should all be configured with their own unique PHY_ADR[2:0] (see below) value before enabling them, otherwise conflicts could occur on the bus resulting in damages to the devices.

PHY_ADR[2:0]:

The PHY_ADR[2:0] is Device Identification Address (PHY_ADR[2:0]). The PHY_ADR[2:0] register bits are the most-significant bits of the address space which this S/UNI-QUAD occupies. When the PHY_ADR[2:0] inputs match the TADR[4:2] or RADR[4:2] inputs, then one of the four quadrants (as determined by the TADR[1:0] or RADR[1:0] inputs) in this S/UNI-QUAD is selected for transmit or receive operations. Note that the null-PHY address 0x1F is the null-PHY address and cannot be assigned to any port on the S/UNI-QUAD.

Register 0x03: S/UNI-QUAD Master Clock Monitor

Bit	Type	Function	Default
Bit 7	R	RCLK4A	X
Bit 6	R	RCLK3A	X
Bit 5	R	RCLK2A	X
Bit 4	R	RCLK1A	X
Bit 3	R	TCLKA	X
Bit 2	R	RFCLKA	X
Bit 1	R	TFCLKA	X
Bit 0	R	REFCLKA	X

This register provides activity monitoring on S/UNI-QUAD clocks. When a monitored clock signal makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read at periodic intervals to detect clock failures.

REFCLKA:

The REFCLK active (REFCLKA) bit monitors for low to high transitions on the REFCLK reference clock input. REFCLKA is set high on a rising edge of REFCLK, and is set low when this register is read.

TFCLKA:

The TFCLK active (TFCLKA) bit monitors for low to high transitions on the TFCLK transmit FIFO clock input. TFCLKA is set high on a rising edge of TFCLK, and is set low when this register is read.

RFCLKA:

The RFCLK active (RFCLKA) bit monitors for low to high transitions on the RFCLK receive FIFO clock input. RFCLKA is set high on a rising edge of RFCLK, and is set low when this register is read.

TCLKA:

The TCLK active (TCLKA) bit monitors for low to high transitions on the TCLK output. TCLKA is set high on a rising edge of TCLK, and is set low when this register is read.

RCLK1A:

The Channel #1 RCLK active (RCLK1A) bit monitors for low to high transitions on the RCLK1 output. RCLK1A is set high on a rising edge of RCLK1, and is set low when this register is read.

RCLK2A:

The Channel #2 RCLK active (RCLK2A) bit monitors for low to high transitions on the RCLK2 output. RCLK2A is set high on a rising edge of RCLK2, and is set low when this register is read.

RCLK3A:

The Channel #3 RCLK active (RCLK3A) bit monitors for low to high transitions on the RCLK3 output. RCLK3A is set high on a rising edge of RCLK3, and is set low when this register is read.

RCLK4A:

The Channel #4 RCLK active (RCLK4A) bit monitors for low to high transitions on the RCLK4 output. RCLK4A is set high on a rising edge of RCLK4, and is set low when this register is read.

Register 0x04: S/UNI-QUAD Master Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	CSUI	X
Bit 3	R	CHNL4I	X
Bit 2	R	CHNL3I	X
Bit 1	R	CHNL2I	X
Bit 0	R	CHNL1I	X

When the interrupt output INTB goes low, this register allows the source of an active interrupt to be identified down to the channel level. Further register accesses are required for the channel in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

CHNL1I:

The CHNL1I bit is high when an interrupt request is active from the channel #1. The Channel #1 Interrupt Status register should be read to identify the source of the interrupt.

CHNL2I:

The CHNL2I bit is high when an interrupt request is active from the channel #2. The Channel #2 Interrupt Status register should be read to identify the source of the interrupt.

CHNL3I:

The CHNL3I bit is high when an interrupt request is active from the channel #3. The Channel #3 Interrupt Status register should be read to identify the source of the interrupt.

CHNL4I:

The CHNL4I bit is high when an interrupt request is active from the channel #4. The Channel #4 Interrupt Status register should be read to identify the source of the interrupt.

CSUI:

The CSUI bit is high when an interrupt request is active from the Clock Synthesis and PISO block (CSPI, Clock Synthesis Unit). The CSUI interrupt sources are enabled in the Clock Synthesis Interrupt Control/Status Register.

Register 0x05: S/UNI-QUAD Channel Reset and Monitoring Update

Bit	Type	Function	Default
Bit 7	R/W	CHRESET	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	TIP	X

This register provides software reset capability on a per channel basis. It also loads, by writing this register (without setting the CHRESET bit), all the error counters in the RSOP, RLOP, RPOP, RXCP and TXCP blocks.

TIP:

The TIP bit is set to a logic one when any value with the CHRESET bit set to logic zero is written to this register. Such a write initiates an accumulation interval transfer and loads all the performance meter registers in the RSOP, RLOP, RPOP, RXCP and TXCP blocks for channel #1. TIP remains high while the transfer is in progress, and is set to a logic zero when the transfer is complete. TIP can be polled by a microprocessor to determine when the accumulation interval transfer is complete.

CHRESET:

The CHRESET bit allows the Channel to be reset under software control. If the CHRESET bit is a logic one, the entire channel is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the channel out of reset. Holding a channel in a reset state places it into a low power, stand-by mode. A hardware reset clears the CHRESET bit, thus negating the software reset. Otherwise, the effect of a software reset is equivalent to that of a hardware reset.

Register 0x06: S/UNI-QUAD Channel Configuration

Bit	Type	Function	Default
Bit 7	R/W	AUTOPFEBE	1
Bit 6	R/W	AUTOLFEBE	1
Bit 5	R/W	AUTOLRDI	1
Bit 4	R/W	AUTOPRDI	1
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	1

AUTOPRDI

The AUTOPRDI bit determines whether STS path remote defect indication (RDI) is sent immediately upon detection of an incoming alarm. When AUTOPRDI is set to logic one, STS path RDI is inserted immediately upon declaration of several alarms. Each alarm can individually be enabled and disabled using the S/UNI-QUAD Channel Path RDI Control Registers.

AUTOLRDI

The AUTOLRDI bit determines if line remote defect indication (RDI) is sent immediately upon detection of an incoming alarm. When AUTOLRDI is set to logic one, line RDI is inserted immediately upon declaration of several alarms. Each alarm can individually be enabled and disabled using the S/UNI-QUAD Channel Line RDI Control Registers.

AUTOPFEBE

The AUTOPFEBE bit determines if the path far end block errors are sent upon detection of an incoming path BIP error events. When AUTOPFEBE is set to logic one, one path FEBE is inserted for each path BIP error event, respectively. When AUTOPFEBE is set to logic zero, incoming path BIP error events do not generate FEBE events.

AUTOLFEBE

The AUTOLFEBE bit determines if line far end block errors are sent upon detection of an incoming line BIP error events. When AUTOLFEBE is set to logic one, one line FEBE is inserted for each line BIP error event, respectively. When AUTOLFEBE is set to logic zero, incoming line BIP error events do not generate FEBE events.

Register 0x07: S/UNI-QUAD Channel Control

Bit	Type	Function	Default
Bit 7	R/W	TFPI_EN	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	RXDINV	0
Bit 4		Unused	X
Bit 3	R/W	PDLE	0
Bit 2	R/W	LLE	0
Bit 1	R/W	SDLE	0
Bit 0	R/W	LOOPT	0

This register controls the timing and high speed loopback features of the S/UNI-QUAD.

LOOPT:

The LOOPT bit selects the source of timing for the transmit section of the channel. When LOOPT is a logic zero, the transmitter timing is derived from input REFCLK (Clock Synthesis Unit) is used. When LOOPT is a logic one, the transmitter timing is derived from the recovered clock. (Clock Recovery Unit).

SDLE:

The SDLE bit enables the serial diagnostic loopback. When SDLE is a logic one, the transmit serial stream is connected to the receive stream. The SDLE and the LLE bits should not be set high simultaneously.

LLE:

The LLE bit enables the S/UNI-QUAD line loopback. When LLE is a logic one, the value on RXD+/- differential inputs is synchronously mapped to the TXD+/- differential outputs, after clock recovery. The SDLE and the LLE bits should not be set high simultaneously.

PDLE:

The PDLE bit enables the parallel diagnostic loopback. When PDLE is a logic one, the transmit parallel stream is connected to the receive stream. The loopback point is between the TPOP and the RPOP blocks. Blocks upstream of the loopback point continue to operate normally. For example line AIS may be inserted in the transmit stream upstream of the loopback point using the TSOP Control register.

RXDINV:

The RXDINV bit selects the active polarity of the RXD+/- signals. The default configuration selects RXD+ to be active high and RXD- to be active low. When RXDINV is set to logic one, RXD+ to be active low and RXD- to be active high.

TFPI_EN:

The TFPI_EN bit controls the framing alignment in the transmit direction. When TFPI_EN is set to logic one the transmit SONET/SDH framing is aligned to a master (available to all four channels) framing pulse counter, which can also be aligned to the TFPI device input. When TFPI_EN is set to logic zero the transmit framing alignment is arbitrary. External framing (TFPI_EN set to logic one) shall only be used when the channel is in self-timed mode. TFPI_EN should always be set to logic zero when the channel is loop-timed (LOOPT set to logic one) or in line loopback (LLE set to logic one).

Register 0x08: S/UNI-QUAD Channel Control Extension

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

This register controls the timing and high speed loopback features of the S/UNI-QUAD.

Reserved:

The reserved bits must be programmed to their default value proper operation.

Register 0x0A: S/UNI-QUAD Channel Interrupt Status #1

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	RASEI	X
Bit 5	R	CRUI	X
Bit 4	R	TXCPI	X
Bit 3	R	RXCPI	X
Bit 2	R	RPOPI	X
Bit 1	R	RLOPI	X
Bit 0	R	RSOPI	X

This register allows the source of an active interrupt to be identified down to the block level within a given channel. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RSOPI:

The RSOPI bit is high when an interrupt request is active from the RSOP block. The RSOP interrupt sources are enabled in the RSOP Control/Interrupt Enable Register.

RLOPI:

The RLOPI bit is high when an interrupt request is active from the RLOP block. The RLOP interrupt sources are enabled in the RLOP Interrupt Enable/Status Register.

RPOPI:

The RPOPI bit is high when an interrupt request is active from the RPOP block. The RPOP interrupt sources are enabled in the RPOP Interrupt Enable Register.

RXCPI:

The RXCPI bit is high when an interrupt request is active from the RXCP block. The RXCP interrupt sources are enabled in the RXCP Interrupt Enable/Status Register.

TXCPI:

The TXCPI bit is high when an interrupt request is active from the TXCP block. The TXCP interrupt sources are enabled in the TXCP Interrupt Control/Status Register.

CRUI:

The CRUI bit is high when an interrupt request is active from the Clock Recovery and SIPO block (CRSI, Clock Recovery Unit). The CRUI interrupt sources are enabled in the Clock Recovery Interrupt Control/Status Register.

RASEI:

The RASEI bit is high when an interrupt request is active from the RASE block. The RASE interrupt sources are enabled in the RASE Interrupt Enable Register.

Register 0x0C: CSPI (Clock Synthesis) Control and Status

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R	TROOLI	X
Bit 4		Unused	X
Bit 3	R	TROOLV	X
Bit 2		Unused	X
Bit 1	R/W	TROOLE	0
Bit 0	R/W	Reserved	0

This register controls the clock synthesis and reports the state of the transmit phase locked loop.

TROOLE:

The TROOLE bit is an interrupt enable for the transmit reference out of lock status. When TROOLE is set to logic one, an interrupt is generated when the TROOLV bit changes state.

TROOLV:

The transmit reference out of lock status indicates the clock synthesis phase locked loop is unable to lock to the reference on REFCLK. TROOLV is a logic one if the divided down synthesized clock frequency is not within 488 ppm of the REFCLK frequency.

TROOLI:

The TROOLI bit is the transmit reference out of lock interrupt status bit. TROOLI is set high when the TROOLV bit of the S/UNI-QUAD Clock Synthesis Control and Status register changes state. TROOLV indicates the clock synthesis phase locked loop is unable to lock to the reference on REFCLK and is a logic one if the divided down synthesized clock frequency is not within 488 ppm of the REFCLK frequency. TROOLI is cleared when this register is read.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x0D: CSPI (Clock Synthesis) Reserved

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x0E: CRSI (Clock Recovery) Control and Status

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R	RROOLI	X
Bit 5	R	RDOOLI	X
Bit 4	R	RROOLV	X
Bit 3	R	RDOOLV	X
Bit 2	R/W	RROOLE	0
Bit 1	R/W	RDOOLE	0
Bit 0	R/W	Reserved	0

This register controls the clock recovery and reports the state of the receive phase locked loop.

RDOOLE:

The RDOOLE bit is an interrupt enable for the receive data out of lock status. When RDOOLE is set to logic one, an interrupt is generated when the RDOOLV bit changes state.

RROOLE:

The RROOLE bit is an interrupt enable for the reference out of lock status. When RROOLE is set to logic one, an interrupt is generated when the RROOLV bit changes state.

RDOOLV:

The receive data out of lock status indicates the clock recovery phase locked loop is unable to lock to the incoming data stream. RDOOLV is a logic one if the divided down recovered clock frequency is not within 488 ppm of the REFCLK frequency or if no transitions have occurred on the RXD+/- inputs for more than 80 bit periods.

RROOLV:

The receive reference out of lock status indicates the clock recovery phase locked loop is unable to lock to the receive reference (REFCLK). RROOLV should be polled after a power up reset to determine when the CRU PLL is operational. When RROOLV is a logic one, the CRU is unable to lock to the receive reference. When RROOLV is a logic zero, the CRU is locked to the receive reference. The RROOLV bit may remain set at logic one for several

hundred milliseconds after the removal of the power on reset as the CRU PLL locks to the receive reference clock.

RDOOLI:

The RDOOLI bit is the receive data out of lock interrupt status bit. RDOOLI is set high when the RDOOLV bit of the S/UNI-QUAD Clock Recovery Control and Status register changes state. RDOOLI is cleared when this register is read.

RROOLI:

The RROOLI bit is the receive reference out of lock interrupt status bit. RROOLI is set high when the RROOLV bit of the Clock Synthesis Control and Status register changes state. RROOLI is cleared when this register is read.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x0F: CRSI (Clock Recovery) Reserved

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x10: RSOP Control/Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	BIPWORD	0
Bit 6	R/W	DDS	0
Bit 5	W	FOOF	X
Bit 4	R/W	ALGO2	0
Bit 3	R/W	BIPEE	0
Bit 2	R/W	LOSE	0
Bit 1	R/W	LOFE	0
Bit 0	R/W	OOFE	0

OOFE:

The OOFE bit is an interrupt enable for the out of frame alarm. When OOFE is set to logic one, an interrupt is generated when the out of frame alarm changes state.

LOFE:

The LOFE bit is an interrupt enable for the loss of frame alarm. When LOFE is set to logic one, an interrupt is generated when the loss of frame alarm changes state.

LOSE:

The LOSE bit is an interrupt enable for the loss of signal alarm. When LOSE is set to logic one, an interrupt is generated when the loss of signal alarm changes state.

BIPEE:

The BIPEE bit is an interrupt enable for the section BIP-8 errors. When BIPEE is set to logic one, an interrupt is generated when a section BIP-8 error (B1) is detected.

ALGO2:

The ALGO2 bit position selects the framing algorithm used to confirm and maintain the frame alignment. When a logic one is written to the ALGO2 bit position, the framer is enabled to use the second of the framing algorithms where only the first A1 framing byte and the first 4 bits of the last A2 framing byte (12 bits total) are examined. This algorithm examines only 12 bits of the framing pattern regardless of the STS mode; all other framing bits are ignored. When a logic zero is written to the ALGO2 bit position, the framer is

enabled to use the first of the framing algorithms where all the A1 framing bytes and all the A2 framing bytes are examined. This algorithm examines all 48 bits of the STS-3c (STM-1/AU3/AU4) framing pattern.

FOOF:

The FOOF bit controls the framing of the RSOP. When a logic one is written to FOOF, the RSOP is forced out of frame at the next frame boundary. The FOOF bit is a write only bit, register reads may yield a logic one or a logic zero.

DDS:

The DDS bit is set to logic one to disable the de-scrambling of the STS-3c (STM-1) stream. When DDS is a logic zero, de-scrambling is enabled.

BIPWORD:

The BIPWORD bit position enables the accumulating of section block BIP errors. When a logic one is written to the BIPWORD bit position, one or more errors in the BIP-8 byte result in a single error accumulated in the B1 error counter. When a logic zero is written to the BIPWORD bit position, all errors in the B1 byte are accumulated in the B1 error counter.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x11: RSOP Status/Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	BIPEI	X
Bit 5	R	LOSI	X
Bit 4	R	LOFI	X
Bit 3	R	OOFI	X
Bit 2	R	LOSV	X
Bit 1	R	LOFV	X
Bit 0	R	OOFV	X

OOFV:

The OOFV bit is read to determine the out-of-frame state of the RSOP. When OOFV is high, the RSOP is out of frame. When OOFV is low, the RSOP is in-frame.

LOFV:

The LOFV bit is read to determine the loss of frame state of the RSOP. When LOFV is high, the RSOP has declared loss of frame.

LOSV:

The LOSV bit is read to determine the loss of signal state of the RSOP. When LOSV is high, the RSOP has declared loss of signal.

OOFI:

The OOFI bit is the out of frame interrupt status bit. OOFI is set high when a change in the out-of-frame state occurs. This bit is cleared when this register is read.

LOFI:

The LOFI bit is the loss of frame interrupt status bit. LOFI is set high when a change in the loss-of-frame state occurs. This bit is cleared when this register is read.

LOSI:

The LOSI bit is the loss of signal interrupt status bit. LOSI is set high when a change in the loss-of-signal state occurs. This bit is cleared when this register is read.

BIPEI:

The BIPEI bit is the section BIP-8 interrupt status bit. BIPEI is set high when a section layer (B1) bit error is detected. This bit is cleared when this register is read.

Register 0x12: RSOP Section BIP-8 LSB

Bit	Type	Function	Default
Bit 7	R	SBE[7]	X
Bit 6	R	SBE[6]	X
Bit 5	R	SBE[5]	X
Bit 4	R	SBE[4]	X
Bit 3	R	SBE[3]	X
Bit 2	R	SBE[2]	X
Bit 1	R	SBE[1]	X
Bit 0	R	SBE[0]	X

Register 0x13: RSOP Section BIP-8 MSB

Bit	Type	Function	Default
Bit 7	R	SBE[15]	X
Bit 6	R	SBE[14]	X
Bit 5	R	SBE[13]	X
Bit 4	R	SBE[12]	X
Bit 3	R	SBE[11]	X
Bit 2	R	SBE[10]	X
Bit 1	R	SBE[9]	X
Bit 0	R	SBE[8]	X

SBE[15:0]:

Bits SBE[15:0] represent the number of section BIP-8 errors (individual or block) that have been detected since the last time the error count was polled. The error count is polled by writing to either of the RSOP Section BIP-8 Register addresses. Such a write transfers the internally accumulated error count to the Section BIP-8 registers within approximately 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

The count can also be polled by writing to the Master Reset and Identity / Load Performance Meters register (0x05). Writing to register 0x05 simultaneously loads all the performance meter registers in the RSOP, RLOP, RPOP, RXCP and TXCP blocks.

Register 0x14: TSOP Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DS	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	LAIS	0

LAIS:

The LAIS bit controls the insertion of line alarm indication signal (AIS). When LAIS is set to logic one, the TSOP inserts AIS into the transmit SONET/SDH stream. Activation or deactivation of line AIS insertion is synchronized to frame boundaries. Line AIS insertion results in all bits of the SONET/SDH frame being set to one prior to scrambling except for the section overhead.

DS:

The DS bit is set to logic one to disable the scrambling of the STS-3c (STM-1) stream. When DS is a logic zero, scrambling is enabled.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x15: TSOP Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	DLOS	0
Bit 1	R/W	DBIP8	0
Bit 0	R/W	DFP	0

DFP:

The DFP bit controls the insertion of a single bit error continuously in the most significant bit (bit 1) of the A1 section overhead framing byte. When DFP is set to logic one, the A1 bytes are set to 0x76 instead of 0xF6.

DBIP8:

The DBIP8 bit controls the insertion of bit errors continuously in the section BIP-8 byte (B1). When DBIP8 is set to logic one, the B1 byte is inverted.

DLOS:

The DLOS bit controls the insertion of all zeros in the transmit stream. When DLOS is set to logic one, the transmit stream is forced to 0x00.

Register 0x18: RLOP Control/Status

Bit	Type	Function	Default
Bit 7	R/W	BIPWORD	0
Bit 6	R/W	ALLONES	0
Bit 5	R/W	AISDET	0
Bit 4	R/W	LRDIDET	0
Bit 3	R/W	BIPWORDO	0
Bit 2	R/W	FEBEWORD	0
Bit 1	R	LAISV	X
Bit 0	R	LRDIV	X

LRDIV:

The LRDIV bit is read to determine the remote defect indication state of the RLOP. When LRDIV is high, the RLOP has declared line RDI.

LAISV:

The LAISV bit is read to determine the line AIS state of the RLOP. When LAISV is high, the RLOP has declared line AIS.

FEBEWORD:

The FEBEWORD bit controls the accumulation of FEBEs. When FEBEWORD is logic one, the FEBE event counter is incremented only once per frame, whenever one or more FEBE bits occur during that frame. When FEBEWORD is logic zero, the FEBE event counter is incremented for each and every FEBE bit that occurs during that frame (the counter can be incremented up to 24).

BIPWORDO:

The BIPWORDO bit controls the indication of B2 errors reported to the TLOP block for insertion as FEBEs. When BIPWORDO is logic one, the BIP errors are indicated once per frame whenever one or more B2 bit errors occur during that frame. When BIPWORD0 is logic zero, BIP errors are indicated once for every B2 bit error that occurs during that frame. The accumulation of B2 error events functions independently and is controlled by the BIPWORD register bit..

LRDIDET:

The LRDIDET bit determines the Line LRDI detection algorithm. When LRDIDET is set to logic one, Line LRDI is declared when a 110 binary pattern is detected in bits 6,7 and 8 of the K2 byte for three consecutive frames. When LRDIDET is set to logic zero, Line LRDI is declared when a 110 binary pattern is detected in bits 6,7 and 8 of the K2 byte for five consecutive frames.

AISDET:

The AISDET bit determines the Line AIS detection algorithm. When AISDET is set to logic one, Line AIS is declared when a 111 binary pattern is detected in bits 6,7 and 8 of the K2 byte for three consecutive frames. When AISDET is set to logic zero, Line AIS is declared when a 111 binary pattern is detected in bits 6,7 and 8 of the K2 byte for five consecutive frames.

ALLONES:

The ALLONES bit controls automatically forcing the SONET frame passed to downstream blocks to logical all-ones whenever LAIS is detected. When ALLONES is set to logic one, the SONET frame is forced to logic one immediately when the LAIS alarm is declared. When LAIS is removed, the received byte is immediately returned to carrying data. When ALLONES is set to logic zero, the received byte carries the data regardless of the state of LAIS.

BIPWORD:

The BIPWORD bit controls the accumulation of B2 errors. When BIPWORD is logic one, the B2 error event counter is incremented only once per frame whenever one or more B2 bit errors occur during that frame. When BIPWORD is logic zero, the B2 error event counter is incremented for each B2 bit error that occurs during that frame (the counter can be incremented up to 24 times per frame).

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x19: RLOP Interrupt Enable/Interrupt Status

Bit	Type	Function	Default
Bit 7	R/W	FEBEE	0
Bit 6	R/W	BIPEE	0
Bit 5	R/W	LAISE	0
Bit 4	R/W	LRDIE	0
Bit 3	R	FEBEI	X
Bit 2	R	BIPEI	X
Bit 1	R	LAISI	X
Bit 0	R	LRDII	X

LRDII:

The LRDII bit is the line far end receive failure interrupt status bit. LRDII is set high when a change in the line RDI state occurs. This bit is cleared when this register is read.

LAISI:

The LAISI bit is the line AIS interrupt status bit. LAISI is set high when a change in the line AIS state occurs. This bit is cleared when this register is read.

BIPEI:

The BIPEI bit is the line BIP interrupt status bit. BIPEI is set high when a line layer (B2) bit error is detected. This bit is cleared when this register is read.

FEBEI:

The FEBEI bit is the line far end block error interrupt status bit. FEBEI is set high when a line layer FEBE (M1) is detected. This bit is cleared when this register is read.

LRDIE:

The LRDIE bit is an interrupt enable for the line remote defect indication alarm. When LRDIE is set to logic one, an interrupt is generated when line RDI changes state.

LAISE:

The LAISE bit is an interrupt enable for line AIS. When LAISE is set to logic one, an interrupt is generated when line AIS changes state.

BIPEE:

The BIPEE bit is an interrupt enable for the line BIP-24 errors. When BIPEE is set to logic one, an interrupt is generated when a line BIP-24 error (B2) is detected.

FEBEE:

The FEBEE bit is an interrupt enable for the line far end block errors. When FEBEE is set to logic one, an interrupt is generated when FEBE (M1) is detected.

Register 0x1A: RLOP Line BIP-24 LSB

Bit	Type	Function	Default
Bit 7	R	LBE[7]	X
Bit 6	R	LBE[6]	X
Bit 5	R	LBE[5]	X
Bit 4	R	LBE[4]	X
Bit 3	R	LBE[3]	X
Bit 2	R	LBE[2]	X
Bit 1	R	LBE[1]	X
Bit 0	R	LBE[0]	X

Register 0x1B: RLOP Line BIP-24

Bit	Type	Function	Default
Bit 7	R	LBE[15]	X
Bit 6	R	LBE[14]	X
Bit 5	R	LBE[13]	X
Bit 4	R	LBE[12]	X
Bit 3	R	LBE[11]	X
Bit 2	R	LBE[10]	X
Bit 1	R	LBE[9]	X
Bit 0	R	LBE[8]	X

Register 0x1C: RLOP Line BIP-24 MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	LBE[19]	X
Bit 2	R	LBE[18]	X
Bit 1	R	LBE[17]	X
Bit 0	R	LBE[16]	X

LBE[19:0]

Bits LBE[19:0] represent the number of line BIP-24 errors (individual or block) that have been detected since the last time the error count was polled. The error count is polled by writing to any of the RLOP Line BIP Registers or Line FEBE Register addresses. Such a write transfers the internally accumulated error count to the Line BIP Registers within approximately 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

The count can also be polled by writing to the S/UNI-QUAD Channel Reset and Monitoring Update register (0x05). Writing to register 0x05 simultaneously loads all the performance meter registers in the RSOP, RLOP, RPOP, RXCP and TXCP blocks.

Register 0x1D: RLOP Line FEBE LSB

Bit	Type	Function	Default
Bit 7	R	LFE[7]	X
Bit 6	R	LFE[6]	X
Bit 5	R	LFE[5]	X
Bit 4	R	LFE[4]	X
Bit 3	R	LFE[3]	X
Bit 2	R	LFE[2]	X
Bit 1	R	LFE[1]	X
Bit 0	R	LFE[0]	X

Register 0x1E: RLOP Line FEBE

Bit	Type	Function	Default
Bit 7	R	LFE[15]	X
Bit 6	R	LFE[14]	X
Bit 5	R	LFE[13]	X
Bit 4	R	LFE[12]	X
Bit 3	R	LFE[11]	X
Bit 2	R	LFE[10]	X
Bit 1	R	LFE[9]	X
Bit 0	R	LFE[8]	X

Register 0x1F: RLOP Line FEBE MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	LFE[19]	X
Bit 2	R	LFE[18]	X
Bit 1	R	LFE[17]	X
Bit 0	R	LFE[16]	X

LFE[19:0]

Bits LFE[19:0] represent the number of line FEBE errors (individual or block) that have been detected since the last time the error count was polled. The error count is polled by writing to any of the RLOP Line BIP Registers or Line FEBE Register addresses. Such a write transfers the internally accumulated error count to the Line FEBE Registers within approximately 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

The count can also be polled by writing to the S/UNI-QUAD Channel Reset and Monitoring Update register (0x05). Writing to register 0x05 simultaneously loads all the performance meter registers in the RSOP, RLOP, RPOP, RXCP and TXCP blocks.

Register 0x20: TLOP Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	APSREG	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	LRDI	0

LRDI:

The LRDI bit controls the insertion of line far end receive failure (LRDI). When LRDI is set to logic one, the TLOP inserts line RDI into the transmit SONET/SDH stream. Line RDI is inserted by transmitting the code 110 in bit positions 6, 7 and 8 of the K2 byte of the transmit stream.

APSREG:

The APSREG bit selects the source for the transmit APS channel. When APSREG is a logic zero, 0x0000 hexadecimal is inserted in the transmit APS channel. When APSREG is a logic one, the transmit APS channel is inserted from the TLOP Transmit K1 Register and the TLOP Transmit K2 Register.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x21: TLOP Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	DBIP	0

DBIP:

The DBIP bit controls the insertion of bit errors continuously in the line BIP byte(s) (B2). When DBIP is set to logic one, the B2 byte(s) are inverted.

Register 0x22: TLOP Transmit K1

Bit	Type	Function	Default
Bit 7	R/W	K1[7]	0
Bit 6	R/W	K1[6]	0
Bit 5	R/W	K1[5]	0
Bit 4	R/W	K1[4]	0
Bit 3	R/W	K1[3]	0
Bit 2	R/W	K1[2]	0
Bit 1	R/W	K1[1]	0
Bit 0	R/W	K1[0]	0

K1[7:0]:

The K1[7:0] bits contain the value inserted in the K1 byte when the APSREG bit in the TLOP Control Register is a logic one. K1[7] is the most significant bit, corresponding to the first bit (bit 1) transmitted. K1[0] is the least significant bit, corresponding to the last bit (bit 8) transmitted. The bits in this register are double buffered so that register writes do not need to be synchronized to SONET/SDH frame boundaries. The insertion of a new APS code value is initiated by a write to this register. The contents of this register, and the TLOP Transmit K2 Register are inserted in the transmit stream starting at the next frame boundary. Successive writes to this register must be spaced at least two frames (250 µs) apart.

Register 0x23: TLOP Transmit K2

Bit	Type	Function	Default
Bit 7	R/W	K2[7]	0
Bit 6	R/W	K2[6]	0
Bit 5	R/W	K2[5]	0
Bit 4	R/W	K2[4]	0
Bit 3	R/W	K2[3]	0
Bit 2	R/W	K2[2]	0
Bit 1	R/W	K2[1]	0
Bit 0	R/W	K2[0]	0

K2[7:0]:

The K2[7:0] bits contain the value inserted in the K2 byte when the APSREG bit in the TLOP Control Register is a logic one. K2[7] is the most significant bit, corresponding to the first bit (bit 1) transmitted. K2[0] is the least significant bit, corresponding to the last bit (bit 8) transmitted. The bits in this register are double buffered so that register writes do not need to be synchronized to SONET/SDH frame boundaries. The insertion of a new APS code value is initiated by a write to the TLOP Transmit K1 Register. A coherent APS code value is ensured by writing the desired K2 APS code value to this register before writing the TLOP Transmit K1 Register.

Register 0x24: S/UNI-QUAD Channel Transmit Sync. Message (S1)

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	TS1[3]	0
Bit 2	R/W	TS1[2]	0
Bit 1	R/W	TS1[1]	0
Bit 0	R/W	TS1[0]	0

TS1[3:0]:

The value written to these bit positions is inserted in the first S1 byte position of the transmit stream. The S1 byte is used to carry synchronization status messages between line terminating network elements. TS1[3] is the most significant bit, corresponding to the first bit transmitted. TS1[0] is the least significant bit, corresponding to the last bit transmitted.

Reserved

The reserved bits must be programmed to logic zero for proper operation.

Register 0x30 (EXTD=0): RPOP Status/Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R	LOPCONV	X
Bit 5	R	LOPV	X
Bit 4	R	PAISONV	X
Bit 3	R	PAISV	X
Bit 2	R	PRDIV	X
Bit 1	R	NEWPTRI	X
Bit 0	R/W	NEWPTRE	0

NOTE: To facilitate additional register mapping, shadow registers have been added to registers 0x30, 0x31 and 0x33. These shadow registers are accessed in the same way as the normal registers.

The EXTD (extend register) bit must be set in register 0x36 to allow switching between accessing the normal registers and the shadow registers.

This register allows the status of path level alarms to be monitored.

NEWPTRE:

The NEWPTRE bit is the interrupt enable for the receive new pointer status. When NEWPTRE is a logic one, an interrupt is generated when the pointer interpreter validates a new pointer.

NEWPTRI:

The NEWPTRI bit is the receive new pointer interrupt status bit. NEWPTRI is a logic one when the pointer interpreter has validated a new pointer value (H1, H2). NEWPTRI is cleared when this register is read.

PRDIV:

The PRDIV bit is read to determine the remote defect indication state. When PRDIV is a logic one, the S/UNI-QUAD has declared path RDI.

PAISV:

The PAISV bit is read to determine the path AIS state. When PAISV is a logic one, the S/UNI-QUAD has declared path AIS.

PAISCONV:

The PAISCONV bit is read to determine the concatenation path AIS state. When PAISCONV is a logic one, the S/UNI-QUAD has declared a concatenation path AIS.

PLOPV:

The PLOPV bit is read to determine the loss of pointer state. When PLOPV is a logic one, the S/UNI-QUAD has declared LOP.

LOPCONV:

The LOPCONV bit is read to determine the loss of pointer concatenation state. When LOPCONV is a logic one, the S/UNI-QUAD has declared loss of pointer concatenation.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x30 (EXTD=1): RPOP Status/Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	IINVCNT	0
Bit 5	R/W	PSL5	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2	R	ERDIV[2]	X
Bit 1	R	ERDIV[1]	X
Bit 0	R	ERDIV[0]	X

NOTE: To facilitate additional register mapping, shadow registers have been added to registers 0x30, 0x31 and 0x33. These shadow registers are accessed in the same way as the normal registers.

The EXTD (extend register) bit must be set in register 0x36 to allow switching between accessing the normal registers and the shadow registers.

The Status Register is provided at RPOP read address 0, if the extend register (EXTD) bit is set in register 0x36.

ERDIV[2:0]:

The ERDIV[2:0] bits reflect the current state of the detected enhanced RDI, (filtered G1 bits 5, 6, and 7).

IINVCNT:

When a logic one is written to the IINVCNT (Intuitive Invalid Pointer Counter) bit, if in the LOP state 3 x new point resets the inv_point count. If this bit is set to 0 the inv_point count will not be reset if in the LOP state and 3 x new pointers are detected.

PSL5:

The PSL5 bit controls the filtering of the path signal label byte (C2). When PSL5 is set high, the PSL is updated when the same value is received for 5 consecutive frames. When the PSL5 is set low, the PSL is updated when the same value is received for 3 consecutive frames.

Register 0x31 (EXTD=0): RPOP Interrupt Status

Bit	Type	Function	Default
Bit 7	R	PSLI	X
Bit 6		Unused	X
Bit 5	R	LOPI	X
Bit 4		Unused	X
Bit 3	R	PAISI	X
Bit 2	R	PRDII	X
Bit 1	R	BIPEI	X
Bit 0	R	FEBEI	X

NOTE: To facilitate additional register mapping, shadow registers have been added to registers 0x30, 0x31 and 0x33. These shadow registers are accessed in the same way as the normal registers.

The EXTD (extend register) bit must be set in register 0x36 to allow switching between accessing the normal registers and the shadow registers.

This register allows identification and acknowledgment of path level alarm and error event interrupts.

FEBEI:

The FEBEI bit is the path FEBE interrupt status bit. FEBEI is a logic one when a FEBE error is detected. This bit is cleared when this register is read.

BIPEI:

The BIPEI bit is the path BIP-8 interrupt status bit. BIPEI is a logic one when a B3 error is detected. This bit is cleared when this register is read.

PRDII:

The PRDII bit is the path remote defect indication interrupt status bit. PRDII is a logic one when a change in the path RDI state or the auxiliary path RDI state occurs. This bit is cleared when this register is read.

PAISI:

The PAISI bit is the path alarm indication signal interrupt status bit. PAISI is a logic one when a change in the path AIS state occurs. This bit is cleared when this register is read.

LOPI:

The LOPI bit is the loss of pointer interrupt status bit. LOPI is a logic one when a change in the LOP state occurs. This bit is cleared when this register is read.

PSLI:

The PSLI bit is the change of path signal label interrupt status bit. PSLI is a logic one when a change is detected in the path signal label register. The current path signal label can be read from the RPOP Path Signal Label register. This bit is cleared when this register is read.

Register 0x31 (EXTD=1): RPOP Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	ERDII	X

NOTE: To facilitate additional register mapping, shadow registers have been added to registers 0x30, 0x31 and 0x33. These shadow registers are accessed in the same way as the normal registers.

The EXTD (extend register) bit must be set in register 0x36 to allow switching between accessing the normal registers and the shadow registers

This register allows identification and acknowledgment of path level alarm and error event interrupts.

ERDII:

The ERDII bit is set to logic one when a change is detected in the received enhanced RDI state. ERDII is cleared when the RPOP Interrupt Status register is read.

Register 0x32: RPOP Pointer Interrupt Status

Bit	Type	Function	Default
Bit 7	R	ILLJREQI	X
Bit 6		Unused	X
Bit 5	R	DISCOPAI	X
Bit 4	R	INVNDFI	X
Bit 3	R	ILLPTRI	X
Bit 2	R	NSEI	X
Bit 1	R	PSEI	X
Bit 0	R	NDFI	X

This register allows identification and acknowledgment of pointer event interrupts.

NDFI:

The NDFI bit is the new data flag interrupt status bit. NDFI is set to a logic one when the NDF field is active in the received pointer (H1, H2). This bit is cleared when this register is read.

PSEI:

The PSEI bit is the positive stuff event interrupt status bit. PSEI is a logic one when a positive stuff event is detected in the received pointer (H1, H2). This bit is cleared when this register is read.

NSEI:

The NSEI bit is the negative stuff event interrupt status bit. NSEI is a logic one when a negative stuff event is detected in the received pointer (H1, H2). This bit is cleared when this register is read.

ILLPTRI:

The ILLPTRI bit is the illegal pointer interrupt status bit. ILLPTRI is a logic one when an illegal pointer value is detected. This bit is cleared when this register is read.

INVNDFI:

The INVNDFI bit is the illegal new data field value interrupt status bit. INVNDFI is a logic one when an illegal NDF field value is detected in the receive payload pointer. An illegal NDF field is any one of the following six values: 0x0, 0x3, 0x5, 0xA, 0xC, and 0xF. This bit is cleared when this register is read.

DISCOPAI:

The DISCOPAI bit is the discontinuous change of pointer interrupt status bit. DISCOPAI is a logic one when a new pointer value is validated without an accompanying NDF indication. This bit is cleared when this register is read.

ILLJREQI:

The ILLJREQI bit is the illegal justification request interrupt status bit. ILLJREQI is a logic one when the pointer interpreter detects an illegal pointer justification request event. This bit is cleared when this register is read.

Register 0x33 (EXTD=0): RPOP Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	PSLE	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	LOPE	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	PAISE	0
Bit 2	R/W	PRDIE	0
Bit 1	R/W	BIPEE	0
Bit 0	R/W	FEBEE	0

NOTE: To facilitate additional register mapping, shadow registers have been added to registers 0x30, 0x31 and 0x33. These shadow registers are accessed in the same way as the normal registers.

The EXTD (extend register) bit must be set in register 0x36 to allow switching between accessing the normal registers and the shadow registers

This register allows interrupt generation to be enabled for path level alarm and error events.

FEBEE:

The FEBEE bit is the interrupt enable for path FEBEs. When FEBEE is a logic one, an interrupt is generated when a path FEBE is detected.

BIPEE:

The BIPEE bit is the interrupt enable for path BIP-8 errors. When BIPEE is a logic one, an interrupt is generated when a B3 error is detected.

PRDIE:

The PRDIE bit is the interrupt enable for path RDI. When PRDIE is a logic one, an interrupt is generated when the path RDI state changes.

PAISE:

The PAISE bit is the interrupt enable for path AIS. When PAISE is a logic one, an interrupt is generated when the path AIS state changes.

LOPE:

The LOPE bit is the interrupt enable for LOP. When LOPE is a logic one, an interrupt is generated when the LOP state changes.

PSLE:

The PSLE bit is the interrupt enable for changes in the received path signal label. When PSLE is a logic one, an interrupt is generated when the received C2 byte changes.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x33 (EXTD=1): RPOP Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	ERDIE	0

NOTE: To facilitate additional register mapping, shadow registers have been added to registers 0x30, 0x31 and 0x33. These shadow registers are accessed in the same way as the normal registers.

The EXTD (extend register) bit must be set in register 0x36 to allow switching between accessing the normal registers and the shadow registers

This register allows interrupt generation to be enabled for path level alarm and error events.

ERDIE:

When EREDIE is a logic one, an interrupt is generated when a path Enhanced RDI is detected.

Register 0x34: RPOP Pointer Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	ILLJREQE	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	DISCOPAE	0
Bit 4	R/W	INVNDFE	0
Bit 3	R/W	ILLPTRE	0
Bit 2	R/W	NSEE	0
Bit 1	R/W	PSEE	0
Bit 0	R/W	NDFE	0

This register is used to enable pointer event interrupts.

NDFE:

When a logic one is written to the NDFE interrupt enable bit position, a change in active offset due to the reception of an enabled NDF (NDF_enabled indication) will activate the interrupt out, INTB.

PSEE:

When a logic one is written to the PSEE interrupt enable bit position, a positive pointer adjustment event will active the interrupt output, INTB.

NSEE:

When a logic one is written to the NSEE interrupt enable bit position, a negative pointer adjustment event will activate the interrupt output, INTB.

ILLPTRE:

When a logic one is written to the ILLPTRE interrupt enable bit position, an illegal pointer will activate the interrupt output, INTB.

INVNDFE:

When a logic one is written to the INVNDFE interrupt enable bit position, an invalid NDF code will activate the interrupt output, INTB.

DISCOPAE:

When a logic one is written to the DISCOPAE interrupt enable bit position, a change of pointer alignment event will activate the interrupt output, INTB.

ILLJREQE:

When a logic one is written tot he ILLJREQE interrupt enable bit position, an illegal pointer justification request will activate the interrupt output, INTB.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x35: RPOP Pointer LSB

Bit	Type	Function	Default
Bit 7	R	PTR[7]	X
Bit 6	R	PTR[6]	X
Bit 5	R	PTR[5]	X
Bit 4	R	PTR[4]	X
Bit 3	R	PTR[3]	X
Bit 2	R	PTR[2]	X
Bit 1	R	PTR[1]	X
Bit 0	R	PTR[0]	X

PTR[7:0]:

The PTR[7:0] bits contain the eight LSBs of the current pointer value that is interpreted from the H1 and H2 bytes. The NDFI, NSEI and PSEI bits of the RPOP Pointer Interrupt Status register should be read before and after reading this register to ensure that the pointer value did not change during the register read.

Register 0x36: RPOP Pointer MSB and RDI Filter Control

Bit	Type	Function	Default
Bit 7	R/W	NDFPOR	0
Bit 6	R/W	EXTD	0
Bit 5	R/W	RDI10	0
Bit 4		Unused	X
Bit 3	R	S1	X
Bit 2	R	S0	X
Bit 1	R	PTR[9]	X
Bit 0	R	PTR[8]	X

PTR[9:8]:

The PTR[9:8] bits contain the two MSBs of the current pointer value that is interpreted from the H1 and H2 bytes. The NDFI, NSEI and PSEI bits of the RPOP Pointer Interrupt Status register should be read before and after reading this register to ensure that the pointer value did not change during the register read.

S0, S1:

The S0 and S1 bits contain the two S bits received in the last H1 byte. These bits should be software debounced by reading this register at least twice.

RDI10:

The RDI10 bit controls the filtering of the remote defect indication and the auxiliary remote defect indication. When RDI10 is a logic one, the PRDI and APRDI status is updated when the same value is received in the corresponding bit of the G1 byte for ten consecutive frames. When RDI10 is a logic zero, the PRDI and APRDI status is updated when the same value is received for five consecutive frames.

NDFPOR:

The NDFPOR (new data flag pointer outside range) bit allows an NDF counter enable, if the pointer value is outside the range (0-782). If this bit is set to logic one the definition for NDF counter enable is enabled NDF + ss. If this bit is set to logic zero the definition for NDF counter enable is enabled NDF + ss + offset in the range of 0 to 782. Note that this bit only allows the NDF counter to count towards LOP when the pointer is out of range, no active offset change will occur.

EXTD:

The EXTD bit extends the registers to facilitate additional mapping. If this bit is set to logic one the register mapping, for registers 0x30, 0x31 and 0x33, are extended.

Register 0x37: RPOP Path Signal Label

Bit	Type	Function	Default
Bit 7	R	PSL[7]	X
Bit 6	R	PSL[6]	X
Bit 5	R	PSL[5]	X
Bit 4	R	PSL[4]	X
Bit 3	R	PSL[3]	X
Bit 2	R	PSL[2]	X
Bit 1	R	PSL[1]	X
Bit 0	R	PSL[0]	X

PSL[7:0]:

The PSL[7:0] bits contain the path signal label byte (C2). The value in this register is updated to a new path signal label value if the same new value is observed for three or five consecutive frames, depending on the status of the PSL5 bit.

Register 0x38: RPOP Path BIP-8 LSB

Bit	Type	Function	Default
Bit 7	R	PBE[7]	X
Bit 6	R	PBE[6]	X
Bit 5	R	PBE[5]	X
Bit 4	R	PBE[4]	X
Bit 3	R	PBE[3]	X
Bit 2	R	PBE[2]	X
Bit 1	R	PBE[1]	X
Bit 0	R	PBE[0]	X

Register 0x39: RPOP Path BIP-8 MSB

Bit	Type	Function	Default
Bit 7	R	PBE[15]	X
Bit 6	R	PBE[14]	X
Bit 5	R	PBE[13]	X
Bit 4	R	PBE[12]	X
Bit 3	R	PBE[11]	X
Bit 2	R	PBE[10]	X
Bit 1	R	PBE[9]	X
Bit 0	R	PBE[8]	X

PBE[15:0]:

PBE[15:0] represent the number of B3 errors (individual or block) that have been detected since the last time the error count was polled. The error count is polled by writing to either of the RPOP Path BIP-8 Register addresses or to either of the RPOP Path FEBE Register addresses. Such a write transfers the internally accumulated error count to the Path BIP-8 registers within a maximum of 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

The count can also be polled by writing to the S/UNI-QUAD Channel Reset and Monitoring Update register (0x05).

Register 0x3A: RPOP Path FEBE LSB

Bit	Type	Function	Default
Bit 7	R	PFE[7]	X
Bit 6	R	PFE[6]	X
Bit 5	R	PFE[5]	X
Bit 4	R	PFE[4]	X
Bit 3	R	PFE[3]	X
Bit 2	R	PFE[2]	X
Bit 1	R	PFE[1]	X
Bit 0	R	PFE[0]	X

Register 0x3B: RPOP Path FEBE MSB

Bit	Type	Function	Default
Bit 7	R	PFE[15]	X
Bit 6	R	PFE[14]	X
Bit 5	R	PFE[13]	X
Bit 4	R	PFE[12]	X
Bit 3	R	PFE[11]	X
Bit 2	R	PFE[10]	X
Bit 1	R	PFE[9]	X
Bit 0	R	PFE[8]	X

These registers allow path FEBEs to be accumulated.

PFE[15:0]:

PFE[15:0] represent the number of path FEBE errors (G1) that have been detected since the last time the error count was polled. The error count is polled by writing to either of the RPOP Path BIP-8 Register addresses or to either of the RPOP Path FEBE Register addresses. Such a write transfers the internally accumulated error count to the Path FEBE Registers within a maximum of 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

The count can also be polled by writing to the S/UNI-QUAD Channel Reset and Monitoring Update register (0x05).

Register 0x3C: RPOP Auxiliary RDI

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	BLKFEBE	0
Bit 3		Unused	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	APRDIE	0
Bit 0	R	APRDIV	X

APRDIE:

The APRDIE bit is the interrupt enable for auxiliary path RDI. When APRDIE is a logic one, an interrupt is generated when the auxiliary path RDI state changes.

APRDIV:

The APRDIV bit is read to determine the auxiliary path RDI state. When APRDIV is a logic one, the S/UNI-QUAD has declared auxiliary path RDI.

BLKFEBE:

When set to logic one, the block FEBE bitg (BLKFEBE) causes path FEBE errors to be reported and accumulated on a block basis. A single path FEBE error is accumulated for a block if the received FEBE code for that block is between 1 and 8 inclusive. When BLKFEBE is set low, path FEBE errors are accumulated on an error basis.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x3D: RPOP Error Event Control

Bit	Type	Function	Default
Bit 7	R/W	SOS	0
Bit 6	R/W	ENSS	0
Bit 5	R/W	BLKBIP	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	BLKBIPO	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

This register contains error event control bits.

BLKBIPO:

When BLKBIPO is a logic one, path FEBE indications are generated on a block basis. A single FEBE is transmitted if one or more path B3 error indications are detected per frame. When BLKBIPO is a logic zero, the transmitted FEBE indicates the number of B3 errors detected (between 0 and 8 errors per frame).

BLKBIP:

When BLKBIP is a logic one, B3 errors are reported and accumulated on a block basis. A single B3 error is accumulated and reported to the TPOP if one or more B3 errors are detected per frame. When BLKBIP is a logic zero, each B3 error is accumulated and reported.

ENSS:

The ENSS bit controls whether the SS bits in the payload pointer are included in the pointer interpreter state machine. When ENSS is a logic one, an incorrect SS bit pattern causes the pointer interpreter to enter the LOP (loss of pointer) state and prevents a new pointer indication. When ENSS is a logic zero, the SS bits are ignored by the pointer interpreter.

SOS:

The SOS controls the spacing between consecutive pointer justification events in the receive stream. When SOS is a logic one, the definition of inc_ind and dec_ind indications includes the requirement that active offset changes have occurred at least three frames ago. When SOS is a logic zero,

pointer justification indications in the receive stream are followed without regard to the proximity of previous active offset changes.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x40: TPOP Control/Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	EPRDIEN	0
Bit 5	R/W	EPRDISRC	0
Bit 4	R/W	PERSIST	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	DBIP8	0
Bit 0	R/W	Reserved	0

This register allows insertion of path level alarms and diagnostic signals.

DBIP8:

The DBIP8 bit controls the insertion of bit errors continuously in the B3 byte. When DBIP8 is a logic one, the B3 byte is inverted.

PERSIST

The path far end receive failure alarm persistence bit (PERSIST) controls the persistence of the RDI asserted into the transmit stream. When PERSIST is a logic one, the RDI code inserted into the transmit stream as a result of consequential actions is asserted for a minimum of 20 frames in non-enhanced RDI mode, or the last valid RDI code before an idle code (idle codes are when bits 5,6,7 are 000, 001, or 011) is asserted for 20 frames in enhanced RDI mode. When PERSIST is logic zero, the transmit RDI code changes immediately based on received alarm conditions.

EPRDISRC

The enhanced path receive defect indication alarm source bit (EPRDISRC) controls the source of RDI input to be inserted onto the G1 byte.. When EPRDIEN is logic zero, the extended RDI bits of the G1 byte not overwritten by the TPOP block, regardless of EPRDISRC. When EPRDIEN is logic one and EPRDISCR is logic zero, the extended RDI bits of the G1 byte, bits 6 and 7, are inserted according to the value in the G1[1:0] register bits (register 0x49). When EPRDIEN is logic one and EPRDISCR is logic one, the value register 0x49 G1[1:0] is ignored and the EPRDI bits in the G1 byte are set according to the setting of the Channel Auto Enhanced Path RDI Control registers (0x92 and 0x93).

EPRDIEN

The enhanced path receive defect indication alarm enable bit (EPRDIEN) controls the use of 3-bit RDI mode. When EPRDIEN is set to logic 0, the basic path RDI scheme is used and only G1[5] is used to indicate PRDI. When EPRDIEN is set to logic 1, the enhanced path RDI scheme is used and the three G1[7:5] bits are used to indicate PRDI. The actual three bit code will be controlled according to the EPRDISRC.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x41: TPOP Pointer Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	FTPTR	0
Bit 5	R/W	SOS	0
Bit 4	R/W	PLD	0
Bit 3	R/W	NDF	0
Bit 2	R/W	NSE	0
Bit 1	R/W	PSE	0
Bit 0	R/W	Reserved	0

This register allows control over the transmitted payload pointer for diagnostic purposes.

PSE:

The PSE bit controls the insertion of positive pointer movements. A logic zero to logic one transition on this bit enables the insertion of a single positive pointer justification in the transmit stream. This register bit is automatically cleared when the pointer movement is inserted.

NSE:

The NSE bit controls the insertion of negative pointer movements. A logic zero to logic one transition on this bit enables the insertion of a single negative pointer justification in the transmit stream. This register bit is automatically cleared when the pointer movement is inserted.

NDF:

The NDF bit controls the insertion of new data flags in the inserted payload pointer. When a logic one is written to this bit position, the pattern contained in the NDF[3:0] bit positions in the TPOP Arbitrary Pointer MSB Register is inserted continuously in the payload pointer. When a logic zero is written to this bit position, the normal pattern (0110) is inserted in the payload pointer.

PLD:

The PLD bit controls the loading of the pointer value contained in the TPOP Arbitrary Pointer Registers. Normally the TPOP Arbitrary Pointer Registers are written to set up the arbitrary new pointer value, the S-bit values, and the NDF pattern. A logic one is then written to this bit position to load the new pointer value. The new data flag bit positions are set to the programmed NDF

pattern for the first frame; subsequent frames have the new data flag bit positions set to the normal pattern (0110) unless the NDF bit described above is set to a logic one. This bit is automatically cleared after the new payload pointer is loaded.

Note: When loading an out of range pointer (that is a pointer with a value greater than 782), the TPOP continues to operate with timing based on the last valid pointer value. The out of range pointer value is inserted in the transmit stream. Although a valid SPE will continue to be generated, it is unlikely to be extracted by downstream circuitry which should be in a loss of pointer state.

SOS:

The SOS bit controls the stuff opportunity spacing between consecutive SPE positive or negative stuff events. When SOS is a logic zero, stuff events may be generated every frame as controlled by the PSE and NSE register bits described above. When SOS is a logic one, stuff events may be generated at a maximum rate of once every four frames.

FTPTR:

The force transient pointer bit (FTPTR) enables the insertion of the pointer value contained in the Arbitrary Pointer Registers into the transmit stream for diagnostic purposes. When FTPTR is a logic one, the APTR[9:0] bits of the Arbitrary Pointer Registers are inserted into the H1 and H2 bytes of the transmit stream. At least one corrupted pointer is guaranteed to be sent. When FTPTR is a logic zero, the pointer value in the Current Pointer registers is inserted in the transmit stream.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x43: TPOP Current Pointer LSB

Bit	Type	Function	Default
Bit 7	R	CPTR[7]	X
Bit 6	R	CPTR[6]	X
Bit 5	R	CPTR[5]	X
Bit 4	R	CPTR[4]	X
Bit 3	R	CPTR[3]	X
Bit 2	R	CPTR[2]	X
Bit 1	R	CPTR[1]	X
Bit 0	R	CPTR[0]	X

CPTR[7:0]:

The CPTR[7:0] bits, along with the CPTR[9:8] bits in the TPOP Current Pointer MSB Register reflect the value of the current payload pointer being inserted in the transmit stream. The value may be changed by loading a new pointer value using the TPOP Arbitrary Pointer LSB and MSB Registers, or by inserting positive and negative pointer movements using the PSE and NSE register bits.

Register 0x44: TPOP Current Pointer MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	CPTR[9]	X
Bit 0	R	CPTR[8]	X

CPTR[9:8]:

The CPTR[9:8] bits, along with the CPTR[7:0] bits in the TPOP Current Pointer LSB Register reflect the value of the current payload pointer being inserted in the transmit stream. The value may be changed by loading a new pointer value using the TPOP Arbitrary Pointer LSB and MSB Registers, or by inserting positive and negative pointer movements using the PSE and NSE register bits.

It is recommended the CPTR[9:0] value be software de-bounced to ensure a correct value is received.

Register 0x45: TPOP Arbitrary Pointer LSB

Bit	Type	Function	Default
Bit 7	R/W	APTR[7]	0
Bit 6	R/W	APTR[6]	0
Bit 5	R/W	APTR[5]	0
Bit 4	R/W	APTR[4]	0
Bit 3	R/W	APTR[3]	0
Bit 2	R/W	APTR[2]	0
Bit 1	R/W	APTR[1]	0
Bit 0	R/W	APTR[0]	0

This register allows an arbitrary pointer to be inserted for diagnostic purposes.

APTR[7:0]:

The APTR[7:0] bits, along with the APTR[9:8] bits in the TPOP Arbitrary Pointer MSB Register are used to set an arbitrary payload pointer value. The arbitrary pointer value is inserted in the transmit stream by writing a logic one to the PLD bit in the TPOP Pointer Control Register.

If the FTPTR bit in the TPOP Pointer Control register is a logic one, the current APTR[9:0] value is inserted into the payload pointer bytes (H1 and H2) in the transmit stream.

Register 0x46: TPOP Arbitrary Pointer MSB

Bit	Type	Function	Default
Bit 7	R/W	NDF[3]	1
Bit 6	R/W	NDF[2]	0
Bit 5	R/W	NDF[1]	0
Bit 4	R/W	NDF[0]	1
Bit 3	R/W	S[1]	1
Bit 2	R/W	S[0]	0
Bit 1	R/W	APTR[9]	0
Bit 0	R/W	APTR[8]	0

This register allows an arbitrary pointer to be inserted for diagnostic purposes.

APTR[9:8]:

The APTR[9:8] bits, along with the APTR[7:0] bits in the TPOP Arbitrary Pointer LSB Register are used to set an arbitrary payload pointer value. The arbitrary pointer value is inserted in the transmit stream by writing a logic one to the PLD bit in the TPOP Pointer Control Register.

If the FTPTR bit in the TPOP Pointer Control register is a logic one, the current APTR[9:0] value is inserted into the payload pointer bytes (H1 and H2) in the transmit stream.

S[1], S[0]:

The S[1:0] bits contain the value inserted in the S[1:0] bit positions (also referred to as the unused bits) in the payload pointer.

NDF[3:0]:

The NDF[3:0] bits contain the value inserted in the NDF bit positions when an arbitrary new payload pointer value is inserted (using the PLD bit in the TPOP Pointer Control Register) or when new data flag generation is enabled using primary input NDF, or the NDF bit in the TPOP Pointer Control Register.

Register 0x48: TPOP Path Signal Label

Bit	Type	Function	Default
Bit 7	R/W	C2[7]	0
Bit 6	R/W	C2[6]	0
Bit 5	R/W	C2[5]	0
Bit 4	R/W	C2[4]	0
Bit 3	R/W	C2[3]	0
Bit 2	R/W	C2[2]	0
Bit 1	R/W	C2[1]	0
Bit 0	R/W	C2[0]	1

This register allows control over the path signal label. Upon reset the register defaults to 0x01, which signifies an equipped but not specific payload. This register should be reprogrammmed with the value 0x13 for Asynchronous Transfer Mode (ATM) mode.

C2[7:0]:

The C2[7:0] bits are inserted in the C2 byte position in the transmit stream. . Upon reset the register defaults to 0x01, which signifies an equipped but not specific payload. This register should be reprogrammed with the value 0x13 when in Asynchronous Transfer Mode (ATM) mode.

Register 0x49: TPOP Path Status

Bit	Type	Function	Default
Bit 7	R/W	FEBE[3]	0
Bit 6	R/W	FEBE[2]	0
Bit 5	R/W	FEBE[1]	0
Bit 4	R/W	FEBE[0]	0
Bit 3	R/W	PRDI	0
Bit 2	R/W	APRDI	0
Bit 1	R/W	G1[1]	0
Bit 0	R/W	G1[0]	0

This register allows control over the path status byte.

G[1:0]:

The G1[1:0] bits are inserted in bits 1 and 2 of the path status byte G1. These bits are ignored when EPRDIEN is logic zero or when EPRDIEN and EPRDISRC are both logic one. See the description of EPRDIEN and EPRDISRC for more details on how G1 can be controlled.

APRDI

The APRDI bit controls the insertion of the auxiliary path remote defect indication. When APRDI is a logic one, the APRDI bit position in the path status byte is set high. When APRDI is a logic zero, the APRDI bit position in the path status byte is set low.

PRDI:

The PRDI bit controls the insertion of the path remote defect indication. When a logic one is written to this bit position, the PRDI bit position in the path status byte is set high. When a logic zero is written to this bit position, the PRDI bit position in the path status byte is set low. This bit is ignored when EPRDIEN is logic zero or when EPRDIEN and EPRDISRC are both logic one and the PRDI bit in the G1 byte (bit 6) is set according to the setting of the Channel Auto Enhanced Path RDI Control registers (0x92 and 0x93).

FEBE[3:0]:

The FEBE[3:0] bits are inserted in the FEBE bit positions in the path status byte. The value contained in FEBE[3:0] is cleared after being inserted in the

path status byte. Any non-zero FEBE value overwrites the value that would normally have been inserted based on the number of receive B3 errors during the last frame. When reading this register, a non-zero value in these bit positions indicates that the insertion of this value is still pending.

Register 0x60: RXCP Configuration 1

Bit	Type	Function	Default
Bit 7	R/W	DDSCR	0
Bit 6	R/W	Reserved	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	HCSADD	1
Bit 1	R/W	Reserved	0
Bit 0	R/W	DISCOR	0

DISCOR:

The DISCOR bit controls the HCS error correction algorithm. When DISCOR is a logic zero, the error correction algorithm is enabled, and single-bit errors detected in the cell header are corrected. When DISCOR is a logic one, the error correction algorithm is disabled, and any error detected in the cell header is treated as an uncorrectable HCS error.

HCSADD:

The HCSADD bit controls the addition of the coset polynomial, $x^6+x^4+x^2+1$, to the HCS octet prior to comparison. When HCSADD is a logic one, the polynomial is added, and the resulting HCS is compared. When HCSADD is a logic zero, the polynomial is not added, and the unmodified HCS is compared.

DDSCR:

The DDSCR bit controls the de-scrambling of the cell payload with the polynomial $x^{43} + 1$. When DDSCR is set to logic one, cell payload de-scrambling is disabled. When DDSCR is set to logic zero, payload de-scrambling is enabled.

Register 0x61: RXCP Configuration 2

Bit	Type	Function	Default
Bit 7	R/W	CCDIS	0
Bit 6	R/W	HCSPASS	0
Bit 5	R/W	IDLEPASS	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	HCSFTR[1]	0
Bit 0	R/W	HCSFTR[0]	0

HCSFTR[1:0]:

The HCS filter bits, HCSFTR[1:0] indicate the number of consecutive error-free cells required, while in detection mode, before reverting back to correction mode.

HCSFTR[1:0]	Cell Acceptance Threshold
00	One ATM cell with correct HCS before resumption of cell acceptance. This cell is accepted.
01	Two ATM cells with correct HCS before resumption of cell acceptance. The last cell is accepted.
10	Four ATM cells with correct HCS before resumption of cell acceptance. The last cell is accepted.
11	Eight ATM cells with correct HCS before resumption of cell acceptance. The last cell is accepted.

IDLEPASS:

The IDLEPASS bit controls the function of the Idle Cell filter. When IDLEPASS is written with a logic zero, all cells that match the Idle Cell Header Pattern and Idle Cell Header Mask are filtered out. When IDLEPASS is a logic one, the Idle Cell Header Pattern and Mask registers are ignored. The default state of this bit and the bits in the Idle Cell Header Mask and Idle Cell Header Pattern Registers enable the dropping of idle cells.

HCSPASS:

The HCSPASS bit controls the dropping of cells based on the detection of an uncorrectable HCS error. When HCSPASS is a logic zero, cells containing an uncorrectable HCS error are dropped. When HCSPASS is a logic one, cells are passed to the receive FIFO regardless of errors detected in the HCS. Additionally, the HCS verification finite state machine never exits the correction mode.

Regardless of the programming of this bit, cells are always dropped while the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states unless the CCDIS bit in this register is set to logic one.

CCDIS:

The CCDIS bit can be used to disable all cell filtering and cell delineation. All payload data read from the RXCP is passed into its FIFO without the requirement of having to find cell delineation first.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x62: RXCP FIFO/UTOPIA Control & Config

Bit	Type	Function	Default
Bit 7	R/W	RXPTYP	0
Bit 6		Unused	X
Bit 5	R/W	RCAINV	0
Bit 4	R/W	RCALEVEL0	1
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset the four-cell receive FIFO. When FIFORST is set to logic zero, the FIFO operates normally. When FIFORST is set to logic one, the FIFO is immediately emptied and ignores writes. The FIFO remains empty and continues to ignore writes until a logic zero is written to FIFORST.

RCALEVEL0:

The RCA (and DRCA[x]) level 0 bit, RCALEVEL0, determines what output RCA (and DRCA[x]) indicates when it transitions low. When RCALEVEL0 is set to logic one, a high-to-low transition on output DRCA[x] and RCA indicates that the receive FIFO is empty (DRCA[x] and RCA, if polled, will de-assert on the rising RFCLK edge after Payload word 24 is output. When RCALEVEL0 is set to logic zero, a high-to-low transition on output DRCA[x] and RCA, if polled, indicates that the receive FIFO is near empty. DRCA[x] and RCA, if polled, will de-assert on the rising RFCLK edge after Payload byte 19 is output.

RCAINV:

The RCAINV bit inverts the polarity of the DRCA[x] and RCA output signal. When RCAINV is a logic one, the polarity of DRCA[x] and RCA is inverted (DRCA[x] and RCA at logic zero means there is a receive cell available to be read). When RCAINV is a logic zero, the polarity of RCA and DRCA[x] is not inverted.

RXPTYP:

The RXPTYP bit selects even or odd parity for output RPRTY. When set to logic one, output RPRTY is the even parity bit for outputs RDAT[15:0]. When

RXPTYP is set to logic zero, RPRTY is the odd parity bit for outputs RDAT[15:0].

Register 0x63: RXCP Interrupt Enables and Counter Status

Bit	Type	Function	Default
Bit 7	R	XFERI	X
Bit 6	R	OVR	X
Bit 5		Unused	X
Bit 4	R/W	XFERE	0
Bit 3	R/W	OOCDE	0
Bit 2	R/W	HCSE	0
Bit 1	R/W	FOVRE	0
Bit 0	R/W	LCDE	0

LCDE:

The LCDE bit enables the generation of an interrupt due to a change in the LCD state. When LCDE is set to logic one, the interrupt is enabled.

FOVRE:

The FOVRE bit enables the generation of an interrupt due to a FIFO overrun error condition. When FOVRE is set to logic one, the interrupt is enabled.

HCSE:

The HCSE bit enables the generation of an interrupt due to the detection of a corrected or an uncorrected HCS error. When HCSE is set to logic one, the interrupt is enabled.

OOCDE:

The OOCDE bit enables the generation of an interrupt due to a change in cell delineation state. When OOCDE is set to logic one, the interrupt is enabled.

XFERE:

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the RXCP Count registers. When XFERE is set to logic one, the interrupt is enabled.

OVR:

The OVR bit is the overrun status of the RXCP Performance Monitoring Count registers. A logic one in this bit position indicates that a previous transfer (indicated by XFERI being logic one) has not been acknowledged before the next accumulation interval has occurred and that the contents of the RXCP

Count registers have been overwritten. OVR is set to logic zero when this register is read.

XFERI:

The XFERI bit indicates that a transfer of RXCP Performance Monitoring Count data has occurred. A logic one in this bit position indicates that the RXCP Count registers have been updated. This update is initiated by writing to one of the RXCP Count register locations or to the S/UNI-QUAD Identification, Master Reset, and Global Monitor Update register. XFERI is set to logic zero when this register is read.

Register 0x64: RXCP Status/Interrupt Status

Bit	Type	Function	Default
Bit 7	R	OOCDV	X
Bit 6	R	LCDV	X
Bit 5		Unused	X
Bit 4	R	OOCDI	X
Bit 3	R	CHCSI	X
Bit 2	R	UHCSI	X
Bit 1	R	FOVRI	X
Bit 0	R	LCDI	X

LCDI:

The LCDI bit is set high when there is a change in the loss of cell delineation (LCD) state. This bit is reset immediately after a read to this register.

FOVRI:

The FOVRI bit is set to logic one when a FIFO overrun occurs. This bit is reset immediately after a read to this register.

UHCSI:

The UHCSI bit is set high when an uncorrected HCS error is detected. This bit is reset immediately after a read to this register.

CHCSI:

The CHCSI bit is set high when a corrected HCS error is detected. This bit is reset immediately after a read to this register.

OOCDI:

The OOCDI bit is set high when the RXCP enters or exits the SYNC state. The OOCDV bit indicates whether the RXCP is in the SYNC state or not. The OOCDI bit is reset immediately after a read to this register.

LCDV:

The LCDV bit gives the Loss of Cell Delineation state. When LCD is logic one, an out of cell delineation (OCD) defect has persisted for the number of cells specified in the LCD Count Threshold register. When LCD is logic zero, no OCD has persisted for the number of cells specified in the LCD Count Threshold register. The cell time period can be varied by using the LCDC[7:0] register bits in the RXCP LCD Count Threshold register.

OOCDV:

The OOCDV bit indicates the cell delineation state. When OOCDV is high, the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states and is hunting for the cell boundaries. When OOCDV is low, the cell delineation state machine is in the 'SYNC' state and cells are passed through the receive FIFO.

Register 0x65: RXCP LCD Count Threshold (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	LCDC[10]	0
Bit 1	R/W	LCDC[9]	0
Bit 0	R/W	LCDC[8]	1

Register 0x66: RXCP LCD Count Threshold (LSB)

Bit	Type	Function	Default
Bit 7	R/W	LCDC[7]	0
Bit 6	R/W	LCDC[6]	1
Bit 5	R/W	LCDC[5]	1
Bit 4	R/W	LCDC[4]	0
Bit 3	R/W	LCDC[3]	1
Bit 2	R/W	LCDC[2]	0
Bit 1	R/W	LCDC[1]	0
Bit 0	R/W	LCDC[0]	0

LCDC[10:0]:

The LCDC[10:0] bits represent the number of consecutive cell periods the receive cell processor must be out of cell delineation before loss of cell delineation (LCD) is declared. Likewise, LCD is not de-asserted until receive cell processor is in cell delineation for the number of cell periods specified by LCDC[10:0].

The default value of LCD[10:0] is 360, which translates to an average cell period of 2.83 µs and a default LCD integration period of 1.02 ms.

Register 0x67: RXCP Idle Cell Header Pattern

Bit	Type	Function	Default
Bit 7	R/W	GFC[3]	0
Bit 6	R/W	GFC[2]	0
Bit 5	R/W	GFC[1]	0
Bit 4	R/W	GFC[0]	0
Bit 3	R/W	PTI[3]	0
Bit 2	R/W	PTI[2]	0
Bit 1	R/W	PTI[1]	0
Bit 0	R/W	CLP	1

GFC[3:0]:

The GFC[3:0] bits contain the pattern to match in the first, second, third, and fourth bits of the first octet of the 53-octet cell, in conjunction with the Idle Cell Header Mask Register. The IDLEPASS bit in the Configuration 2 Register must be set to logic zero to enable dropping of cells matching this pattern. Note that an all-zeros pattern must be present in the VPI and VCI fields of the idle or unassigned cell.

PTI[2:0]:

The PTI[2:0] bits contain the pattern to match in the fifth, sixth, and seventh bits of the fourth octet of the 53-octet cell, in conjunction with the Idle Cell Header Mask Register. The IDLEPASS bit in the Configuration 2 Register must be set to logic zero to enable dropping of cells matching this pattern.

CLP:

The CLP bit contains the pattern to match in the eighth bit of the fourth octet of the 53-octet cell, in conjunction with the Match Header Mask Register. The IDLEPASS bit in the RXCP Configuration 2 Register must be set to logic zero to enable dropping of cells matching this pattern.

Register 0x68: RXCP Idle Cell Header Mask

Bit	Type	Function	Default
Bit 7	R/W	MGFC[3]	1
Bit 6	R/W	MGFC[2]	1
Bit 5	R/W	MGFC[1]	1
Bit 4	R/W	MGFC[0]	1
Bit 3	R/W	MPTI2]	1
Bit 2	R/W	MPTI[1]	1
Bit 1	R/W	MPTI[0]	1
Bit 0	R/W	MCLP	1

MGFC[3:0]:

The MGFC[3:0] bits contain the mask pattern for the first, second, third, and fourth bits of the first octet of the 53-octet cell. This mask is applied to the Idle Cell Header Pattern Register to select the bits included in the cell filter. A logic one in any bit position enables the corresponding bit in the pattern register to be compared. A logic zero causes the masking of the corresponding bit.

MPTI[3:0]:

The MPTI[3:0] bits contain the mask pattern for the fifth, sixth, and seventh bits of the fourth octet of the 53-octet cell. This mask is applied to the Idle Cell Header Pattern Register to select the bits included in the cell filter. A logic one in any bit position enables the corresponding bit in the pattern register to be compared. A logic zero causes the masking of the corresponding bit.

MCLP:

The CLP bit contains the mask pattern for the eighth bit of the fourth octet of the 53-octet cell. This mask is applied to the Idle Cell Header Pattern Register to select the bits included in the cell filter. A logic one in this bit position enables the MCLP bit in the pattern register to be compared. A logic zero causes the masking of the MCLP bit.

Register 0x69: RXCP Corrected HCS Error Count

Bit	Type	Function	Default
Bit 7	R	CHCS[7]	X
Bit 6	R	CHCS[6]	X
Bit 5	R	CHCS[5]	X
Bit 4	R	CHCS[4]	X
Bit 3	R	CHCS[3]	X
Bit 2	R	CHCS[2]	X
Bit 1	R	CHCS[1]	X
Bit 0	R	CHCS[0]	X

CHCS[7:0]:

The CHCS[7:0] bits indicate the number of corrected HCS error events that occurred during the last accumulation interval. The contents of these registers are valid a maximum of 40 RCLK periods after a transfer is triggered by a write to one of RXCP's performance monitor counters or to the S/UNI-QUAD Channel Reset, and Monitoring Update register.

Register 0x6A: RXCP Uncorrected HCS Error Count

Bit	Type	Function	Default
Bit 7	R	UHCS[7]	X
Bit 6	R	UHCS[6]	X
Bit 5	R	UHCS[5]	X
Bit 4	R	UHCS[4]	X
Bit 3	R	UHCS[3]	X
Bit 2	R	UHCS[2]	X
Bit 1	R	UHCS[1]	X
Bit 0	R	UHCS[0]	X

UHCS[7:0]:

The UHCS[7:0] bits indicate the number of uncorrectable HCS error events that occurred during the last accumulation interval. The contents of these registers are valid a maximum of 40 RCLK periods after a transfer is triggered by a write to one of RXCP's performance monitor counters or to the S/UNI-QUAD Channel Reset and Monitoring Update register.

Register 0x6B: RXCP Receive Cell Counter (LSB)

Bit	Type	Function	Default
Bit 7	R	RCELL[7]	X
Bit 6	R	RCELL[6]	X
Bit 5	R	RCELL[5]	X
Bit 4	R	RCELL[4]	X
Bit 3	R	RCELL[3]	X
Bit 2	R	RCELL[2]	X
Bit 1	R	RCELL[1]	X
Bit 0	R	RCELL[0]	X

Register 0x6C: RXCP Receive Cell Counter

Bit	Type	Function	Default
Bit 7	R	RCELL[15]	X
Bit 6	R	RCELL[14]	X
Bit 5	R	RCELL[13]	X
Bit 4	R	RCELL[12]	X
Bit 3	R	RCELL[11]	X
Bit 2	R	RCELL[10]	X
Bit 1	R	RCELL[9]	X
Bit 0	R	RCELL[8]	X

Register 0x6D: RXCP Receive Cell Counter (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	RCELL[18]	X
Bit 1	R	RCELL[17]	X
Bit 0	R	RCELL[16]	X

RCELL[20:0]:

The RCELL[18:0] bits indicate the number of cells received and written into the receive FIFO during the last accumulation interval. Cells received and filtered due to HCS errors or Idle cell matches are not counted. The counter should be polled every second to avoid saturation. The contents of these registers are valid a maximum of 67 RCLK periods after a transfer is triggered

by a write to one of RXCP's performance monitor counters or to the S/UNI-QUAD Channel Reset and Monitoring Update register.

Register 0x6E: RXCP Idle Cell Counter (LSB)

Bit	Type	Function	Default
Bit 7	R	ICELL[7]	X
Bit 6	R	ICELL[6]	X
Bit 5	R	ICELL[5]	X
Bit 4	R	ICELL[4]	X
Bit 3	R	ICELL[3]	X
Bit 2	R	ICELL[2]	X
Bit 1	R	ICELL[1]	X
Bit 0	R	ICELL[0]	X

Register 0x6F: RXCP Idle Cell Counter

Bit	Type	Function	Default
Bit 7	R	ICELL[15]	X
Bit 6	R	ICELL[14]	X
Bit 5	R	ICELL[13]	X
Bit 4	R	ICELL[12]	X
Bit 3	R	ICELL[11]	X
Bit 2	R	ICELL[10]	X
Bit 1	R	ICELL[9]	X
Bit 0	R	ICELL[8]	X

Register 0x70: RXCP Idle Cell Counter (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	ICELL[18]	X
Bit 1	R	ICELL[17]	X
Bit 0	R	ICELL[16]	X

ICELL[18:0]:

The ICELL[18:0] bits indicate the number of idle cells received during the last accumulation interval. The counter should be polled every second to avoid saturation. The contents of these registers are valid a maximum of 67 RCLK periods after a transfer is triggered by a write to one of RXCP's performance monitor counters or to the S/UNI-QUAD's Channel Reset, and Monitoring Update register.

Register 0x80: TXCP Configuration 1

Bit	Type	Function	Default
Bit 7	R/W	TPTYP	0
Bit 6	R/W	TCALEVEL0	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	HCSB	0
Bit 2	R/W	HCSADD	1
Bit 1	R/W	DSCR	0
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset the four cell transmit FIFO. When FIFORST is set to logic zero, the FIFO operates normally. When FIFORST is set to logic one, the FIFO is immediately emptied and ignores writes. The FIFO remains empty and continues to ignore writes until a logic zero is written to FIFORST. Null/unassigned cells are transmitted until a subsequent cell is written to the FIFO.

DSCR:

The DSCR bit controls the scrambling of the cell payload. When DSCR is a logic one, cell payload scrambling is disabled. When DSCR is a logic zero, payload scrambling is enabled.

HCSADD:

The HCSADD bit controls the addition of the coset polynomial, $x^6+x^4+x^2+1$, to the HCS octet prior to insertion in the synchronous payload envelope. When HCSADD is a logic one, the polynomial is added, and the resulting HCS is inserted. When HCSADD is a logic zero, the polynomial is not added, and the unmodified HCS is inserted. HCSADD takes effect unconditionally regardless of whether a null/unassigned cell is being transmitted or whether the HCS octet was read from the FIFO.

HCSB:

The active low HCSB bit enables the internal generation and insertion of the HCS octet into the transmit cell stream. When HCSB is logic zero, the HCS is generated and inserted internally. If HCSB is logic one , then no HCS octet is inserted in the transmit data stream.

TCALEVEL0:

The active high TCA (and DTCA[x]) level 0 bit, TCALEVEL0 determines what output TCA (and DTCA[x]) indicates when it transitions low. When TCALEVEL0 is set to logic one, output TCA (and DTCA[x]) indicates that the transmit FIFO is full and can accept no more writes. When TCALEVEL0 is set to logic zero, output TCA (and DTCA[x]) indicates that the transmit FIFO is near full.

TPTYP:

The TPTYP bit selects even or odd parity for input TPRTY. When set to logic one, input TPRTY is the even parity bit for the TDAT input bus. When set to logic zero, input TPRTY is the odd parity bit for the TDAT input bus. Reserved

The reserved bits must be programmed to logic zero for proper operation.

Register 0x81: TXCP Configuration 2

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	TCAINV	0
Bit 3	R/W	FIFODP[1]	0
Bit 2	R/W	FIFODP[0]	0
Bit 1	R/W	DHCS	0
Bit 0	R/W	HCSCTLEB	0

HCSCTLEB:

The active low HCS control enable, HCSCTLEB bit enables the XORing of the HCS Control byte with the generated HCS. When set to logic zero, the HCS Control byte provided in the third word of the 27 word data structure is XORed with the generated HCS. When set to logic one, XORing is disabled and the HCS Control byte is ignored.

DHCS:

The DHCS bit controls the insertion of HCS errors for diagnostic purposes. When DHCS is set to logic one, the HCS octet is inverted prior to insertion in the synchronous payload envelope. DHCS takes effect unconditionally regardless of whether a null/unassigned cell is being transmitted or whether the HCS octet was read from the FIFO. DHCS occurs after any error insertion caused by the Control Byte in the 27-word data structure.

FIFODP[1:0]:

The FIFODP[1:0] bits determine the transmit FIFO cell depth at which TCA and DTCA[x] de-assert. FIFO depth control may be important in systems where the cell latency through the TXCP must be minimized. When the FIFO is filled to the specified depth, the transmit cell available signal, TCA (and DTCA[x]) is asserted. Note that regardless of what fill level FIFODP[1:0] is set to, the transmit cell processor can store 4 complete cells. The selectable FIFO cell depths are shown below:

FIFODP[1]	FIFODP[0]	FIFO DEPTH
0	0	4 cells
0	1	3 cells
1	0	2 cells
1	1	1 cell

TCAINV:

The TCAINV bit inverts the polarity of the TCA (and DTCA[x]) output signal. When TCAINV is a logic one, the polarity of TCA (and DTCA[x]) is inverted (TCA (and DTCA[x]) at logic zero means there is transmit cell space available to be written to). When TCAINV is a logic zero, the polarity of TCA (and DTCA[x]) is not inverted.

Register 0x82: TXCP Cell Count Status/Configuration Options

Bit	Type	Function	Default
Bit 7	R/W	XFERE	0
Bit 6	R	XFERI	X
Bit 5	R	OVR	X
Bit 4		Unused	X
Bit 3	R/W	Reserved	1
Bit 2	R/W	H4INSB	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

H4INSB:

The active low H4 insert enable, H4INSB, determines the contents of the H4 byte in the outgoing path overhead. If H4INSB is set to logic one, the H4 byte is set to the value of 00 hexadecimal. If H4INSB is set to logic zero, the H4 byte is set to the cell indicator offset value.

XFERI:

The XFERI bit indicates that a transfer of Transmit Cell Count data has occurred. A logic one in this bit position indicates that the Transmit Cell Count registers have been updated. This update is initiated by writing to one of the Transmit Cell Count register locations or to the S/UNI-QUAD Identification, Master Reset, and Global Monitor Update register. XFERI is set to logic zero when this register is read.

OVR:

The OVR bit is the overrun status of the Transmit Cell Count registers. A logic one in this bit position indicates that a previous transfer (indicated by XFERI being logic one) has not been acknowledged before the next accumulation interval has occurred and that the contents of the Transmit Cell Count registers have been overwritten. OVR is set to logic zero when this register is read.

XFERE:

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the Transmit Cell Count registers. When XFERE is set to logic one, the interrupt is enabled.

Reserved:

These bits should be set to their default values for proper operation

Register 0x83: TXCP Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R/W	TPRTYE	0
Bit 6	R/W	FOVRE	0
Bit 5	R/W	TSOCE	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	TPRTYI	X
Bit 1	R	FOVRI	X
Bit 0	R	TSOCI	X

TSOCI:

The TSOCI bit is set high when the TSOC input is sampled high during any position other than the first word of the selected data structure. The write address counter is reset to the first word of the data structure when TSOC is sampled high. This bit is reset immediately after a read to this register.

FOVRI:

The FOVRI bit is set high when an attempt is made to write into the FIFO when it is already full. This bit is reset immediately after a read to this register

TPRTYI:

The TPRTYI bit indicates if a parity error was detected on the TDAT input bus. When logic one, the TPRTYI bit indicates a parity error over the active TDAT bus. This bit is cleared when this register is read. Odd or even parity is selected using the TPTYPE bit.

TSOCE:

The TSOCE bit enables the generation of an interrupt when the TSOC input is sampled high during any position other than the first word of the selected data structure. When TSOCE is set to logic one, the interrupt is enabled.

FOVRE:

The FOVRE bit enables the generation of an interrupt due to an attempt to write the FIFO when it is already full. When FOVRE is set to logic one, the interrupt is enabled.

TPRTYE:

The TPRTYE bit enables transmit parity interrupts. When set to logic one, parity errors are indicated on INT and TPRTYI. When set to logic zero, parity errors are indicated using bit TPRTYI but are not indicated on output INT.

Register 0x84: TXCP Idle Cell Header Control

Bit	Type	Function	Default
Bit 7	R/W	GFC[3]	0
Bit 6	R/W	GFC[2]	0
Bit 5	R/W	GFC[1]	0
Bit 4	R/W	GFC[0]	0
Bit 3	R/W	PTI[2]	0
Bit 2	R/W	PTI[1]	0
Bit 1	R/W	PTI[0]	0
Bit 0	R/W	CLP	1

CLP:

The CLP bit contains the eighth bit position of the fourth octet of the idle/unassigned cell pattern. Cell rate decoupling is accomplished by transmitting idle cells when the TXCP detects that no outstanding cells exist in the transmit FIFO.

PTI[3:0]:

The PTI[3:0] bits contains the fifth, sixth, and seventh bit positions of the fourth octet of the idle/unassigned cell pattern. Idle cells are transmitted when the TXCP detects that no outstanding cells exist in the transmit FIFO.

GFC[3:0]:

The GFC[3:0] bits contain the first, second, third, and fourth bit positions of the first octet of the idle/unassigned cell pattern. Idle/unassigned cells are transmitted when the TXCP detects that no outstanding cells exist in the transmit FIFO. The all zeros pattern is transmitted in the VCI and VPI fields of the idle cell.

Register 0x85: TXCP Idle Cell Payload Control

Bit	Type	Function	Default
Bit 7	R/W	PAYLD[7]	0
Bit 6	R/W	PAYLD[6]	1
Bit 5	R/W	PAYLD[5]	1
Bit 4	R/W	PAYLD[4]	0
Bit 3	R/W	PAYLD[3]	1
Bit 2	R/W	PAYLD[2]	0
Bit 1	R/W	PAYLD[1]	1
Bit 0	R/W	PAYLD[0]	0

PAYLD[7:0]:

The PAYLD[7:0] bits contain the pattern inserted in the idle cell payload. Idle cells are inserted when the TXCP detects that the transmit FIFO contains no outstanding cells. PAYLD[7] is the most significant bit and is the first bit transmitted. PAYLD[0] is the least significant bit.

Register 0x86: TXCP Transmit Cell Count (LSB)

Bit	Type	Function	Default
Bit 7	R	TCELL[7]	X
Bit 6	R	TCELL[6]	X
Bit 5	R	TCELL[5]	X
Bit 4	R	TCELL[4]	X
Bit 3	R	TCELL[3]	X
Bit 2	R	TCELL[2]	X
Bit 1	R	TCELL[1]	X
Bit 0	R	TCELL[0]	X

Register 0x87: TXCP Transmit Cell Count

Bit	Type	Function	Default
Bit 7	R	TCELL[15]	X
Bit 6	R	TCELL[14]	X
Bit 5	R	TCELL[13]	X
Bit 4	R	TCELL[12]	X
Bit 3	R	TCELL[11]	X
Bit 2	R	TCELL[10]	X
Bit 1	R	TCELL[9]	X
Bit 0	R	TCELL[8]	X

Register 0x88: TXCP Transmit Cell Count (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	TCELL[18]	X
Bit 1	R	TCELL[17]	X
Bit 0	R	TCELL[16]	X

TCELL[18:0]:

The TCELL[18:0] bits indicate the number of cells read from the transmit FIFO and inserted into the transmission stream during the last accumulation interval. Idle cells inserted into the transmission stream are not counted.

A write to any one of the TXCP_50 Transmit Cell Counter registers or to the S/UNI-QUAD Channel Reset and Monitoring Update register (Register 0x05)

loads the registers with the current counter value and resets the internal 19 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Transmit Cell Counter registers. The counter should be polled every second to avoid saturating. The contents of these registers are valid after a maximum of 5 µs after a transfer is triggered by a write to a TXCP_50 Transmit Cell count Register or the S/UNI-QUAD Channel Reset and Monitoring Update register (Register 0x05).

Register 0x90: S/UNI-QUAD Channel Auto Line RDI Control

Bit	Type	Function	Default
Bit 7	R/W	SDLRDI	0
Bit 6	R/W	SFLRDI	0
Bit 5	R/W	LOFLRDI	1
Bit 4	R/W	LOSLRDI	1
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	LAISLRDI	1
Bit 0		Unused	X

This register controls the auto assertion of line RDI in the local TLOP. Since the S/UNI-QUAD provides STS-3c (STM-1/AU4) mappings, this register controls the assertion of line RDI for the entire SONET/SDH stream.

LAISLRDI:

The Line Alarm Indication Signal LRDI (LAISLRDI) controls the insertion of a Line RDI in the transmit data stream upon detection of this alarm condition. When LAISLRDI is set to logic one, the transmit line RDI will be inserted. When LAISLRDI is set to logic zero, no action is taken. This register bit has effect only if the AUTOLRDI register bit is also set to logic one.

LOSLRDI:

The Loss of Signal LRDI (LOSLRDI) controls the insertion of a Line RDI in the transmit data stream upon detection of this alarm condition. When LOSLRDI is set to logic one, the transmit line RDI will be inserted. When LOSLRDI is set to logic zero, no action is taken. This register bit has effect only if the AUTOLRDI register bit is also set to logic one.

LOFLRDI:

The Loss of Frame LRDI (LOFLRDI) controls the insertion of a Line RDI in the transmit data stream upon detection of this alarm condition. When LOFLRDI is set to logic one, the transmit line RDI will be inserted. When LOFLRDI is set to logic zero, no action is taken. This register bit has effect only if the AUTOLRDI register bit is also set to logic one.

SFLRDI:

The Signal Fail BER LRDI (SFLRDI) controls the insertion of a Line RDI in the transmit data stream upon detection of this alarm condition. When SFLRDI is set to logic one, the transmit line RDI will be inserted. When SFLRDI is set to

logic zero, no action is taken. This register bit has effect only if the AUTOLRDI register bit is also set to logic one.

SDLRDI:

The Signal Degrade BER LRDI (SDLRDI) controls the insertion of a Line RDI in the transmit data stream upon detection of this alarm condition. When SDLRDI is set to logic one, the transmit line RDI will be inserted. When SDLRDI is set to logic zero, no action is taken. This register bit has effect only if the AUTOLRDI register bit is also set to logic one.

Register 0x91: S/UNI-QUAD Channel Auto Path RDI Control

Bit	Type	Function	Default
Bit 7	R/W	LCDPRDI	0
Bit 6	R/W	ALRMPRDI	0
Bit 5	R/W	PAISPRDI	1
Bit 4	R/W	Reserved	1
Bit 3	R/W	LOPPRDI	1
Bit 2	R/W	LOPCONPRDI	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

This register controls the auto assertion of path RDI (G1 bit 5) in the local TPOP. Since the S/UNI-QUAD provides STS-3c (STM-1/AU4) mappings, this register controls the assertion of path RDI for the entire SONET/SDH stream. See also the S/UNI-QUAD Channel Auto Enhanced Path RDI register.

LOPCONPRDI:

The Loss of Pointer Concatenation Indication PRDI (LOPCONPRDI) controls the insertion of a Path RDI in the transmit data stream upon detection of this alarm condition. When LOPCONPRDI is set to logic one, the transmit line RDI will be inserted. When LOPCONPRDI is set to logic zero, no action is taken. This register bit has effect only if the AUTOPRDI register bit is also set to logic one.

LOPPRDI:

The Loss of Pointer PRDI (LOPPRDI) controls the insertion of a Path RDI in the transmit data stream upon detection of this alarm condition. When LOPPRDI is set to logic one, the transmit line RDI will be inserted. When LOPPRDI is set to logic zero, no action is taken. This register bit has effect only if the AUTOPRDI register bit is also set to logic one.

PAISPRDI:

The Path Alarm Indication Signal PRDI (PAISPRDI) controls the insertion of a Path RDI in the transmit data stream upon detection of this alarm condition. When PAISPRDI is set to logic one, the transmit line RDI will be inserted. When PAISPRDI is set to logic zero, no action is taken. This register bit has effect only if the AUTOPRDI register bit is also set to logic one.

ALRMPRDI:

The Line Alarm Indication Signal PRDI (ALRMPRDI) controls the insertion of a Path RDI in the transmit data stream upon detection of one of the following alarm conditions: Loss of Signal (LOS), Loss of Frame (LOF) and Line Alarm Indication Signal (LAIS). When ALRMPRDI is set to logic one, the transmit line RDI will be inserted. When ALRMPRDI is set to logic zero, no action is taken. This register bit has effect only if the AUTOPRDI register bit is also set to logic one.

LCDPRDI

The Loss of ATM Cell Delineation Signal PRDI (LCDPRDI) controls the insertion of Path RDI in the transmit data stream upon detection of this alarm. When LCDPRDI is set to logic zero, no action is taken. This register bit is used only if the AUTOPRDI register bit is also set to logic one.

Register 0x92: S/UNI-QUAD Channel Auto Enhanced Path RDI Control

Bit	Type	Function	Default
Bit 7	R/W	LCDEPRDI	0
Bit 6	R/W	NOALMEPRDI	0
Bit 5	R/W	NOPAISEPRDI	0
Bit 4	R/W	PSLMEPRDI	1
Bit 3	R/W	NOLOPEPRDI	0
Bit 2	R/W	NOLOPCONEPRDI	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	1

This register and the S/UNI-QUAD Channel Auto Path RDI Control register controls the auto assertion of enhanced path RDI (G1 bits 5,6,7) in the local TPOP. Since the S/UNI-QUAD provides a STS-3c (STM-1) mapping, this register with its companion register controls auto enhanced path RDI assertion on the entire transmit stream.

NOLOPCONEPRDI:

When set high, the NOLOPCONEPRDI bit disables enhanced path RDI assertion when loss of pointer concatenation (LOPCON) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte is set low while bit 7 of the G1 byte is set high. NOLOPCONEPRDI has precedence over PSLMERDI and UNEQERDI.

When NOLOPCONEPRDI is set low, reporting of enhanced RDI is according to PSLMERDI and UNEQERDI and the associated alarm states.

NOLOPEPRDI:

When set high, the NOLOPEPRDI bit disables enhanced path RDI assertion when loss of pointer (LOP) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte is set low while bit 7 of the G1 byte is set high. NOLOPEPRDI has precedence over PSLMERDI and UNEQERDI.

When NOLOPEPRDI is set low, reporting of enhanced RDI is according to PSLMERDI and UNEQERDI and the associated alarm states.

PSLMEPRDI:

When set high, the PSLMEPRDI bit enables enhanced path RDI assertion when path signal label mismatch (PSLM) events are detected in the receive

stream. If enabled, when the event occurs, bit 6 of the G1 byte is set high while bit 7 of the G1 byte is set low.

When PSLMEPRDI is set low, path signal label mismatch events have no effect on path RDI. In addition, this bit has no effect when EPRDI_EN is set low.

NOPAISEPRDI:

When set high, the NOPAISEPRDI bit disables enhanced path RDI assertion when the path alarm indication signal state (PAIS) is detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte is set low while bit 7 of the G1 byte is set high. NOPAISEPRDI has precedence over PSLMERDI and UNEQERDI.

When NOPAISEPRDI is set low, reporting of enhanced RDI is according to PSLMERDI and UNEQERDI and the associated alarm states.

NOALMEPRDI:

When set high, the NOALMEPRDI bit disables enhanced path RDI assertion when loss of signal (LOS), loss of frame (LOF) or line alarm indication signal (LAIS) events are detected in the receive stream. If enabled, when these events occurs, bit 6 of the G1 byte is set low while bit 7 of the G1 byte is set high. NOALMEPRDI has precedence over PSLMERDI and UNEQERDI.

When NOALMEPRDI is set low, reporting of enhanced RDI is according to PSLMERDI and UNEQERDI and the associated alarm states.

LCDEPRDI:

When set high, the LCDEPRDI bit enables enhanced path RDI assertion when loss of cell delineation (LCD) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte is set high while bit 7 of the G1 byte is set low.

When LCDEPRDI is set low, loss of ATM cell delineation has no effect on path RDI. In addition, this bit has no effect when EPRDI_EN is set low.

Register 0x93: S/UNI-QUAD Channel Receive RDI and Enhanced RDI Control Extensions

Bit	Type	Function	Default
Bit 7	R/W	PAISCONPRDI	0
Bit 6	R/W	NOPAISCONEPRDI	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	W	EPRDI_EN	0
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

This register along with the S/UNI-QUAD Channel Path RDI Control register controls the auto assertion of path RDI on the TPOP transmit stream. This register along with the S/UNI-QUAD Channel Enhanced Path RDI Control register controls the auto assertion of enhanced path RDI on the TPOP transmit stream.

Since the S/UNI-QUAD provides STS-3c (STM-1) mapping, this register controls the entire SONET/SDH stream.

EPRDI_EN:

The EPRDI_EN bit enables the automatic insertion of enhanced RDI in the local transmitter. When EPRDI_EN is a logic one, auto insertion is enabled using the event enable bits in this register. When EPRDI_EN is a logic zero, enhanced path RDI is not automatically inserted in the transmit stream.

NOPAISCONEPRDI:

When set high, the NOPAISCONEPRDI bit disables enhanced path RDI assertion when path AIS concatenation (PAISCON) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte is set low while bit 7 of the G1 byte is set high. NOPAISCONEPRDI has precedence over PSLMERDI and UNEQERDI.

When NOPAISCONEPRDI is set low, reporting of enhanced RDI is according to PSLMERDI and UNEQERDI and the associated alarm states.

PAISCONPRDI:

When set high, the PAISCONPRDI bit enables path RDI assertion when path AIS concatenation (PAISCON) events are detected in the receive stream. When PAISCONPRDI is set low, path AIS concatenation events have no effect on path RDI.

Register 0x94: S/UNI-QUAD Channel Receive Line AIS Control

Bit	Type	Function	Default
Bit 7	R/W	SDINS	0
Bit 6	R/W	SFINS	0
Bit 5	R/W	LOFINS	1
Bit 4	R/W	LOSINS	1
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1		Unused	X
Bit 0	R/W	Reserved	0

LOSINS:

This bit is active only when the ALLONES bit in the RLOP Control/Status register is set high; it is ignored if the ALLONES bit is set low. The LOSINS bit enables the insertion of line AIS in the receive direction upon the declaration of loss of signal (LOS). If LOSINS is a logic one, line AIS is inserted into the SONET/SDH frame when LOS is declared. Line AIS is terminated when LOS is removed.

LOFINS:

This bit is active only when the ALLONES bit in the RLOP Control/Status register is set high; it is ignored if the ALLONES bit is set low. The LOFINS bit enables the insertion of line AIS in the receive direction upon the declaration of loss of frame (LOF). If LOSINS is a logic one, line AIS is inserted into the SONET/SDH frame when LOS is declared. Line AIS is terminated when LOS is removed.

SFINS:

This bit is active only when the ALLONES bit in the RLOP Control/Status register is set high; it is ignored if the ALLONES bit is set low. The SFINS bit enables the insertion of line AIS in the receive direction upon the declaration of signal fail (SF). If SFINS is a logic one, line AIS is inserted into the SONET/SDH frame when SF is declared. Line AIS is terminated when SF is removed.

SDINS:

This bit is active only when the ALLONES bit in the RLOP Control/Status register is set high; it is ignored if the ALLONES bit is set low. The SDINS bit enables the insertion of line AIS in the receive direction upon the declaration of signal degrade (SD). If SDINS is a logic one, line AIS is inserted into the

SONET/SDH frame when SD is declared. Line AIS is terminated when SD is removed.

Register 0x95: S/UNI-QUAD Channel Receive Path AIS Control

Bit	Type	Function	Default
Bit 7	R/W	PAISCONPAIS	1
Bit 6	R/W	LOPCONPAIS	1
Bit 5	R/W	Reserved	1
Bit 4	R/W	Reserved	1
Bit 3	R/W	LOPPAIS	1
Bit 2	R/W	PAISPAIS	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

This register controls the auto assertion of path AIS on the receive side of the system interface. AIS forces a loss of cell delineation.

PAISPAIS:

When set high, the PAISPAIS bit enables path AIS insertion when path AIS events are detected in the receive stream. When PAISPAIS is set low, path AIS events will not assert path AIS.

LOPPAIS:

When set high, the LOPPAIS bit enables path AIS insertion when loss of pointer (LOP) events are detected in the receive stream. When LOPPAIS is set low, loss of pointer events will not assert path AIS.

LOPCONPAIS:

When set high, the LOPCONPAIS bit enables path AIS insertion when loss of pointer concatenation (LOPCON) events are detected in the receive stream. When LOPCONPAIS is set low, loss of pointer concatenation events have will not assert path AIS.

PAISCONPAIS:

When set high, the PAISCONPAIS bit enables path AIS insertion when Path AIS concatenation (PAISCON) events are detected in the receive stream. When PAISCONPAIS is set low, Path AIS concatenation events will not assert path AIS.

Register 0x96: S/UNI-QUAD Channel Receive Alarm Control #1

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	PERDIEN	0
Bit 3	R/W	PRDIEN	0
Bit 2	R/W	PAISEN	0
Bit 1	R/W	LCDEN	0
Bit 0	R/W	LOPEN	0

Register 0x97: S/UNI-QUAD Channel Receive Alarm Control #2

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	SFBEREN	0
Bit 5	R/W	SDBEREN	0
Bit 4	R/W	LRDIEN	0
Bit 3	R/W	LAISEN	0
Bit 2	R/W	OOFEN	0
Bit 1	R/W	LOFEN	0
Bit 0	R/W	LOSEN	0

LOSEN, LOFEN, OOFEN, LAISEN, LRDIEN, SDBEREN, SFBEREN, LOPEN, LCDEN, PAISEN, PRDIEN, PERDIEN:

The above enable bits allow the corresponding alarm indications to be reported (Ored) into the RALRM output. When the enable bit is high, the corresponding alarm indication is combined with other alarm indications and output on RALRM. When the enable bit is low, the corresponding alarm indication does not affect the RALRM output.

Alarm	Description
LOS	Loss of signal
LOF	Loss of frame
OOF	Out of Frame
LAIS	Line Alarm Indication Signal
LRDI	Line Remote Defect Indication
SDBER	Signal Degrade Bit Error Rate
SFBER	Signal Fail Bit Error Rate
LOP	Loss of Pointer
LCD	Loss of cell delineation
PAIS	Path Alarm Indication Signal
PRDI	Path Remote Defect Indication
PERDI	Path Enhanced Remote Defect Indication
PSLM	Path Signal Label Mismatch

Register 0xE0: RASE Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	PSBFE	0
Bit 6	R/W	COAPSE	0
Bit 5	R/W	Z1/S1E	0
Bit 4	R/W	SFBERE	0
Bit 3	R/W	SDBERE	0
Bit 2	R/W	Unused	X
Bit 1	R/W	Unused	X
Bit 0	R/W	Unused	X

SDBERE:

The SDBERE bit is the interrupt enable for the signal degrade threshold alarm. When SDBERE is a logic one, an interrupt is generated when the SD alarm is declared or removed.

SFBERE:

The SFBERE bit is the interrupt enable for the signal fail threshold alarm. When SFBERE is a logic one, an interrupt is generated when the SF alarm is declared or removed.

Z1/S1E:

The Z1/S1 interrupt enable is an interrupt mask for changes in the received synchronization status. When Z1/S1E is a logic one, an interrupt is generated when a new synchronization status message is extracted into the Receive Z1/S1 register.

COAPSE:

The COAPS interrupt enable is an interrupt mask for changes in the received APS code. When COAPSE is a logic one, an interrupt is generated when a new K1/K2 code value is extracted into the RASE Receive K1 and RASE Receive K2 registers.

PSBFE:

The PSBF interrupt enable is an interrupt mask for protection switch byte failure alarms. When PSBFE is a logic one, an interrupt is generated when PSBF is declared or removed.

Register 0xE1: RASE Interrupt Status

Bit	Type	Function	Default
Bit 7	R	PSBFI	X
Bit 6	R	COAPSI	X
Bit 5	R	Z1/S1I	X
Bit 4	R	SFBERI	X
Bit 3	R	SDBERI	X
Bit 2	R	SFBERV	X
Bit 1	R	SDBERV	X
Bit 0	R	PSBFV	X

PSBFV:

The PSBFV bit indicates the protection switching byte failure alarm state. The alarm is declared (PSBFV is set high) when twelve successive frames have been received without three consecutive frames containing identical K1 bytes. The alarm is removed (PSBFV is set low) when three consecutive frames containing identical K1 bytes have been received.

SDBERV:

The SDBERV bit indicates the signal degrade threshold crossing alarm state. The alarm is declared (SDBERV is set high) when the bit error rate exceeds the threshold programmed in the RASE SD Declaring Threshold registers. The alarm is removed (SDBERV is set low) when the bit error rate is below the threshold programmed in the RASE SD Clearing Threshold registers.

SFBERV:

The SFBERV bit indicates the signal failure threshold crossing alarm state. The alarm is declared (SFBERV is set high) when the bit error rate exceeds the threshold programmed in the RASE SF Declaring Threshold registers. The alarm is removed (SFBERV is set low) when the bit error rate is below the threshold programmed in the RASE SF Clearing Threshold registers.

SDBERI:

The SDBERI bit is set high when the signal degrade threshold crossing alarm is declared or removed. This bit is cleared when the RASE Interrupt Status register is read.

SFBERI:

The SFBERI bit is set high when the signal failure threshold crossing alarm is declared or removed. This bit is cleared when the RASE Interrupt Status register is read.

Z1/S1I:

The Z1/S1I bit is set high when a new synchronization status message is extracted into the RASE Receive Z1/S1 register. This bit is cleared when the RASE Interrupt Status register is read.

COAPSI:

The COAPSI bit is set high when a new APS code value is extracted into the RASE Receive K1 and RASE Receive K2 registers. This bit is cleared when the RASE Interrupt Status register is read.

PSBFI:

The PSBFI bit is set high when the protection switching byte failure alarm is declared or removed. This bit is cleared when the RASE Interrupt Status register is read.

Register 0xE2: RASE Configuration/Control

Bit	Type	Function	Default
Bit 7	R/W	Z1/S1_CAP	0
Bit 6	R/W	SFBERTEN	0
Bit 5	R/W	SFSMODE	0
Bit 4	R/W	SFCMODE	0
Bit 3	R/W	SDBERTEN	0
Bit 2	R/W	SDSMODE	0
Bit 1	R/W	SDCMODE	0
Bit 0	R/W	Unused	X

SDCMODE:

The SDCMODE alarm bit selects the RASE window size to use for clearing the SD alarm. When SDCMODE is a logic zero the RASE clears the SD alarm using the same window size used for declaration. When SDCMODE is a logic one the RASE clears the SD alarm using a window size that is 8 times longer than the alarm declaration window size. The declaration window size is determined by the RASE SD Accumulation Period registers.

SDSMODE:

The SDSMODE bit selects the RASE saturation mode. When SDSMODE is a logic zero the RASE limits the number of B2 errors accumulated in one frame period to the RASE SD Saturation Threshold register value. When SDSMODE is a logic one the RASE limits the number of B2 errors accumulated in one window subtotal accumulation period to the RASE SD Saturation Threshold register value. Note that the number of frames in a window subtotal accumulation period is determined by the RASE SD Accumulation Period register value.

SDBERTEN:

The SDBERTEN bit selects automatic monitoring of line bit error rate threshold events by the RASE. When SDBERTEN is a logic one, the RASE continuously monitors line BIP errors over a period defined in the RASE configuration registers. When SDBERTEN is a logic zero, the RASE BIP accumulation logic is disabled, and the RASE logic is reset to the declaration monitoring state.

All RASE accumulation period and threshold registers should be set up before SDBERTEN is written.

SFCMODE:

The SFCMODE alarm bit selects the RASE window size to use for clearing the SF alarm. When SFCMODE is a logic zero the RASE clears the SF alarm using the same window size used for declaration. When SFCMODE is a logic one the RASE clears the SF alarm using a window size that is 8 times longer than the alarm declaration window size. The declaration window size is determined by the RASE SF Accumulation Period registers.

SFSMODE:

The SFSMODE bit selects the RASE saturation mode. When SFSMODE is a logic zero the RASE limits the number of B2 errors accumulated in one frame period to the RASE SF Saturation Threshold register value. When SFSMODE is a logic one the RASE limits the number of B2 errors accumulated in one window subtotal accumulation period to the RASE SF Saturation Threshold register value. Note that the number of frames in a window subtotal accumulation period is determined by the RASE SF Accumulation Period register value.

SFBERTEN:

The SFBERTEN bit enables automatic monitoring of line bit error rate threshold events by the RASE. When SFBERTEN is a logic one, the RASE continuously monitors line BIP errors over a period defined in the RASE configuration registers. When SFBERTEN is a logic zero, the RASE BIP accumulation logic is disabled, and the RASE logic is reset to the declaration monitoring state.

All RASE accumulation period and threshold registers should be set up before SFBERTEN is written.

Z1/S1_CAP:

The Z1/S1_CAP bit enables the Z1/S1 Capture algorithm. When Z1/S1_CAP is a logic one, the Z1/S1 clock synchronization status message nibble must have the same value for eight consecutive frames before writing the new value into the RASE Receive Z1/S1 register. When Z1/S1_CAP is logic zero, the Z1/S1 nibble value is written directly into the RASE Receive Z1/S1 register.

Register 0xE3: RASE SF Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SFSAP[7]	0
Bit 6	R/W	SFSAP[6]	0
Bit 5	R/W	SFSAP[5]	0
Bit 4	R/W	SFSAP[4]	0
Bit 3	R/W	SFSAP[3]	0
Bit 2	R/W	SFSAP[2]	0
Bit 1	R/W	SFSAP[1]	0
Bit 0	R/W	SFSAP[0]	0

Register 0xE4: RASE SF Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SFSAP[15]	0
Bit 6	R/W	SFSAP[14]	0
Bit 5	R/W	SFSAP[13]	0
Bit 4	R/W	SFSAP[12]	0
Bit 3	R/W	SFSAP[11]	0
Bit 2	R/W	SFSAP[10]	0
Bit 1	R/W	SFSAP[9]	0
Bit 0	R/W	SFSAP[8]	0

Register 0xE5: RASE SF Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SFSAP[23]	0
Bit 6	R/W	SFSAP[22]	0
Bit 5	R/W	SFSAP[21]	0
Bit 4	R/W	SFSAP[20]	0
Bit 3	R/W	SFSAP[19]	0
Bit 2	R/W	SFSAP[18]	0
Bit 1	R/W	SFSAP[17]	0
Bit 0	R/W	SFSAP[16]	0

SFSAP[23:0]:

The SFSAP[23:0] bits represent the number of 8 KHz frames used to accumulate the B2 error subtotal. The total evaluation window to declare the SF alarm is broken into 8 subtotals, so this register value represents 1/8 of the total sliding window size. Refer to the Operations section for recommended settings.

Register 0xE6: RASE SF Saturation Threshold

Bit	Type	Function	Default
Bit 7	R/W	SFSTH[7]	0
Bit 6	R/W	SFSTH[6]	0
Bit 5	R/W	SFSTH[5]	0
Bit 4	R/W	SFSTH[4]	0
Bit 3	R/W	SFSTH[3]	0
Bit 2	R/W	SFSTH[2]	0
Bit 1	R/W	SFSTH[1]	0
Bit 0	R/W	SFSTH[0]	0

Register 0xE7: RASE SF Saturation Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SFSTH[11]	0
Bit 2	R/W	SFSTH[10]	0
Bit 1	R/W	SFSTH[9]	0
Bit 0	R/W	SFSTH[8]	0

SFSTH[11:0]:

The SFSTH[11:0] value represents the allowable number of B2 errors that can be accumulated during an evaluation window before an SF threshold event is declared. Setting this threshold to 0xFFF disables the saturation functionality. Refer to the Operations section for the recommended settings.

Register 0xE8: RASE SF Declaring Threshold

Bit	Type	Function	Default
Bit 7	R/W	SFDTH[7]	0
Bit 6	R/W	SFDTH[6]	0
Bit 5	R/W	SFDTH[5]	0
Bit 4	R/W	SFDTH[4]	0
Bit 3	R/W	SFDTH[3]	0
Bit 2	R/W	SFDTH[2]	0
Bit 1	R/W	SFDTH[1]	0
Bit 0	R/W	SFDTH[0]	0

Register 0xE9: RASE SF Declaring Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SFDTH[11]	0
Bit 2	R/W	SFDTH[10]	0
Bit 1	R/W	SFDTH[9]	0
Bit 0	R/W	SFDTH[8]	0

SFDTH[11:0]:

The SFDTH[11:0] value determines the threshold for the declaration of the SF alarm. The SF alarm is declared when the number of B2 errors accumulated during an evaluation window is greater than or equal to the SFDTH[11:0] value. Refer to the Operations section for the recommended settings.

Register 0xEA: RASE SF Clearing Threshold

Bit	Type	Function	Default
Bit 7	R/W	SFCTH[7]	0
Bit 6	R/W	SFCTH[6]	0
Bit 5	R/W	SFCTH[5]	0
Bit 4	R/W	SFCTH[4]	0
Bit 3	R/W	SFCTH[3]	0
Bit 2	R/W	SFCTH[2]	0
Bit 1	R/W	SFCTH[1]	0
Bit 0	R/W	SFCTH[0]	0

Register 0xEB: RASE SF Clearing Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SFCTH[11]	0
Bit 2	R/W	SFCTH[10]	0
Bit 1	R/W	SFCTH[9]	0
Bit 0	R/W	SFCTH[8]	0

SFCTH[11:0]:

The SFCTH[11:0] value determines the threshold for the removal of the SF alarm. The SF alarm is removed when the number of B2 errors accumulated during an evaluation window is less than the SFCTH[11:0] value. Refer to the Operations section for the recommended settings.

Register 0xEC: RASE SD Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SDSAP[7]	0
Bit 6	R/W	SDSAP[6]	0
Bit 5	R/W	SDSAP[5]	0
Bit 4	R/W	SDSAP[4]	0
Bit 3	R/W	SDSAP[3]	0
Bit 2	R/W	SDSAP[2]	0
Bit 1	R/W	SDSAP[1]	0
Bit 0	R/W	SDSAP[0]	0

Register 0xED: RASE SD Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SDSAP[15]	0
Bit 6	R/W	SDSAP[14]	0
Bit 5	R/W	SDSAP[13]	0
Bit 4	R/W	SDSAP[12]	0
Bit 3	R/W	SDSAP[11]	0
Bit 2	R/W	SDSAP[10]	0
Bit 1	R/W	SDSAP[9]	0
Bit 0	R/W	SDSAP[8]	0

Register 0xEE: RASE SD Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SDSAP[23]	0
Bit 6	R/W	SDSAP[22]	0
Bit 5	R/W	SDSAP[21]	0
Bit 4	R/W	SDSAP[20]	0
Bit 3	R/W	SDSAP[19]	0
Bit 2	R/W	SDSAP[18]	0
Bit 1	R/W	SDSAP[17]	0
Bit 0	R/W	SDSAP[16]	0

SDSAP[23:0]:

The SDSAP[23:0] bits represent the number of 8 KHz frames used to accumulate the B2 error subtotal. The total evaluation window to declare the SD alarm is broken into 8 subtotals, so this register value represents 1/8 of the total sliding window size. Refer to the Operations section for recommended settings.

Register 0xEF: RASE SD Saturation Threshold

Bit	Type	Function	Default
Bit 7	R/W	SDSTH[7]	0
Bit 6	R/W	SDSTH[6]	0
Bit 5	R/W	SDSTH[5]	0
Bit 4	R/W	SDSTH[4]	0
Bit 3	R/W	SDSTH[3]	0
Bit 2	R/W	SDSTH[2]	0
Bit 1	R/W	SDSTH[1]	0
Bit 0	R/W	SDSTH[0]	0

Register 0xF0: RASE SD Saturation Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SDSTH[11]	0
Bit 2	R/W	SDSTH[10]	0
Bit 1	R/W	SDSTH[9]	0
Bit 0	R/W	SDSTH[8]	0

SDSTH[11:0]:

The SDSTH[11:0] value represents the allowable number of B2 errors that can be accumulated during an evaluation window before an SD threshold event is declared. Setting this threshold to 0xFFF disables the saturation functionality. Refer to the Operations section for the recommended settings.

Register 0xF1: RASE SD Declaring Threshold

Bit	Type	Function	Default
Bit 7	R/W	SDDTH[7]	0
Bit 6	R/W	SDDTH[6]	0
Bit 5	R/W	SDDTH[5]	0
Bit 4	R/W	SDDTH[4]	0
Bit 3	R/W	SDDTH[3]	0
Bit 2	R/W	SDDTH[2]	0
Bit 1	R/W	SDDTH[1]	0
Bit 0	R/W	SDDTH[0]	0

Register 0xF2: RASE SD Declaring Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SDDTH[11]	0
Bit 2	R/W	SDDTH[10]	0
Bit 1	R/W	SDDTH[9]	0
Bit 0	R/W	SDDTH[8]	0

SDDTH[11:0]:

The SDDTH[11:0] value determines the threshold for the declaration of the SD alarm. The SD alarm is declared when the number of B2 errors accumulated during an evaluation window is greater than or equal to the SDDTH[11:0] value. Refer to the Operations section for the recommended settings.

Register 0xF3: RASE SD Clearing Threshold

Bit	Type	Function	Default
Bit 7	R/W	SDCTH[7]	0
Bit 6	R/W	SDCTH[6]	0
Bit 5	R/W	SDCTH[5]	0
Bit 4	R/W	SDCTH[4]	0
Bit 3	R/W	SDCTH[3]	0
Bit 2	R/W	SDCTH[2]	0
Bit 1	R/W	SDCTH[1]	0
Bit 0	R/W	SDCTH[0]	0

Register 0xF4: RASE SD Clearing Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SDCTH[11]	0
Bit 2	R/W	SDCTH[10]	0
Bit 1	R/W	SDCTH[9]	0
Bit 0	R/W	SDCTH[8]	0

SDCTH[11:0]:

The SDCTH[11:0] value determines the threshold for the removal of the SD alarm. The SD alarm is removed when the number of B2 errors accumulated during an evaluation window is less than the SDCTH[11:0] value. Refer to the Operations section for the recommended settings.

Register 0xF5: RASE Receive K1

Bit	Type	Function	Default
Bit 7	R	K1[7]	X
Bit 6	R	K1[6]	X
Bit 5	R	K1[5]	X
Bit 4	R	K1[4]	X
Bit 3	R	K1[3]	X
Bit 2	R	K1[2]	X
Bit 1	R	K1[1]	X
Bit 0	R	K1[0]	X

K1[7:0]:

The K1[7:0] bits contain the current K1 code value. The contents of this register are updated when a new K1 code value (different from the current K1 code value) is received for three consecutive frames. An interrupt may be generated when a new code value is received (using the COAPSE bit in the RASE Interrupt Enable Register). K1[7] is the most significant bit corresponding to bit 1, the first bit received. K1[0] is the least significant bit, corresponding to bit 8, the last bit received.

Register 0xF6: RASE Receive K2

Bit	Type	Function	Default
Bit 7	R	K2[7]	X
Bit 6	R	K2[6]	X
Bit 5	R	K2[5]	X
Bit 4	R	K2[4]	X
Bit 3	R	K2[3]	X
Bit 2	R	K2[2]	X
Bit 1	R	K2[1]	X
Bit 0	R	K2[0]	X

K2[7:0]:

The K2[7:0] bits contain the current K2 code value. The contents of this register are updated when a new K2 code value (different from the current K2 code value) is received for three consecutive frames. An interrupt may be generated when a new code value is received (using the COAPSE bit in the RASE Interrupt Enable Register). K2[7] is the most significant bit corresponding to bit 1, the first bit received. K2[0] is the least significant bit, corresponding to bit 8, the last bit received.

Register 0xF7: RASE Receive Z1/S1

Bit	Type	Function	Default
Bit 7	R	Z1/S1[7]	X
Bit 6	R	Z1/S1[6]	X
Bit 5	R	Z1/S1[5]	X
Bit 4	R	Z1/S1[4]	X
Bit 3	R	Z1/S1[3]	X
Bit 2	R	Z1/S1[2]	X
Bit 1	R	Z1/S1[1]	X
Bit 0	R	Z1/S1[0]	X

Z1/S1[3:0]:

The lower nibble of the first Z1/S1 byte contained in the receive stream is extracted into this register. The Z1/S1 byte is used to carry synchronization status messages between line terminating network elements. Z1/S1[3] is the most significant bit corresponding to bit 5, the first bit received. Z1/S1[0] is the least significant bit, corresponding to bit 8, the last bit received. An interrupt may be generated when a byte value is received that differs from the value extracted in the previous frame (using the Z1/S1E bit in the RASE Interrupt Enable Register). In addition, debouncing can be performed where the register is not loaded until eight of the same consecutive nibbles are received. Debouncing is controlled using the Z1/S1_CAP bit in the RASE Configuration/Control register.

Z1/S1[7:4]:

The upper nibble of the first Z1/S1 byte contained in the receive stream is extracted into this register. No interrupt is asserted on the change of this nibble. In addition, when the Z1/S1_CAP bit in the RASE Configuration/Control register selects debouncing, the upper nibble is only updated when eight of the same consecutive lower nibbles are received.

12 TEST FEATURES DESCRIPTION

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the S/UNI-QUAD. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[10]) is high.

Test mode registers may also be used for board testing. When all of the TSBs within the S/UNI-QUAD are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

In addition, the S/UNI-QUAD also supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced via the JTAG test port.

Table 6: Test Mode Register Memory Map

Address	Register
0x000-0x3FF	Normal Mode Registers
0x400	Master Test Register
0x401-0x7FF	Reserved For Test

12.1 Master Test Register

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

2. Writable test mode register bits are not initialized upon reset unless otherwise noted.

Register 0x400: Master Test

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	W	Reserved	X
Bit 5	W	PMCATST	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	0
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	0
Bit 0	R/W	HIZIO	0

This register is used to enable S/UNI-QUAD test features. All bits, except PMCTST, PMCATST and BYPASS are reset to zero by a reset of the S/UNI-QUAD using either the RSTB input or the Master Reset register. PMCTST and BYPASS are reset when CSB is logic one. PMCATST is reset when both CSB is high and RSTB is low. PMCTST, PMCATST and BYPASS can also be reset by writing a logic zero to the corresponding register bit.

HIZIO, HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the S/UNI-QUAD . While the HIZIO bit is a logic one, all output pins of the S/UNI-QUAD except the data bus and output TDO are held tri-state. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles. The HIZDATA bit is overridden by the DBCTRL bit.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each TSB block in the S/UNI-QUAD for board level testing. When IOTST is a logic one, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequentially the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic one and either IOTST or PMCTST are logic one, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the S/UNI-QUAD to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

PMCTST:

The PMCTST bit is used to configure the S/UNI-QUAD for PMC's manufacturing tests. When PMCTST is set to logic one, the S/UNI-QUAD microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and can be cleared by setting CSB to logic one or by writing logic zero to the bit.

PMCATST:

The PMCATST bit is used to configure the analog portion of the S/UNI-QUAD for PMC's manufacturing tests.

Reserved:

The reserved bit must be programmed to logic one for proper operation.

12.2 Test Mode 0 Details

In test mode 0, the S/UNI-QUAD allows the logic levels on the device inputs to be read through the microprocessor interface and allows the device outputs to be forced to either logic level through the microprocessor interface. The IOTST bit in the Master Test register must be set to logic one to access the device I/O.

To enable test mode 0, the IOTST bit in the Master Test register is set to logic one and the following addresses must be written with 00H: TBD.

Reading the following address locations returns the values on the indicated inputs:

Table 7: Test Mode 0 Read Locations

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08H								
0FH								

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
8BH								
8CH								

The following inputs cannot be read using the IOTST feature: D[7:0], A[7:0], ALE, CSB, WRB, RDB, RSTB, TRSTB, TMS, TCK, and TDI.

Writing the following address locations forces the outputs to the value in the corresponding bit position (zeros should be written to all unused test register locations):

Table 8: Test Mode 0 Write Locations

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06H								
8BH								
8CH								
90H								

The following outputs can not be controlled using the IOTST feature: D[7:0], and TDO.

1. INT corresponds to output INTB. INTB is an open drain output and should be pulled high for proper operation. Writing a logic one to the INT bit allows the S/UNI-QUAD to drive INTB low. Writing a logic zero to the INT bit tristates the INTB output.

12.3 JTAG Test Port

The S/UNI-QUAD JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 9: Instruction Register (Length - 3 bits)

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000

Instructions	Selected Register	Instruction Codes, IR[2:0]
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 10: Identification Register

Length	32 bits
Version number	0H
Part Number	5349H
Manufacturer's identification code	0CDH
Device identification	053490CDH

Table 11: Boundary Scan Register

Length - 155 bits

Pin/ Enable	Register Bit	Cell Type	I.D. Bit	Pin/ Enable	Register Bit	Cell Type	I.D. Bit
A[7:0]5	154:147	IN_CELL	00000 101				
ALE	146	IN_CELL	0				
CSB	145	IN_CELL	0				
WRB	144	IN_CELL	1				
RDB	143	IN_CELL	1				
RSTB	142	IN_CELL	0				
D[7:0]	141:134	IO_CELL	10101 010				

NOTES:

1. OENB is the active low output enable for D[7:0].
2. RDATENB is the active low output enable for RSOC, RDAT[15:0], and RXPRTY[1:0].
3. When set high, INTB will be set to high impedance.
4. HIZ is the active low output enable for all OUT_CELL types except D[7:0], RXPRTY[1:0], RDAT[15:0], and INTB
5. A[7] is the first bit of the boundary scan chain.

12.3.1 Boundary Scan Cells

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table located above.

Figure 6: Input Observation Cell (IN_CELL)

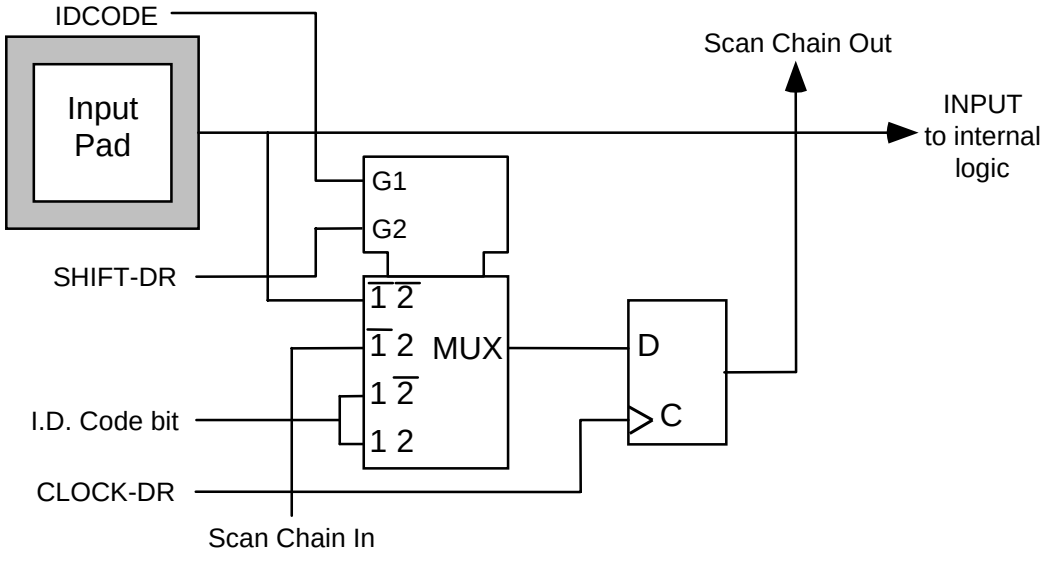


Figure 7: Output Cell (OUT_CELL)

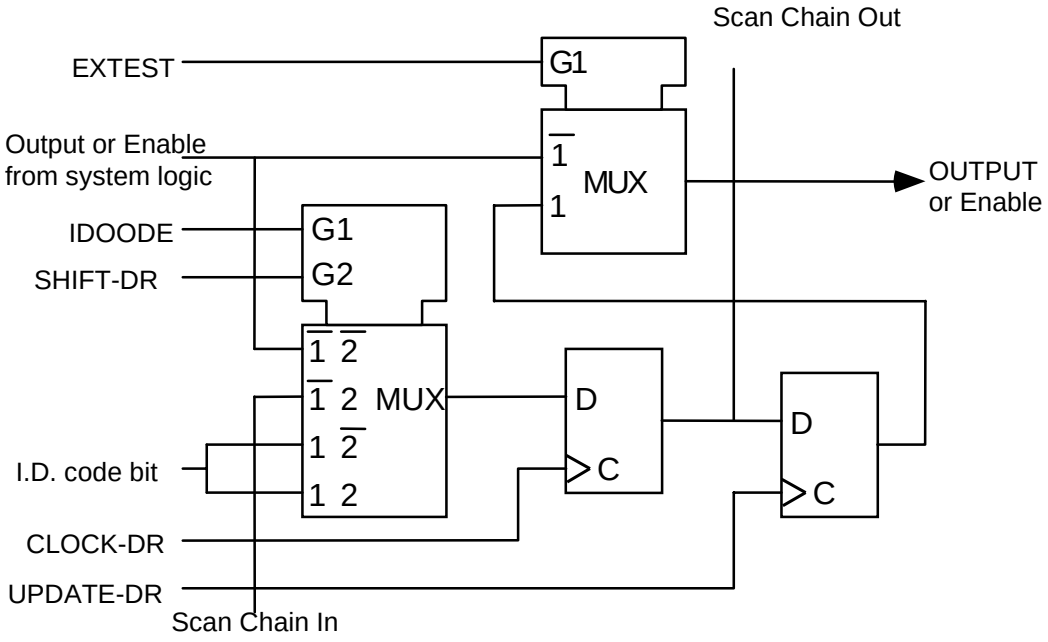


Figure 8: Bidirectional Cell (IO_CELL)

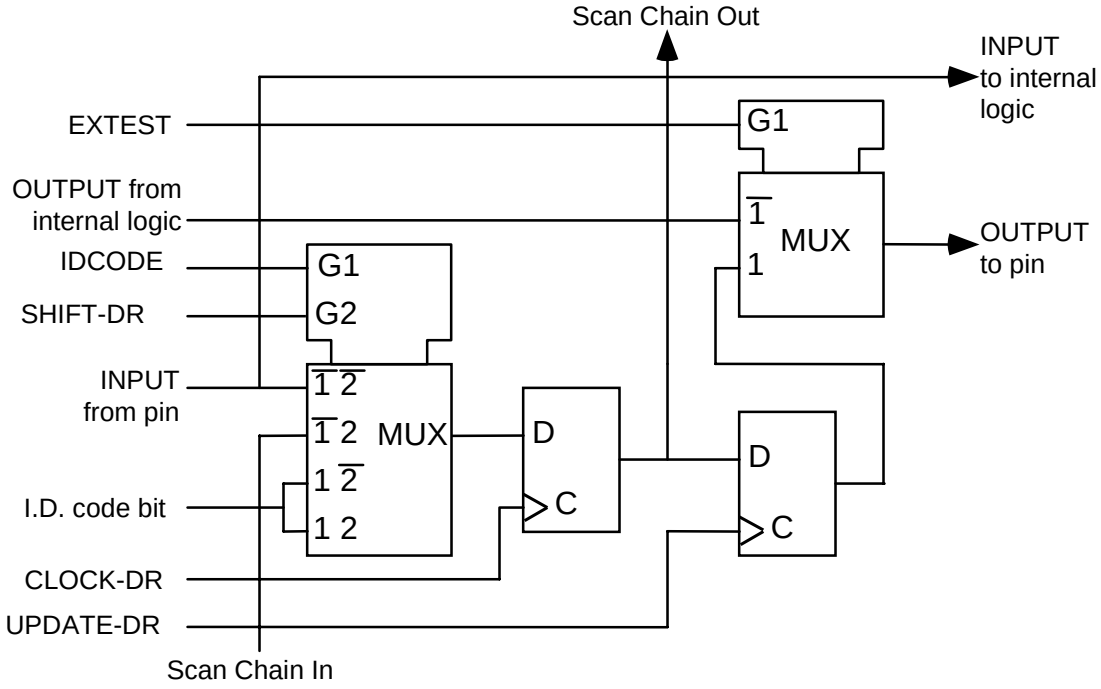
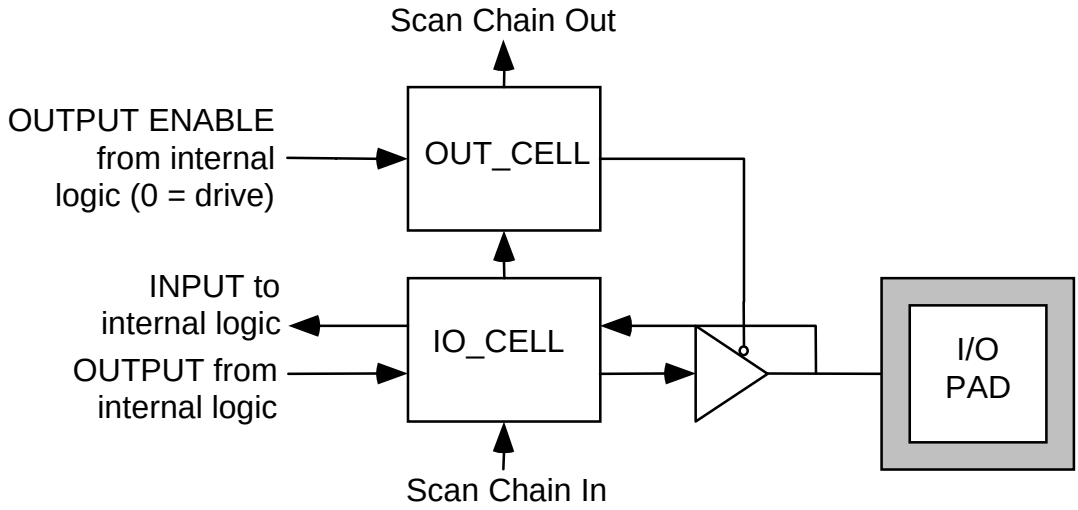


Figure 9: Layout of Output Enable and Bidirectional Cells



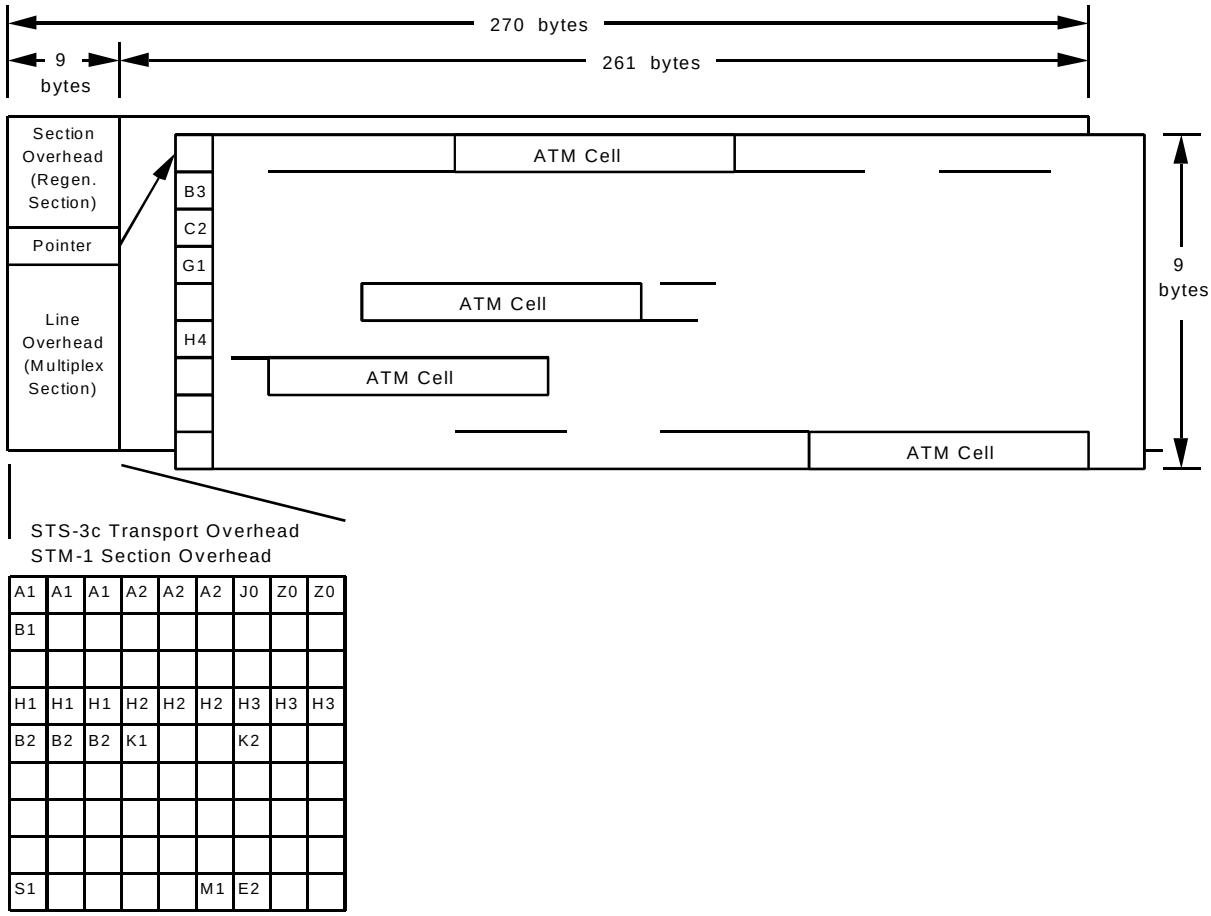
13 OPERATION

13.1 SONET/SDH Frame Mappings and Overhead Byte Usage

13.1.1 ATM Mapping

The S/UNI-QUAD processes the ATM cell mapping for STS-3c (STM-1) as shown below in Figure 10. The S/UNI-QUAD processes the transport and path overhead required to support ATM UNIs and NNIs. In addition, the S/UNI-QUAD provides support for the APS bytes. In Figure 10, the STS-3c (STM-1) mapping is shown. In this mapping, no stuff columns are included in the SPE. The entire SPE is used for ATM cells.

Figure 10: ATM Mapping into the STS-3c (STM-1) SPE



13.1.2 Transport and Path Overhead Bytes

Under normal operating conditions, the S/UNI-QUAD processes a subset of the complete transport overhead present in an STS-3c (STM-1) stream. The byte positions processed by the S/UNI-QUAD are indicated in Figure 11.

Figure 11: STS-3c (STM-1) Overhead

A1	A1	A1	A2	A2	A2	J0	Z0	Z0	
B1									B3
									C2
H1	H1	H1	H2	H2	H2	H3	H3	H3	G1
B2	B2	B2	K1			K2			
									H4
S1					M1				

TRANSPORT OVERHEAD SOH

PATH OVERHEAD POH

Transport Overhead Bytes

A1, A2: The frame alignment bytes (A1, A2) locate the SONET/SDH frame in the STS-3c (STM-1) serial stream.

Z0: The Z0 bytes are currently defined as the STS-3c (STM-1) section growth bytes for SONET/SDH. Z0 bytes are not scrambled by the frame synchronous scrambler.

B1: The section bit interleaved parity byte provides a section error monitoring function.

H1, H2: The pointer value bytes locate the path overhead column in the SONET/SDH frame.

H3: The pointer action bytes contain synchronous payload envelope data when a negative stuff event occurs. The all zeros pattern is inserted in the transmit direction. This byte is ignored in the receive direction unless a negative stuff event is detected.

B2: The line bit interleaved parity bytes provide a line error monitoring function.

K1, K2: The K1 and K2 bytes provide the automatic protection switching channel. The K2 byte is also used to identify line layer maintenance signals. Line RDI is indicated when bits 6, 7, and 8 of the K2 byte are set to the pattern '110'. Line AIS is indicated when bits 6, 7, and 8 of the K2 byte are set to the pattern '111'.

S1: The S1 byte provides the synchronization status byte. Bits 5 through 8 of the synchronization status byte identifies the synchronization source of the STS-3c (STM-1) signal. Bits 1 through 4 are currently undefined.

M1: The M1 byte is located in the third STS-1 locations of a STS-3c (STM-1) and provides a line far end block error function for remote performance monitoring.

Path Overhead Bytes

J1: This byte is set to transmit continuous null characters. Null is defined as the ASCII code, 0x00.

B3: The path bit interleaved parity byte provides a path error monitoring function.

C2: The path signal label indicator identifies the equipped payload type. For ATM payloads, the identification code is 0x13

G1: The path status byte provides a path FEBE function, and a path remote defect indication function. Three bits are allocated for remote defect indications: bit 5 (the path RDI bit), bit 6 (the auxiliary path RDI bit) and bit 7 (Enhanced RDI bit). Taken together these bits provide a eight state path RDI code that can be used to categorize path defect indications.

H4: The multiframe indicator byte is a payload specific byte, and is not used for ATM payloads.

13.2 ATM Cell Data Structure

ATM cells may be passed to/from the S/UNI-QUAD using a twenty-seven word, 16-bit Utopia level 2 compliant data structure. This data structure is shown in Figure 12.

Figure 12: 16-bit Wide, 27 Word ATM Cell Structure

	Bit 15 – Bit 8	Bit 7 – Bit 0
Word 1	**H1**	**H2**
Word 2	**H3**	**H4**
Word 3	**H5**	**HCS STATUS/CONTROL**
Word 4	**PAYLOAD1**	**PAYLOAD2**
Word 5	**PAYLOAD3**	**PAYLOAD4**
Word 6	**PAYLOAD5**	**PAYLOAD6**
⋮	⋮	⋮
Word 27	**PAYLOAD47**	**PAYLOAD48**

Bit 15 of each word is the most significant bit (which corresponds to the first bit transmitted or received). The header check sequence octet (HCS) is passed through this structure. The start of cell indication input and output (TSOC and RSOC) are coincident with Word 1 (containing the first two header octets). Word 3 of this structure contains the HCS octet in bits 15 to 8.

In the receive direction, the lower 8 bits of Word 3 contain the HCS status octet. An all-zeros pattern in these 8 bits indicates that the associated header is error

free. An all-ones pattern indicates that the header contains an uncorrectable error (if the HCSPASS bit in the RXCP Control Register is set to logic zero, the all-ones pattern will never be passed in this structure). An alternating ones and zeros pattern (0xAA) indicates that the header contained a correctable error. In this case the header passed through the structure is the "corrected" header.

In the transmit direction, the HCS bit in the TXCP Control register determines whether the HCS is calculated internally or is inserted directly from the upper 8 bits of Word 3. The lower 8 bits of Word 3 contain the HCS control octet. The HCS control octet is an error mask that allows the insertion of one or more errors in the HCS octet. A logic one in a given bit position causes the inversion of the corresponding HCS bit position (for example a logic one in bit 7 causes the most significant bit of the HCS to be inverted).

13.3 Bit Error Rate Monitor

The S/UN-QUAD provides two BERM blocks. One can be dedicated to monitor at the Signal Degrade (SD) error rate and the other dedicated to monitor at the Signal Fail (SF) error rate.

The Bit Error Rate Monitor (BERM) block counts and monitor line BIP errors over programmable periods of time (window size). It can monitor to declare an alarm or to clear it if the alarm is already set. A different threshold and accumulation period must be used to declare or clear the alarm, whether or not those two operations are not performed at the same BER. The following table list the recommended content of the BERM registers for different error rates (BER). Both BERMs in the TSB are equivalent and are programmed similarly. In a normal application they will be set to monitor different BER.

When the SF/SD CMODE bit is 1 this indicates that the clearing monitoring is recommended to be performed using a window size that is 8 times longer than the declaration window size. When the SF/SD CMODE bit is 0 this indicates that the clearing monitoring is recommended to be performed using a window size equal to the declaration window size. In all cases the clearing threshold is calculated for a BER that is 10 times lower than the declaration BER, as required in the references. The table indicates the declare BER and evaluation period only.

The Saturation threshold is not listed in the table, and should be programmed with the value 0xFFF by default, deactivating saturation. Saturation capabilities are provided to allow the user to address issues associated with error bursts.

Table 12: Recommended BERM settings

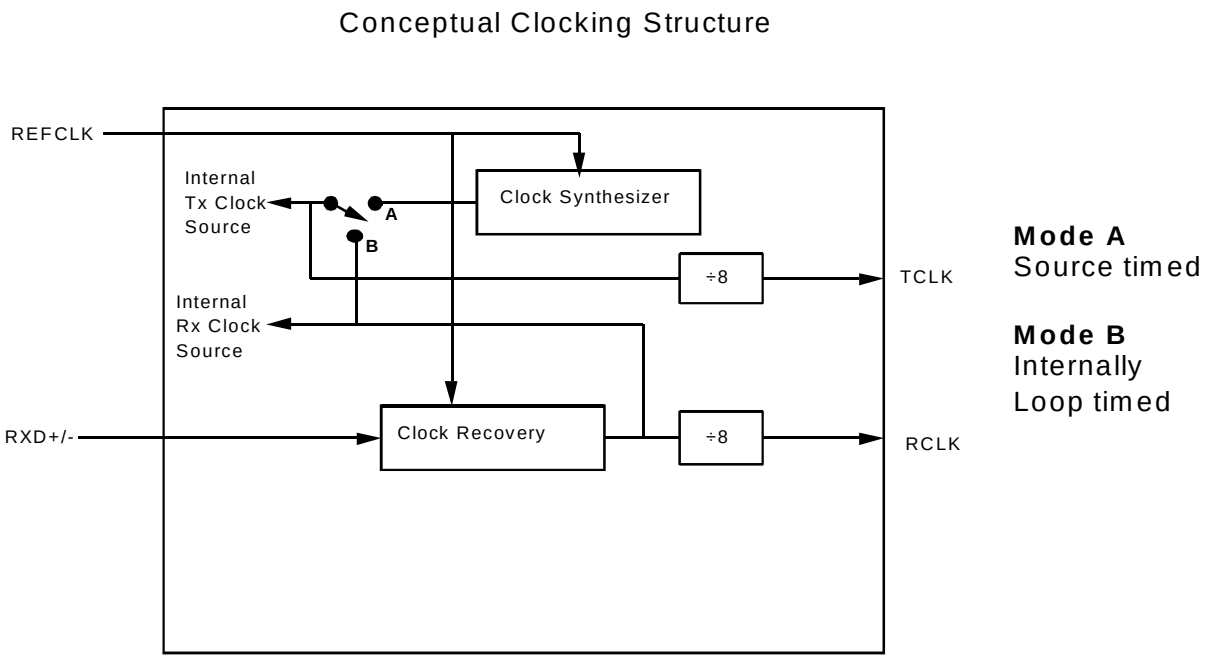
declare BER	Eval Per (s)	SF/SD SMODE	SF/SD CMODE	SF/SD SAP	SF/SD DTH	SF/SD CTH
10^{-3}	0.008	0	0	0x000008	0x245	0x083
10^{-4}	0.013	0	1	0x00000D	0x0A3	0x0B4
10^{-5}	0.100	0	1	0x000064	0x084	0x08E
10^{-6}	1.000	0	1	0x0003E8	0x085	0x08E
10^{-7}	10.000	0	1	0x002710	0x085	0x08E
10^{-8}	83.000	0	1	0x014438	0x06D	0x077
10^{-9}	667.000	0	1	0x0A2D78	0x055	0x061

It is important to notice that the Table 12 was designed around the Bellcore GR-253 specification. Please refer to the SONET/SDH/SDH Bit error Threshold Monitoring application note for more details as well as a recommended programming meeting the ITU G.783 specification.

13.4 Clocking Options

The S/UNI-QUAD supports several clocking modes. Figure 13 is an abstraction of the clocking topology.

Figure 13: Conceptual Clocking Structure



Mode A is provided for all public user network interfaces (UNIs) and for private UNIs and private network node interfaces (NNIs) that are not synchronized to the recovered clock.

The transmit clock in a private UNI or a private NNI may be locked to an external reference or may free-run. The simplest implementation requires an oscillator free-running at 19.44 MHz.

Mode A is selected by clearing the LOOPT bit of the Channel Control register. REFCLK is multiplied by 8 to become the 155.52 MHz MHz transmit clock. REFCLK must be jitter free. The source REFCLK is also internally used as the clock recovery reference.

Mode B is provided for private UNIs and private NNIs that require synchronization to the recovered clock. Mode B is selected by setting the LOOPT bit of the Master Control register. Normally, the transmit clock is locked to the receive data. In the event of a loss of signal condition, the transmit clock is synthesized from REFCLK.

13.5 Loopback Operation

The S/UNI-QUAD supports three loopback functions: line loopback, parallel diagnostic loopback and serial diagnostic loopback. Each channel's loopback modes operate independently. The loopback modes are activated by the PDLE, LLE and SDLE bits contained in the S/UNI-QUAD Channel Control Register.

The line loopback, see Figure 14, connects the high speed receive data and clock to the high speed transmit data and clock, and can be used for line side investigations (including clock recovery and clock synthesis). While in this mode, the entire receive path is operating normally and cells can be received through the FIFO interface.

The serial diagnostic loopback, see Figure 15, connects the high speed transmit data and clock to the high speed receive data and clock. While in this mode, the entire transmit path is operating normally and data is transmitted on the TXD+/- outputs.

The parallel diagnostic loopback, see Figure 16, connects the byte wide transmit data and clock to the byte wide receive data and clock. While in this mode, the entire transmit path is operating normally and data is transmitted on the TXD+/- outputs.

Figure 14: Line Loopback Mode

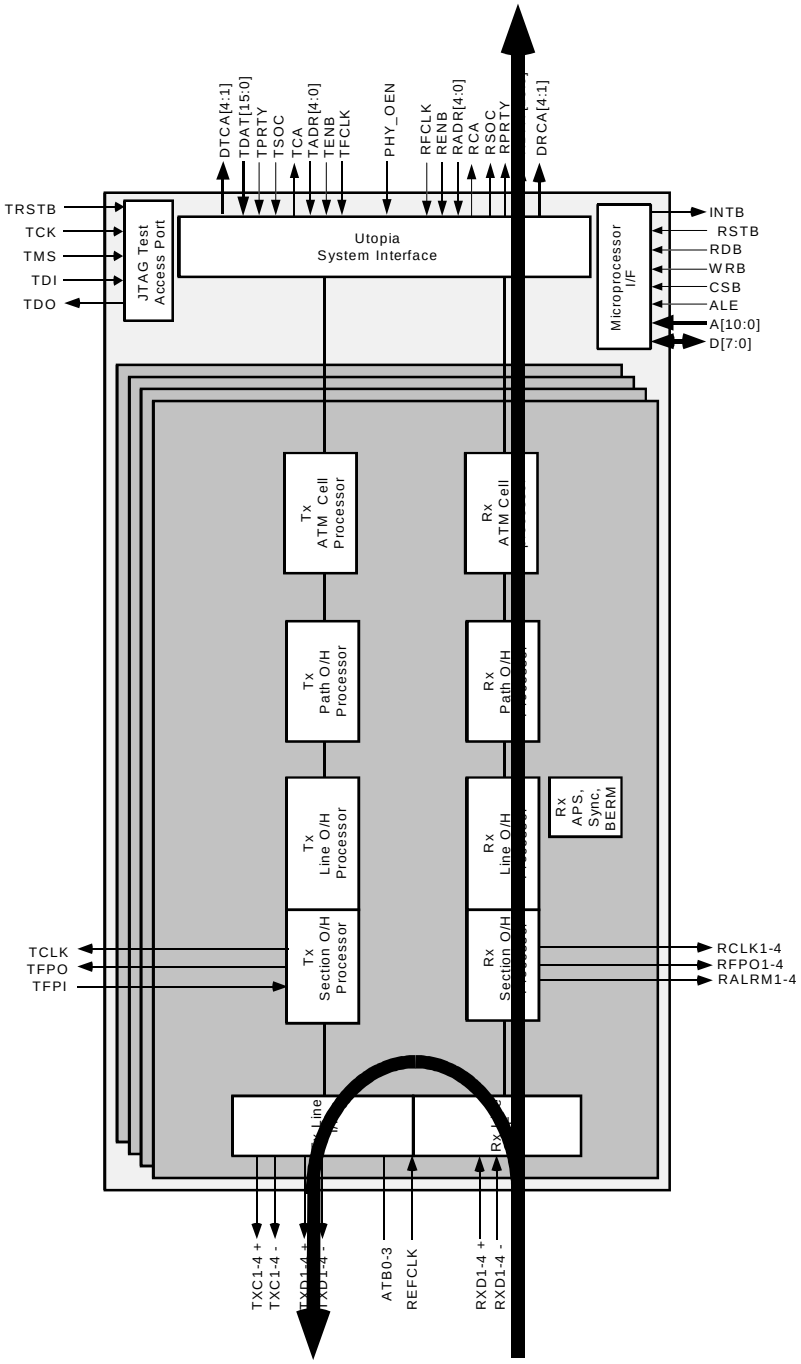


Figure 15: Serial Diagnostic Loopback Mode

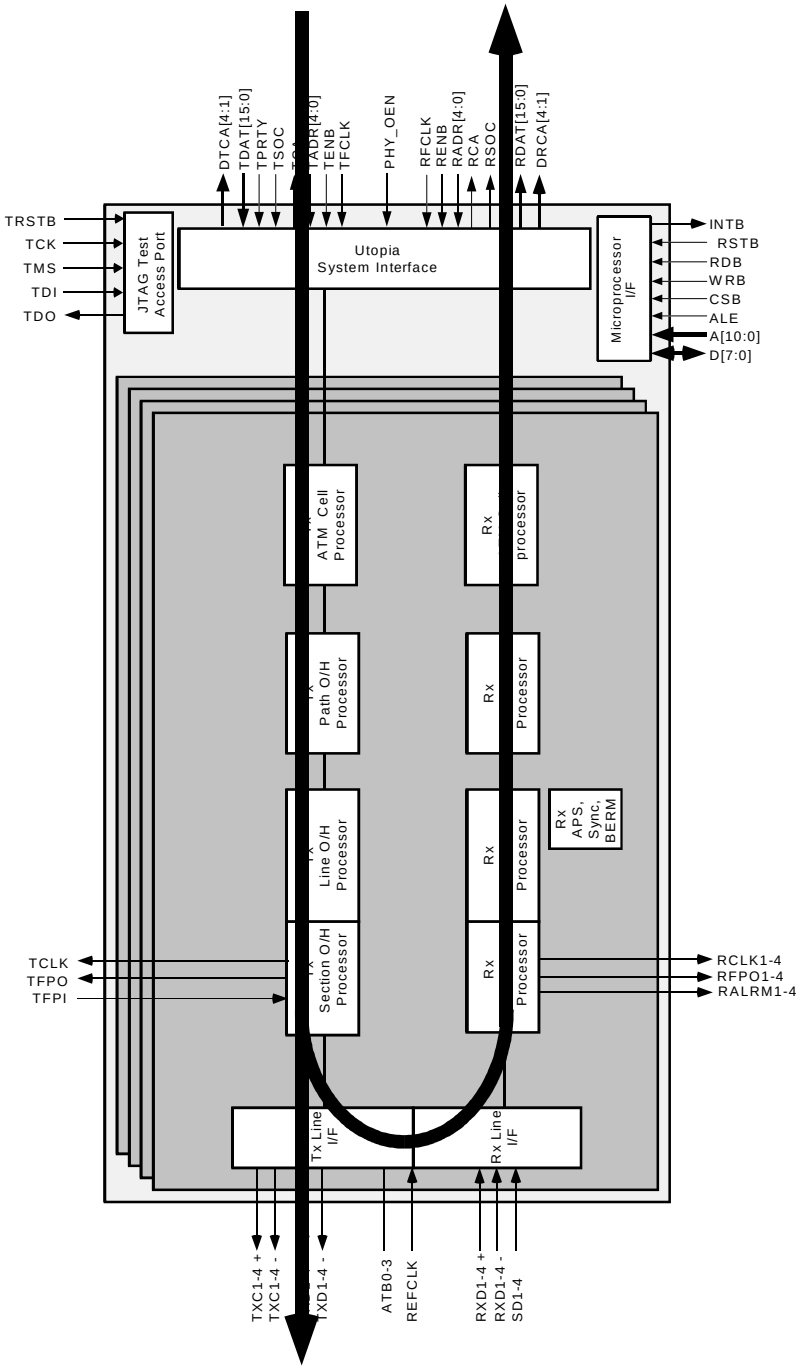
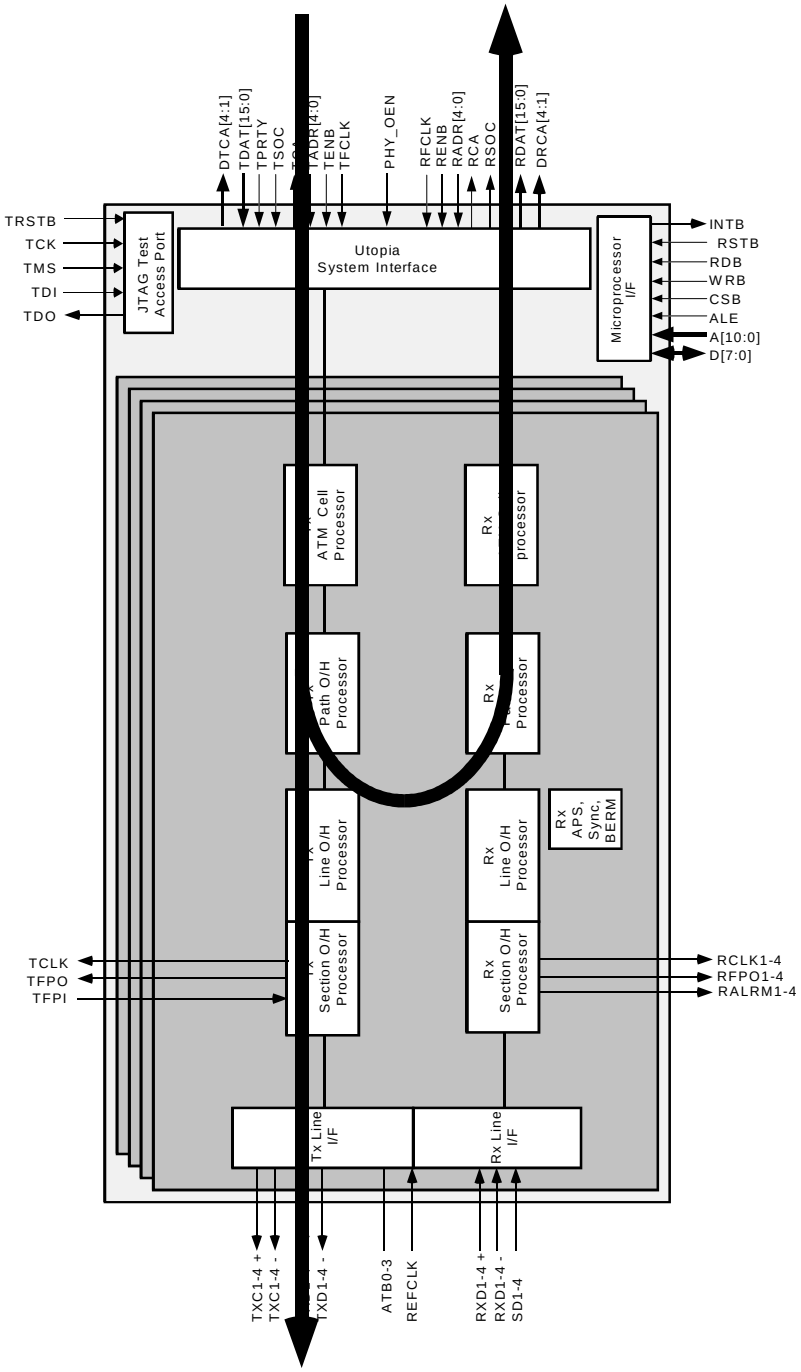


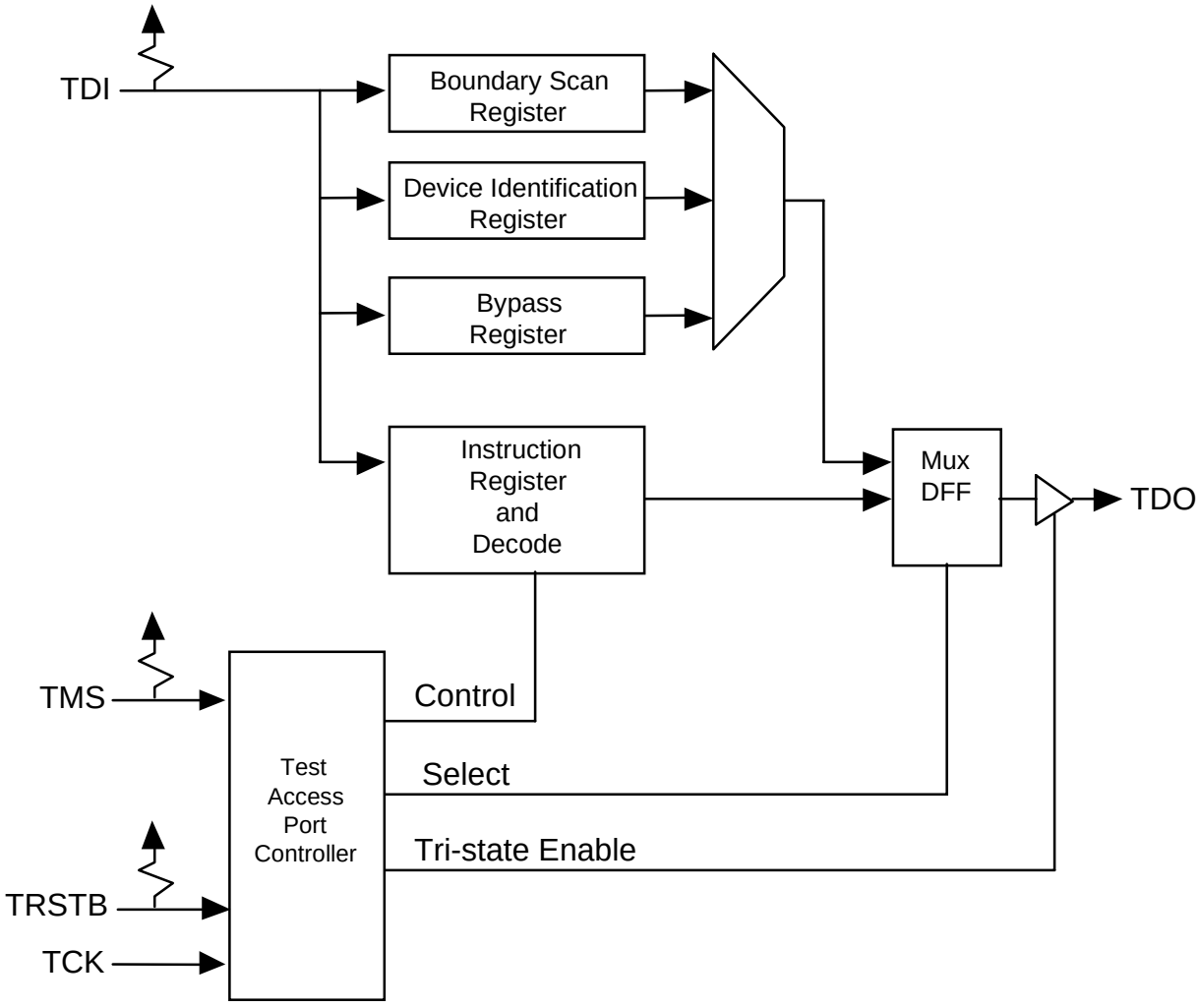
Figure 16: Parallel Diagnostic Loopback Mode



13.6 JTAG Support

The S/UNI-QUAD supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 17: Boundary Scan Architecture



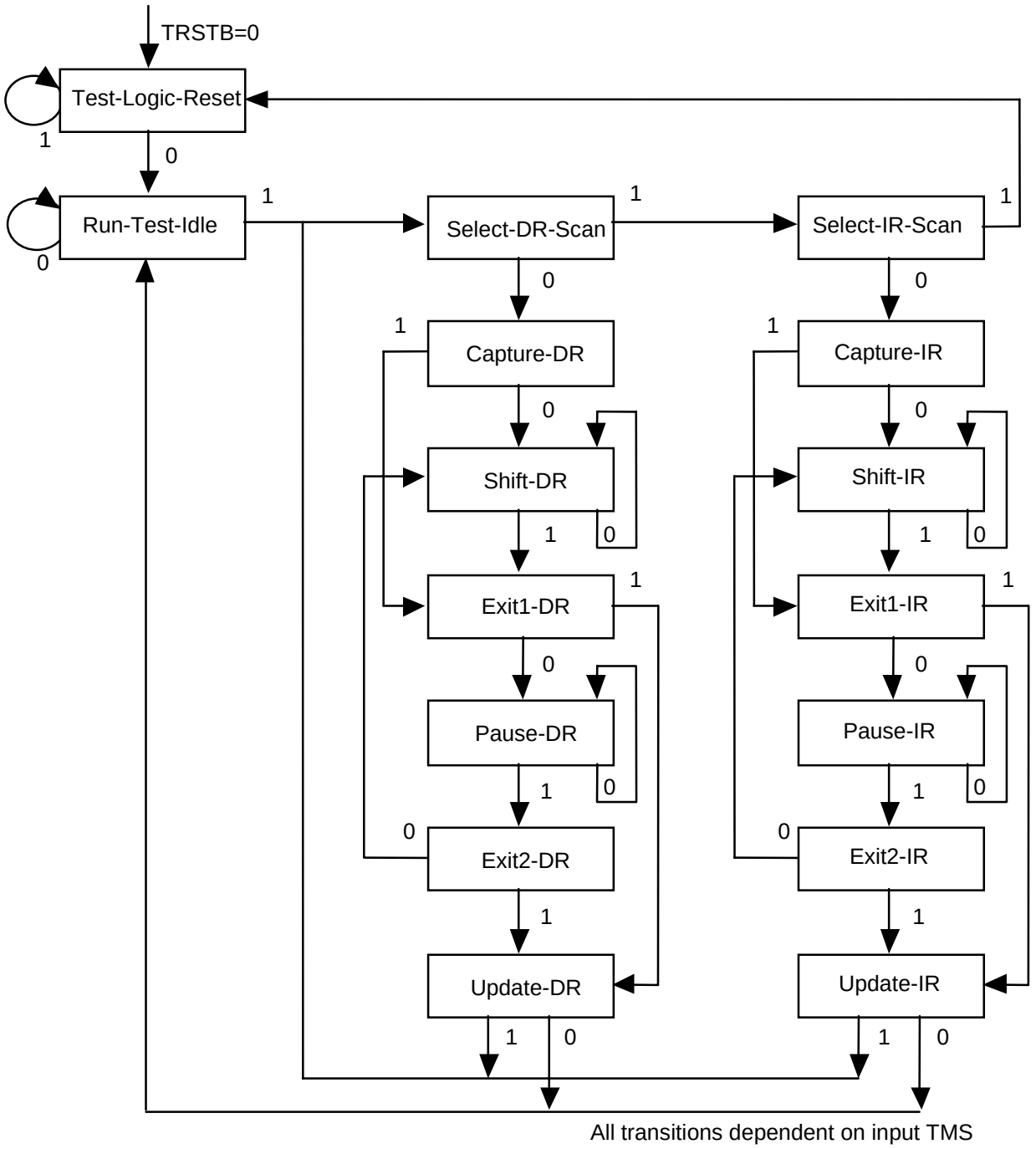
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

13.6.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 18: TAP Controller Finite State Machine



13.6.1.1 States

Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is an description of the standard instructions. Each instruction selects an serial test data register path between input, TDI and output, TDO.

13.6.1.2 Instructions

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary

device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

13.7 Board Design Recommendations

The noise environment and signal integrity are often the limiting factors in system performance. Therefore, the following board design guidelines must be followed in order to ensure proper operation:

1. Use a single plane for both digital and analog grounds.

2. Provide separate +3.3 volt analog transmit, +3.3 volt analog receive, and +3.3 volt digital supplies, but otherwise connect the supply voltages together at one point close to the connector where +3.3 volts is brought to the card.

3. Ferrite beads are not advisable in digital switching circuits because inductive spiking (di/dt noise) is introduced into the power rail. Simple RC filtering is probably the best approach provided care is taken to ensure the IR drop in the resistance does not lower the supply voltage below the recommended operating voltage.

4. Separate high-frequency decoupling capacitors are recommended for each analog power (TAVD, RAVD and QAVD) pin as close to the package pin as possible. Separate decoupling is required to prevent the transmitter from coupling noise into the receiver and to prevent transients from coupling into some reference circuitry.

5. The high speed serial streams (TXD+/- and RXD+/) must be routed with controlled impedance circuit board traces and must be terminated with a matched load. Normal CMOS-type design rules are not recommended and will reduce the performance of the device.

13.8 Power Supply Sequencing

Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions it is possible to blow these ESD protection devices or trigger latch up. The recommended power supply sequencing follows:

1.) To prevent damage to the ESD protection on the device inputs the maximum DC input current specification must be respected. This is accomplished by either ensuring that the VDD power is applied before input pins are driven or by increasing the source impedance of the driver so that the maximum driver short circuit current is less than the maximum DC input current specification. (20 mA)

2.) QAVD power must be supplied either after VDD or simultaneously with VDD to prevent current flow through the ESD protection devices which exist between QAVD and VDD power supplies. To prevent forward biasing the ESD protection diode between QAVD supplies and VDD the differential voltage measured between these power supplies must be less than 0.5 volt. This recommended differential voltage is to include peak to peak noise on the VDD power supply as digital noise will otherwise be coupled into the analog circuitry. Current limiting can be accomplished by using an off chip three terminal voltage regulator supplied by a quiet high voltage supply.

3.) BIAS voltage must be supplied either before VDD or simultaneously with VDD to prevent current flow through the ESD protection devices which exist between BIAS and VDD power supplies.

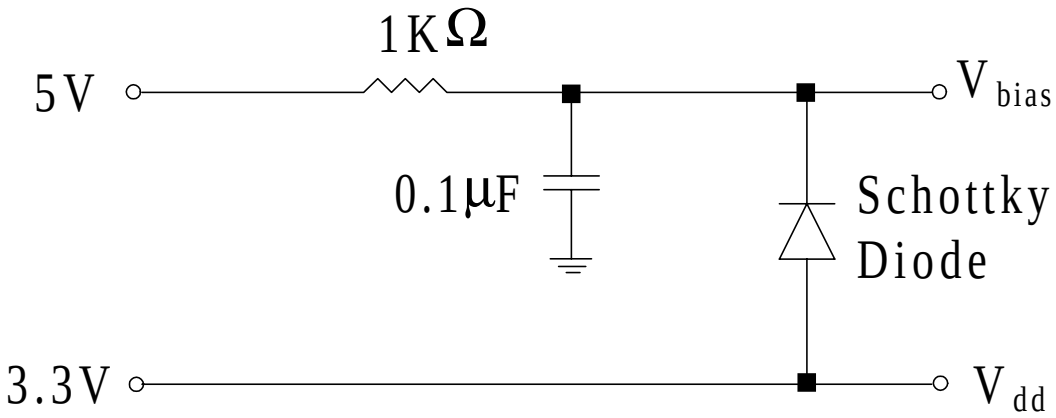
4.) Analog power supplies (AVD, includes RAVDs, TAVDs but not QAVD) should be applied after QAVD, but can be applied at the same time as QAVD providing the 100ohm resistor in series with QAVD (shown in Figure 29 and Figure 30) is in place. The AVD supplies should also be current limited to the maximum latchup current specification (100 mA). To prevent forward biasing the ESD protection diode between AVD supplies and QAVD the differential voltage measured between these power supplies must be less than 0.5 volt. This recommended differential voltage is to include peak to peak noise on the QAVD and AVD power supplies as digital noise will

otherwise be coupled into the analog circuitry. Current limiting can be accomplished by using an off chip three terminal voltage regulator supplied by a quiet high voltage supply. If the VDD power supply is relatively quiet, VDD can be filtered using a ferrite bead and a high frequency decoupling capacitor to supply AVD. The relative power sequencing of the multiple AVD power supplies is not important.

5.) Power down the device in the reverse sequence. Use the above current limiting technique for the analog power supplies. Small offsets in VDD / AVD discharge times will not damage the device.

Figure 19 illustrates a power sequencing circuit to avoid latch-up or damage to 3.3V devices that are 5V tolerant. This circuit will ensure V_{bias} is greater than V_{dd} and protect against designs which require the 3.3V power supply appearing before the 5V supply.

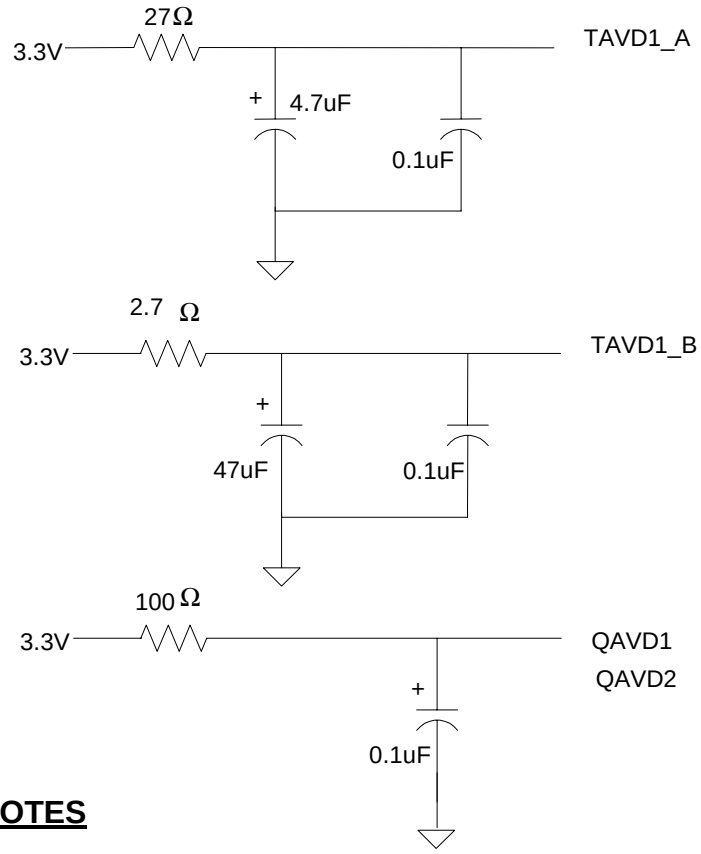
Figure 19: Power Sequencing Circuit



13.9 Analog Power Supply Filtering

The noise environment and signal integrity are often the limiting factors of the system performance, thus the following analog power filtering scheme is recommended.

Figure 20: LAN Mode Analog Power Filters with 3.3V Supply



NOTES

1) Use 0.1uF on all other analog and digital power pins
2) place 0.1uF as close to power pin as possible.
3) 47uF and resistors do not have to be very close to power pins

Please note: TAVD1_A is pin # L3
TAVD1_B is pin # L1
QAVD1 is pin # AA6
QAVD2 is pin # C6

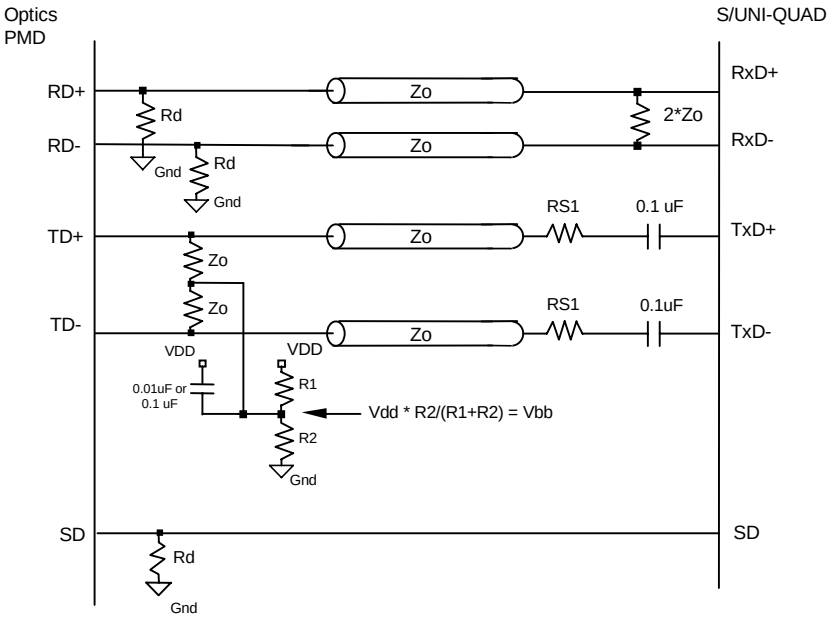
13.10 Interfacing to ECL or PECL Devices

Although the TXD+/- outputs are TTL compatible, only a few passive components are required to convert the signals to ECL (or PECL) logic levels. Figure 21 illustrates the recommended configuration. The capacitors AC couple the outputs so that the ECL inputs are free to swing around the ECL bias voltage (V_{BB}). The combination of the RS, RS1 and Z0 resistors divide the voltage down to a nominally 800mV swing. The Z0 resistors also terminate the signals.

The RXD+/- inputs to the S/UNI-QUAD are DC coupled as shown. The device has a true PECL receiver so only termination resistors are required.

Ceramic coupling capacitors are recommended.

Figure 21: Interfacing to ECL or PECL



Notes: Vpp is minimum input swing required by the optical PMD device.

Vbb is the switching threshold of the PMD device (typically Vdd - 1.3 volts)

Vpp is Voh - Vol (typically 800 mVolts)

Vpp = (Zo/((RS1+Rs)+Z0) * Vdd
- Vdd (S/UNI-QUAD's analog transmit power) 3.3V
- Zo (trace impedance) typically 50Ω
- Rs (TxD source impedance) typically 15-20Ω
- RS1 : ~ 158Ω

For interfacing to 5.0V ODL, R1 : 237Ω , R2 : 698Ω
Rd : 330Ω
For interfacing to 3.3V ODL, R1 : 220Ω, R2: 330Ω
Rd : 150Ω

13.11 Initializing the S/UNI-QUAD

The S/UNI-QUAD defaults to the Asynchronous Transfer Mode (ATM) operation but it is recommended to implement the following initialization sequence.

1. Reset the device. This can be done by asserting the RSTB pin or setting the RESET bit in the Master Reset and ID Register (Register 00).

2. Set the TPOP Path Signal Label (Register 0x48) to 0x13, which indicates an ATM payload.

3. For every channel, reset all the Rx and Tx ATM FIFO's by setting the FIFORST register bit in the TXCP and RXCP blocks. Keep this bit set for at least 1 μs, then set the bit back to its inactive logic zero value.

4. For every channel, reset the performance monitoring counters in TXCP and RXCP blocks, and preferably in all the blocks. The easiest way to do this is to use the TIP register bit.

13.12 Using the S/UNI-QUAD with a 5 Volt ODL

The S/UNI-QUAD defaults to a 3.3V PECL optical data link (ODL) module interface. It can also be used with a 5V ODL. This is accomplished by setting to logic 1 the PECLV bit located in the Master Configuration Register (Register 0x01). Notice that all four channels are reconfigured.

14 FUNCTIONAL TIMING

All functional timing diagrams assume that polarity control is not being applied to input and output data and clock lines (i.e. polarity control bits in the S/UNI-QUAD registers are set to their default states).

14.1 ATM Utopia Level 2 System Interface

Figure 22: Multi-PHY Polling and Addressing Transmit Cell Interface

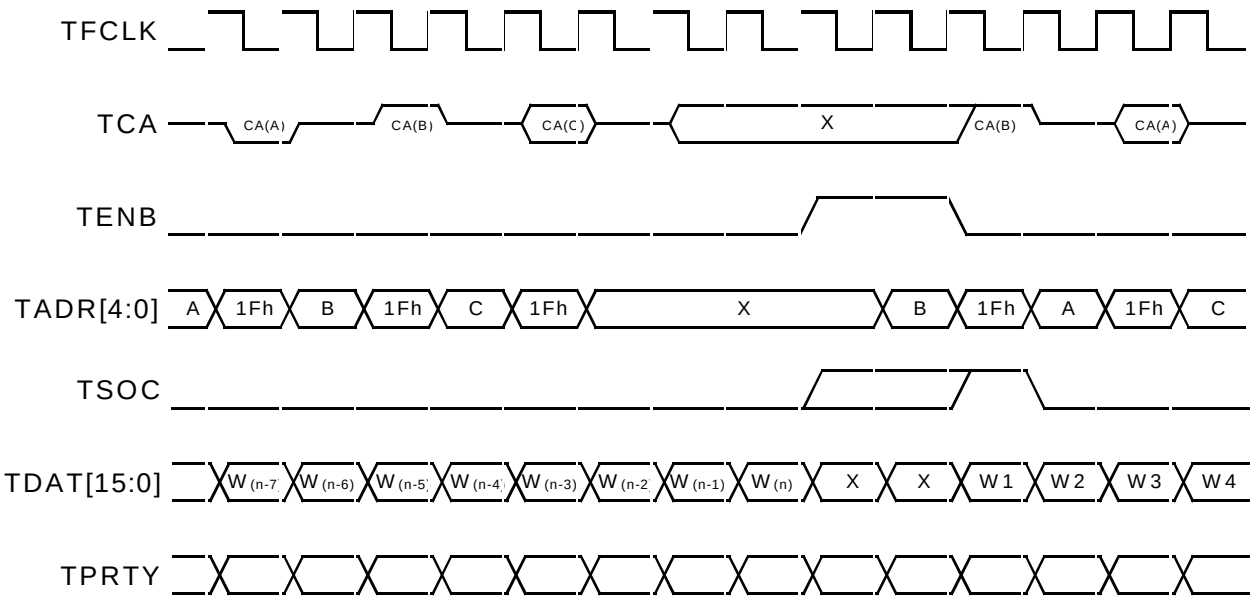


Figure 66 is an example of the multi-PHY polling and selection sequence supported by the S/UNI-QUAD. "A", "B", and "C" represent any arbitrary address values of PHY devices which may be occupied by the S/UNI-QUAD. The ATM Layer device is not restricted in its polling order. The PHY associated with address "A" indicates it cannot accept a cell, but PHY "B" indicates it is willing to accept a cell. As a result, the ATM Layer places address "B" on TADR[4:0] the cycle before TENB is asserted to select PHY "B" as the next cell destination. In this example, the PHY "C" status is ignored. The ATM Layer device is not constrained to select the latest PHY polled. As soon as the cell transfer is started, the polling process may be restarted.

During multi-PHY operation, several PHY layer devices share the TCA signal. As a result, this signals must be tri-stated in all PHY devices which have not been selected for polling by the ATM Layer. The value of TADR[4:0] selects the PHY being polled for the TCA signal, and all devices not corresponding to this address must tri-state its TCA output. This multi-PHY operation is directly supported by the S/UNI-QUAD.

Figure 23: Multi-PHY Polling and Addressing Receive Cell Interface

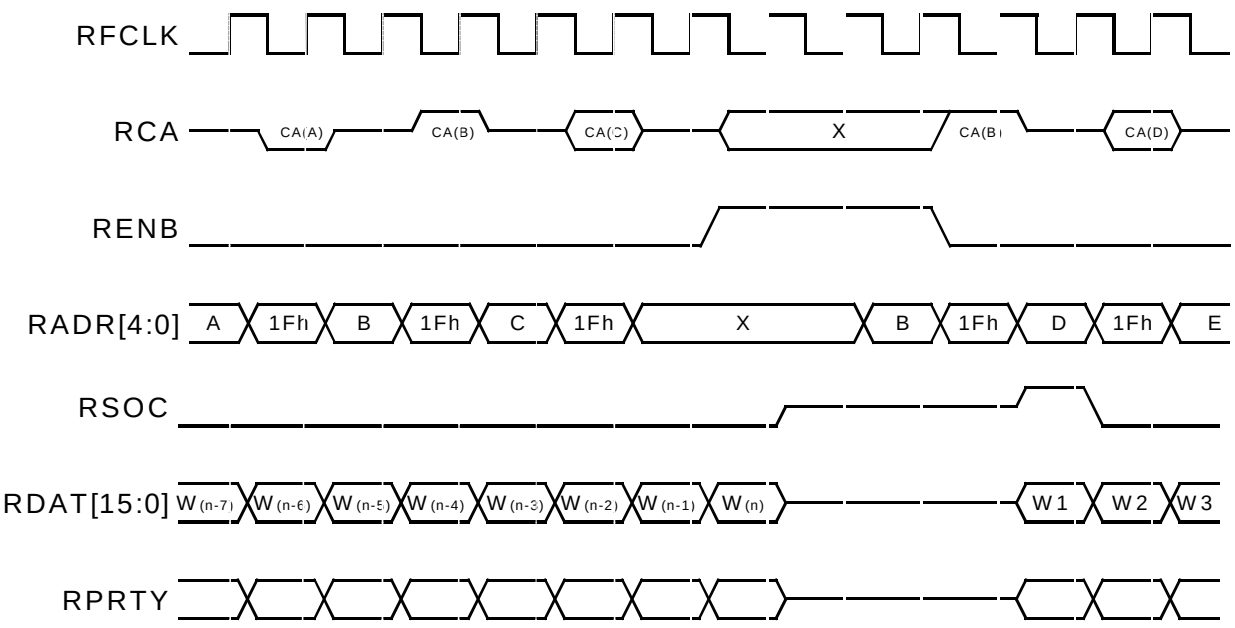


Figure 67 shows an example of the multi-PHY polling and selection sequence supported by the S/UNI-QUAD. "A", "B", "C", "D", and "E" represent any arbitrary address values which may be occupied by the S/UNI-QUAD. The ATM Layer device is not restricted in its polling order. The PHY associated with address "A" indicates it does not have a cell available, but PHY "B" indicates that it does. As a result, the ATM Layer places address "B" on RADR[4:0] the cycle before RENB is asserted to select PHY "B" as the next cell source. In this example, PHY "C"s status is ignored. The ATM Layer device is not constrained to select the latest PHY polled. As soon as the cell transfer is started, the polling process may be restarted.

During multi-PHY operation, several PHY layer devices share the RDAT[15:0], RSOC, RPRTY, and RCA signals. As a result, these signals must be tri-stated in all PHY devices which have not been selected for reading or polling by the ATM

Layer. Selection of which PHY layer device is being read is made by the value on RADR[4:0] the cycle before RENB is asserted and affects the RDAT[15:0], RSOC, and RPRTY signals. The value of RADR[4:0] selects the PHY being polled for the RCA signal, and all devices not corresponding to this address must tri-state its RCA output. These multi-PHY operations are directly supported by the S/UNI-QUAD.

15 ABSOLUTE MAXIMUM RATINGS

Maximum rating are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 13: Absolute Maximum Ratings

Ambient Temperature under Bias	-40°C to +85°C
Storage Temperature	-40°C to +125°C
Supply Voltage	-0.3V to +4.6V
Bias Voltage (V_{BIAS})	(V_{DD} - .3) to +5.5V
Voltage on Any Pin	-0.3V to V_{BIAS}+0.3V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+230°C
Absolute Maximum Junction Temperature	+150°C

16 D.C. CHARACTERISTICS

T_A = -40°C to +85°C, V_{DD} = 3.3V ±10%, V_{DD} < BIAS < 5.5V
(Typical Conditions: T_A = 25°C, V_{DD} = 3.3V, V_{BIAS} = 5V)

Table 14: D.C Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Power Supply	2.97	3.3	3.63	Volts	
BIAS	5V Tolerant Bias	VDD	5.0	5.5	Volts	
V_{IL}	Input Low Voltage (TTL Only)	0		0.8	Volts	Guaranteed Input Low voltage.
V_{PIL}	Input Low Voltage (PECL Only)	A_{VD} - 1.8		A_{VD} - 1.6	Volts	Guaranteed Input Low voltage.
V_{IH}	Input High Voltage (TTL Only)	2.0			Volts	Guaranteed Input High voltage.
V_{PIH}	Input Low Voltage (PECL Only)	A_{VD} –1.0		A_{VD} –0.8	Volts	Guaranteed Input High voltage.
V_{OL}	Output or Bi-directional Low Voltage			0.4	Volts	Guaranteed output Low voltage at VDD=2.97V and I_{OL}=maximum rated for pad. Note 4.
V_{OH}	Output or Bi-directional High Voltage	2.4			Volts	Guaranteed output High voltage at VDD=2.97V and I_{OH}=maximum rated current for pad. Note 4.
V_{T+}	Reset Input High Voltage	2.0			Volts	Applies to RSTB and TRSTB only.
V_{T-}	Reset Input Low Voltage			0.8	Volts	Applies to RSTB and TRSTB only.
V_{TH}	Reset Input Hysteresis Voltage		TBD		Volts	Applies to RSTB and TRSTB only.

I_{ILPU}	Input Low Current	-100	-50	-4	µA	V_{IL} = GND. Notes 1 and 3.
I_{IHPU}	Input High Current	-10	0	+10	µA	$V_{IH} = V_{DD}$. Notes 1 and 3.
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND. Notes 2 and 3.
I_{IH}	Input High Current	-10	0	+10	µA	$V_{IH} = V_{DD}$. Notes 2 and 3.
C_{IN}	Input Capacitance		5		pF	t_A=25°C, f = 1 MHz
C_{OUT}	Output Capacitance		5		pF	t_A=25°C, f = 1 MHz
C_{IO}	Bi-directional Capacitance		5		pF	t_A=25°C, f = 1 MHz
I_{DDOP}	Operating Current		320	530	mA	V_{DD} = 3.63V, Outputs Unloaded

Notes on D.C. Characteristics:

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. Refer to the footnotes at the bottom of the PIN DESCRIPTION table for the DC current rating of each device output.

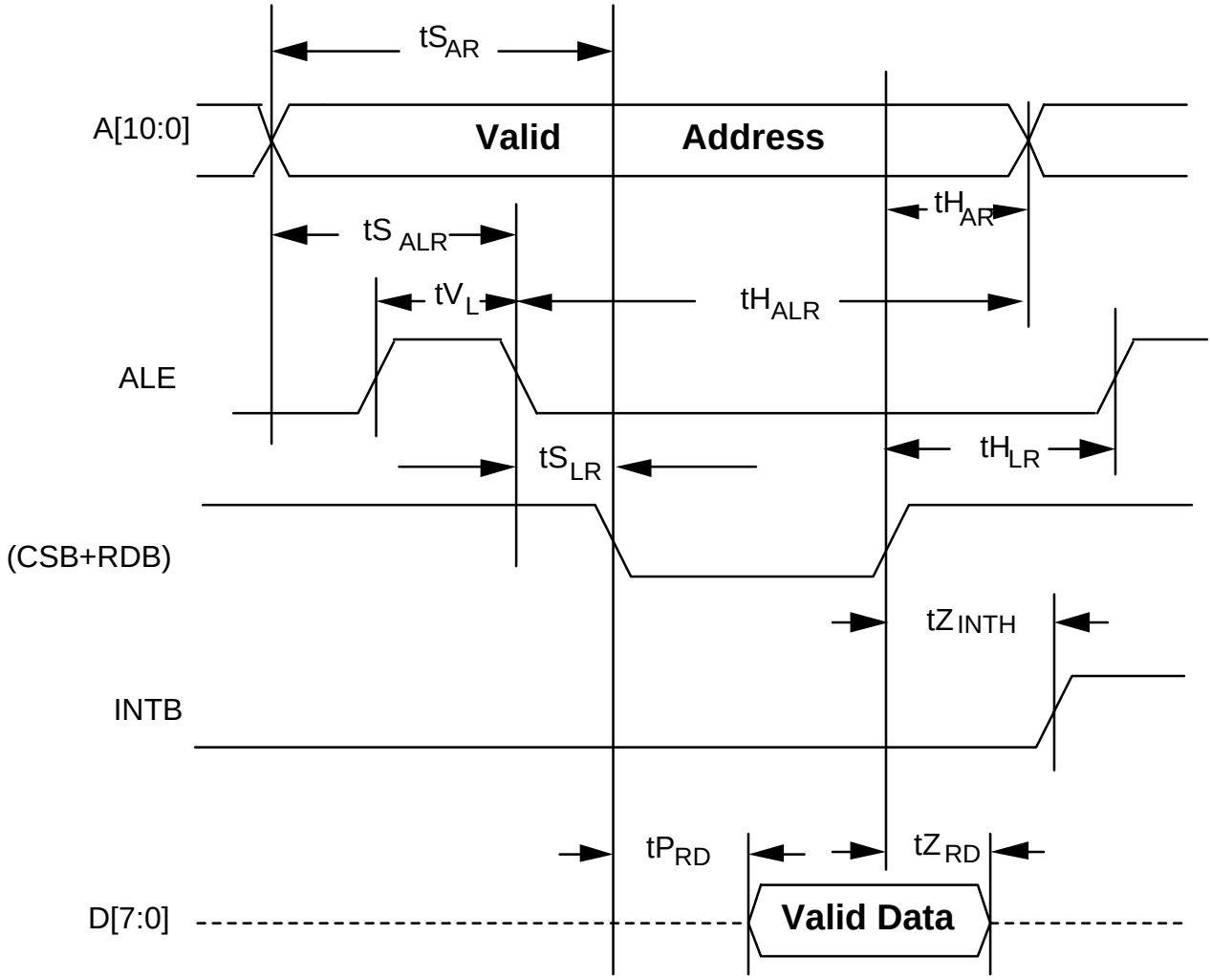
17 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T_A = -40°C to +85°C, V_{DD} = 3.3V ±10%)

Table 15: Microprocessor Interface Read Access (Figure 24)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	10		ns
tH_{AR}	Address to Valid Read Hold Time	5		ns
tS_{ALR}	Address to Latch Set-up Time	10		ns
tH_{ALR}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	5		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	5		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		70	ns
tZ_{RD}	Valid Read Negated to Output Tri-state		20	ns
tZ_{INTH}	Valid Read Negated to Output Tri-state		50	ns

Figure 24: Microprocessor Interface Read Timing



Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).

3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.

4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALR}, tH_{ALR}, tV_L, tS_{LR}, and tH_{LR} are not applicable.

5. Parameter tH_{AR} is not applicable if address latching is used.

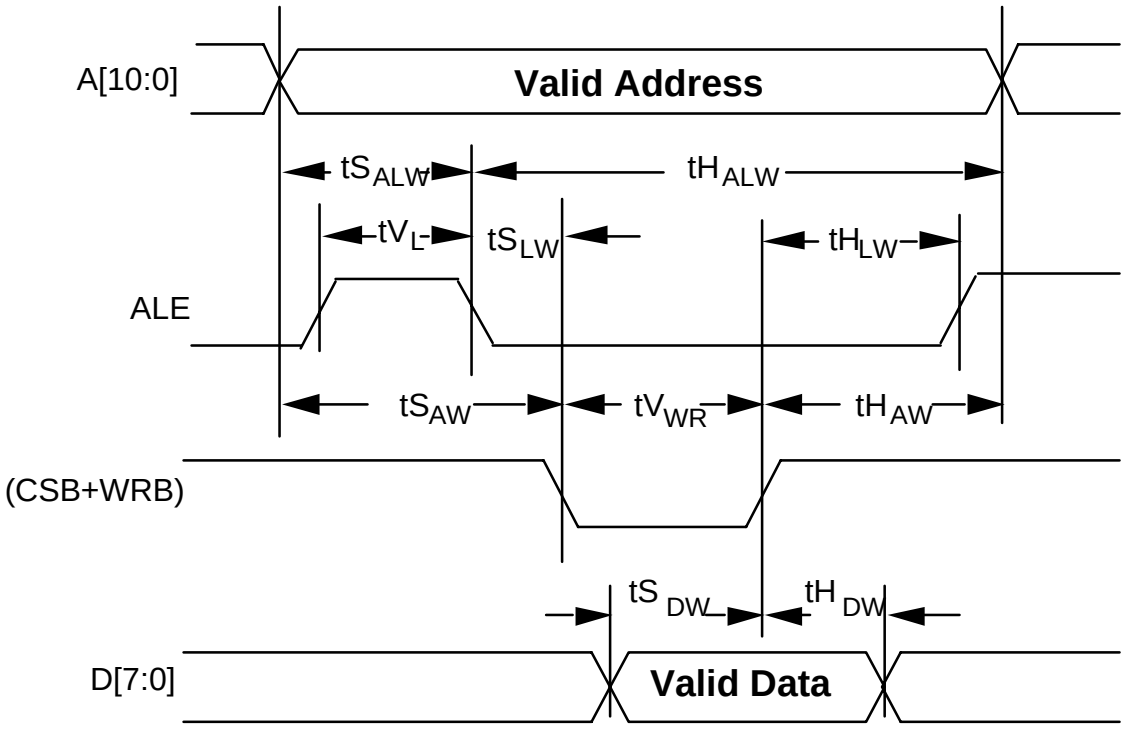
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 16: Microprocessor Interface Write Access (Figure 25)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	10		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	10		ns
tH_{ALW}	Address to Latch Hold Time	10		ns
tV_L	Valid Latch Pulse Width	5		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	5		ns
tH_{DW}	Data to Valid Write Hold Time	5		ns
tH_{AW}	Address to Valid Write Hold Time	5		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Figure 25: Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1 A valid write cycle is defined as a logical OR of the CSB and the WRB signals.

2 In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALW}, tH_{ALW}, tV_L, tS_{LW}, and tH_{LW} are not applicable.

3 Parameter tH_{AW} is not applicable if address latching is used.

4 When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

5 When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

18 A.C. TIMING CHARACTERISTICS

(T_A = -40°C to +85°C, V_{DD} = 3.3V ±10%)

18.1 System Reset Timing

Table 17: RSTB Timing (Figure 26)

Symbol	Description	Min	Max	Units
tV_{RSTB}	RSTB Pulse Width	100		ns

Figure 26: RSTB Timing Diagram

18.2 Reference Timing

Line Side Reference Clock

Symbol	Description	Min	Max	Units
	REFCLK Nominal Frequency	19.44	19.44	MHz
	REFCLK Duty Cycle	30	70	%
	REFCLK Frequency Tolerance	-50	+50	ppm

18.3 ATM System Interface Timing

Table 18: Transmit ATM System Interface Timing (Figure 27)

Symbol	Description	Min	Max	Units
f_{TFCLK}	TFCLK Frequency		50	MHz
D_{TFCLK}	TFCLK Duty Cycle	40	60	%
tS_{TENB}	TENB Set-up time to TFCLK	3		ns
tH_{TENB}	TENB Hold time to TFCLK	0		ns
tS_{TADR}	TADR[4:0] Set-up time to TFCLK	3		ns
tH_{TADR}	TADR[4:0] Hold time to TFCLK	0		ns
tS_{TDAT}	TDAT[15:0] Set-up time to TFCLK	3		ns
tH_{TDAT}	TDAT[15:0] Hold time to TFCLK	0		ns
tS_{TPRTY}	TPRTY Set-up time to TFCLK	3		ns
tH_{TPRTY}	TPRTY Hold time to TFCLK	0		ns
tS_{TSOC}	TSOC Set-up time to TFCLK	3		ns
tH_{TSOC}	TSOC Hold time to TFCLK	0		ns
tP_{DTCA}	TFCLK High to DTCA[4:1] Valid	1	12	ns
tP_{TCA}	TFCLK High to TCA Valid	1	12	ns
tZ_{TCA}	TFCLK High to TCA Tri-state	1	10	ns
tZB_{TCA}	TFCLK High to TCA Driven	0		ns

Figure 27: Transmit ATM System Interface Timing Diagram

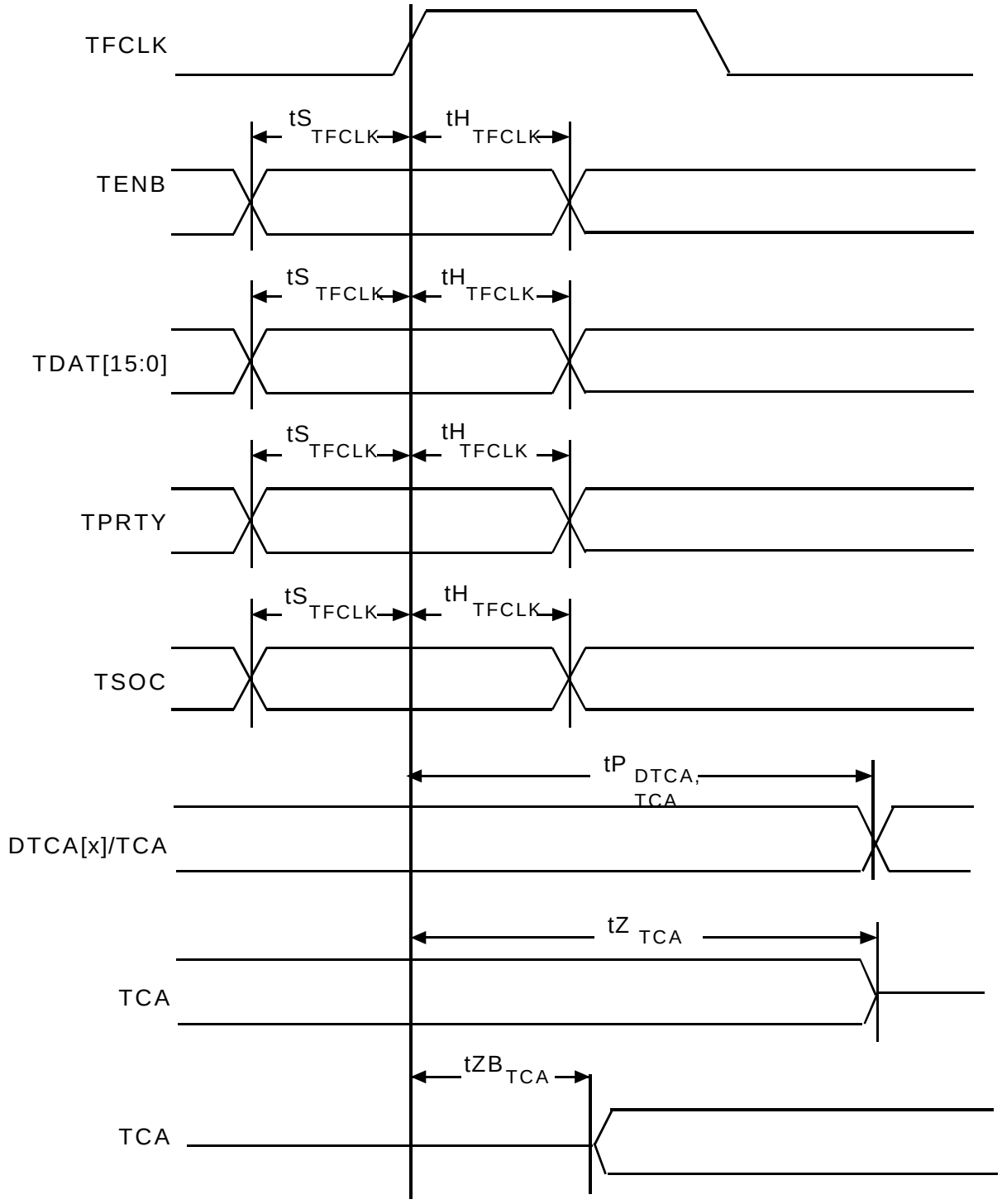
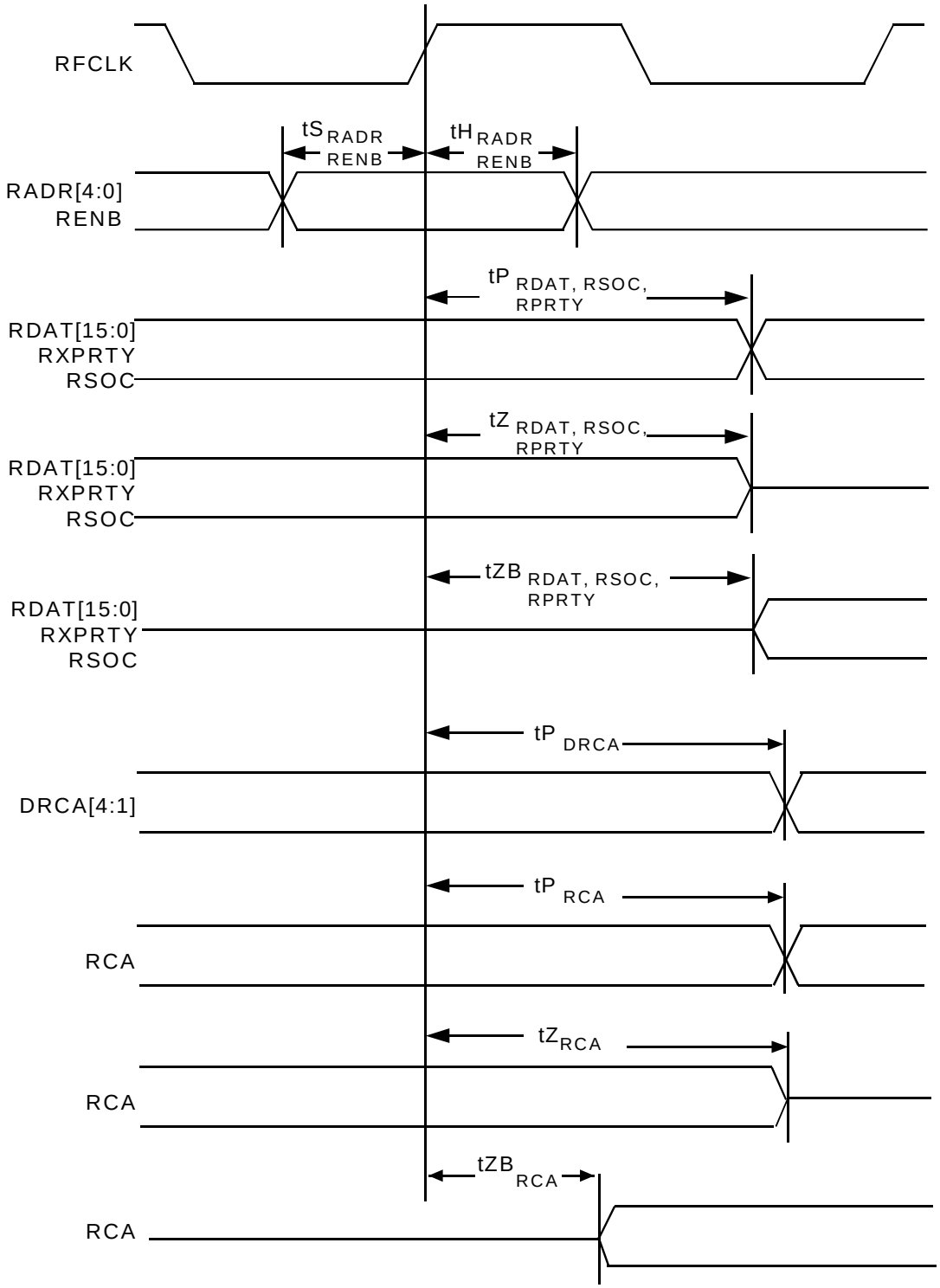


Table 19: Receive ATM System Interface Timing (Figure 28)

Symbol	Description	Min	Max	Units
f_{RFCLK}	RFCLK Frequency		50	MHz
D_{RFCLK}	RFCLK Duty Cycle	40	60	%
tS_{RENB}	RENB Set-up time to RFCLK	3		ns
tH_{RENB}	RENB Hold time to RFCLK	0		ns
tS_{RADR}	RADR[4:0] Set-up time to RFCLK	3		ns
tH_{RADR}	RADR[4:0] Hold time to RFCLK	0		ns
tP_{RDAT}	RFCLK High to RDAT Valid	1	12	ns
tZ_{RDAT}	RFCLK High to RDAT Tri-state	1	12	ns
tZB_{RDAT}	RFCLK High to RDAT Driven	0		ns
tP_{RSOC}	RFCLK High to RSOC Valid	1	12	ns
tZ_{RSOC}	RFCLK High to RSOC Tri-state	1	12	ns
tZB_{RSOC}	RFCLK High to RSOC Driven	0		ns
tP_{RPRTY}	RFCLK High to RPRTY Valid	1	12	ns
tZ_{RPRTY}	RFCLK High to RPRTY Tri-state	1	12	ns
tZB_{RPRTY}	RFCLK High to RPRTY Driven	0		ns
tP_{RCA}	RFCLK High to RCA Valid	1	12	ns
tZ_{RCA}	RFCLK High to RCA Tri-state	1	12	ns
tZB_{RCA}	RFCLK High to RCA Driven	0		ns
tP_{DRCA}	RFCLK High to DRCA[4:1] Valid	1	12	ns

Figure 28: Receive ATM System Interface Timing Diagram

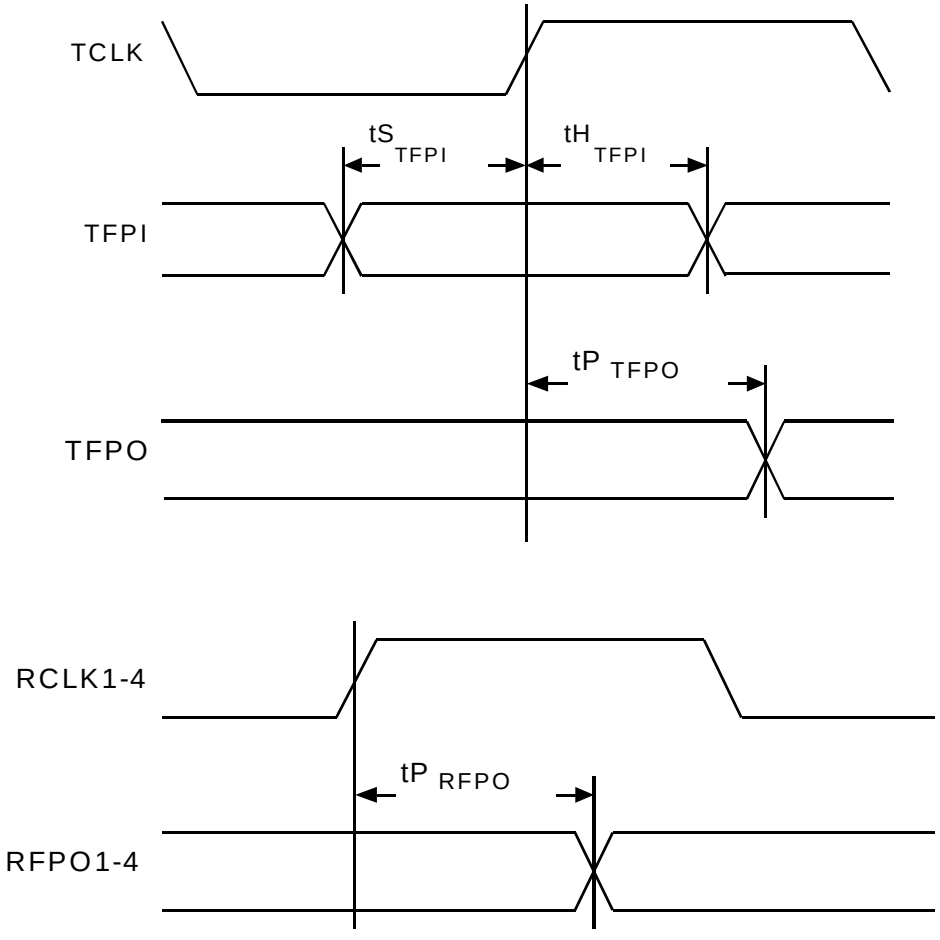


18.4 Transmit and Receive Frame Pulses

Table 20: Transmit and Receive Frame Pulse Timing (Figure 29)

Symbol	Description	Min	Max	Units
tS_{TFPI}	TFPI Set-up Time to TCLK High	15		ns
tH_{TFPI}	TFPI Hold Time to TCLK High	0		ns
tP_{TFPO}	TCLK High to TFPO Valid	0	10	ns
tP_{RFPO}	RCLK1-4 High to RFPO1-4 Valid	0	10	ns

Figure 29: Transmit and Receive Frame Pulses

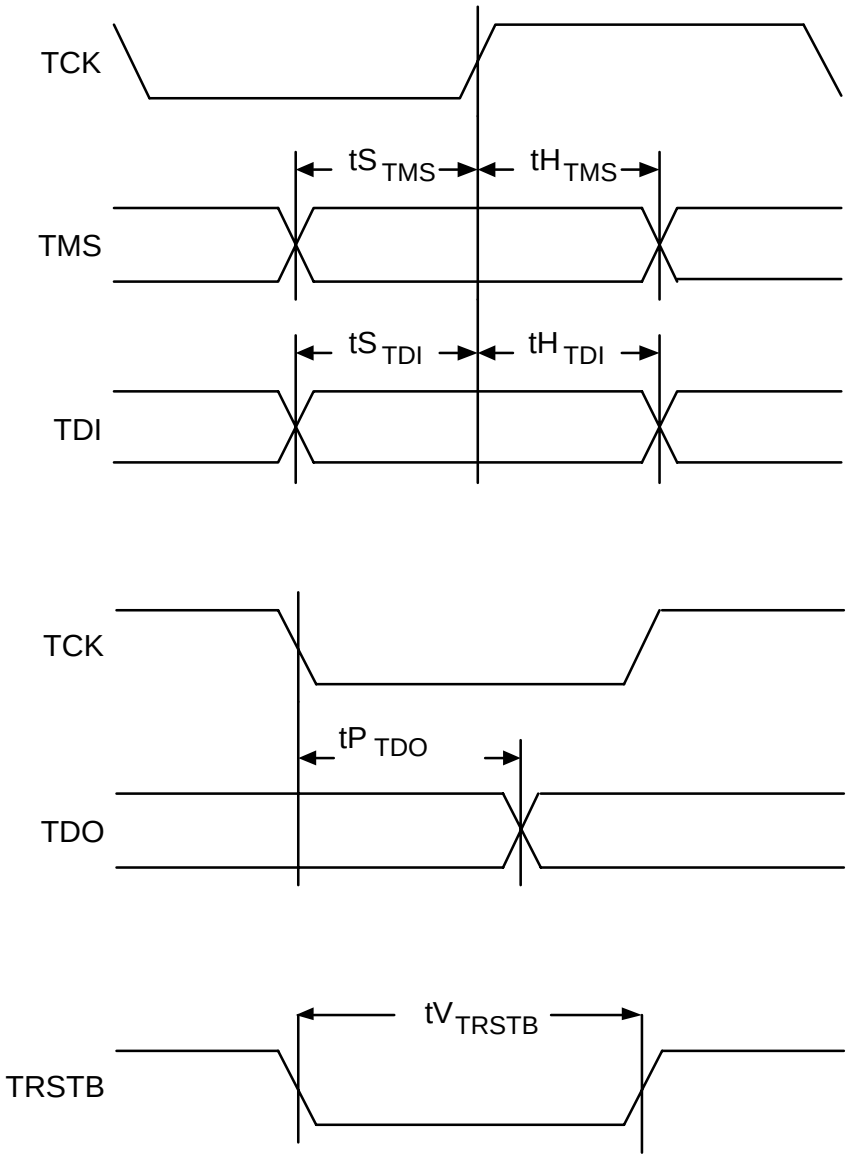


18.5 JTAG Test Port Timing

Table 21: JTAG Port Interface (Figure 30)

Symbol	Description	Min	Max	Units
	TCK Frequency		1	MHz
	TCK Duty Cycle	40	60	%
tSTMS	TMS Set-up time to TCK	50		ns
tHTMS	TMS Hold time to TCK	50		ns
tSTDI	TDI Set-up time to TCK	50		ns
tHTDI	TDI Hold time to TCK	50		ns
tPTDO	TCK Low to TDO Valid	2	50	ns
tVTRSTB	TRSTB Pulse Width	100		ns

Figure 30: JTAG Port Interface Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 50 pF load on the outputs with the exception of the RDAT[15:0], RPRTY, RSOC, RCA, DRCA[4:1], TCA, DTCA[4:1] for which propagation delays are measured with a 30 pF load.

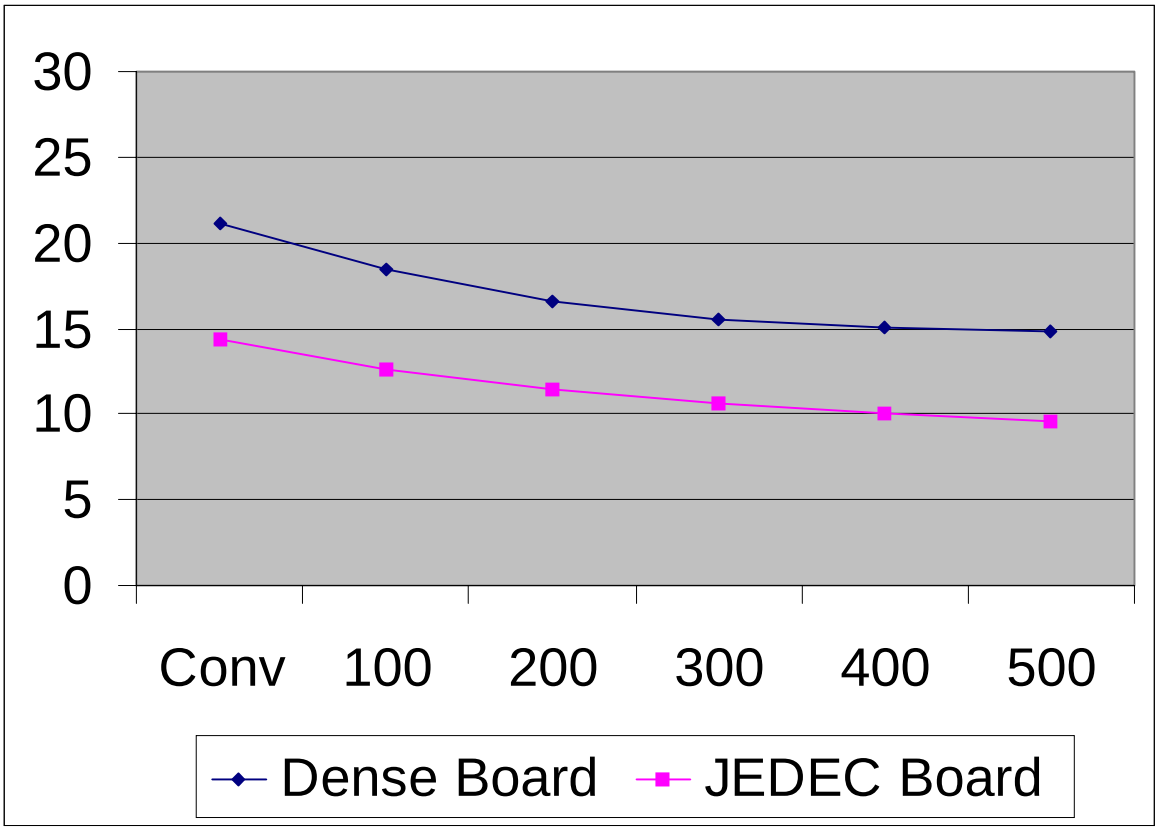
19 ORDERING AND THERMAL INFORMATION

Table 22: Ordering Information

PART NO.	DESCRIPTION
PM5349-BI	304-pin Ball Grid Array (SBGA)

Table 23: Thermal Information

PART NO.	AMBIENT TEMPERATURE	Theta Ja	Theta Jc
PM5349-BI	-40°C to 85°C	22 °C/W	1 °C/W



The junction temperature (Tj) is less than 105°C for a ambient temperature (Ta) of 60°C and a 300LFM of airflow. The device must operate at Ta=70°C with 100LFM and must not be damaged with Ta=70°C and no airflow. This assumes a dense board and a ThetaJA of 16.

Loaded power at 3.63V with TXC pins enable, mean = 2.83W

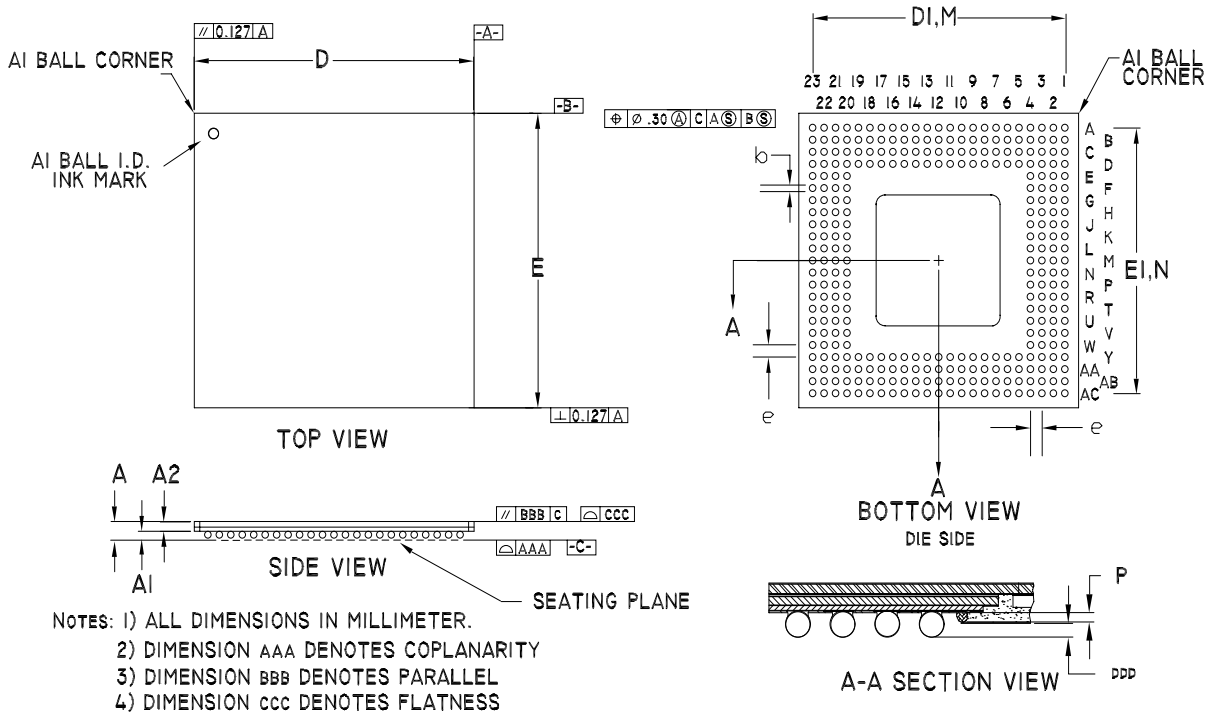
Loaded power at 3.63V with TXC pins enable, mean + 2 sigma = 2.89W

The junction temperature = 105°C.

Therefore, the package is approved for use without enhanced cooling.

20 MECHANICAL INFORMATION

Figure 31:- Mechanical Drawing 304 Pin Super Ball Grid Array (SBGA)



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION AAA DENOTES COPLANARITY
3) DIMENSION BBB DENOTES PARALLEL
4) DIMENSION CCC DENOTES FLATNESS

PACKAGE TYPE: 304 PIN THERMAL BALL GRID ARRAY															
BODY SIZE: 31 x 31 x 1.45 MM															
DIM.	A	A1	A2	D	D1	E	E1	M,N	e	b	AAA	BBB	CCC	DDD	P
MIN.	1.41	0.56	0.85	30.90	27.84	30.90	27.84			0.60				0.15	0.20
NOM.	1.54	0.63	0.91	31.00	27.94	31.00	27.94	23x23	1.27	0.75				0.33	0.30
MAX.	1.67	0.70	0.97	31.10	28.04	31.10	28.04			0.90	0.15	0.15	0.20	0.50	0.35

NOTES

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