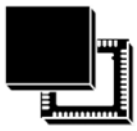
PM6600

6-rows 30 mA LEDs driver with boost regulator for LCD panels backlight

Features

- Boost section
  - 4.7 V to 28 V input voltage range
  - Internal power MOSFET
  - Internal +5 V LDO for device supply
  - Up to 36 V output voltage
  - Constant frequency peak current-mode control
  - 200 kHz to 1 MHz adjustable switching frequency
  - External synchronization for multi-device application
  - Pulse-skip power saving mode at light load
  - Programmable soft-start
  - Programmable OVP protection
  - Stable with ceramic output capacitors
  - Thermal shutdown
- Backlight driver section
  - Six rows with 30 mA maximum current capability (adjustable)
  - Up to 10 WLEDs per row
  - Unused rows detection
  - 500 ns minimum dimming time (1 % minimum dimming duty-cycle at 20 kHz)
  - ±2.1 % current accuracy
  - ±2 % current matching between rows
  - LED failure (open and short circuit) detection



VFQFPN-24 4x4

Description

The PM6600 consists of a high efficiency monolithic boost converter and six controlled current generators (ROWs), specifically designed to supply LEDs arrays used in the backlight of LCD panels. The device can manage a nominal output voltage up to 36 V (i.e. 10 White-LEDs per ROW). The generators can be externally programmed to sink up to 30 mA and they can be dimmed via a PWM signal (1% dimming duty-cycle at 20 kHz can be managed). The device allows to detect and manage the open and shorted LED faults and to let unused ROWs floating. Basic protections (Output Over-Voltage, internal MOSFET Over-Current and Thermal Shutdown) are provided.

Applications

- Notebook monitors backlight
- UMPC backlight

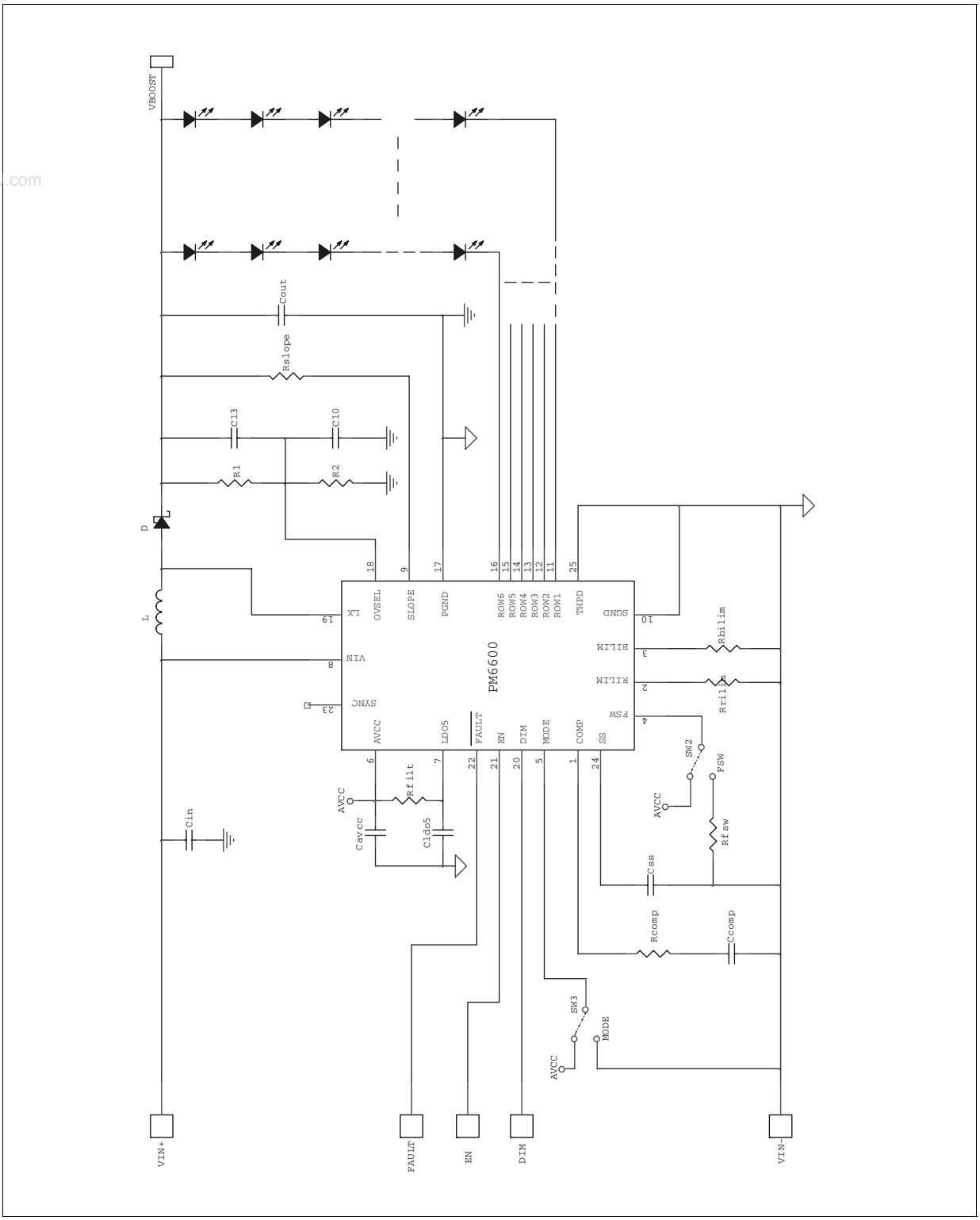
Table 1. Device summary

Part number	Package	Packaging
PM6600	VFQFPN-24 4x4 (exposed pad)	Tube
PM6600TR		Tape and reel

Contents

1 Typical application circuit

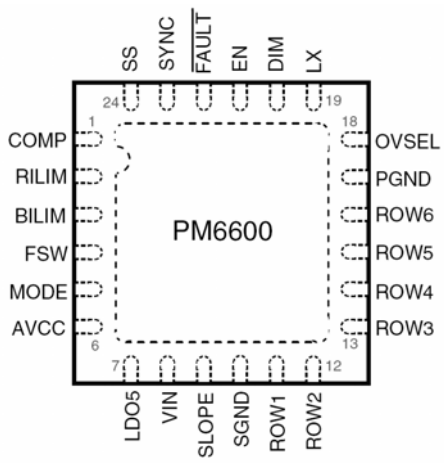
Figure 1. Application circuit



2 Pin settings

2.1 Connections

Figure 2. Pin connection (through top view)



2.2 Pin description

Table 2. Pin functions

N°	Pin	Function
1	COMP	Error amplifier output. A simple RC series between this pin and ground is needed to compensate the loop of the boost regulator.
2	RILIM	Output generators current limit setting. The output current of the ROWs can be programmed connecting a resistor to SGND.
3	BILIM	Boost converter current limit setting. The internal MOSFET current limit can be programmed connecting a resistor to SGND.
4	FSW	Switching frequency selection and external sync input. A resistor to SGND is used to set the desired switching frequency. The pin can also be used as external synchronization input. See section 1.3 for details.
5	MODE	Current generators fault management selector. It allows to detect and manage LEDs failures. See section 3.2 for details.
6	AVCC	+5 V analog supply. Connect to LDO5 through a simple RC filter.
7	LDO5	Internal +5 V LDO output and power section supply. Bypass to SGND with a 1 µF ceramic capacitor.
8	VIN	Input voltage. Connect to the main supply rail.

Table 2. Pin functions (continued)

N°	Pin	Function
9	SLOPE	Slope compensation setting. A resistor between the output of the boost converter and this pin is needed to avoid sub-harmonic instability. Refer to section 1.4 for details.
10	SGND	Signal ground. Supply return for the analog circuitry and the current generators.
11	ROW1	Row driver output #1.
12	ROW2	Row driver output #2.
13	ROW3	Row driver output #3.
14	ROW4	Row driver output #4.
15	ROW5	Row driver output #5.
16	ROW6	Row driver output #6.
17	PGND	Power ground. Source of the internal power-MOSFET.
18	OVSEL	Over-voltage selection. Used to set the desired OV threshold by an external divider. See section 1.2 for details.
19	LX	Switching node. Drain of the internal power-MOSFET.
20	DIM	Dimming input. Used to externally set the brightness of the LEDs by using a PWM signal.
21	EN	Enable input. When low, the device is turned off. If tied high or left floating, the device is turned on and a Soft-Start sequence takes place.
22	FAULT	Fault signal output. Open drain output. The pin goes low when a fault condition is detected (see section 3.1 for details).
23	SYNC	Synchronization output. Used as external synchronization output.
24	SS	Soft start. Connect a capacitor to SGND to set the desired Soft-Start duration.

3 Electrical data

3.1 Maximum rating

Table 3. Absolute maximum ratings (1)

Symbol	Parameter	Value	Unit
V_{AVCC}	AVCC to SGND	-0.3 to 6	V
V_{LDO5}	LDO5 to SGND	-0.3 to 6	
	PGND to SGND	-0.3 to 0.3	
V_{IN}	VIN to PGND	-0.3 to 40	
V_{LX}	LX to SGND	-0.3 to 40	
	LX to PGND	-0.3 to 40	
	RILIM, BILIM, SYNC, OVSEL, SS to SGND	-0.3 to V_{AVCC} + 0.3	
	EN, DIM, FSW, MODE, FAULT to SGND	-0.3 to 6	
	ROWx to PGND/ SGND	-0.3 to 40	
	SLOPE to VIN	V_{IN} - 0.3 to V_{IN} + 6	
	SLOPE to SGND	-0.3 to 40	
	Maximum LX RMS current	2.0	A
P_{TOT}	Power dissipation @=25°C	2.3	W
	Maximum withstanding voltage range test condition: CDF-AEC-Q100-002- “Human Body Model” acceptance criteria: “Normal Performance”	±1000	V

1. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient	42	°C/W
T_{STG}	Storage temperature range	-50 to 150	°C
T_J	Junction operating temperature range	-40 to 125	°C
T_A	Operating ambient temperature range	-40 to 85	°C

3.3 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter		Values			Unit
			Min	Typ	Max	
Supply section						
V_{IN}	Input voltage range		4.7		28	V
Boost section						
V_{BST}	Output voltage range				36	V
f_{SW}	Adjustable switching frequency	FSW connected to R_{FSW}	200		1000	kHz
	FSW sync input Duty-Cycle				40	%
	ROWs output maximum current				30	mA

4 Electrical characteristics

V_{IN} = 12 V; T_A = 0 °C to 85 °C and MODE connected to AVCC unless specified [1].

Table 6. Electrical characteristics

Symbol	Parameter	Test condition	Values			Unit
			Min	Typ	Max	
Supply section						
V_{LDO5}, V_{AVCC}	LDO output and IC supply voltage	EN High, I_{LDO5} = 0 mA	4.6	5	5.5	V
$I_{IN,Q}$	Operating quiescent current	R_{RILIM} = 51 kΩ, R_{BILIM} = 220 kΩ, R_{SLOPE} = 680 kΩ DIM tied to SGND.		1		mA
$I_{IN,SHDN}$	Operating current in shutdown	EN low		20	30	µA
$V_{UVLO,ON}$	LDO5 under voltage lockout upper threshold			4.6	4.75	V
$V_{UVLO,OFF}$	LDO5 under voltage lockout lower threshold		3.8	4.0		
LDO linear regulator						
	Line regulation	6 V = V_{IN} = 28 V, I_{LDO5} = 30 mA			25	mV
	LDO dropout voltage	V_{IN} = 4.3 V, I_{LDO5} = 10 mA		80	120	
	LDO maximum output current limit	V_{LDO5} > $V_{UVLO,ON}$	25	40	60	mA
		V_{LDO5} < $V_{UVLO,OFF}$			30	

1. T_A = T_J. All parameters at operating temperature extremes are guaranteed by design and statistical analysis (not production tested)

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Values			Unit
			Min	Typ	Max	
Boost section						
$t_{on,min}$	Minimum switching on time				200	ns
	Default switching frequency	FSW connected to AVCC	570	660	750	kHz
	Minimum FSW Sync frequency			210		
	FSW Sync Input low level threshold		240			mV
	FSW Sync Input hysteresis			60		
	FSW Sync Min ON time				270	ns
	SYNC output Duty-Cycle	FSW connected to AVCC (Internal Oscillator Selected)		34	40	%
	SYNC output High Level	I_{SYNC} = 10 uA	V_{AVCC} -20			mV
	SYNC output Low Level	I_{SYNC} = -10 uA			20	
Power switch						
K_B	LX current coefficient	R_{BILIM} = 300 kΩ	5.7e5	6.7e5	7.7e5	V
	Internal MOSFET RDSon			280	500	mΩ
OV protections						
$V_{TH,OVP}$	Over-voltage protection reference (OVSEL) threshold		1.190	1.235	1.280	V
$V_{TH,FRD}$	Floating ROWs detection (OVSEL) threshold		1.100	1.145	1.190	
$\Delta V_{OVP,FRD}$	Voltage gap between the OVP and FRD thresholds			90		mV

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Values			Unit
			Min	Typ	Max	
Soft start and power management						
	EN, Turn-On level threshold				1.6	V
	EN, Turn-Off level threshold		0.8			
	DIM, high level threshold				1.3	
	DIM, low level threshold		0.8			
	EN, Pull-up current			2.5		µA
	SS, charge current		4	5	6	
	SS, End-Of-Startup threshold		2	2.4	2.8	V
	SS, Reduced switching frequency Release threshold			0.8		
Current generators section						
$T_{DIM-ON,min}$	Minimum dimming On-Time	R_{RILIM} = 51 kΩ		500		ns
K_R	ROWs current coefficient accuracy	R_{RILIM} = 51 kΩ		998	±21	V
ΔI_{ROWx}	ROWs current mismatch(1)	R_{RILIM} = 51 kΩ			±2	%
V_{IFB}	Feedback regulation voltage	No LEDs mismatch		400		mV
$V_{TH,FAULT}$	Shorted LED fault detection threshold			8.2		V
$V_{FAULT,LOW}$	FAULT pin low-level voltage	$I_{FAULT,SINK}$ = 4 mA			350	mV
Thermal shutdown						
T_{SHDN}	Thermal shutdown Turn-off temperature			150		°C

Note: The Current Mismatch is the maximum current difference among the ROWs of one device.

5 Typical operating characteristics

All the measures are done with a standard PM6600EVAL demoboard and a standard WLED6021NB demoboard, with the components listed in the EVAL_KIT document.

The measures are done with this working conditions, unless specified:

- Vin = 12 V
- Vout = 6 rows x 10 WLEDs = 34 V (typ)
- Iout = 20 mA each row
- fsw = 660 kHz (nominal switching frequency, with FSW .. AVCC)
- Vrow1 to Vrow6 = {0.697, 0.75, 0.818, 0.696, 0.822, 0.363} V

Figure 3. Efficiency vs DIM duty cycle @ f_{DIM} = 200 Hz

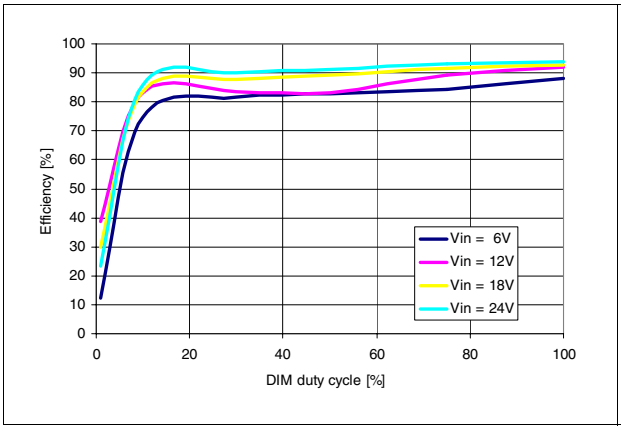


Figure 4. Efficiency vs DIM duty cycle @ f_{DIM} = 500 Hz

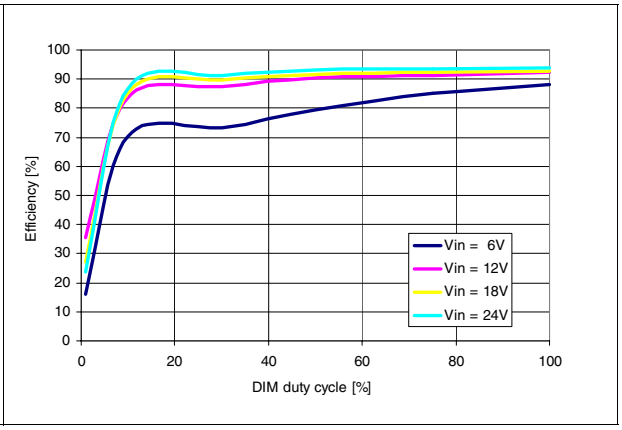


Figure 5. Efficiency vs DIM duty cycle @ f_{DIM} = 1 kHz

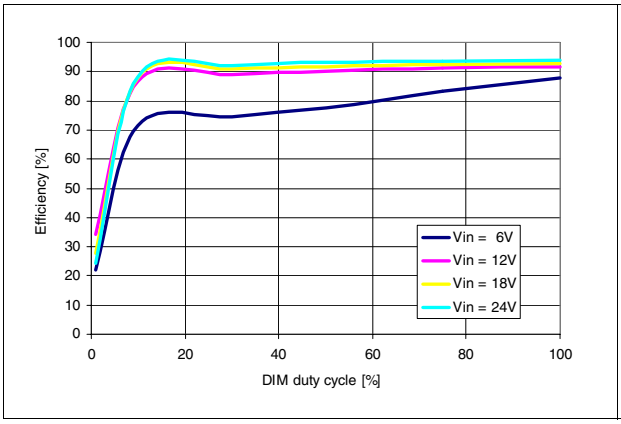


Figure 6. Efficiency vs DIM duty cycle @ f_{DIM} = 5 kHz

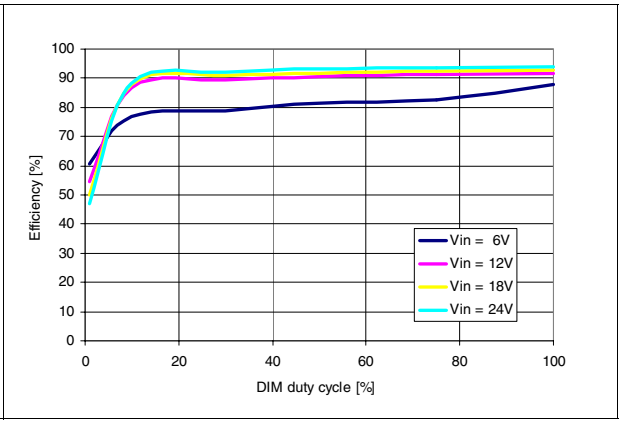


Figure 7. Efficiency vs DIM duty cycle @ f_{DIM} = 10 kHz

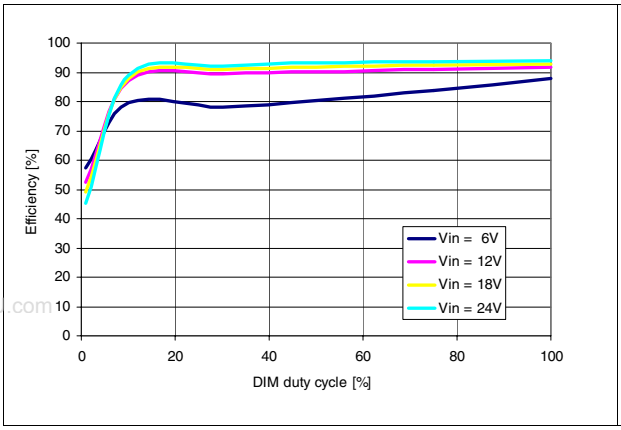


Figure 8. Efficiency vs DIM duty cycle @ f_{DIM} = 20 kHz

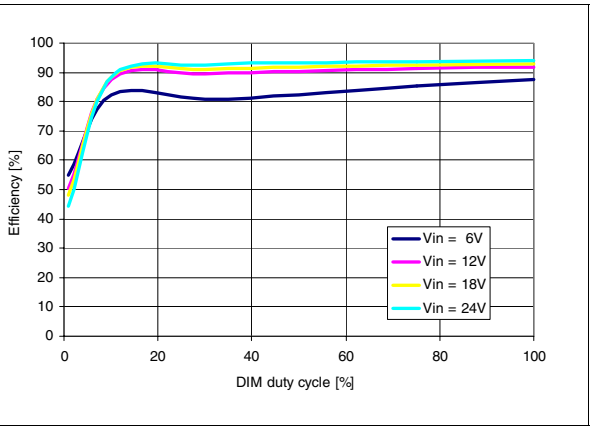


Figure 9. Efficiency vs DIM duty cycle @ Vin = 8 V

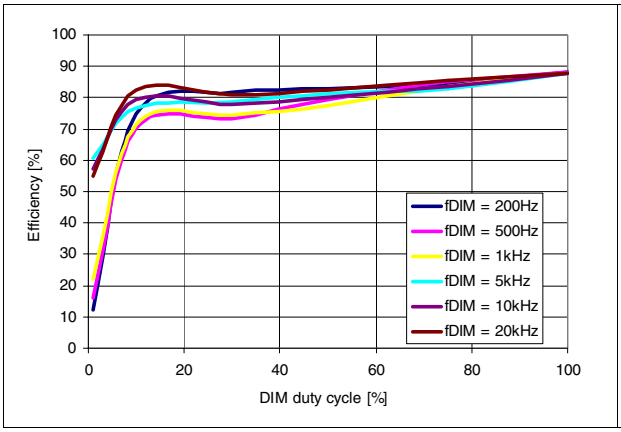


Figure 10. Efficiency vs DIM duty cycle @ Vin = 12 V

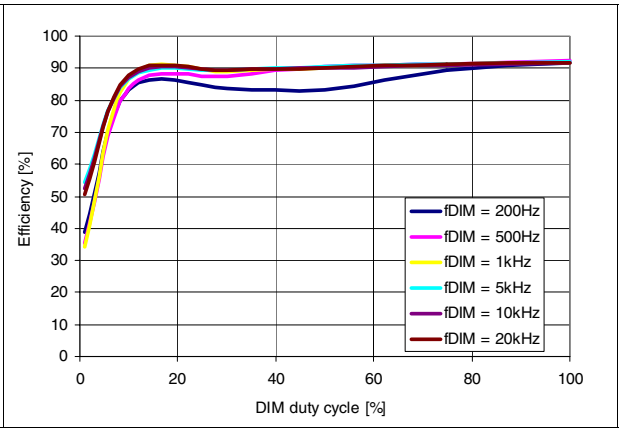


Figure 11. Efficiency vs DIM duty cycle @ Vin = 18 V

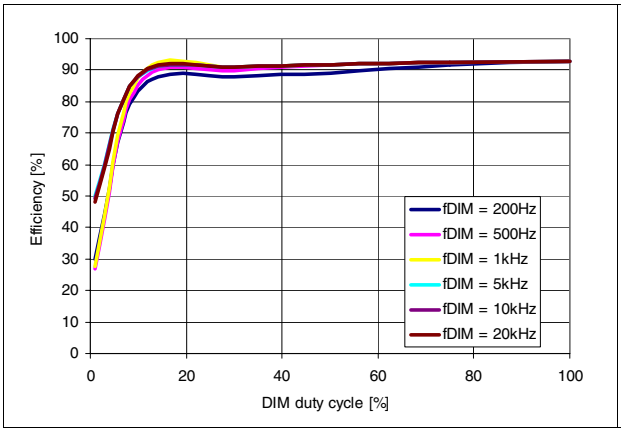


Figure 12. Efficiency vs DIM duty cycle @ Vin = 24 V

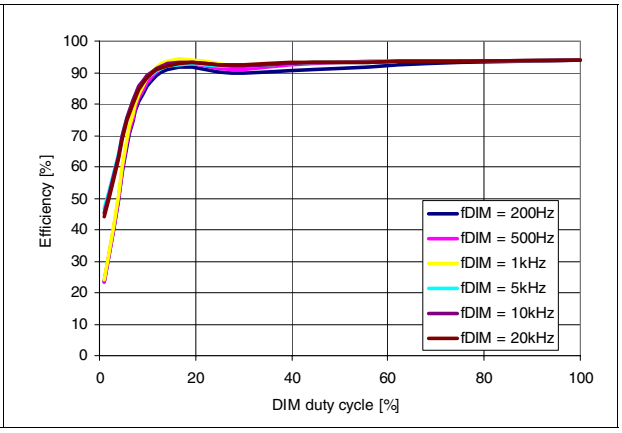


Figure 13. Efficiency vs Vin @ DIM duty cycles = 10 %

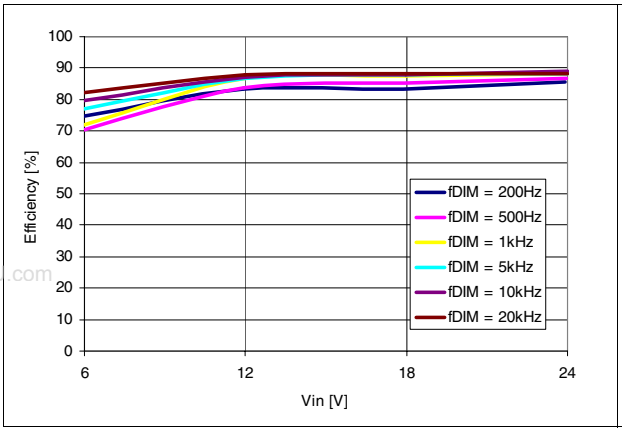


Figure 14. Efficiency vs Vin @ DIM duty cycles = 50 %

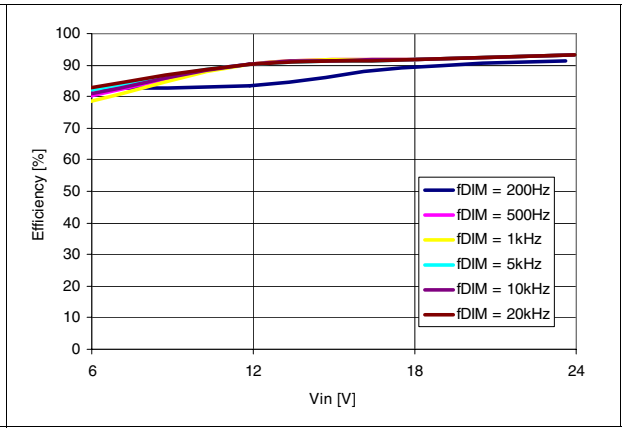


Figure 15. Efficiency vs Vin @ DIM duty cycles = 75 %

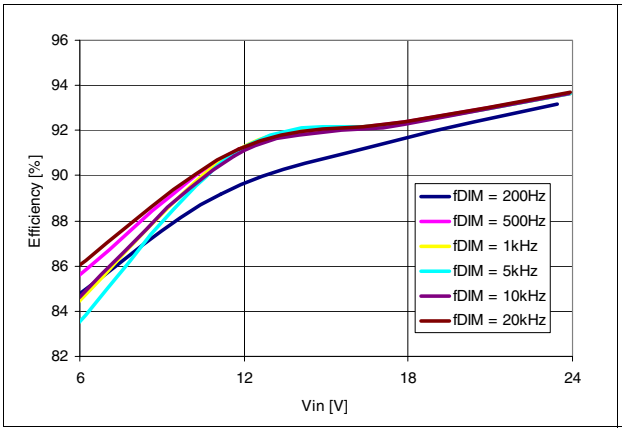


Figure 16. Efficiency vs Vin @ DIM duty cycles = 100 %

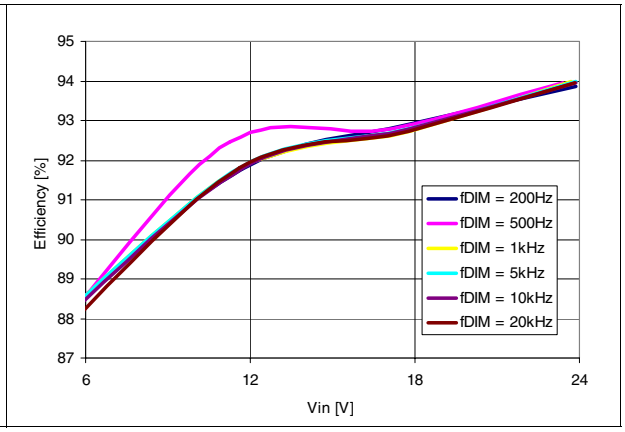


Figure 17. Working waveforms @ f_{DIM} = 100 Hz, D = 1 %

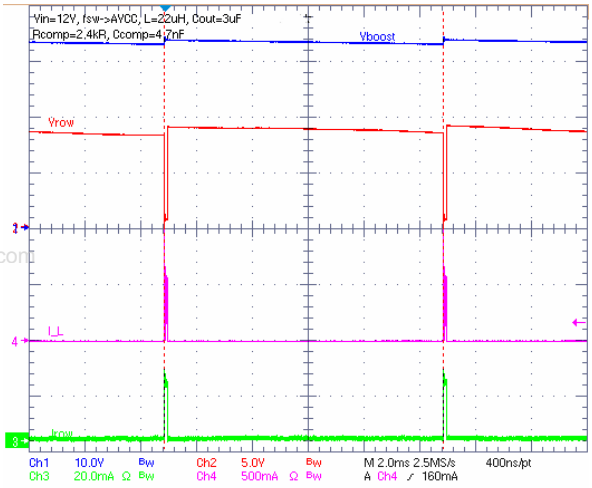


Figure 18. Working waveforms @ f_{DIM} = 100 Hz, D = 10 %

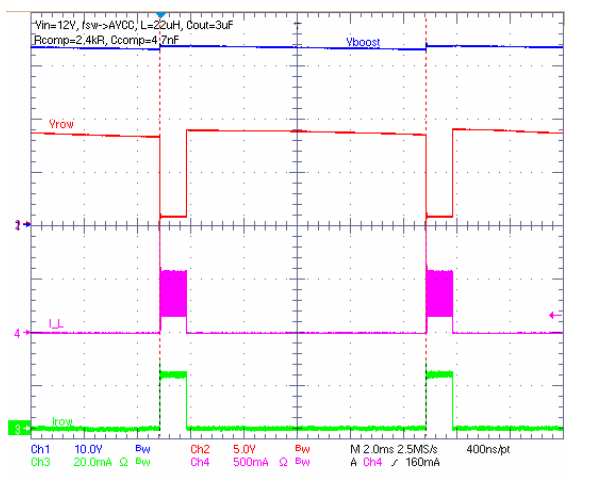


Figure 19. Working waveforms @ f_{DIM} = 100 Hz, D = 50 %

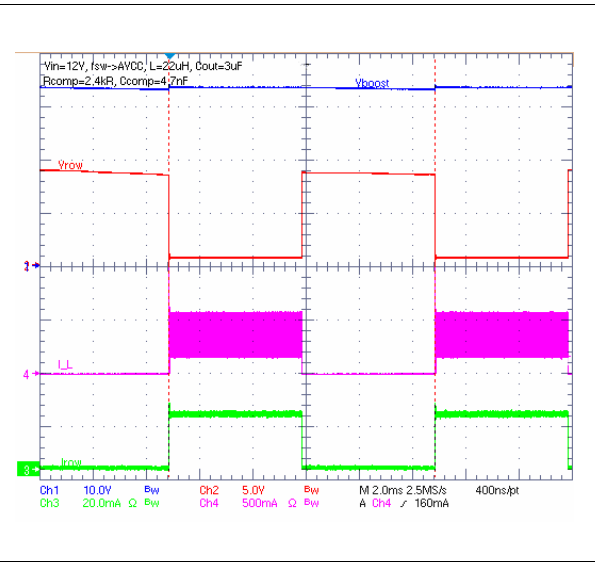


Figure 20. Working waveforms @ f_{DIM} = 100 Hz, D = 80 %

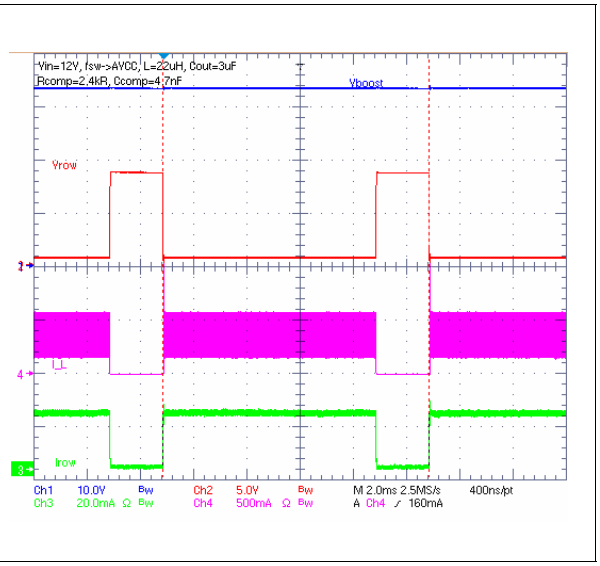


Figure 21. Working waveforms @ f_{DIM} = 200 Hz, D = 1 %

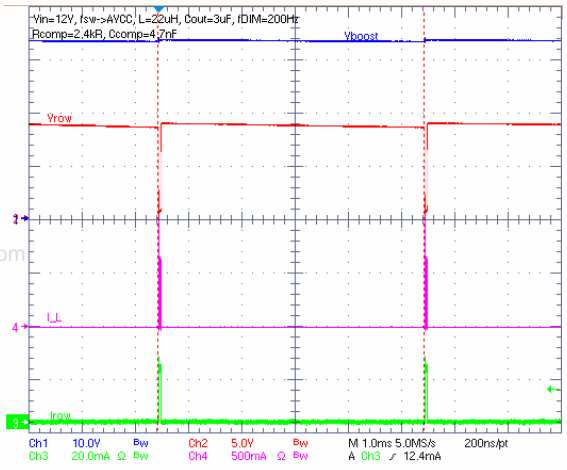


Figure 22. Working waveforms @ f_{DIM} = 200 Hz, D = 20 %

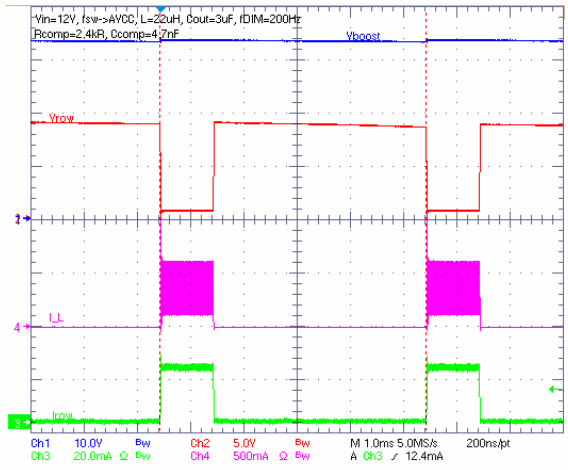


Figure 23. Working waveforms @ f_{DIM} = 200 Hz, D = 50 %

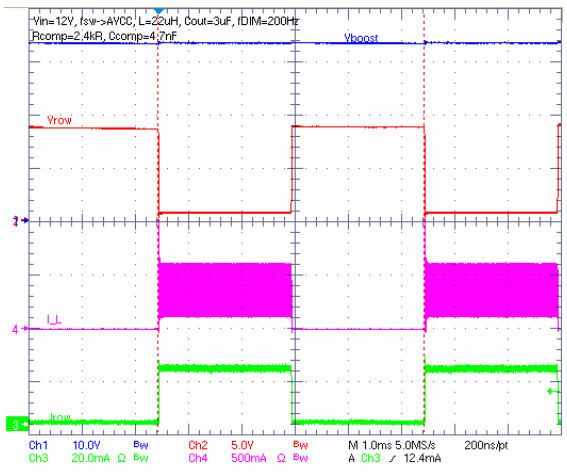


Figure 24. Working waveforms @ f_{DIM} = 200 Hz, D = 80 %

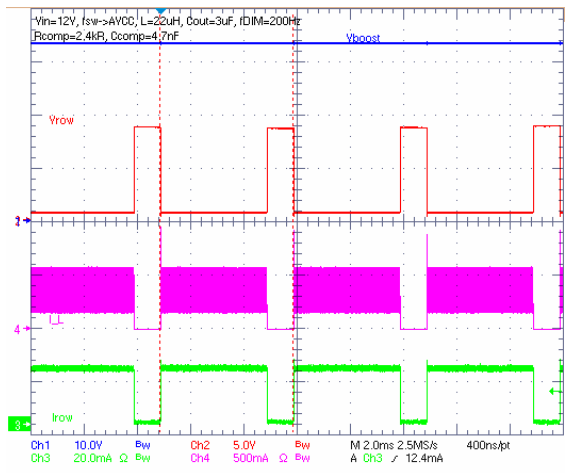


Figure 25. Working waveforms @ f_{DIM} = 500 Hz, D = 1 %

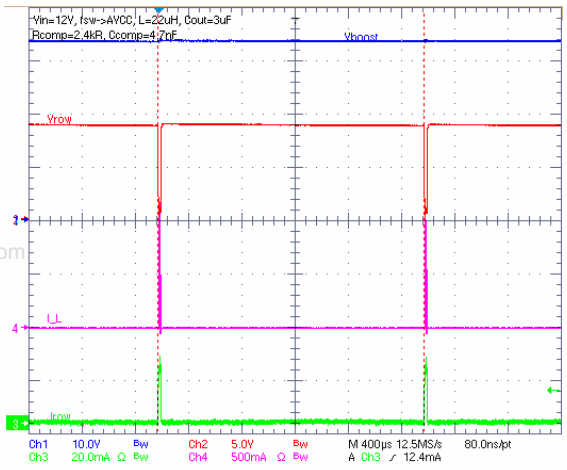


Figure 26. Working waveforms @ f_{DIM} = 500 Hz, D = 50 %

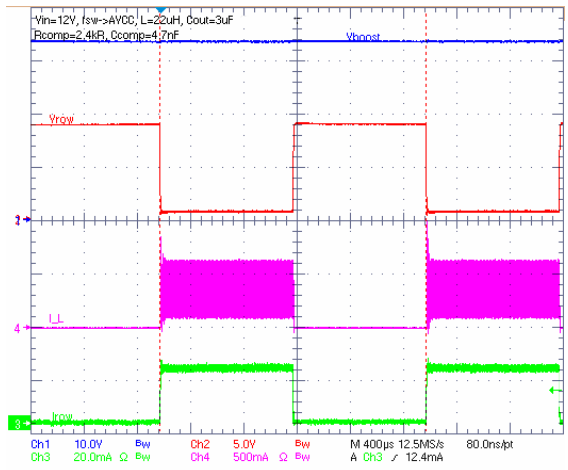


Figure 27. Working waveforms @ f_{DIM} = 1 kHz, D = 1%

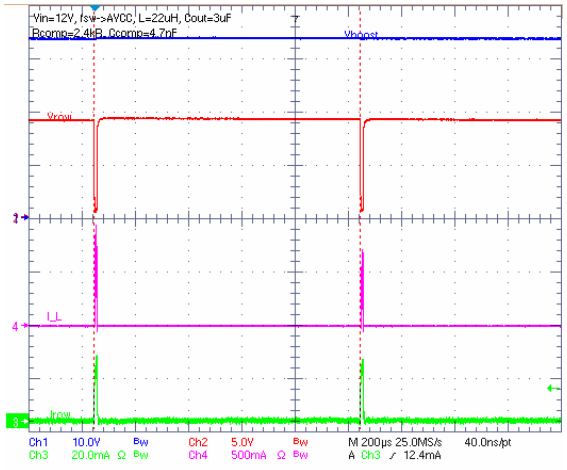


Figure 28. Working waveforms @ f_{DIM} = 1 kHz, D = 50 %

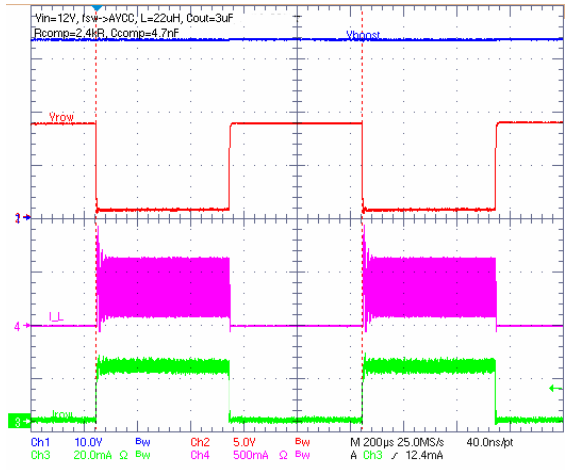


Figure 29. Working waveforms @ f_{DIM} = 10 kHz, D = 1 %

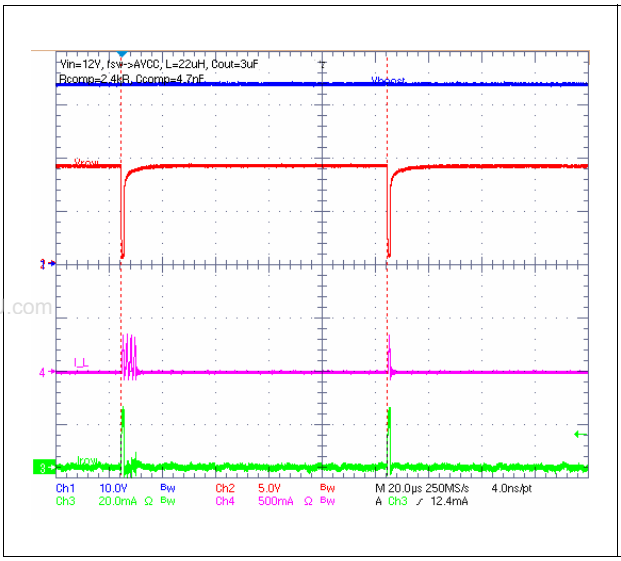


Figure 30. Working waveforms @ f_{DIM} = 10 kHz, D = 50 %

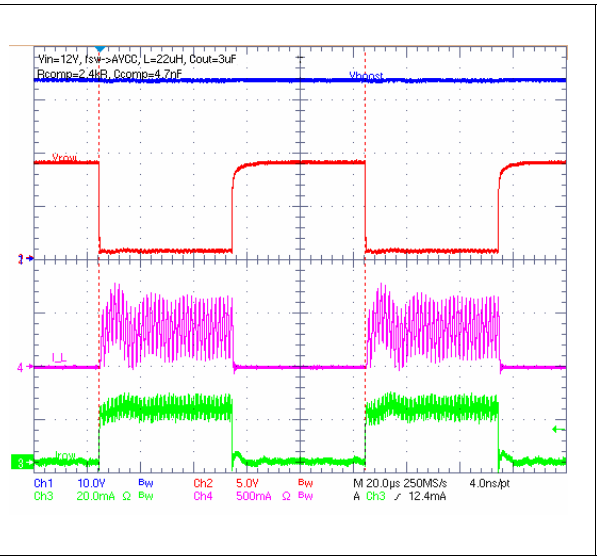


Figure 31. Working waveforms @ f_{DIM} = 20 kHz, D = 1 %

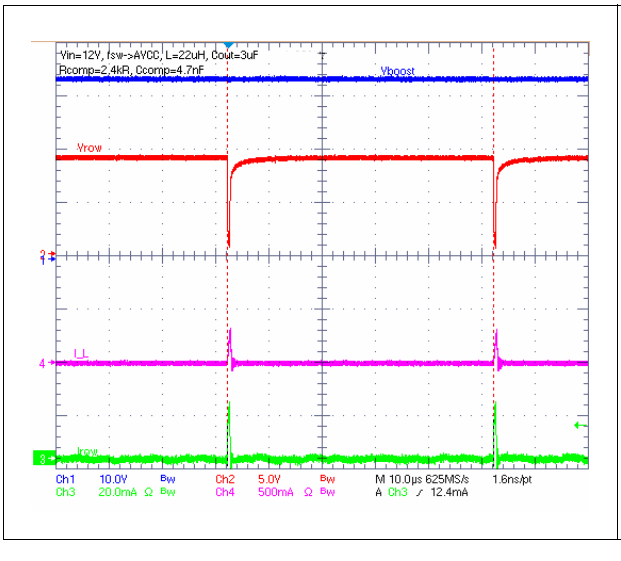


Figure 32. Working waveforms @ f_{DIM} = 20 Hz, D = 50 %

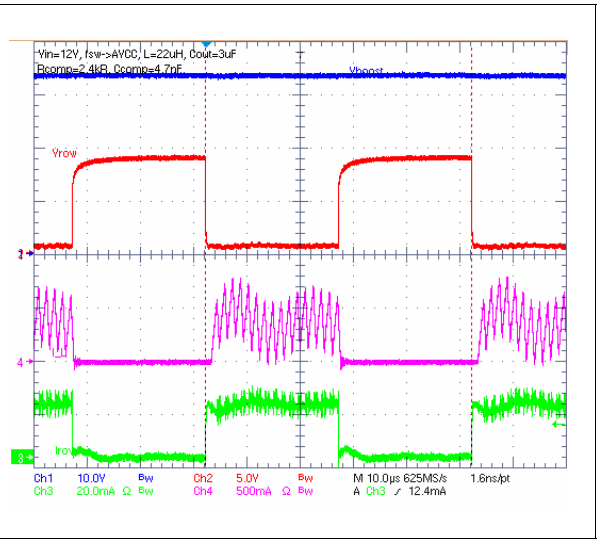


Figure 33. Output voltage ripple @ f_{DIM} = 200 Hz, D = 1 %

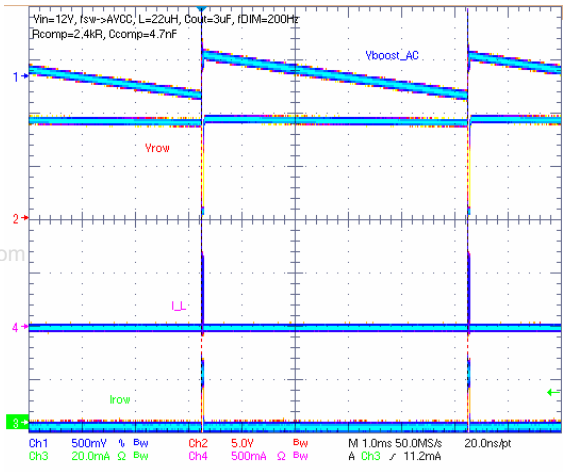


Figure 34. Output voltage ripple @ f_{DIM} = 200 Hz, D = 20 %

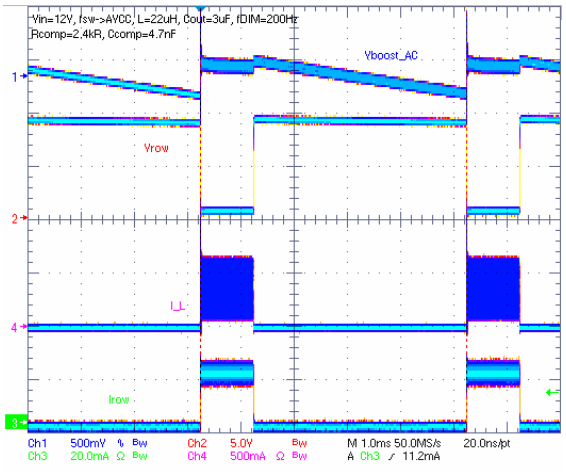


Figure 35. Output voltage ripple @ f_{DIM} = 200 Hz, D = 50 %

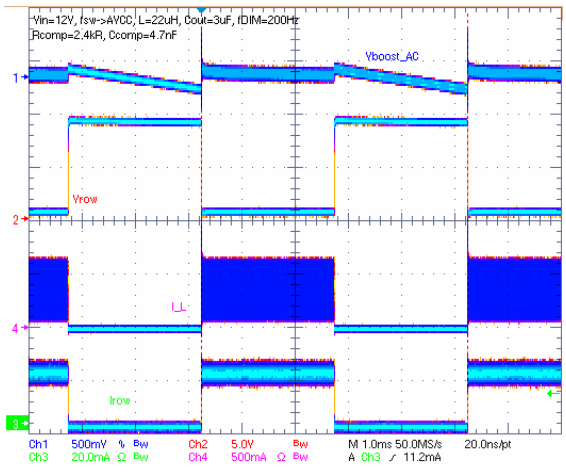


Figure 36. Output voltage ripple @ f_{DIM} = 200 Hz, D = 80 %

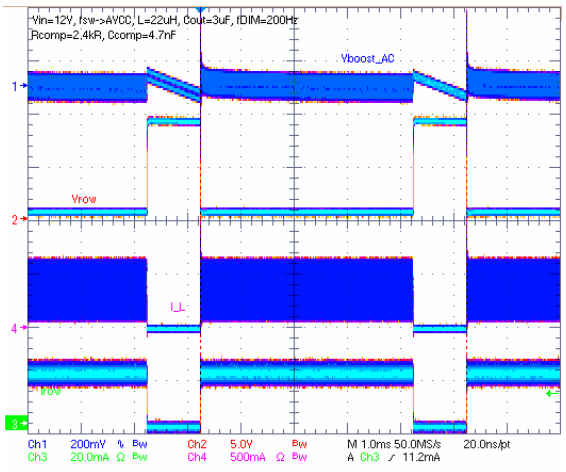


Figure 37. Shorted LED protection @ f_{DIM} = 200 Hz All WLEDs connected

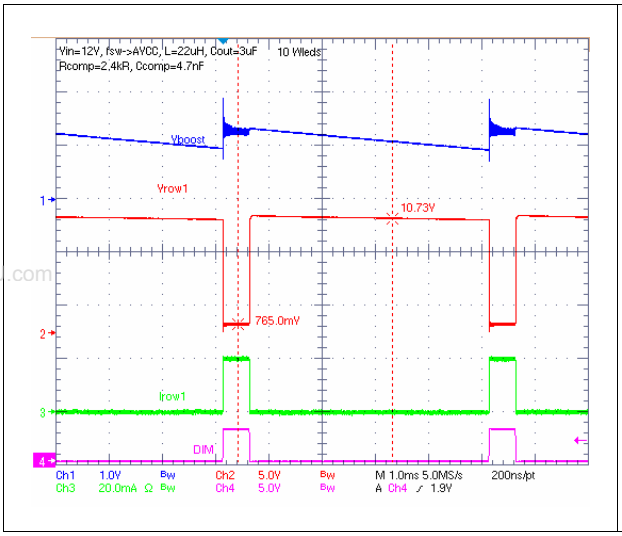


Figure 38. Shorted LED protection @ f_{DIM} = 200 Hz 1 WLED shorted

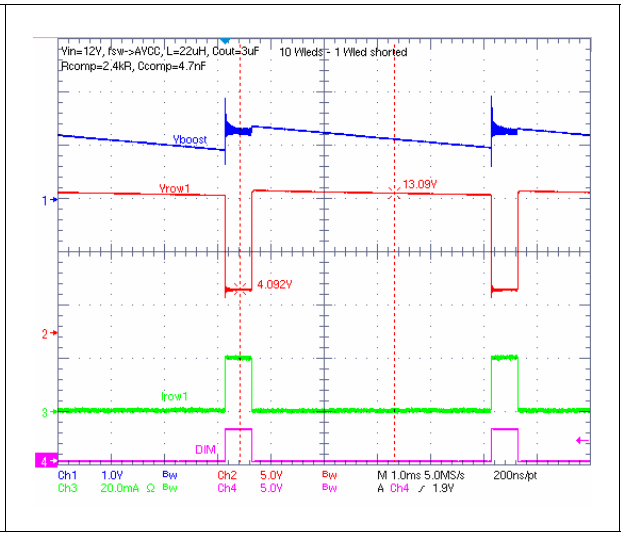


Figure 39. Shorted LED protection @ f_{DIM} = 200 Hz 2 WLEDs shorted

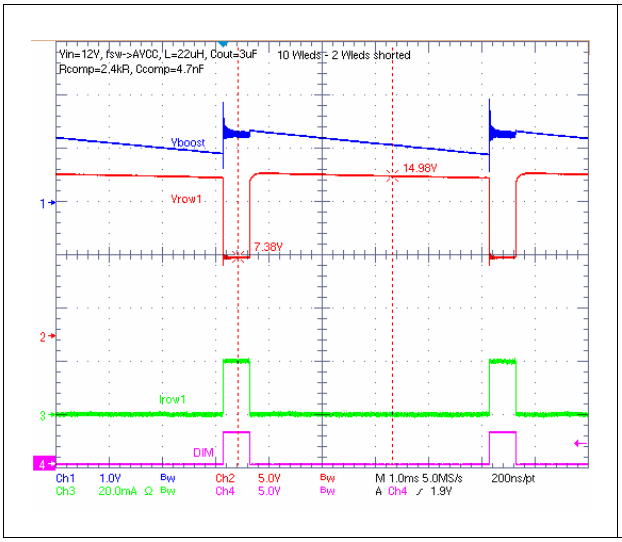


Figure 40. Shorted LED protection @ f_{DIM} = 200 Hz 3 WLEDs shorted - ROW disabled

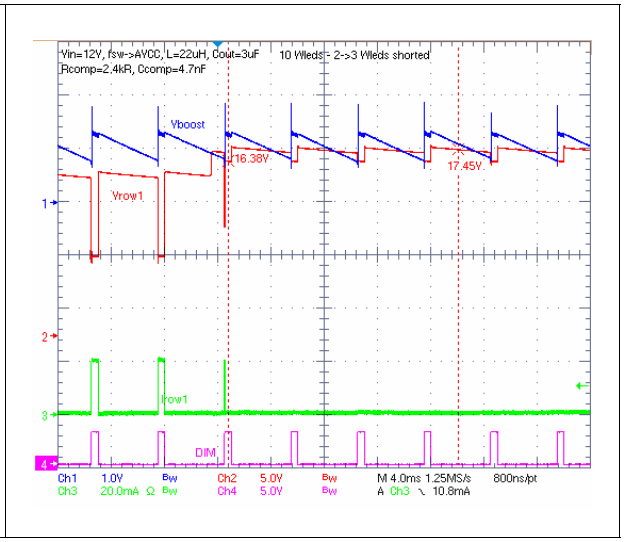
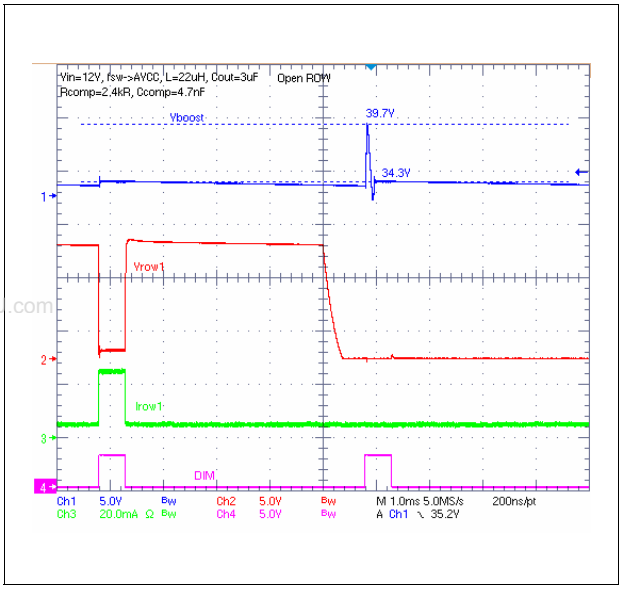
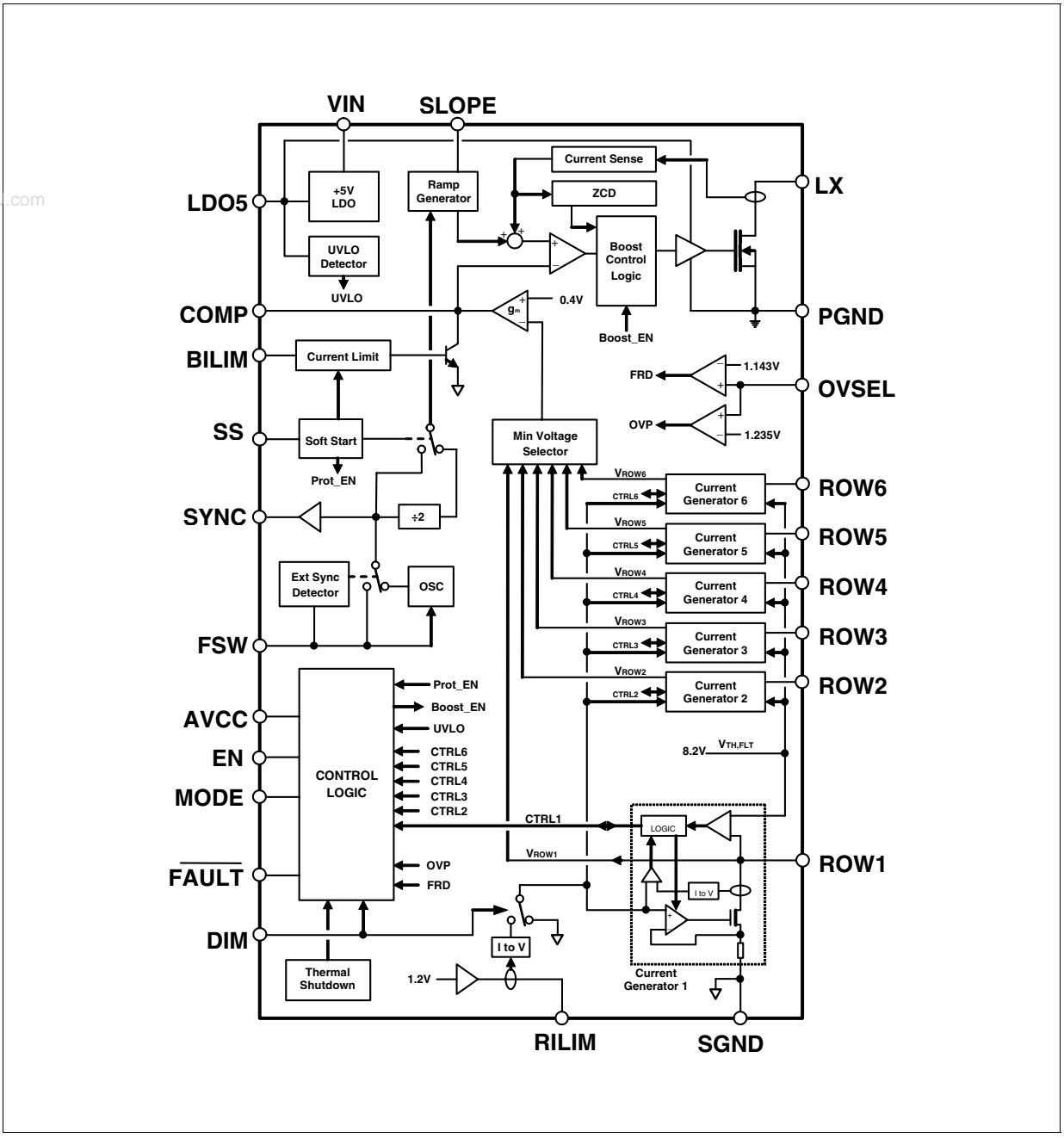


Figure 41. Open ROW detection @ f_{DIM} = 200 Hz



6 Block diagram

Figure 42. Simplified block diagram



7 Operation description

7.1 Boost section

7.1.1 Functional description

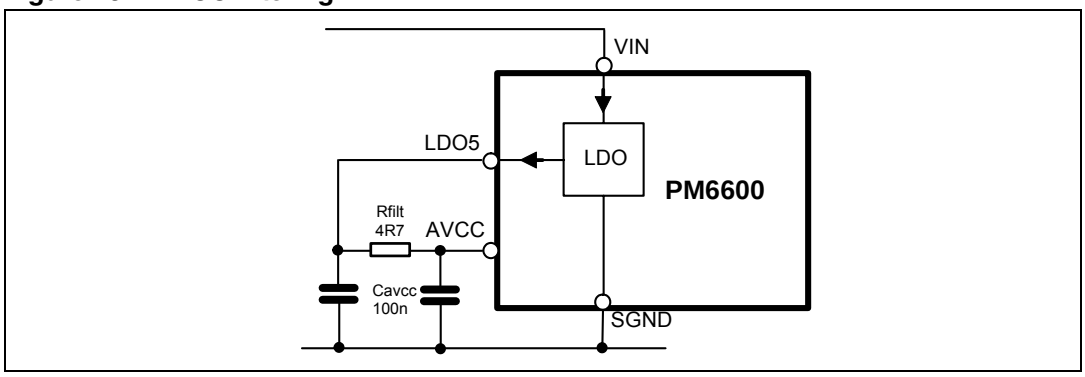
The PM6600 is a monolithic LEDs driver for the backlight of LCD panels and it consists of a boost converter and six PWM-dimmable current generators.

The input voltage range is from 4.7 V up to 28 V.

The boost section is based on a constant switching frequency, Peak Current-Mode architecture. The boost output voltage is controlled such that the lowest ROWs' voltage, referred to SGND, is equal to an internal reference voltage (400 mV typ.).

In addition, the PM6600 has an internal LDO that supplies the internal circuitry of the device and is capable to deliver up to 40 mA. The input of the LDO is the VIN pin. The LDO5 pin is the LDO output and the supply for the power-MOSFET driver at the same time. The AVCC pin is the supply for the analog circuitry and should be connected to the LDO output through a simple RC filter, in order to improve the noise rejection.

Figure 43. AVCC filtering



Two loops are involved in regulating the current sunk by the generators.

The main loop is related to the boost regulator and uses a constant frequency Peak Current-Mode architecture (see figure 10), while an internal current loop regulates the same current at each ROW according to the set value (RILIM pin).

A dedicated circuit automatically selects the lowest voltage drop among all the ROWs and provides this voltage the main loop that, in turn, regulates the output voltage. In fact, once the reference generator has been detected, the error amplifier compares its voltage drop to the internal reference voltage and varies the COMP output. The voltage at the COMP pin determines the inductor peak current at each switching cycle. The output voltage of the boost regulator is thus determined by the total forward voltage of the LEDs strings:

Equation 1

$$V_{OUT} = \max_{i=1}^{N_{ROWS}} \left(\sum_{j=1}^{m_{LEDS}} V_{F,j} \right) + 400mV$$

where the first term represents the highest total forward voltage drop over active ROWs and the second is the voltage drop across the leading generator (400 mV typ.).

The device continues to monitor the voltage drop across all the rows and automatically switches to the current generator having the lowest voltage drop.

7.2 Over voltage protection

An adjustable Over-Voltage Protection is available. It can be set feeding the OVSEL pin with a partition of the output voltage. The voltage of the central tap of the divider is thus compared to a fixed 1.235 V threshold. When the voltage on the OVSEL pin exceeds the OV threshold, the FAULT pin is tied low (see section 3) and the device is turned off; this condition is latched and the PM6600 is restarted by toggling the EN pin or by performing a Power-On Reset (the POR occurs when the LDO output falls below the lower UVLO threshold and subsequently crosses the upper UVLO threshold during the rising phase of the input voltage). Normally, the value of the high-side resistors of the divider is in the order of 100kΩ to reduce the output capacitor discharge when the boost converter is off (during the off phase of the dimming cycle).

The OVSEL divider should be a compensated one, with the capacitors C10 (typically in the 100 pF-330 pF range) that improves noise rejection at the OVSEL pin (see figure 5) and C13 (typically 22 pF) that avoids OVP fault detection when a row is open.

The following formula permits to properly select the OVP threshold, according to the VOUT value and considering the worst case:

Equation 2

$$V_{OUT} < V_{OVP} < V_{OUT} + (V_{ROWx,FAULT} - V_{ROW\_MAX})$$

where

Equation 3

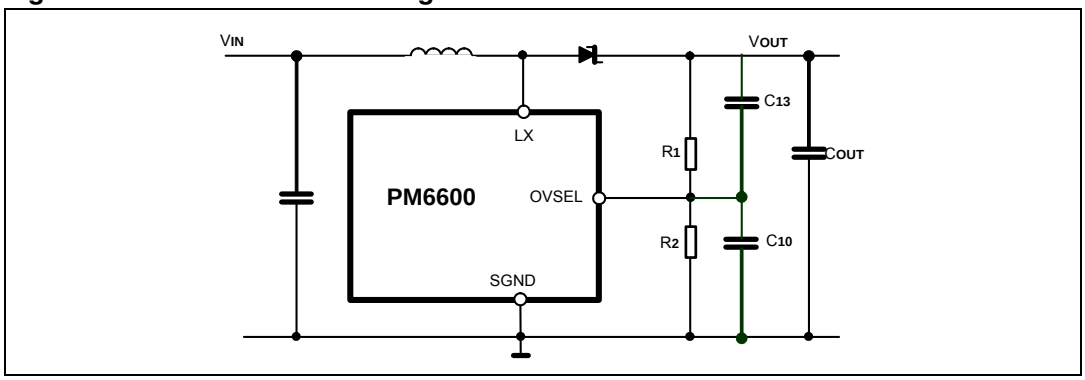
$$V_{OUT} = n_{WLED\_series} \cdot V_{F\_WLED} + 0.4V$$

V_{OVP} is the Over-Voltage Protection threshold

$V_{ROWx,FAULT}$ is the Shorted LED threshold

V_{ROW_MAX} is the maximum voltage drop across the current generators, measured in the ROWx pin with the leds' series with minimum V_{F_WLED}: Forward Voltage of the single LED.

Figure 44. OVP threshold setting



7.3 Switching frequency selection and synchronization

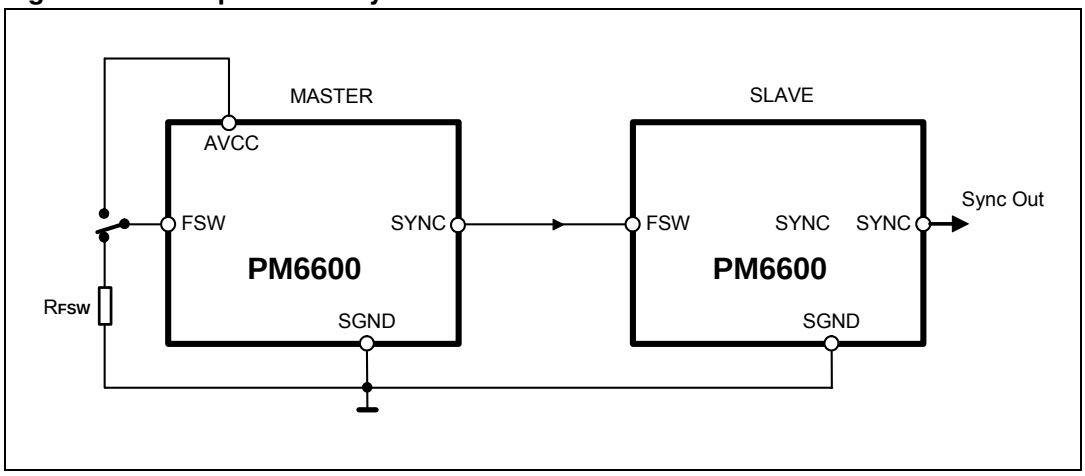
The switching frequency of the boost converter can be set in the 200 kHz-1 MHz range by connecting the FSW pin to ground through a resistor. Calculation of the setting resistor is made using equation 3 and should not exceed the 80 kΩ-400 kΩ range.

Equation 4

$$R_{FSW} = \frac{f_{SW}}{2.5}$$

In addition, when the FSW pin is tied to AVCC, the PM6600 uses a default 660 kHz fixed switching frequency, allowing to save a resistor in minimum components-count applications.

Figure 45. Multiple device synchronization



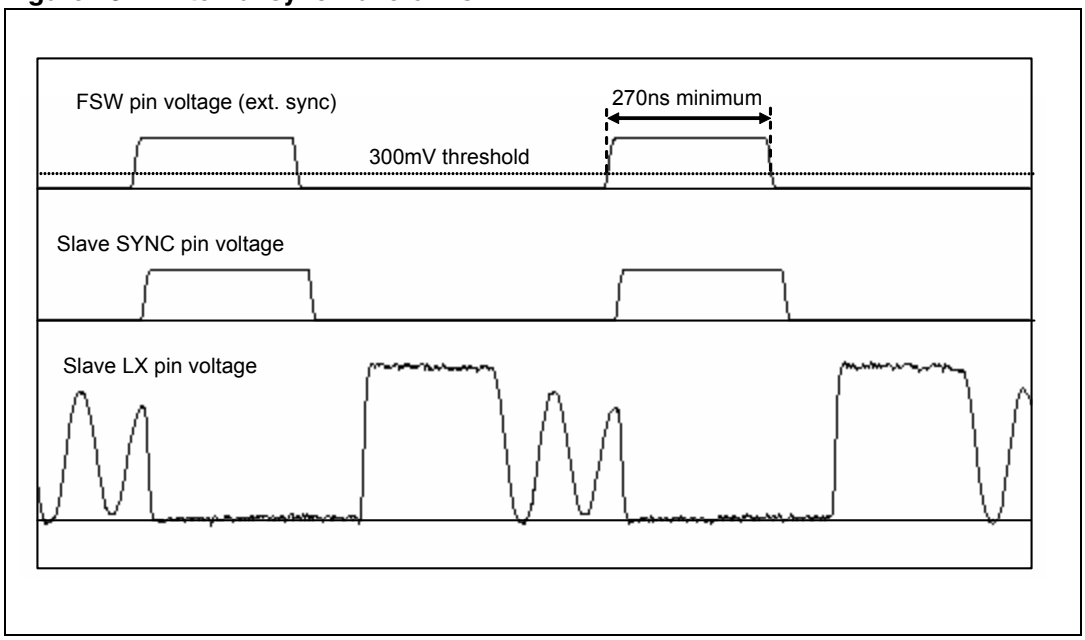
The FSW pin can also be used as a synchronization input, allowing the PM6600 to operate both as master or slave device. If a clock signal with a 210 kHz minimum frequency is applied to this pin, the device locks synchronized (300 mV threshold). An Internal timeout allows synchronization as long as the external clock frequency is greater than 210 kHz.

Keeping the FSW pin voltage lower than 300 mV for more than 1/210 kHz ≈ 5 µs results in the device turn off. Normal operation is resumed as soon as FSW rises above the mentioned threshold and the Soft-Start sequence is repeated.

The SYNC pin is a synchronization output and provides a 34 % (typ.) duty-cycle clock when the PM6600 is used as master or a replica of the FSW pin when used as slave. It is used to connect multiple devices in a daisy-chain configuration or to synchronize other switching converters running in the system with the PM6600 (master operation).

When an external synchronization clock is applied to the FSW pin, the internal oscillator is overdriven: each switching cycle begins at the rising edge of clock, while the slope compensation ramp starts at the falling edge of the same signal. Thus, the external synchronization clock is required to have a 40 % maximum duty-cycle when the boost converter is working in Continuous-Conduction Mode (CCM). The minimum pulse width which allows the synchronizing pulses to be detected is 270 ns.

Figure 46. External sync waveforms



7.4 System stability

The boost section of the PM6600 is a Fixed Frequency, Peak Current-Mode converter. During normal operation, a minimum voltage selection circuit compares all the voltage drops across the active current generators and provides the minimum one to the error amplifier. The output voltage of the error amplifier determines the inductor peak current in order to keep its inverting input equal to the reference voltage (400 mV typ). The compensation network consists of a simple RC series (R_{COMP} - C_{COMP}) between the COMP pin and ground.

The calculation of R_{COMP} and C_{COMP} is fundamental to achieve optimal loop stability and dynamic performance of the boost converter and is strictly related to the operating conditions.

7.4.1 Loop compensation

The compensation network can be quickly calculated using equations 4 through 9. Once both R_{COMP} and C_{COMP} have been determined, a fine-tuning phase may be required in order to get the optimal dynamic performance from the application.

The first parameter to be fixed is the switching frequency. Normally, a high switching frequency allows reducing the size of the inductor but increases the switching losses and negatively affects the dynamic response of the converter. For most of applications, the fixed value (660 kHz) represents a good trade-off between power dissipation and dynamic response, allowing to save an external resistor at the same time. In low-profile applications, the inductor value is often kept low to reduce the number of turns; an inductor value in the 4.7 µH-15 µH range is a good starting choice.

Even if the loop bandwidth of the boost converter should be chosen as large as possible, it should be set to 20 % of the switching frequency, taking care not to exceed the CCM-mode Right Half-Plane Zero (RHPZ).

Equation 5

$$f_U \leq 0.2 \cdot f_{SW}$$

Equation 6

$$f_U \leq 0.2 \cdot \frac{M^2 R}{2\pi \cdot L} = 0.2 \cdot \frac{\left(\frac{V_{IN,min}}{V_{OUT}}\right)^2 \left(\frac{V_{OUT}}{I_{OUT}}\right)}{2\pi \cdot L}$$

Where $V_{IN,min}$ is the minimum input voltage, I_{OUT} is the overall output current,

$$M = \frac{V_{IN,min}}{V_{OUT}} \quad R = \frac{V_{OUT}}{I_{OUT}}$$

Note that, the lower the inductor value (or the lower the switching frequency) the higher the bandwidth can be achieved. The output capacitor is directly involved in the loop of the boost converter and must be large enough to avoid excessive output voltage drop in case of a sudden line transition from the maximum to the minimum input voltages (ΔV_{OUT} should not exceed 50-100 mV):

Equation 7

$$\Delta V_{OUT} = \frac{I_{OUT}}{2\pi \cdot f_U \cdot C}\left(1 - \frac{V_{IN\_MIN}}{V_{IN\_MAX}}\right)$$

Once the output capacitor has been chosen, the R_{COMP} can be calculated as:

Equation 8

$$R_{COMP} = \frac{2\pi \cdot f_U \cdot C}{G_M \cdot g_{EA} \cdot M}$$

Where G_M = 2.7 S and g_{EA} = 375 µS.

The C_{COMP} capacitor is determined to place the frequency of the compensation zero 5 times lower than the loop bandwidth:

Equation 9

$$C_{COMP} = \frac{1}{2\pi \cdot f_Z \cdot R_{COMP}}$$

Where $f_Z = f_U / 5$.

The close loop gain function (G_{LOOP}) is thus given by equation 10:

Equation 10

$$G_{LOOP} = G_M \cdot g_{EA} \cdot \left(R_{COMP} + \frac{1}{sC_{COMP}}\right) \cdot RM \frac{1 - s\frac{L}{M^2R}}{1 + sRC}$$

A simple technique to optimize different applications is to replace R_{COMP} with a 20kΩ trimmer and adjust its value to properly damp the output transient response. Insufficient damping will result in excessive ringing at the output and poor phase margin. Figures 5a and 5b give an example of compensation adjustment for a typical application.

Figure 47. Poor phase margin (a) and properly damped (b) load transient responses

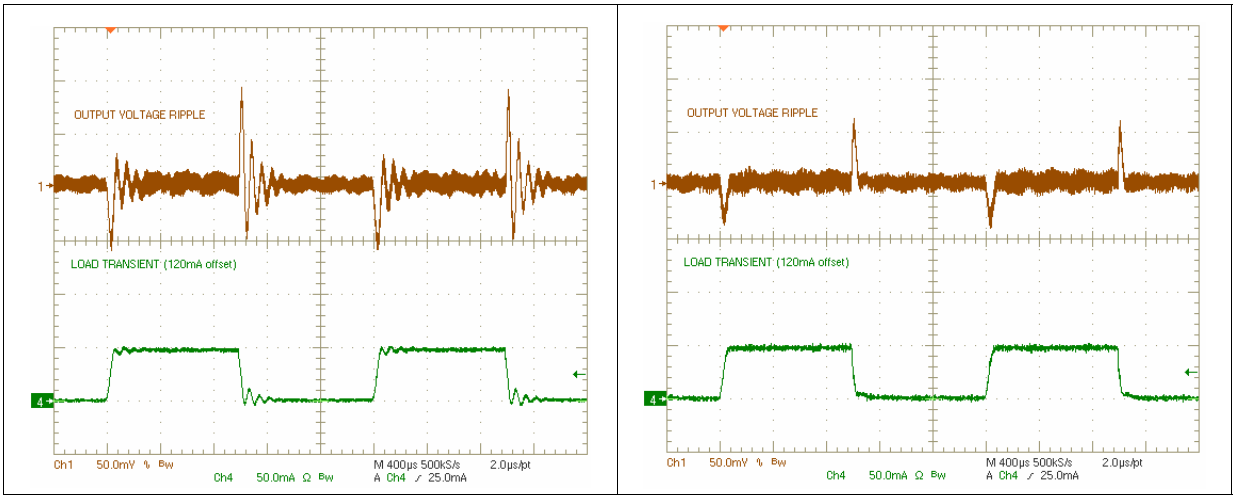
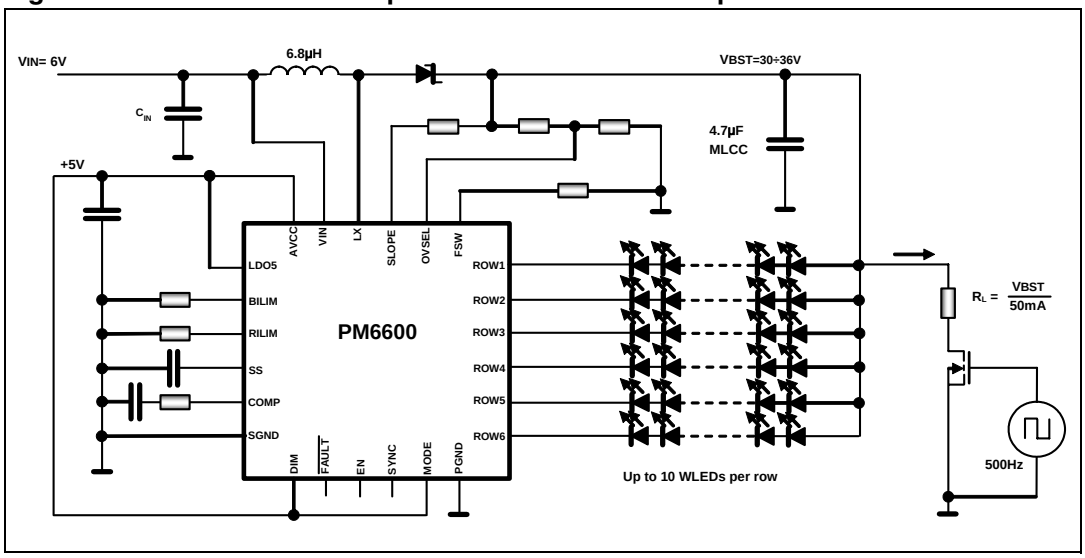


Figure 48. Load transient response measurement set-up

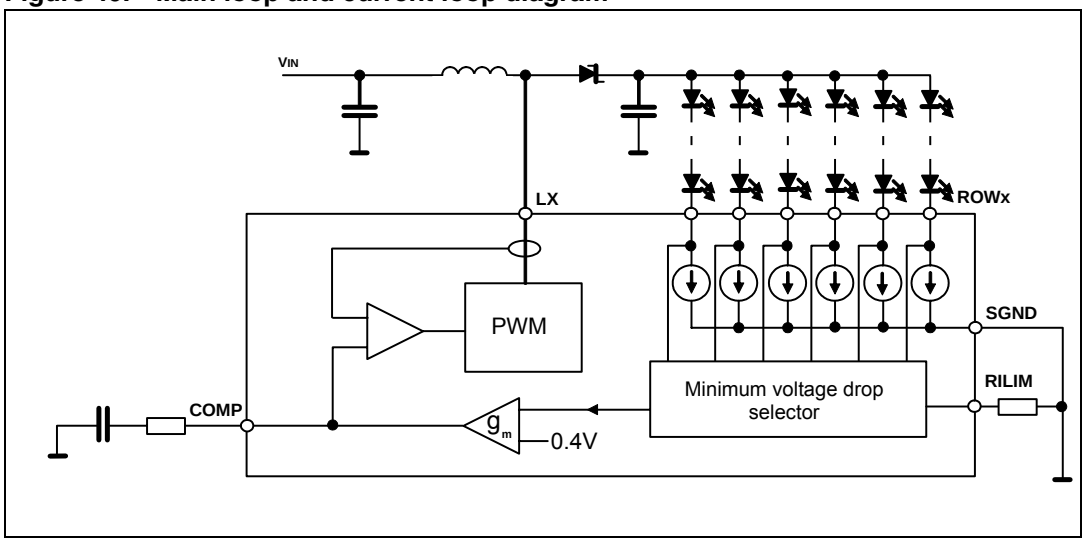


7.4.2 Slope compensation

The Constant Frequency, Peak Current-Mode topology has the advantage of very easy loop compensation with output ceramic capacitors (reduced cost and size of the application) and fast transient response. In addition, the intrinsic peak-current measurement simplifies the current limit protection, avoiding undesired saturation of the inductor.

On the other side, this topology has a drawback: there is inherent open loop instability when operating with a duty-ratio greater than 0.5. This phenomenon is known as "Sub-Harmonic Instability" and can be avoided by adding an external ramp to the one coming from the sensed current. This compensating technique, based on the additional ramp, is called "Slope Compensation". In figure 11, where the switching duty-cycle is higher than 0.5, the small perturbation ΔIL dies away in subsequent cycles thanks to the slope compensation and the system reverts to a stable situation.

Figure 49. Main loop and current loop diagram



The SLOPE pin allows to properly set the amount of slope compensation connecting a simple resistor R_{SLOPE} between the SLOPE pin and the output. The compensation ramp starts at 35 % (typ.) of each switching period and its slope is given by the following equation:

Equation 11

$$S_E = K_{SLOPE}\left(\frac{V_{OUT} - V_{IN} - V_{BE}}{R_{SLOPE}}\right)$$

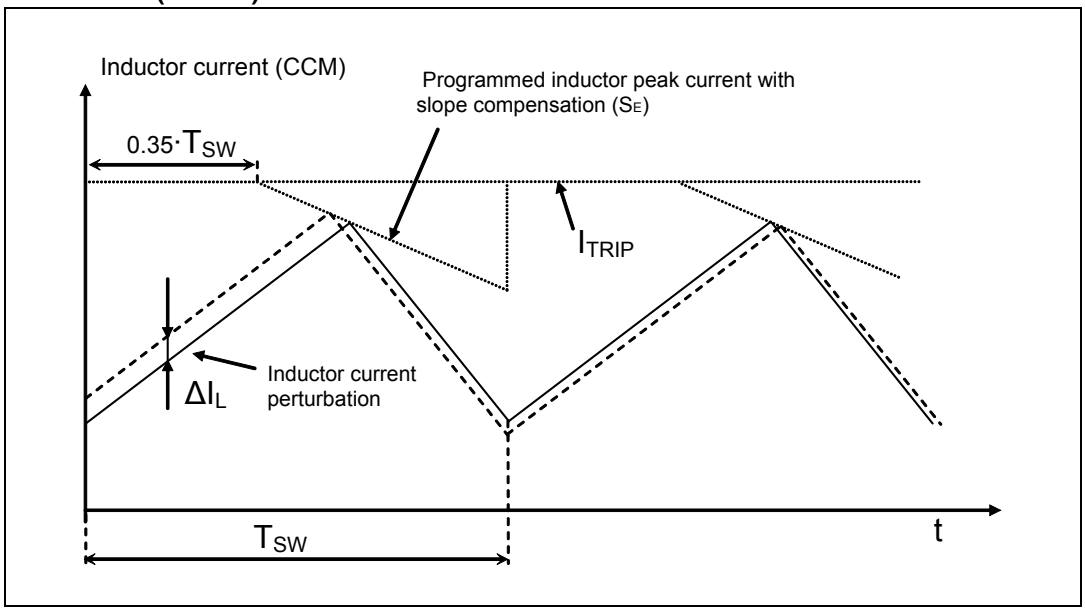
Where K_{SLOPE}, V_{BE} = 2 V (typ.) and SE is the slope ramp in [A/s].

To avoid sub-harmonic instability, the compensating slope should be at least half the slope of the inductor current during the off-phase for a duty-cycle greater than 50 % (i.e. at the lowest input voltage). The value of R_{SLOPE} can be calculated according to equation 9.

Equation 12

$$R_{SLOPE} \leq \frac{2 \cdot K_{SLOPE} \cdot L \cdot (V_{OUT} - V_{IN} - V_{BE})}{(V_{OUT} - V_{IN})}$$

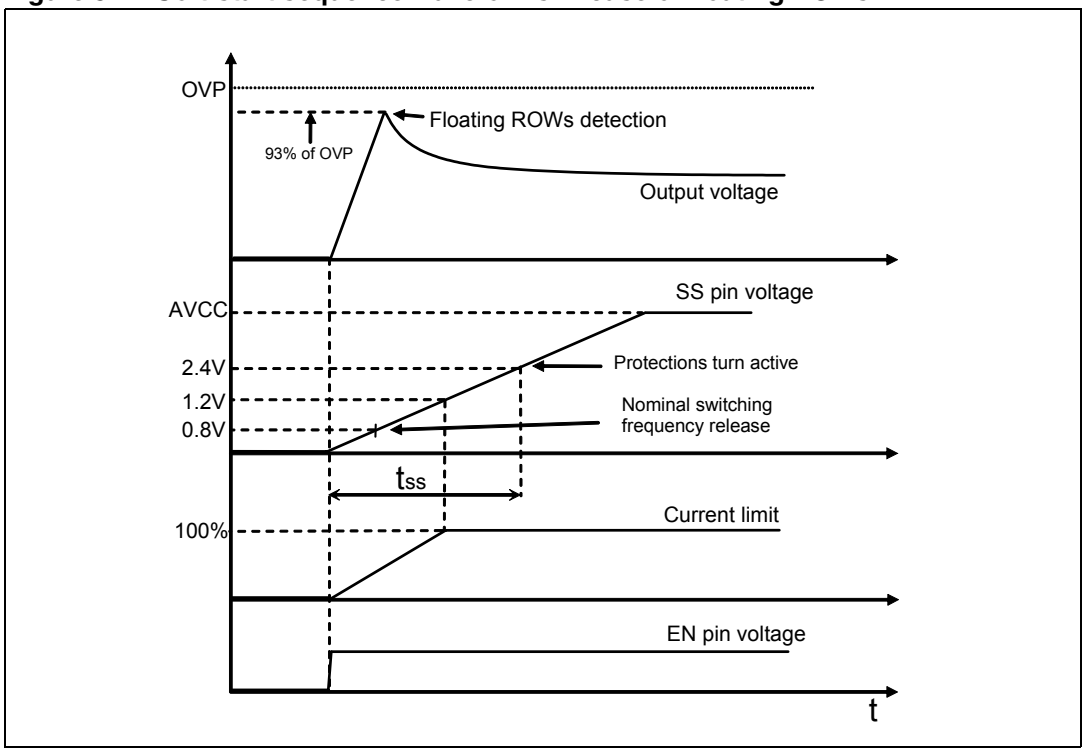
Figure 50. Effect of slope compensation on small inductor current perturbation (D > 0.5)



7.5 Soft-start

The Soft-Start function is required to perform a correct start-up of the system, controlling the inrush current required to charge the output capacitor and to avoid output voltage overshoot. The Soft-Start duration is set connecting an external capacitor between the SS pin and ground. This capacitor is charged with a 5 µA constant current, forcing the voltage on the SS pin to ramp up. When this voltage increases from zero to nearly 1.2 V, the current limit of the power-MOSFET is proportionally released to its final value. In addition, during the initial part of the Soft-Start, the switching frequency of the boost converter is reduced to half of the nominal value to permit to use inductors with lower saturation current value; the nominal switching frequency is restored after the SS pin voltage has crossed 0.8 V. In this mode, the current runaway is avoided.

Figure 51. Soft-start sequence waveforms in case of floating ROWs



During the soft-start phase it is also performed the floating ROWs detection. In presence of one or more floating ROWs, the error amplifier is unbalanced and the output voltage increases; when it reaches the Floating ROW Detection (FRD) threshold (93 % of the OVP threshold), the floating ROWs are managed according to Table 3 (see Section 3). After the SS voltage reaches a 2.4 V threshold, the start-up finishes and all the protections turn active. The soft-start capacitor CSS can be calculated according to equations 12.

Equation 13

$$C_{SS} \cong \frac{I_{SS} t_{SS}}{2.5}$$

$$C_{SS} \cong 12 \cdot 10^{-6} \cdot C_{OUT} \cdot (V_{OUT,max} - V_{IN,min})$$

Where I_{SS} = 5 µA and t_{SS} is the desired Soft-start duration.

7.6 Boost current limit

The design of the external components, especially the inductor and the flywheel diode, must be optimized in terms of size relying on the programmable peak current limit. The PM6600 improves the reliability of the final application giving the way to limit the maximum current flowing into the critical components. A simple resistor connected between the BILIM pin and ground sets the desired value. The voltage at the BILIM pin is internally fixed to 1.2 V and the current limit is proportional to the current flowing through the setting resistor, according to the following equation:

Equation 14

$$I_{BOOST,PEAK} = \frac{K_B}{R_{BILIM}}$$

where $K_B = 6.7 \cdot 10^5\,V \pm 15\%$.

The maximum allowed current limit is 5 A, resulting in a minimum setting resistor $R_{BILIM} > 120\ k\Omega$. The maximum guaranteed RMS current in the power switch is 2 Arms. The current limitation works by clamping the COMP pin voltage proportionally to R_{BILIM}. Peak inductor current is limited to the above threshold decreased by the slope compensation contribution.

In a boost converter the r.m.s. current through the internal MOSFET depends on both the input and output voltages, according to equations 15a (DCM) and 15b (CCM).

Equation 15 a

$$I_{MOS,rms} = \frac{V_{IN} \cdot D}{F_{SW} \cdot L}\sqrt{\frac{D}{3}}$$

Equation 15 b

$$I_{MOS,rms} = I_{OUT}\sqrt{\left(\frac{D}{(1-D)^2} + \frac{1}{12}\left(\frac{V_{OUT}}{I_{OUT} \cdot f_{SW} \cdot L}\right)^2 (D(1-D))^3\right)}$$

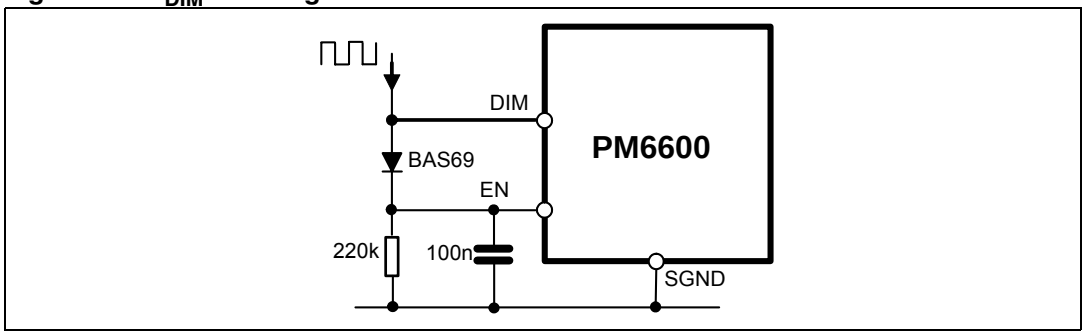
7.7 Enable function

The PM6600 is enabled by the EN pin. This pin is active high and, when forced to SGND, the device is turned off. This pin is connected to a permanently active 2 µA current source; when sudden device turn-on at power-up is required, this pin must be left floating or connected to a delay capacitor. When turned off, the PM6600 quickly discharges the Soft-Start capacitor and turns off the power-MOSFET, the current generators and the LDO. The power consumption is thus reduced to 20 µA only.

The proper startup sequence is DIM ' VIN ' EN, or VIN ' DIM ' EN. If the dimming signal is applied after the EN pin, the device will not perform the soft start again, in fact it will start switching with the maximum current limit in order to recover the output voltage.

In applications where the dimming signal is used to turn on and off the device, the EN pin can be connected to the DIM pin as shown in *Figure 52*.

Figure 52. f_{DIM} enabling schematic



7.8 Thermal protection

In order to avoid damage due to high junction temperature, a thermal shutdown protection is implemented. When the junction temperature rises above 150 °C (typ.), the device turns off both the control logic and the boost converter and holds the FAULT pin low.

In order to turn on the device again, it is possible to perform a POR (Power On Reset) once the junction temperature has been reduced by 30 °C.

8 Backlight driver section

8.1 Current generators

The PM6600 is a LEDs driver with six channels (ROWs); each ROW is able to drive multiple LEDs in series (max. 40 V) and to sink up to 30 mA maximum current, allowing to manage different kinds of LEDs.

The LEDs current can be set by connecting an external resistor (R_{RILIM}) between the RILIM pin and ground. The voltage across the RILIM pin is internally set to 1.2 V and the ROWs current is proportional to the RILIM current according to the following equation:

Equation 16

$$I_{ROWx} = \frac{K_R}{R_{RILIM}}$$

Where K_R = 998 ± 21 V (± 2.1 %).

The current accuracy between the ROWs of more than one device is, consequently:

Equation 17

$$\Delta I_{ROW,MAX} = \frac{I_{ROW\_K_R=1019} - I_{ROW\_K_R=998}}{I_{ROW\_K_R=998}} \leq +2.1\%$$

$$\Delta I_{ROW,MIN} = \frac{I_{ROW\_K_R=977} - I_{ROW\_K_R=998}}{I_{ROW\_K_R=998}} \geq -2.1\%$$

In the table below there are the maximum, typical and minimum I_{ROW} values versus the R_{RILIM}:

Table 7. I_{ROW} values versus R_{RILIM}

R_{RILIM}	I_{ROW} @ KR=977	I_{ROW} @ KR=998	I_{ROW} @ KR=1019
47.0 kΩ	20.79 mA	21.68 mA	21.68 mA
49.9 kΩ	19.58 mA	20.00 mA	20.42 mA
51.0 kΩ	19.16 mA	19.57 mA	19.98 mA

The maximum current mismatch between the ROWs of one device is ± 2 % @ I_{ROWx} = 20 mA, according to the formula:

Equation 18

$$\Delta I_{ROWx,max} = \frac{I_{ROW\_max} - I_{ROW\_mean}}{I_{ROW\_mean}} \leq +2\%$$

$$\Delta I_{ROWx,min} = \frac{I_{ROW\_min} - I_{ROW\_mean}}{I_{ROW\_mean}} \geq -2\%$$

$$I_{ROW\_mean} = \frac{\sum_{i=1}^{6} I_{ROWi}}{6}$$

Due to the spread of the LEDs' forward voltage, the total drop across the LED's strings will be different. The device will manage the unconnected ROWs according to the MODE pin setting (see *Table 3*).

8.2 PWM dimming

The brightness control of the LEDs is performed by a Pulse-Width Modulation of the ROWs current. When a PWM signal is applied to the DIM pin, the current generators are turned on and off mirroring the DIM pin behavior. Actually, the minimum dimming duty-cycle depends on the dimming frequency. The real limit to the PWM dimming is the minimum on-time that can be managed for the current generators; this minimum on-time is approximately 500 ns.

Thus, the minimum dimming duty-cycle depends on the dimming frequency according to the following formula:

Equation 19

$$D_{DIM,min} = 500ns \cdot f_{DIM}$$

For example, at a dimming frequency of 20 kHz, 1% of dimming duty-cycle can be managed.

During the off-phase of the PWM signal the boost converter is paused, the current generators are turned off and the output voltage is frozen across the output capacitor.

During the start-up sequence the dimming duty-cycle is forced to 100 % to detect floating ROWs regardless of the applied dimming signal.

9 Fault management

The main loop keeps the ROW having the lowest voltage drop regulated to about 400 mV. This value slightly depends on the voltage across the remaining active ROWs. After the soft-start sequence, all protections turn active and the voltage across the active current generators is monitored to detect shorted LEDs.

9.1 FAULT pin

The FAULT pin is an open-collector output, active low, which gives information regarding faulty conditions eventually detected. This pin can be used either to drive a status LED (with a series resistor to not exceed 4 mA current) or to warn the host system. The FAULT pin status is strictly related to the MODE pin setting (see *Table 3* for details).

9.2 MODE pin

The MODE pin is a digital input and can be connected to AVCC or SGND in order to choose the desired fault detection and management. The PM6600 can manage a faulty condition in two different ways, according to the application needs. *Table 3* summarizes how the device detects and handles the internal protections related to the boost section (Over-Current, Over-Temperature and Over-Voltage) and to the current generators section (open and shorted LEDs).

Table 8. Faults management summary

FAULT	MODE to GND	MODE to VCC
Internal MOSFET over current	FAULT pin HIGH Power-MOS turned OFF	FAULT pin HIGH Power-MOS turned OFF
Output over voltage	FAULT pin LOW Device turned OFF Latched	FAULT pin LOW Device turned OFF Latched
Thermal shutdown	FAULT pin LOW Device turned OFF Latched	FAULT pin LOW Device turned OFF Latched
Shorted LEDs on a single row	FAULT pin LOW Faulty ROW DISABLED VTH,FAULT = 8.2 V	FAULT pin LOW Faulty ROW DISABLED VTH,FAULT = 8.2 V
Shorted LEDs on more rows	FAULT pin LOW Device Latched OFF VTH,FAULT = 8.2 V	FAULT pin LOW Faulty ROWs DISABLED VTH,FAULT = 8.2 V
Open row	FAULT pin LOW Faulty ROW DISABLED	FAULT pin HIGH Faulty ROW DISABLED
More than one open rows	FAULT pin LOW Device Latched OFF	FAULT pin HIGH Faulty ROWs DISABLED
Open rows plus shorted led (different rows)	FAULT pin LOW Device Latched OFF VTH,FAULT = 8.2 V	FAULT pin LOW Faulty ROWs DISABLED VTH,FAULT = 8.2 V

9.3 Open LED fault

In case a ROW is not connected or a LED fails open, the device has two different behaviors according to the MODE pin status.

If the MODE pin is high (connected to AVCC), the open ROW is excluded from the control loop and the device continues to work properly with the remaining ROWs, without asserting the FAULT pin.

Connecting the MODE pin to SGND, the PM6600 behaves in a different manner: as soon as one open ROW is detected, the FAULT pin is tied low. In case a second open ROW is detected, the device is turned off. The internal logic latches this status: to restore the normal operation, the device must be restarted by toggling the EN pin or performing a Power On Reset (POR occurs when the voltage at the LDO5 pin falls below the lower UVLO threshold and subsequently rises above the upper one).

As a consequence, If less than six ROWs are used in the application, the MODE pin must be set high.

9.4 Shorted LED fault

When a LED is shorted, the voltage across the related current generator increases of an amount equal to the missing voltage drop of the faulty LED. Since the feedback voltage on each active generator is constantly compared with a fixed fault threshold $V_{TH,FAULT}$ = 8.2 V, the device detects the faulty condition and acts according to the MODE pin status.

In case the MODE pin is connected to AVCC, the PM6600 disconnects the ROWs whose voltage is higher than the threshold and the FAULT pin is tied low. This option is also useful to avoid undesired triggering of the shorted-LED protection simply due to the high voltage drop spread across the LEDs.

If the MODE pin is low, when the voltage across one ROW is higher than $V_{TH,FAULT}$ threshold, the FAULT pin is set low and that ROW is disabled. If the voltage of a second ROW becomes higher than $V_{TH,FAULT}$ threshold, the device is turned off. The internal logic latches this status until the EN pin is toggled or a POR is performed.

9.5 Intermittent connection

For intermittent connection it is intended the condition where the flat cable connector from the leds backlight driver to the leds can have some issues on moving the panel of the notebook. This kind of issue is represented as an intermittent connection, that means the physical electrical connection between the ROWx pins of the PM6600 device and the White LEDs can be open for a while.

The device will detect an open row fault.

There is one possible solution to determine whether the fault is due to the intermittent connection or to a broken persistent electrical connection (open circuit). Since the device disables the open rows during the intermittent connection, one possible solution is, on the customer side, to toggle the EN pin and verify if the fault condition is still present.

In fact, once you disconnect one row, it will result as a off-row (Fault -> open row, latched). When you connect it again, it is as a shorted led (Vrow higher than the threshold).

This is because the short led detection is still active.

If the fault disappears after toggling the EN pin, it means that the connection is again on and the problem can be detected as a previous intermittent connection.

If the fault persists also after toggling the EN pin, it means that the problem is on the leds (one or more open leds) or on the flat cable or the cable connector (broken wire).

The resultant Fault Management table will be:

Table 9. Intermittent connection faults management summary

FAULT	MODE to GND	MODE to VCC
Internal MOSFET over current	FAULT pin HIGH Power-MOS turned OFF	FAULT pin HIGH Power-MOS turned OFF
Output over voltage	FAULT pin LOW Device turned OFF Latched	FAULT pin LOW Device turned OFF Latched
Thermal shutdown	FAULT pin LOW Device turned OFF Latched	FAULT pin LOW Device turned OFF Latched
Shorted LED on a single row	FAULT pin LOW Faulty ROW DISABLED VTH,FAULT = 8.2 V	FAULT pin LOW Faulty ROW DISABLED VTH,FAULT = 8.2 V
Shorted LEDs on more row	FAULT pin LOW Device Latched OFF VTH,FAULT = 8.2 V	FAULT pin LOW Faulty ROWs DISABLED VTH,FAULT = 8.2 V
Open row	FAULT pin LOW Faulty ROW DISABLED	FAULT pin LOW Faulty ROW DISABLED
More than one open rows	FAULT pin LOW Device Latched OFF	FAULT pin LOW Faulty ROWs DISABLED
Open row plus shorted LED (different rows)	FAULT pin LOW Device Latched OFF VTH,FAULT = 8.2 V	FAULT pin LOW Faulty ROWs DISABLED VTH,FAULT = 8.2 V

10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 10. VFQFPN-24 mechanical data

Dim.	Min	Typ	Max
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20	
b	0.18	0.25	0.30
D	3.85	4.00	4.15
D2	2.40	2.50	2.60
E	3.85	4.00	4.15
E2	2.40	2.50	2.60
e		0.50	
L	0.30	0.40	0.50
ddd			0.08

Figure 53. VFQFPN-24 mechanical data

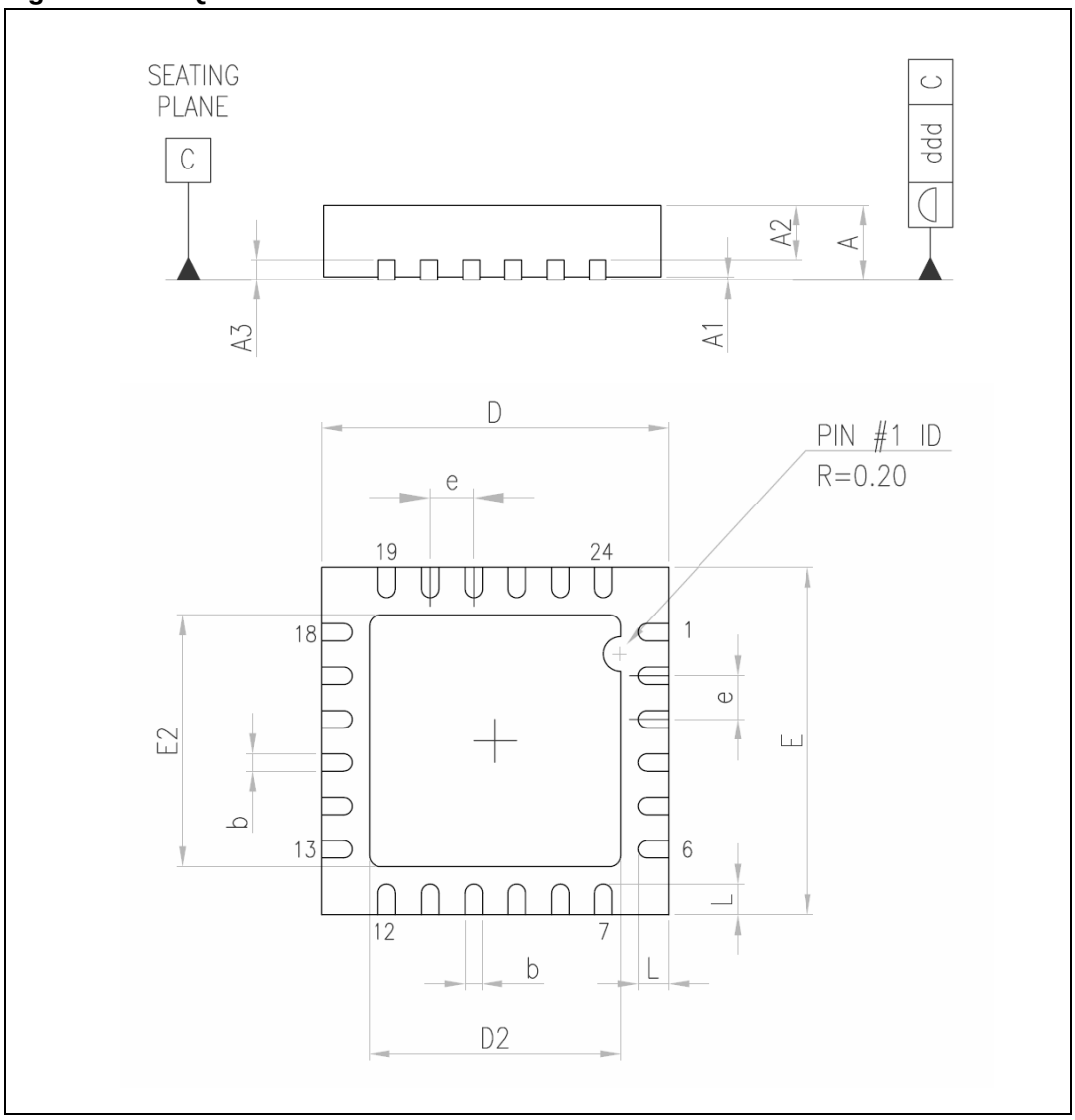
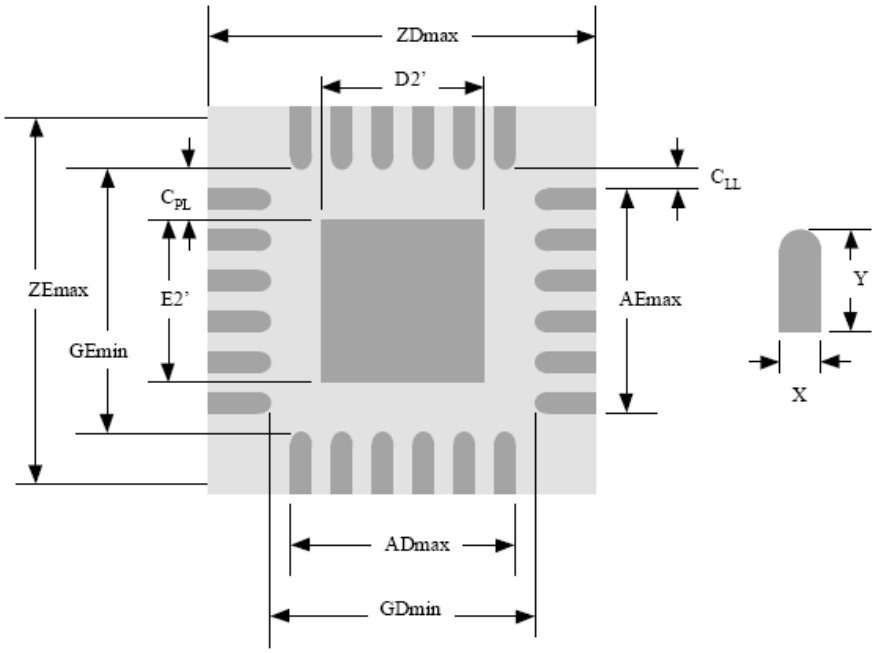


Table 11. VFQFPN-24 footprint

Dim.	Min	Typ	Max
X			0.28
Y		0.69	
ADmax = AEmax			2.78
GDmin = GEmin	2.93		
ZDmax = ZEmax			4.31
D2' = E2'			2.63

Figure 54. VFQFPN-24 footprint



11 Revision history

Table 12. Document revision history

Date	Revision	Changes
07-Dec-2007	1	Initial release
21-Jan-2008	2	Updated *Table 4*, *Table 5* and *Table 6 on page 9*

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