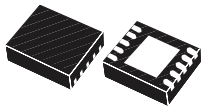
PM6644

350 mA adjustable step-down regulator

Datasheet – production data

Features

- 4.5 V to 25 V input voltage range
- Output voltage V_{OUT}: fixed 3.47 V or adjustable 0.9 V to 8 V
- 350 mA valley current limit
- Constant-on-time control
- Programmable switching frequency
- Pulse skipping mode (skip mode) at light loads
- Independent EN signals
- Latched OVP and UVP



DFN10

Applications

- Networking power supply
- Portable applications
- Microcontroller supply
- Industrial supply

Description

The PM6644 is a 350 mA valley current limit step-down regulator capable of delivering an adjustable output voltage in the range between 0.9 V and 8 V. A fixed value of output voltage is also available (3.47 V), saving the external resistor divider. It is housed in a small DFN10 3x3 package. The switching regulator is based on COT (constant-on-time) architecture, that assures fast load transient response; the embedded voltage feed-forward provides nearly constant switching frequency operation. The pulse skipping technique increases efficiency at very light load. The switching frequency can be adjusted from 200 kHz to 600 kHz through a simple resistor. The switching regulator can be programmed to regulate a fixed value of 3.47 V or it can deliver an adjustable voltage, depending on the FB pin set-up.

Table 1. Device summary

Part number	Package	Packing
PM6644	DFN10	Tube
PM6644TR	DFN10	Tape and reel

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1 Simplified application schematic

Figure 1. V_{OUT} = 3.47 V fixed configuration

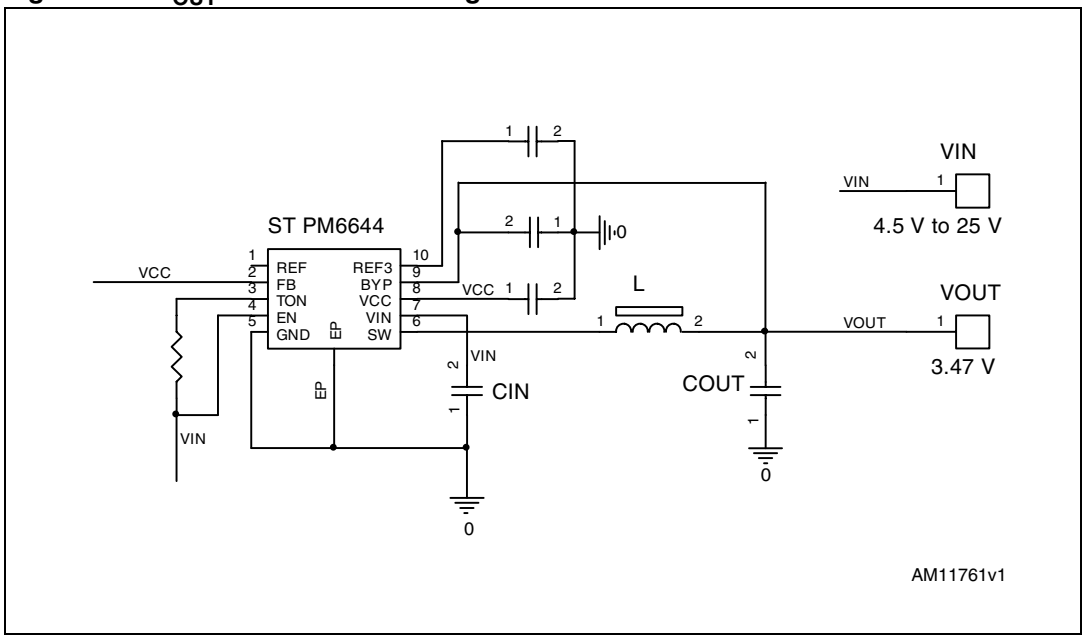


Figure 2. Adjustable V_{OUT} configuration

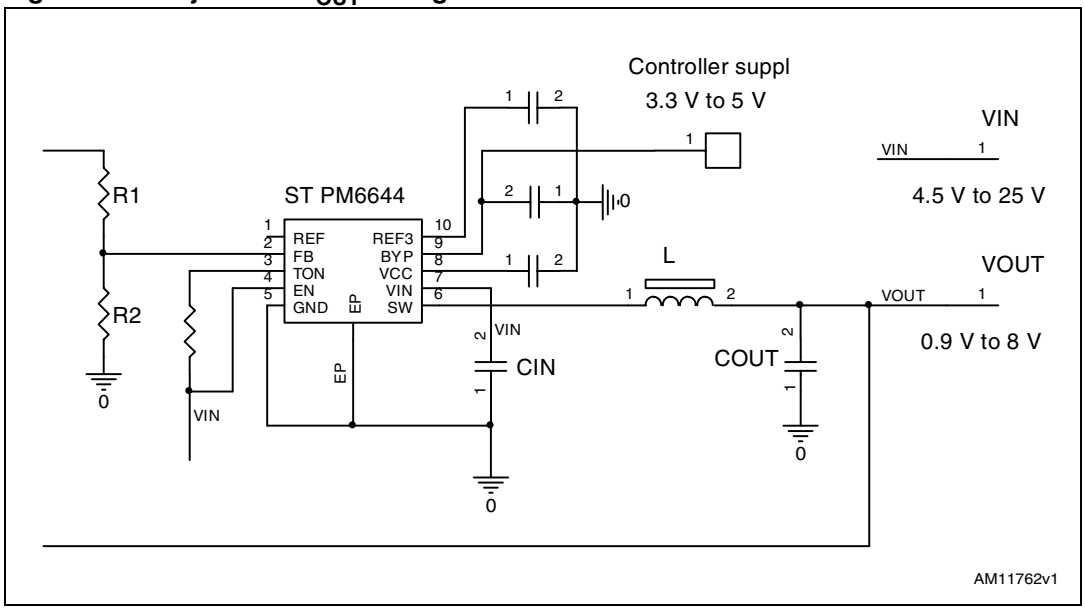
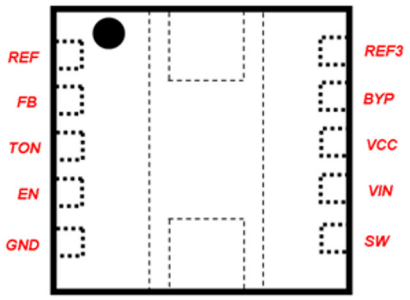


Figure 3. Pinout



1.1 Pin description

Table 2. Pin description

Pin	Name	Description
1	REF	1.216 V internal reference voltage. Do not connect this pin to any external component.
2	FB	Feedback input for the switching section: If this pin is connected to VCC, OUT operates at 3.47 V (Fixed mode). If this pin is connected to a resistive divider from OUT to GND, OUT can be adjusted from 0.9 V to 8 V.
3	T_{ON}	Switching frequency setting. Connect to VIN with a resistor to properly set the switching frequency.
4	EN	ENABLE (EN) pin. The EN pin is used to enable both the switching regulator and internal reference. Tie to ground to shut down the device. Apply 2.1 V or more for normal operation. If the EN pin is not used for power sequencing, tie this pin to the VIN pin.
5	GND	Power and signal ground connection.
6	SW	The SW pin is the switching node of the switching regulator with integrated power MOSFETs. Connect this pin to the inductor.
7	VIN	Input voltage for the switching regulator. Bypass to GND with a 1-2.2 µF MLCC capacitor. The VIN pin supplies current to the internal switching regulator and to the integrated voltage generator that supplies VCC if BYP < 2.4 V.
8	VCC	Output of a regulator that supplies the main switching controller. Bypass to GND with a 1 µF capacitor. An integrated voltage generator regulates at 3.8 V (when VIN> = 6 V) if BYP< 2.4 V. When BYP > 3.2 V, the integrated voltage generator shuts down and VCC is connected to BYP through a MOSFET switch (see *Figure 18*).
9	BYP	VCC BYPASS pin (BYP). If BYP > 3.2 V, VCC is supplied by BYP through a MOSFET switch. Bypass to GND with a 10-100 nF capacitor.
10	REF3	Integrated 3.3 V high accuracy reference voltage. Bypass to GND with a 100 nF capacitor. VREF3 is the voltage at REF3 pin.
EXP PAD	EXP PAD	Exposed pad. Connect to signal ground.

1.2 Absolute maximum ratings

Table 3. Absolute maximum ratings

Parameter	Value	Unit
VIN to GND	-0.3 to 35	V
EN, SW, TON to GND	-0.3 to VIN +0.3	V
VCC, BYP	-0.3 to 6	V
REF, FB to GND	-0.3 to VCC +0.3	V
REF3 to GND	-0.3 to BYP +0.3	V
Power dissipation at Tamb = 25 °C	2.25	W
Maximum withstanding voltage range test condition: CDF-AECQ100-002- “human body model” acceptance criteria: “normal performance”.	±1000	V

1.3 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thj-a}	Thermal resistance junction to ambient	45	°C/W
T_j	Junction operating temperature range	-40 to 125	°C

1.4 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
VIN	Input voltage range	4.5		25	V
EN	EN voltage range	0		25	V
BYP	BYP operative voltage range	0		5	V
Switching regulator embedded high-side MOSFET(1)	RMS current capability			300	mA
Switching regulator embedded low-side MOSFET				300	mA

1. Refer to *Section 3.1.4: Maximum RMS output current*.

1.5 Electrical characteristics

V_{IN}=12 V, no load on REF3, EN=V_{IN}, FB=VCC, R=1 MΩ between TON and VIN, T_j=25 °C unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Switching controller output accuracy						
BYP	Fixed output voltage valley regulation	FB=VCC, no load	3.40	3.47	3.54	V
FB	Adjustable output voltage valley regulation (FB=ADJ)	No load, BYP=3.47 V; T_j=0 °C - 70 °C(1)	0.88		0.92	V
Current limit and zero crossing comparator						
	Valley current limit		350	380		mA
	Zero crossing current threshold	SW voltage ramp slew rate = 40 V/ms	14	22	30	mA
3.3 V voltage reference						
REF3	REF3 output voltage (VREF3 voltage)	BYP=3.47 V external voltage, no load	3.2	3.3	3.4	V
	Line regulation	BYP=3.47 V to 5 V, no load		2.3	6.3	mV/V
	Load regulation	BYP=3.47 V external voltage, 0 mA < Iload < 2 mA		500		µV
VCC supply						
VCC	VCC voltage	BYP< BYP falling threshold, V_{IN}> 6	3.4	3.8	4.2	V
BYP	BYP falling threshold/ REF3 turn-off threshold		2.4	2.7		V
	BYP rising threshold (i.e. VCC=BYP)/ REF3 turn-on threshold			2.9	3.2	V
Regulator bias currents						
V_{IN}	V_{IN} shutdown current	EN=0 V		13	21	µA
	V_{IN} quiescent current with BYP > BYP falling threshold	BYP=3.47 V (not switching), REF3@no load		26	35	µA
BYP	BYP quiescent current with BYP > BYP falling threshold	BYP=3.47 V (not switching), REF3@no load		190	230	µA
Fault management						
VCC	VCC UVLO threshold	Rising edge of PVCC		2.7	3	V
		Falling edge of PVCC	2.1	2.6		V

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
FB	Overvoltage trip threshold	Referred to FB nominal regulation point, BYP= 3.47 V	+14		+20	%
FB	Undervoltage threshold	Referred to FB nominal regulation point, BYP= 3.47 V	62		73	%
Inputs and outputs						
FB	FB logic level	FB logic level to be in fixed mode	VCC-0.8			V
EN	EN level	All circuitry OFF			1.3	V
		All circuitry ON	2.4			V

1. In the range T_j = 0 °C-70 °C limits are guaranteed by design and statistical analysis, not production tested. Production test at T_j=25 °C.

1.6 Typical operating characteristics

FB = VCC, R_{TON} = 1 MΩ, V_{IN} = 12 V, EN = VIN, BYP connected to the switching regulator output, no load unless specified. Measurements performed on the evaluation kit (PM6644_DFN).

Figure 4. Efficiency vs. load

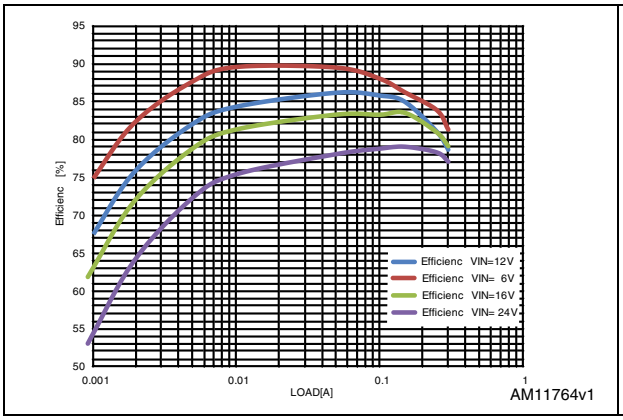


Figure 5. Switching frequency vs. load

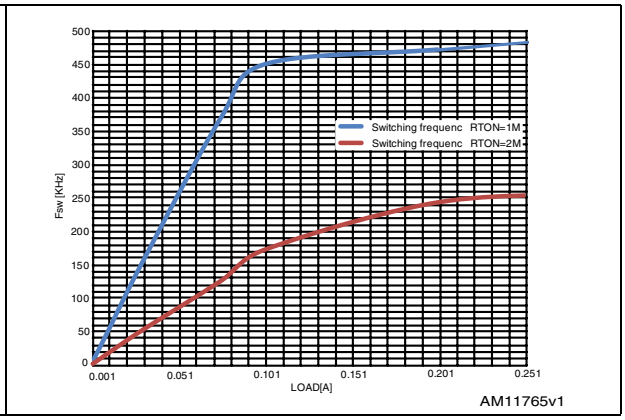


Figure 6. V_{OUT} vs. load

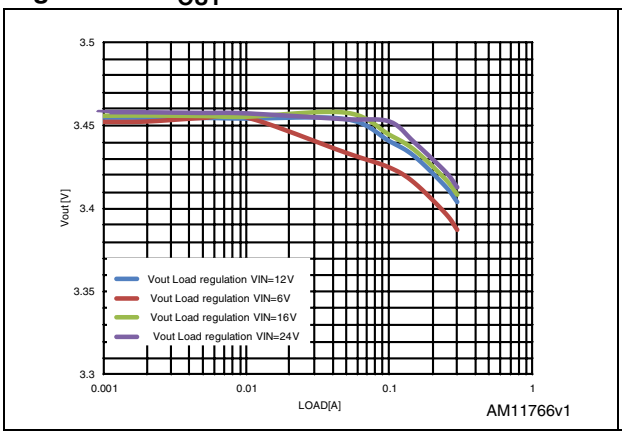


Figure 7. VREF3 vs. output load

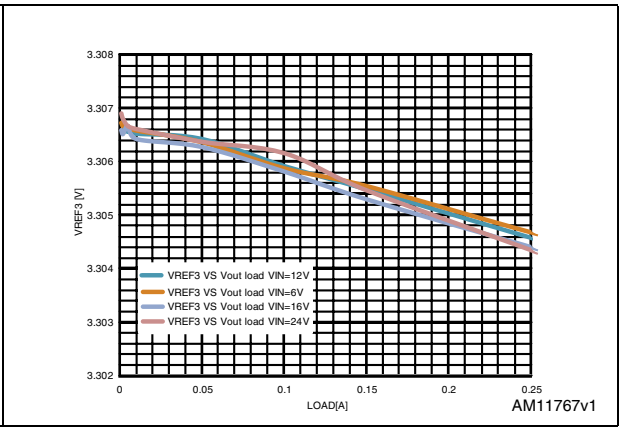


Figure 8. Shutdown V_{IN} current vs. V_{IN} (EN=0 V)

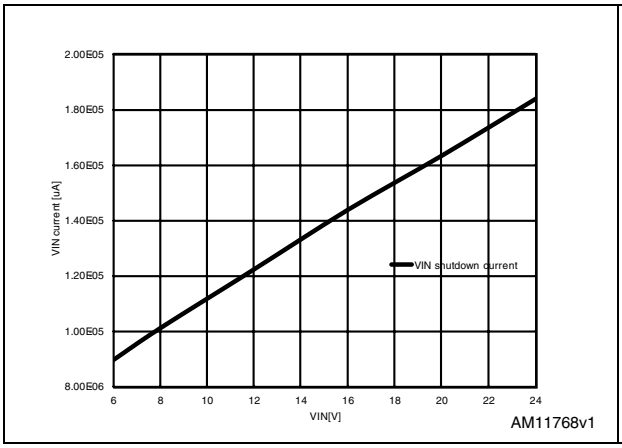


Figure 9. No load V_{IN} current vs. V_{IN} (EN=V_{IN})

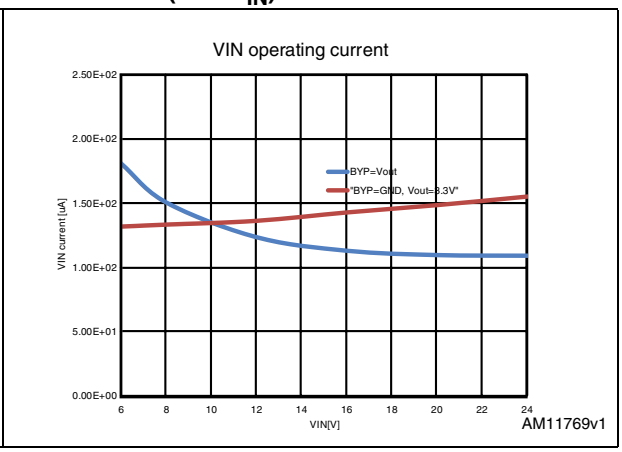


Figure 10. Power-up sequence, no load

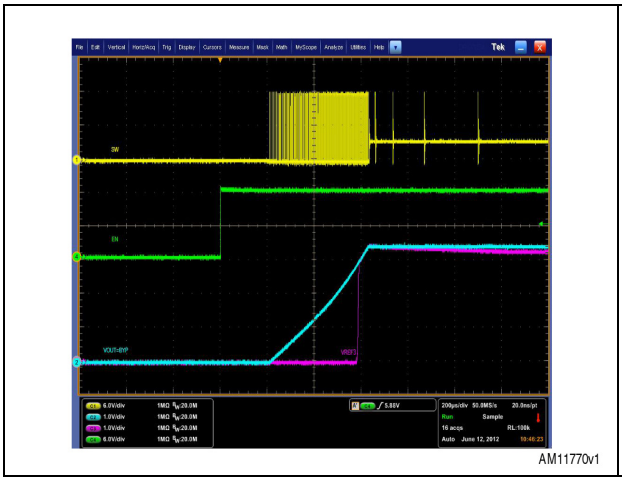


Figure 11. Power-up sequence, 69 Ω load

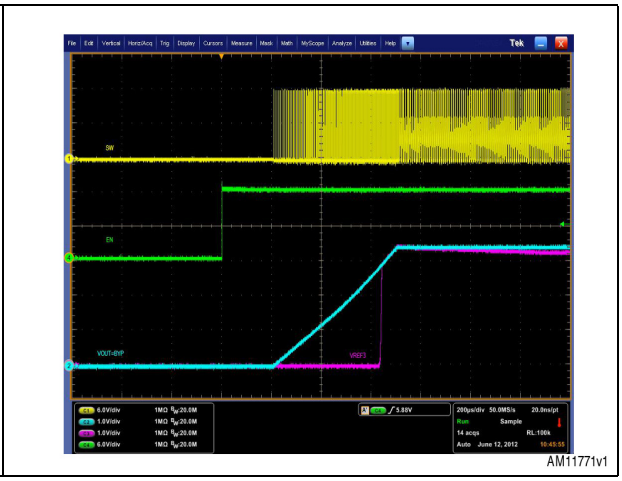


Figure 12. Soft-end, no load

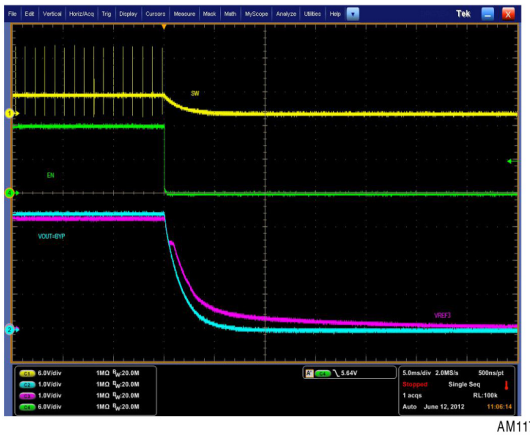


Figure 13. Soft-end, 69 Ω load

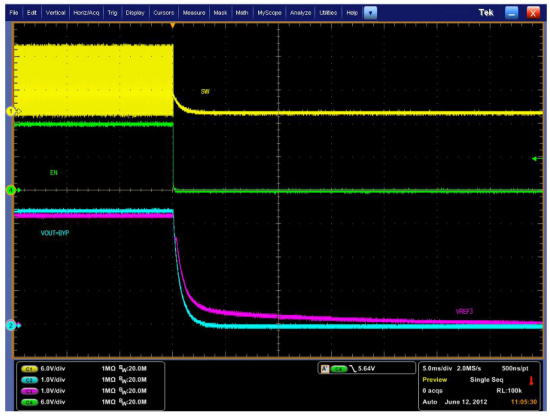


Figure 14. Load transient 0-200 mA

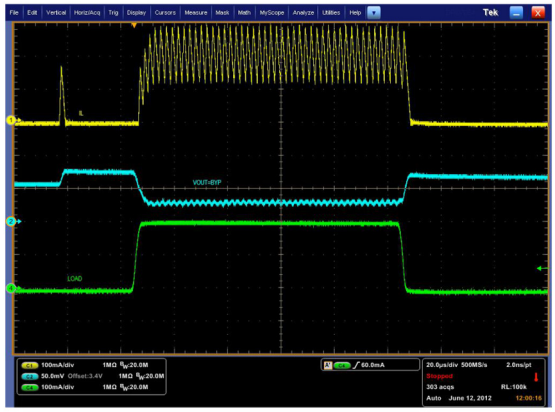


Figure 15. VREF3 load regulation

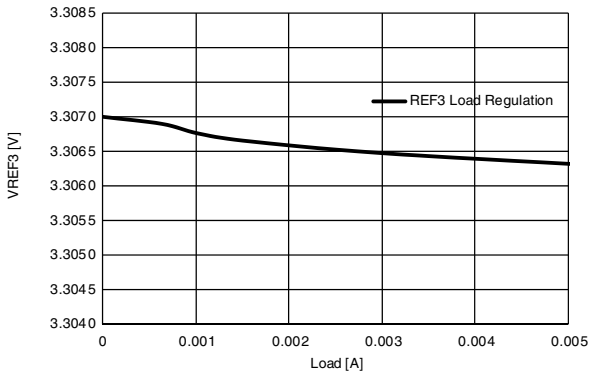


Figure 16. VREF3 line regulation

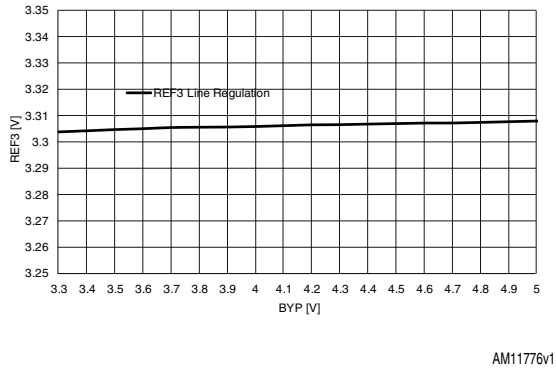


Figure 17. VREF3 line transient

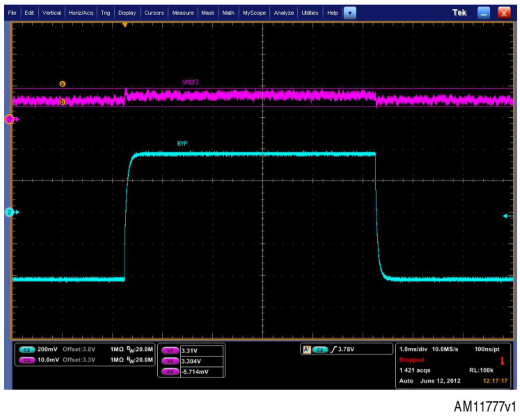
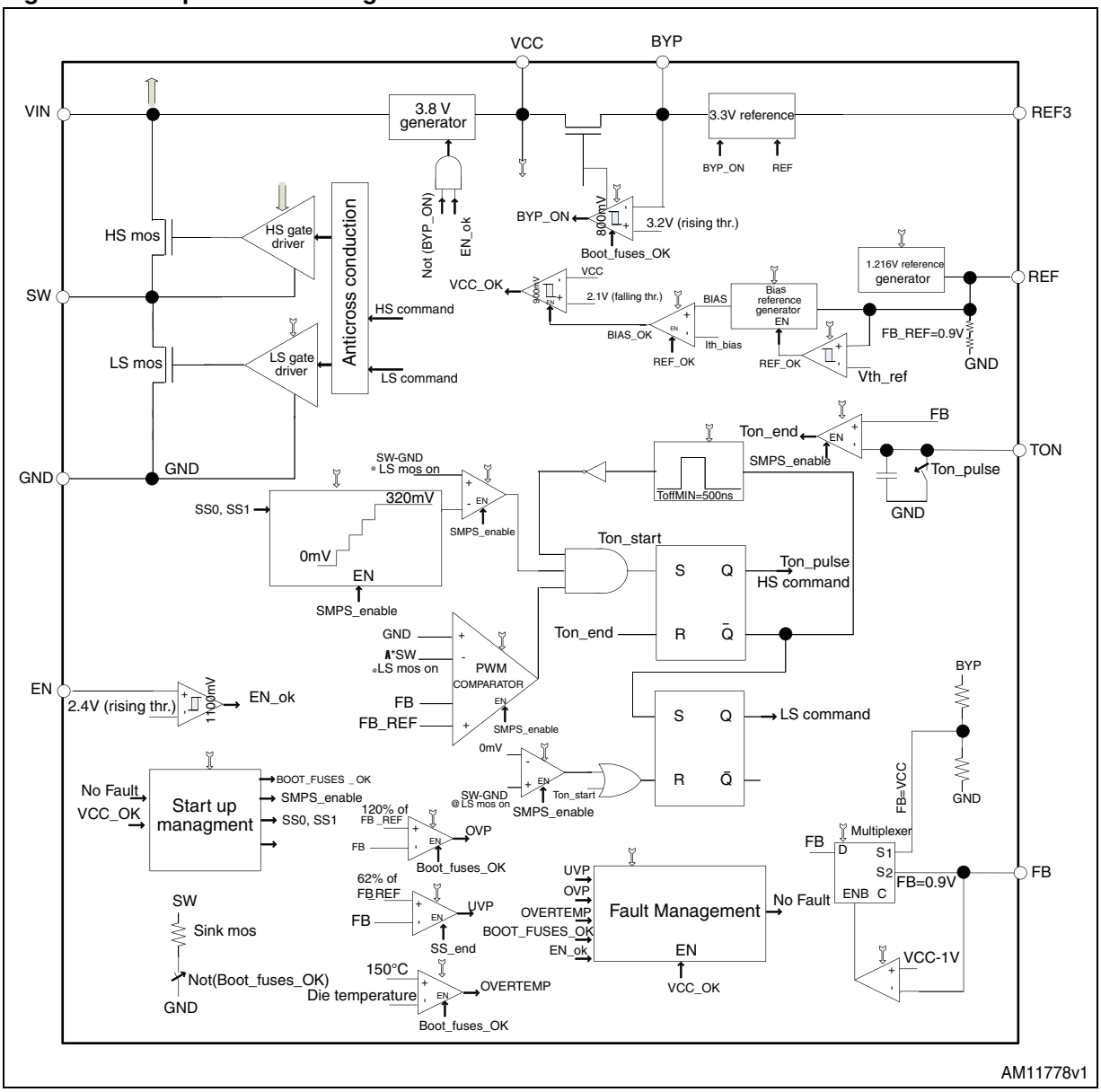


Figure 18. Simplified block diagram



2 Device description

The PM6644 combines a 350 mA valley current limit step-down regulator with a high accuracy 3.3 V voltage reference in a small DFN10 3x3 package.

The switching regulator is based on constant-on-time (COT) architecture. This type of control offers a very fast load transient response with a minimum external component count. The switching regulator can regulate 3.47 V in Fixed mode (the FB pin tied at VCC) or it can deliver an adjustable voltage between 0.9 V and 8 V (the FB pin connected to the output voltage rail through an external resistor divider).

The switching frequency can be adjusted from 200 kHz to 600 kHz by a resistor between TON and the VIN pin.

The embedded input and output voltage feed-forward provides nearly constant switching frequency operation.

A pulse skipping technique allows increasing efficiency at very light load.

The switching regulator has protection against overvoltage, undervoltage and overcurrent.

The power MOSFET and switching controller of the switching regulator are supplied by VCC voltage. An integrated voltage generator from V_{IN} > 6 V provides 3.8 V at the VCC pin when the BYP pin < 2.4 V if BYP > 3.2 V, the integrated voltage generator is turned off and VCC is connected to BYP through a MOSFET switch (switch-over function).

An integrated 3.3 V linear regulator (supplied by VCC) provides an accurate 3.3 V output (REF3).

The PM6644 also provides protection against overtemperature, turning off both switching regulator and 3.3 V reference.

2.1 Switching regulator

2.1.1 Output voltage set-up

The switching sections can be configured in several ways.

Output voltage is configured with the FB pin. If the FB pin is tied to VCC, the PM6644 regulates 3.47 V. Using an external resistor divider the output can be adjusted following this equation:

Equation 1

$$V_{out} = 0.9V \cdot \left(\frac{R1}{R2} + 1\right)$$

where R1, R2 are the resistors of the FB pin divider. REF is a voltage reference used to internally generate the 0.9 V threshold used to set the output voltage of the switching regulator.

2.1.2 Constant-on-time control (COT)

The PM6644 implements a pseudo-fixed frequency algorithm using the COT architecture.

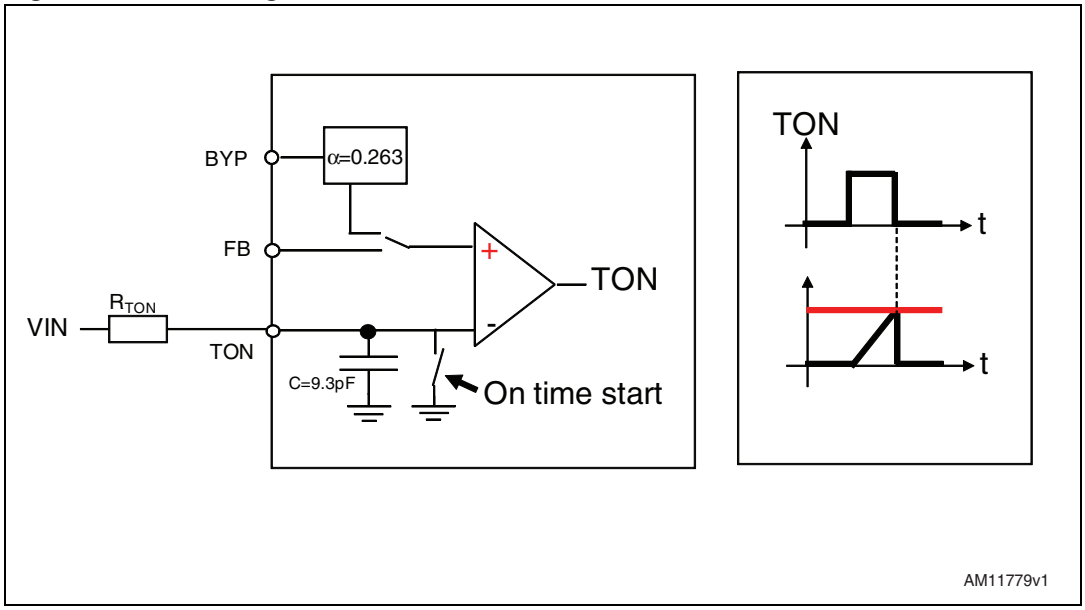
The COT architecture bases its algorithm on the output ripple derived across the output capacitor's ESR. The controller has an internal on-time (T_{ON}) generator triggered on the output voltage valley: when V_{OUT} reaches the regulation value a new T_{ON} starts. The T_{ON} duration is given by the following equation:

Equation 2

$$T_{ON} = \frac{0.9V \cdot R_{TON} \cdot C}{V_{IN}}$$

where T_{ON} is the on-time duration, C is an integrated capacitance (9.3 pF typ.), R_{TON} is the resistor between the VIN and TON pins, V_{OUT} is the sensed output voltage and V_{IN} is the input voltage (sensed at the VIN pin). *Figure 19* shows how the on-time is generated.

Figure 19. On-time generator



The duty cycle in a buck converter is:

Equation 3:

$$\frac{T_{ON}}{T_{SW}} = D = \frac{V_{OUT}}{V_{IN}}$$

The switching frequency in continuous current mode (CCM) is:

Equation 4

$$f_{sw} = \frac{D}{T_{ON}} = \frac{\frac{V_{OUT}}{V_{IN}}}{\frac{0.9V \cdot R_{TON} \cdot C}{V_{IN}}} = \frac{V_{OUT}}{0.9V \cdot R_{TON} \cdot C}$$

In order to reduce noise in T_{ON} generation, a further capacitance C_1 may be added between the TON pin and the GND pin. In this case the switching frequency is:

Equation 5

$$f_{sw} = \frac{D}{T_{ON}} = \frac{\frac{V_{OUT}}{V_{IN}}}{\frac{0.9V \cdot R_{TON} \cdot (C + C_1)}{V_{IN}}} = \frac{V_{OUT}}{0.9V \cdot R_{TON} \cdot (C + C_1)}$$

The switching frequency is theoretically constant, but in a real application it depends on parasitic voltage drops that occur during the charging path (high-side switch resistance, inductor resistance (DCR)) and discharging path (low-side switch resistance, DCR). As a result, the switching frequency increases as a function of the load current. The following table shows some examples of switching frequencies that can be selected through the TON pin (C_1 not mounted):

Table 7. Frequency configurations

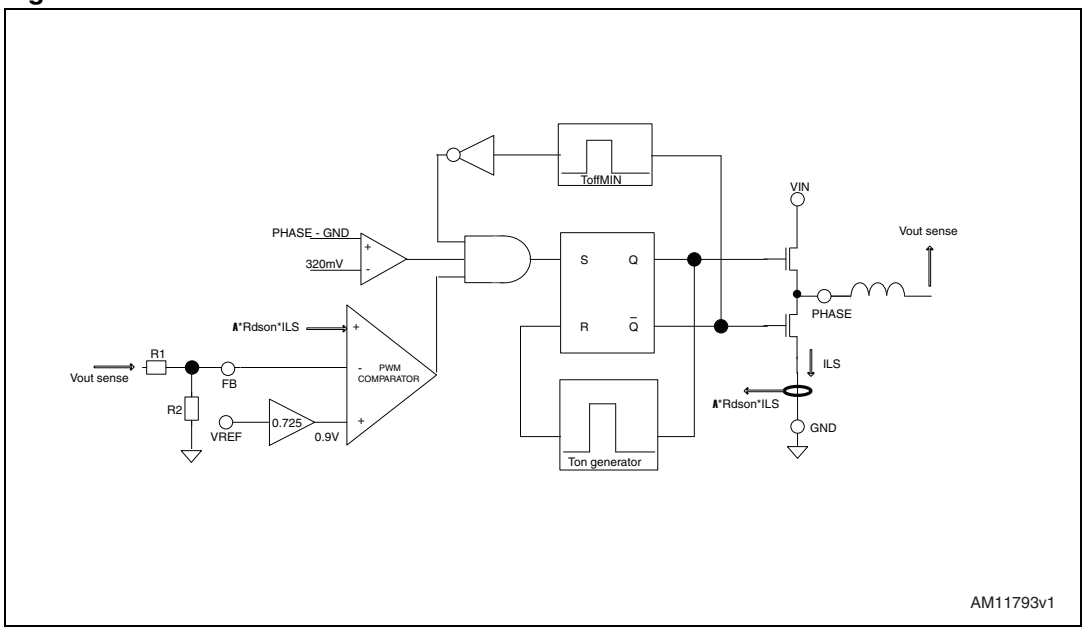
T_{ON} resistor R_T_{ON}	V_{OUT} = 3.47 V frequency load = 200 mA (PWM mode)	V_{OUT} = 0. 9 V frequency load = 200 mA (PWM mode)
2 M	245 kHz	
1 M	470 kHz	
500 K		260 kHz
250 K		495 kHz

2.1.3 PWM control

Figure 20 shows the simplified schematic of the constant-on-time controller. The COT architecture uses a minimum OFF-time (T_{OFFMIN} = 500 ns typ.) to allow inductor valley current sensing on the synchronous switch. A minimum on-time is also introduced to assure the correct startup sequence.

An adaptive anti-cross conduction algorithm avoids current paths between VIN and GND during switching transition.

Figure 20. Constant-on-time controller architecture



The PM6644 has a one-shot generator that turns on the high-side MOSFET when the following conditions are satisfied simultaneously:

- The PWM comparator is high
- The inductor valley current is below the current limit threshold
- The minimum OFF-time has timed out

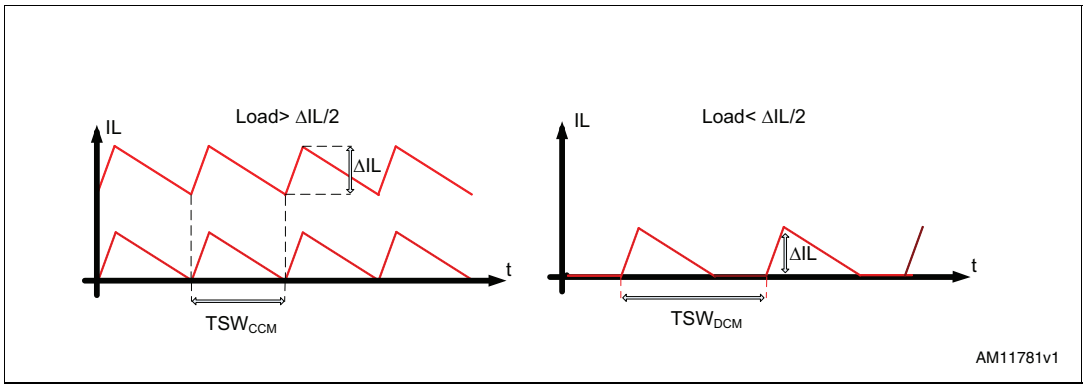
A slope proportional to the low-side MOSFET current (A * $R_{DS(on)}$ * I_{LS}) is added at the input of the PWM comparator in order to ensure stability. The slope determines a load line on the output voltage of about 0.16 Ω when the controller works in PWM mode.

2.1.4 Skip mode management

To improve efficiency at light load, the PM6644 implements pulse skip operation mode. The inductor current is sensed and, if it is equal to zero, the synchronous MOSFET is turned off. As a consequence, the output capacitor is left floating and the discharge depends only on the current sourced by the load. The new T_{ON} starts when the output reaches the voltage regulation. As a consequence, at light load conditions the switching frequency decreases, improving the total efficiency of the converter. Working in discontinuous current mode, the switching and the conduction losses are reduced by skipping some cycles.

If the output load is high enough to make the system work in CCM (continuous conduction mode), Skip mode is automatically changed into PWM mode.

Figure 21. Inductor current in skip mode



2.1.5 Current sensing and current limit

The PM6644 implements a positive valley current limit to protect the application from an overcurrent fault. The inductor current is sensed during the OFF-time T_{OFF} by measuring the voltage drop across the integrated low-side MOSFET using the MOSFET $R_{DS(on)}$ as a lossless sensing element. The voltage drop is then compared with a fixed voltage threshold so that the inductor (or low-side MOSFET) trip current of the comparator is about 350 mA (minimum value).

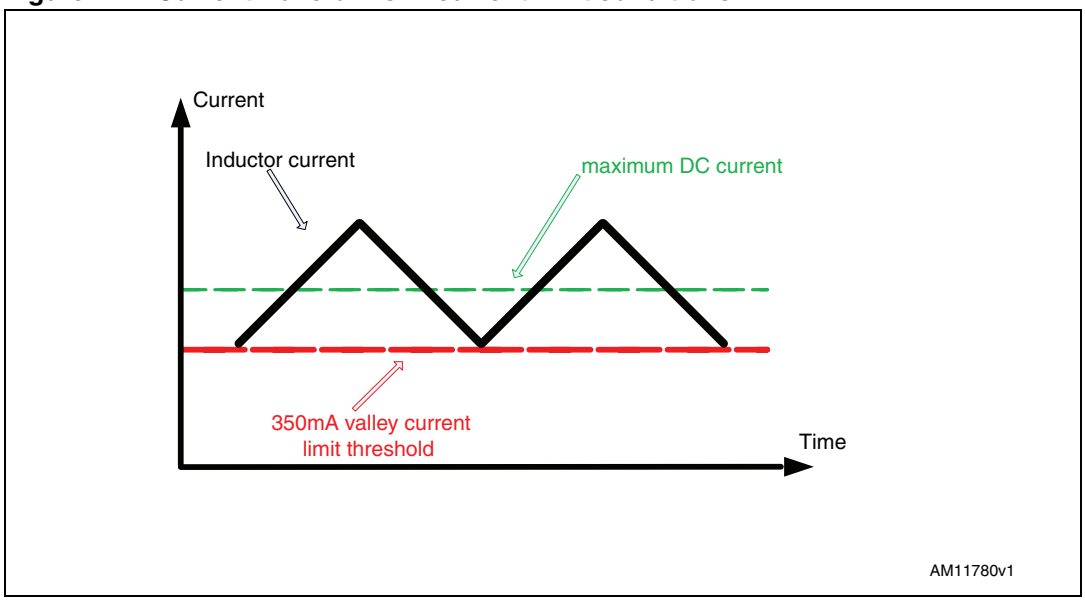
A new switching cycle cannot start until the inductor current goes lower than the 350 mA current limit threshold. As a result, the device can work with a maximum inductor RMS current I_{LRMS} (max) equal to:

Equation 6

$$I_{LRMS}(max) = 350mA + \frac{\Delta I_L}{2}$$

where ΔI_L is the inductor current ripple.

Figure 22. Current waveforms in current limit conditions



2.1.6 Soft-start and soft-end

The switching section has an EN pin. A non-programmable soft-start procedure takes place when the EN pin rises above 2.1 V.

To prevent high input inrush currents, the current limit is increased from 25% to 100% of the current limit threshold with steps of 25%.

The procedure is not programmable and ends typically in 2.8 ms. The overvoltage protection is always active while the undervoltage protection is enabled at the end of the 2.8 ms.

Driving one EN pin below 1.8 V makes the section perform a soft-end: gate driving signals are pulled low and the output is discharged through an internal MOSFET with $R_{DS(on)}$ of 50 Ω typ.

2.1.7 Monitoring

The PM6644 controls its switching output to prevent any damage or uncontrolled working condition.

2.1.8 Overvoltage protection

The PM6644 provides a latched overvoltage protection (OVP). If the output voltage rises above 120% of the nominal value, a latched OVP protection is activated. The controller turns on the low-side MOSFET keeping the output voltage at 0 V.

The protection is latched and this fault is cleared by cycling VCC < 2.1 V and then > 3 V.

2.1.9 Undervoltage protection

If, during regulation, the output voltage drops under 62% of the nominal value, an undervoltage latched fault is detected. The controller performs a soft-end procedure (see *Section 2.1.6*). The undervoltage fault is reset by toggling the EN pin or by cycling VCC < 2.1 V and then > 3 V.

2.1.10 VCC undervoltage

The device monitors the voltage at the VCC pin. The switching section can start operating only if the voltage at the PVCC pin is above 3 V. If PVCC falls below 2.1 V, the switching section is turned off until PVCC voltage goes over 3 V.

Table 8. Fault management summary

Fault	Condition	Device behavior
Overvoltage	V_{OUT} > +120%	The low-side MOSFET is turned on keeping the output voltage at 0 V. Latched fault, cleared toggling EN or cycling VCC < 2.1 V and then > 3 V.
Undervoltage	V_{OUT} < 62%	The controller performs a soft-end. Latched fault cleared toggling EN or cycling VCC < 2.1 V and then > 3 V.
VCC undervoltage	V_{CC} < 2.1 V	The controller turns off the switching section until PVCC voltage goes over 3 V. Not latched fault.

2.1.11 VCC and BYP power management

VCC supplies both the controller and the drivers of the integrated high-side and low-side MOSFETs. An integrated 3.8 V generator from the VIN pin provides the voltage to the VCC pin.

The PM6644 provides a switch-over function that allows the turning-off of the 3.8 V generator when a voltage is applied at the BYP pin. If the voltage at the BYP pin is higher than 3.2 V, the internal generator is turned off and the VCC pin is connected with an internal switch (16 Ω typ.) to the BYP pin. This feature decreases the power dissipation of the device.

If BYP < 2.4 V, the internal switch is turned off and the VCC output is supplied with the 3.8 V generator.

Table 9. VCC and BYP management (EN pin > 2 V)

BYP	VIN	VCC	5 V generator	Switch-over resistance
< 2.4 V	< 6 V	V_{IN}- 1 V	Enabled	
< 2.4 V		3.8 V	Enabled	
> 3.2 V		BYP	Disabled	16 Ω

2.1.12 3.3 V linear regulator section (REF3)

The PM6644 has an integrated linear regulator (REF3) that can provide a maximum RMS current of 5 mA. The input of the linear regulator is the BYP pin. The linear regulator is turned on when BYP > 3.2 V. Connect pin REF3 with a 100 nF ceramic capacitor to GND.

2.1.13 General fault management: thermal protection

If the internal temperature of the device exceeds typically +150 °C, the controller shuts down immediately all the internal circuitry. The switching section performs the soft-end management. Toggling EN or cycling VCC < 2.1 V and then VCC > 3 V, resets the latched fault.

3 Application information

3.1 External component selection

3.1.1 Inductor selection

Once the switching frequency is defined, inductor selection depends on the desired inductor ripple current and load transient performance.

Low inductance means greater ripple current and may generate greater output noise. On the other hand, low inductor values involve fast load transient response.

A good compromise between the transient response time, the efficiency, the cost and the size, is to choose the inductor value in order to maintain the inductor current ripple ΔI_L between 20% and 50% of the maximum output current I_{LOAD}(max.). The maximum ΔI_L occurs at the maximum input voltage. With these considerations, the inductor value can be calculated with the following relationship:

Equation 7

$$L = \frac{V_{IN} - V_{OUT}}{f_{sw} \cdot \Delta I_L} \cdot \frac{V_{OUT}}{V_{IN}}$$

where f_{SW} is the switching frequency, V_{IN} is the input voltage, V_{OUT} is the output voltage and ΔI_L is the selected inductor current ripple.

In order to prevent overtemperature working conditions, the inductor must be able to provide an RMS current greater than the maximum RMS inductor current I_{LRMS}:

Equation 8

$$I_{LRMS} = \sqrt{(I_{LOAD}(max))^2 + \frac{(\Delta I_L(max))^2}{12}}$$

where ΔI_L (max.) is the maximum current ripple:

Equation 9

$$\Delta I_L(max) = \frac{V_{INmax} - V_{OUT}}{f_{sw} \cdot L} \cdot \frac{V_{OUT}}{V_{INmax}}$$

If hard saturation inductors are used, the inductor saturation current should be much greater than the maximum inductor peak current Ipeak:

Equation 10

$$Ipeak = I_{LOAD}(max) + \frac{\Delta I_L(max)}{2}$$

Using soft saturation inductors it is possible to choose inductors with a saturation current limit at nearly Ipeak. In *Table 10* there is a list of some inductor part numbers.

.

Table 10. Inductor part number

Manufacturer	Part number	Inductance (µH)	DCR (Ω)	RMS current (A)(1)	Saturation current (A)(2)
Coilcraft	EPL3015-333ML	33	0.989	0.59	0.32
Coilcraft	LPS3314-333ML	33	0.92	0.58	0.38
Coilcraft	MSS5121-333ML	33	0.48	0.76	0.64

1. 40 °C temperature rise.
2. 20% inductance drop.

3.1.2 Input capacitor selection

In a buck topology converter the current that flows into the input capacitor is a pulsed current with zero average value. The input RMS current of the switching regulator can be roughly estimated as follows:

Equation 11

$$I_{CinRMS} = I_{LOAD}(max) \cdot \sqrt{D \cdot (1 - D)}$$

where D is the duty cycles and I_{LOAD}(max.) is the maximum load current of the switching regulator. The input capacitor should be chosen with an RMS rated current higher than the maximum RMS current given by the formula.

Tantalum capacitors are good in terms of low ESR and small size, but they can occasionally burn out if subjected to very high current during the charge.

Ceramic capacitors usually have a higher RMS current rating with smaller size and they remain the best choice. In battery-powered applications, a 1-2.2 µF input ceramic capacitor can be enough.

Table 11 shows an example of ceramic capacitor part numbers.

Table 11. Input capacitor part numbers

Manufacturer	Part number	Capacitor value (µF)	Rated voltage
TAYIO YUDEN	TMK212BJ225MG-T	2.2	25

3.1.3 Output capacitor selection

The controller can work with ceramic or tantalum output capacitors.

The selection of the output capacitor impacts on the stability of the controller:

Equation 12

$$C_{OUT} > \frac{18 \cdot \alpha}{2 \cdot \Pi \cdot f_{sw} \cdot k}$$

Equation 13

$$\alpha = \frac{0.9V}{V_{OUT}}$$

K is a constant (< 0.1) that defines the ratio between the controller bandwidth and the switching frequency.

The output capacitor must store the inductor energy generating an output ripple within the output voltage ripple requirements.

If an output tantalum capacitor is used, in CCM the voltage ripple $V_{RIPPLEout}$ is given by:

Equation 14

$$V_{RIPPLEout} = R_{out} \cdot \Delta I_L$$

A low ESR capacitor is required to reduce the output voltage ripple.

If an output ceramic capacitor is used, in CCM the voltage ripple $V_{RIPPLEout}$ is given by:

Equation 15

$$V_{RIPPLEout} = \frac{T_{sw} \cdot \Delta I_L}{8 \cdot C_{OUT}}$$

Finally the output capacitor choice heavily impacts the load transient response.

Table 12 shows a list of some capacitor part numbers.

Table 12. Output capacitor part number

Manufacturer	Part number	Capacitor value (µF)	Rated voltage (V)	ESR max. (MΩ)
TAYIO YUDEN	JMK212BJ226MG-T	22	6.3	70
SANYO	POSCAP 6TPC33M	33	6.3	7 to 15

3.1.4 Maximum RMS output current

Both high-side and low-side embedded power MOSFETs of the switching regulator can withstand a maximum RMS current of 300 mA.

The maximum sustainable RMS output current $I_{LOADRMS}$ of the switching regulator depends on the application specifications of:

- input voltage V_{IN}
- output voltage V_{OUT}
- inductor current ripple ΔI_L (that depends on the switching frequency F_{SW} and on the inductor value L, according to *Equation 7*).

The maximum RMS currents of high-side ($I_{RMS,HS}$) and low-side ($I_{RMS,LS}$) MOSFETs are given by:

Equation 16

$$I_{RMS,\ HS} = D \cdot I_{LRMS} = D \cdot \sqrt{(I_{LOAD})^2 + \frac{(\Delta I_L)^2}{12}} = 300mA$$

Equation 17

$$I_{RMS,\ LS} = I_{LRMS} = (1-D) \cdot \sqrt{(I_{LOAD})^2 + \frac{(\Delta I_L)^2}{12}} = 300mA$$

where I_{LOAD} is the RMS output current.

The minimum I_{LOAD} between equation 16 and equation 17, combined with RMS load current limitation due to valley current limit (*Equation 6*), determines the maximum RMS output current $I_{LOADRMS}$ sustained by the switching regulator:

Equation 18

$$I_{LOADRMS} = MIN\left\{\begin{array}{c}\sqrt{\left(\frac{300mA}{D}\right)^2 - \frac{(\Delta I_L)^2}{12}} \\ \sqrt{\left(\frac{300mA}{1-D}\right)^2 - \frac{(\Delta I_L)^2}{12}} \\ 350mA + \frac{\Delta I_L}{2}\end{array}\right\}$$

Example 1

V_{IN} = 5 V, FB = VCC (V_{OUT} = 3.47 V), ΔI_L= 68.5 mA (L = 33 uH, Fsw = 470 kHz).

High-side can withstand a load current of $I_{LOADRMS}$ = 432 mA.

Low-side can withstand a load current of $I_{LOADRMS}$ = 977 mA.

$I_{LOADRMS}$ due to valley current limit = 384 mA.

As a result, $I_{LOADRMS}$ = 384 mA (limitation determined by the valley current limit).

The PM6644 switching regulator can source 384 mA RMS. 384 mA is also the peak load current.

Example 2

V_{IN} = 25 V, FB = VCC (V_{OUT} = 3.47 V), ΔI_L = 192.5 mA (L = 33 uH, Fsw = 470 kHz).

High-side can withstand a load current of $I_{LOADRMS}$ = 2164 mA.

Low-side can withstand a load current of $I_{LOADRMS}$ = 344 mA.

$I_{LOADRMS}$ due to valley current limit = 446 mA.

As a result, $I_{LOADRMS}$ = 344 mA (limitation determined by the low-side RMS max. current).

The PM6644 switching regulator can source 344 mA RMS. The peak load current is 446 mA.

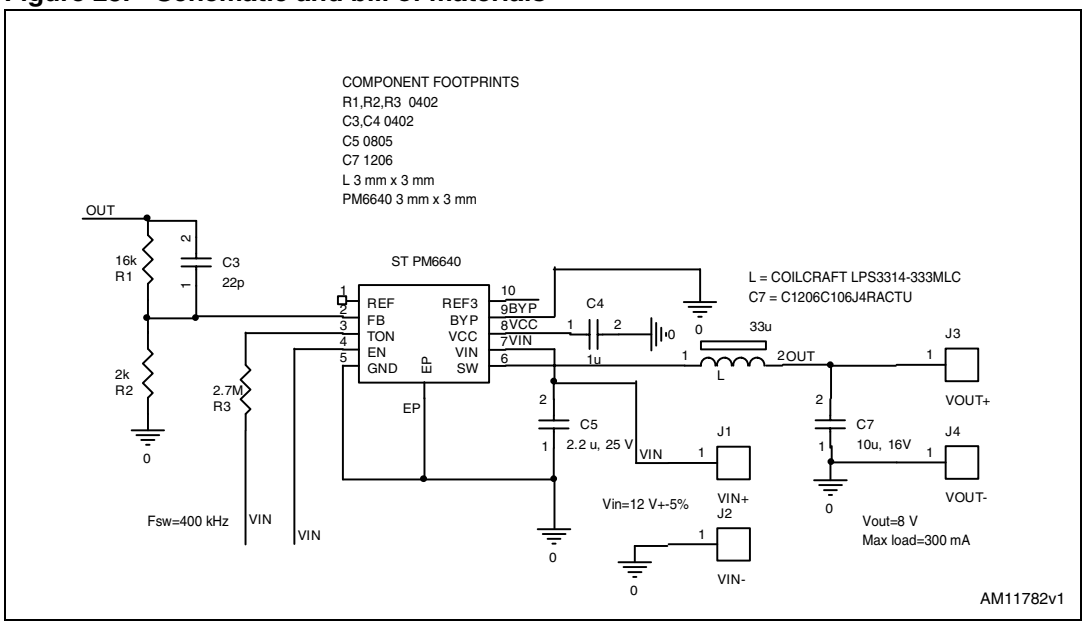
4 Typical application configuration V_{OUT} = 8 V

This section is intended as a guideline for all the measurements involving the PM6644 device with V_{IN} = 12 V ±5%, V_{OUT} = 8 V.

4.1 Test set configuration

The device-under-test (D.U.T.) has been mounted on the designed evaluation kit with the following schematic and bill of materials.

Figure 23. Schematic and bill of materials



4.2 Characterization report

Steady-state waveforms

Figure 24. No load

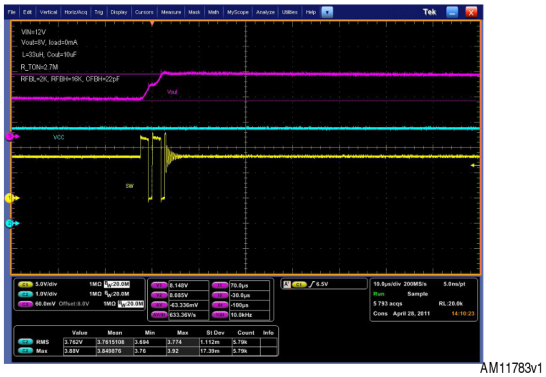


Figure 25. Load = 50 mA

Figure 26. Load = 100 mA. Switching frequency = 370 kHz

AM11785v1

Figure 27. Load = 300 mA. Switching frequency = 410 kHz

AM11786v1

Figure 28. Load step = 0 to 300 mA

AM11787v1

4.3 Efficiency vs. load (V_{IN} = 12 V, V_{OUT} = 8 V)

The output voltage varies from 8.096 V at light load to 7.916 V at heavy load. Load regulation = 180 mV.

Figure 29. Efficiency

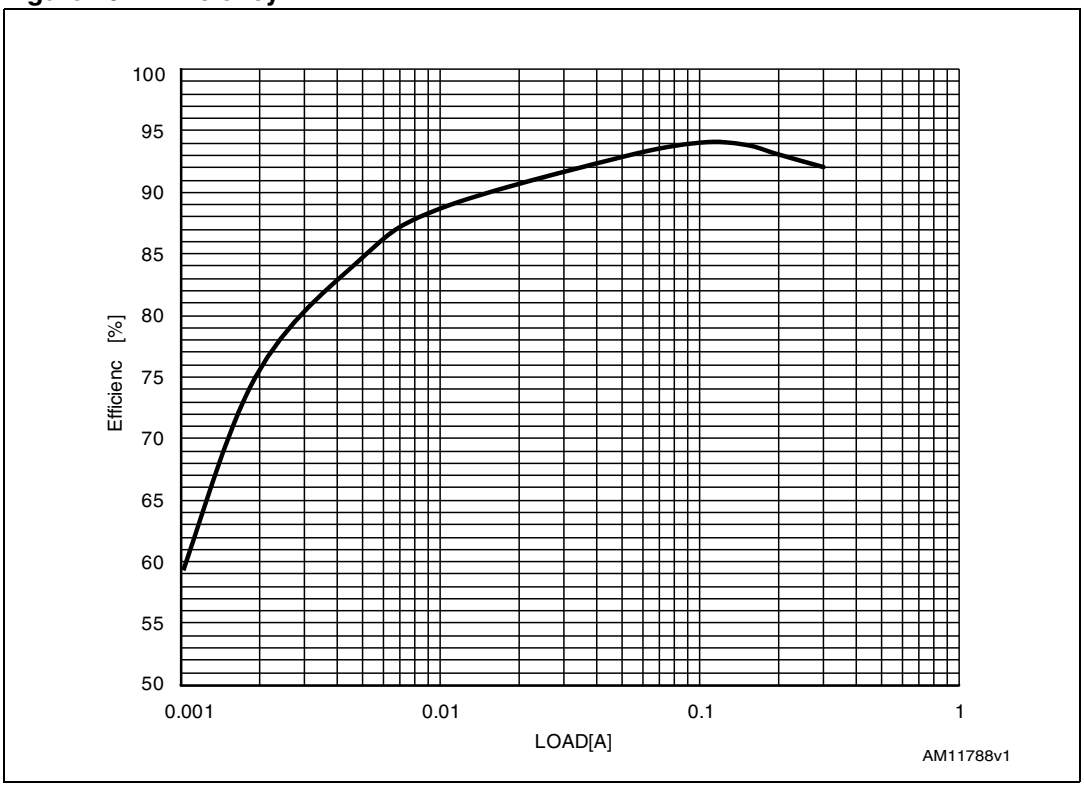
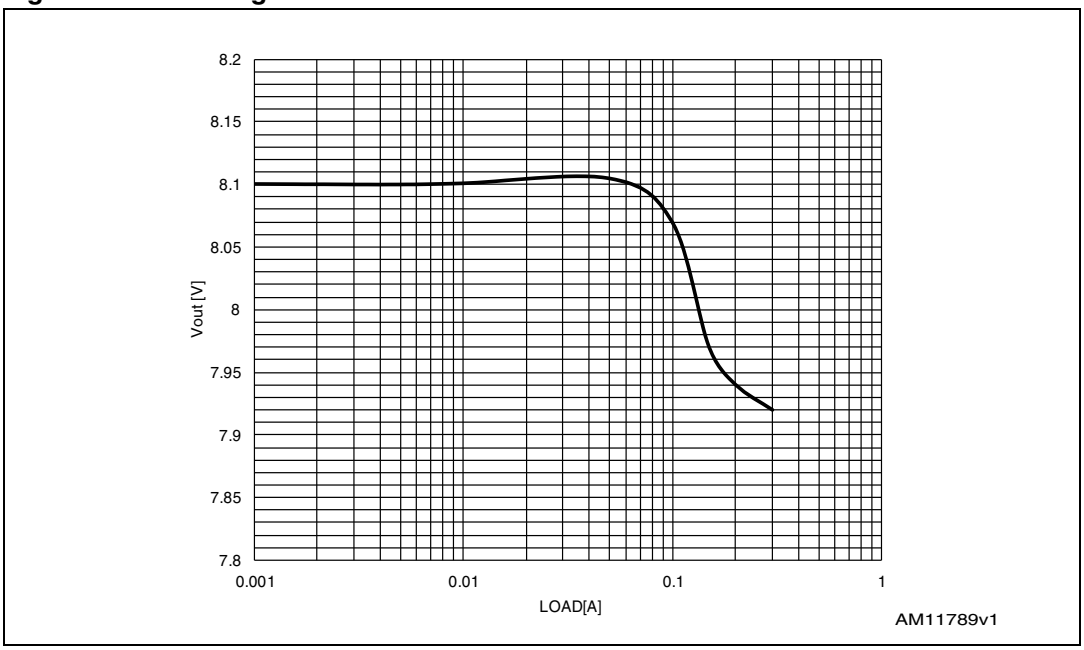


Figure 30. Load regulation



Bias current

VIN =12.158 V	VIN = 12.158 V
V_{out} = 8.150 V (externally forced)	V_{out} = 8.107 V
No switching	No load, pulse skipping (820 Hz, double pulses)
BYP = GND	BYP = GND
IVIN = 126 µA	IVIN = 444 µA

5 Conclusion

The device regulates V_{OUT} = 8 V properly with the designed schematic and bill of material. The 12 V input voltage range should have an accuracy of ± 5%.

PCB design guidelines

The layout is very important in terms of efficiency, stability and system noise. It is possible to refer to the PM6644 evaluation kit board for a complete layout example.

For good PC board layout, follow these guidelines:

- Place all the power components (inductors, input and output capacitors) on the top side. Refer them to a ground plan, GND in an inner layer. Connect the exposed pad of the PM6644 to the GND plan with vias (design a GND pad on the top side with the same size as the exposed pad). On the top side connect the GND pin with a short trace to the exposed pad.
- Place input capacitors close to the VIN pin, in order to minimize AC current drops during high-side MOSFET turn-on. Add vias to the GND plan.
- Place the output capacitor close to the GND pin, in order to minimize AC current drops during high-side and low-side MOSFET turn-on. Add vias to the GND plan.
- Place filtering capacitors close to pins REF3, BYP and VCC.
- Place the resistor near the TON pin in order to minimize parasitic capacitance on the TON pin.

Figure 31. Recommended layout - top layer

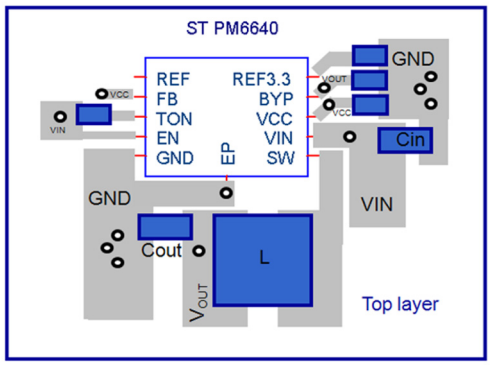


Figure 32. Recommended layout - inner layer

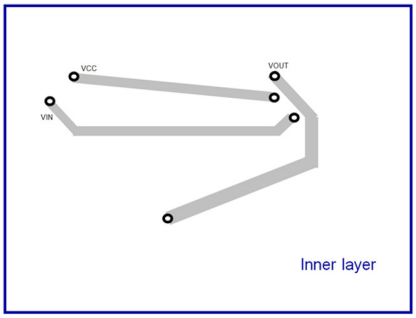
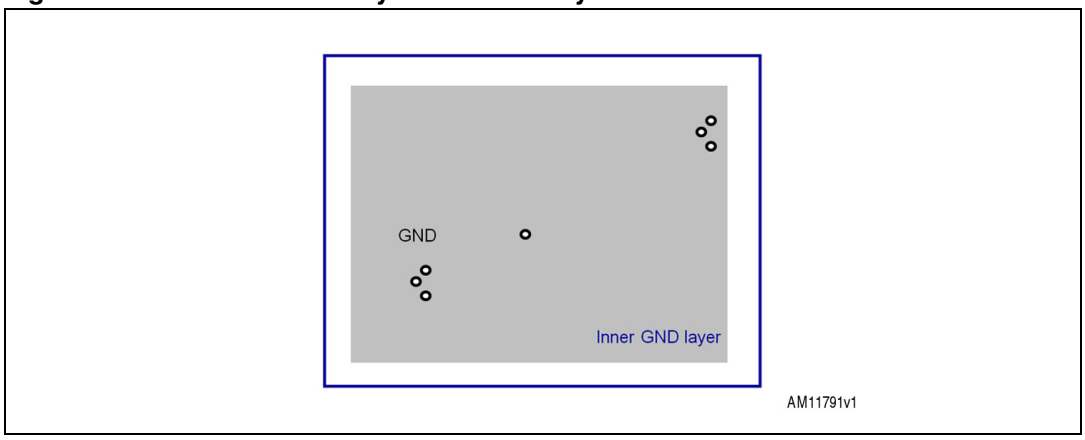


Figure 33. Recommended layout - bottom layer



6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 13. DFN10 (3x3 mm) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1		0.02	0.05
A2	0.55	0.65	0.80
A3		0.20	
b	0.18	0.25	0.30
D	2.85	3.00	3.15
D2	2.20		2.70
E	2.85	3.00	3.15
E2	1.40		1.75
e		0.50	
L	0.30	0.40	0.50
ddd			0.08

Figure 34. DFN10 (3x3 mm)

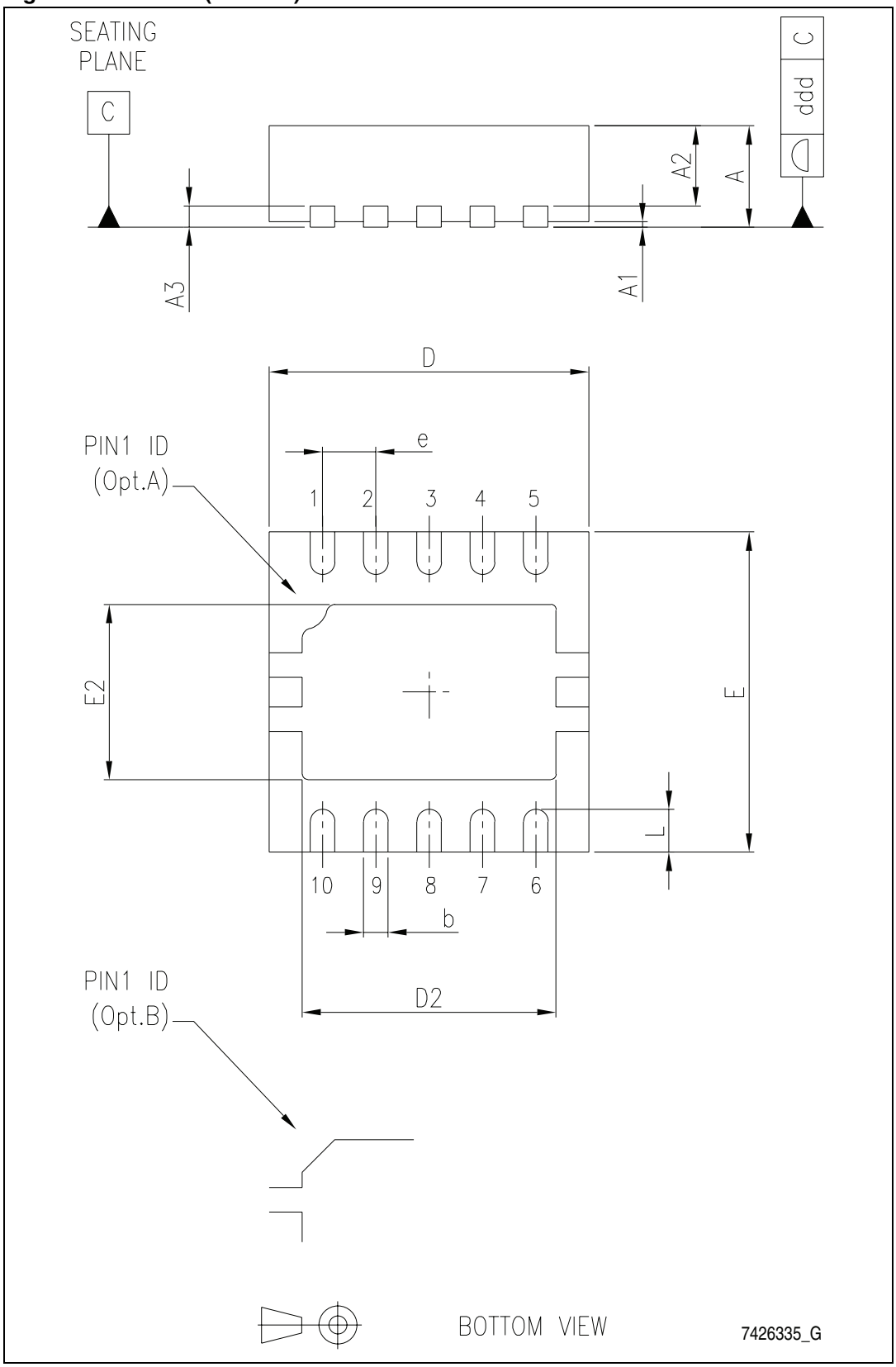
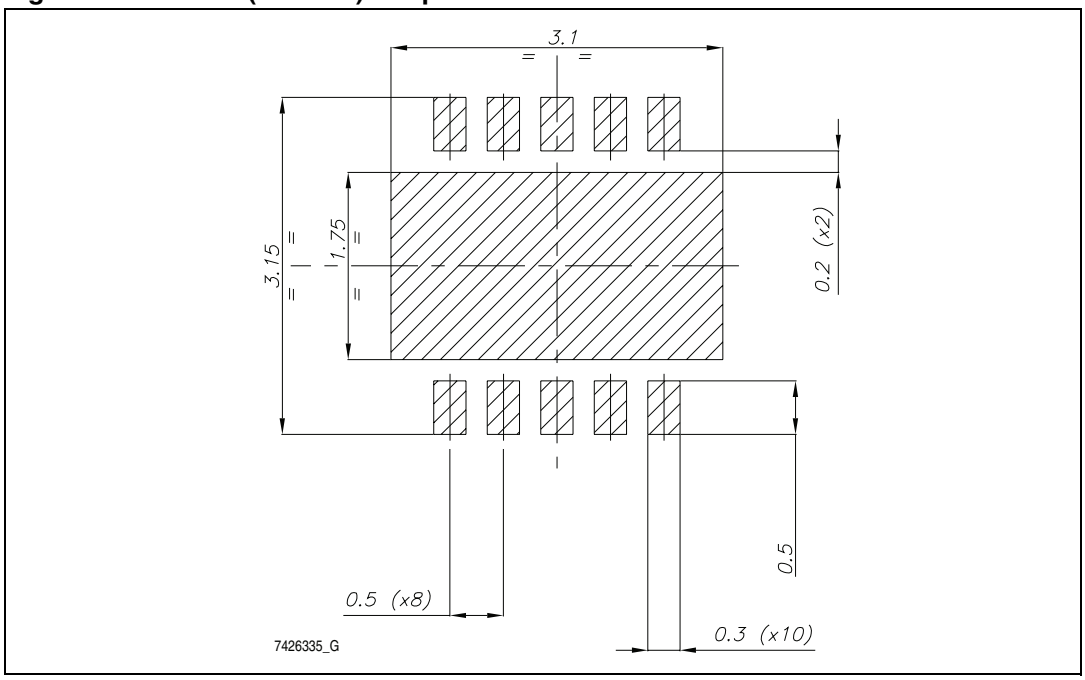


Figure 35. DFN10 (3x3 mm) footprint



7 Revision history

Table 14. Document revision history

Date	Revision	Changes
19-Jun-2012	1	Initial release.

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