PM6670A

Complete DDR2/3 memory power supplies controller

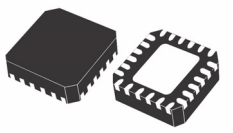
Preliminary Data

Features switching

- Switching section (VDDQ)
  - 4.5V to 36V input voltage range
  - 0.9V, ±1% voltage reference
  - 1.8V (DDR2) or 1.5V (DDR3) fixed output voltages
  - 0.9V to 2.6V adjustable output voltage
  - 1.237V ±1% reference voltage available
  - Very fast load transient response using constant-on-time control loop
  - No R_{SENSE} current sensing using low side MOSFETs' $R_{DS(ON)}$
  - Negative current limit
  - Latched OVP and UVP
  - Soft start internally fixed at 3ms
  - Selectable pulse skipping at light load
  - selectable No-Audible (33KHz) pulse skip mode
  - Ceramic output capacitors supported
  - Output voltage ripple compensation
- VTT LDO and VTTREF
  - 2Apk LDO with foldback for VTT
  - Remote VTT sensing
  - High-Z VTT output in S3
  - Ceramic output capacitors supported
  - ±15mA Low noise buffered reference

Applications

- DDR2/3 memory supply
- Digital TV system
- Handheld and PDAs
- CPU and chipset I/O supplies
- SSTL18, SSTL15 and HSTL bus termination



VFQFPN-24 4x4

Description

The device PM6670A is a complete DDR2/3 power supply regulator designed to meet JEDEC specifications.

It integrates a Constant On-Time (C.O.T.) buck controller, a 2Apk sink/source Low Drop Out regulator and a 15mA low noise buffered reference.

The C.O.T. architecture assures fast transient response supporting both electrolytic and ceramic output capacitors. An embedded integrator control loop compensates the DC voltage error due to the output ripple.

The 2Apk sink/source linear regulator provides the memory termination voltage with fast load transient response.

The device is full compliant with system sleep states S3 and S4/S5, providing LDO output high impedance in Suspend-To-RAM and Tracking Discharge of all outputs in Suspend-To-Disk.

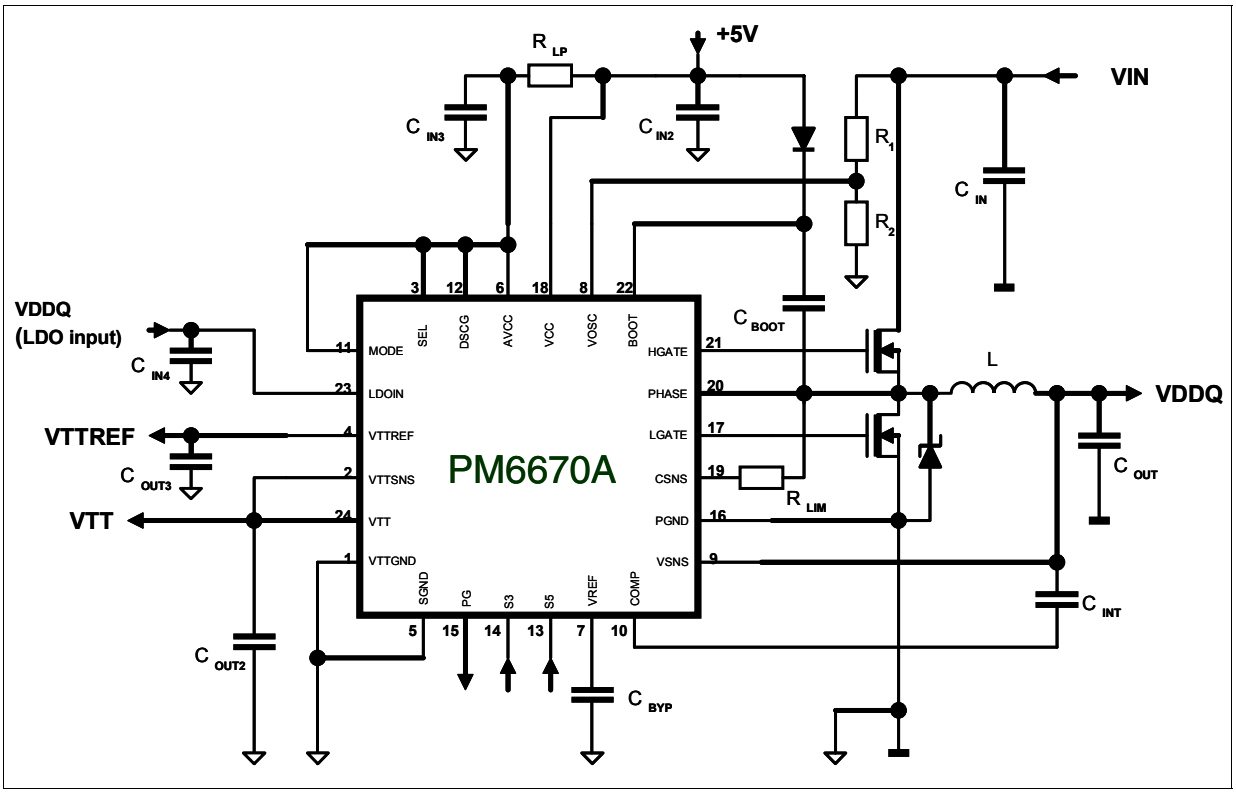
Order codes

Part number	Package	Packaging
PM6670A	VFQFPN-24 4x4 (Exposed Pad)	Tube

Contents

1 Typical application circuit

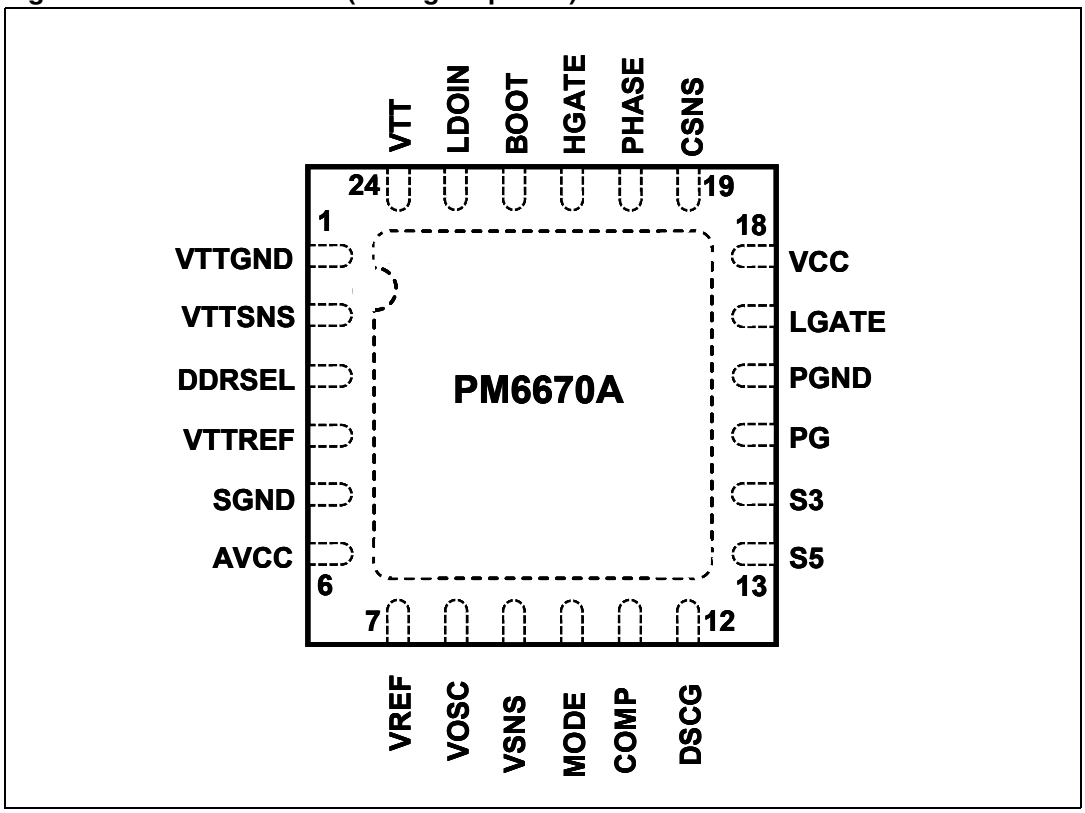
Figure 1. Application circuit



2 Pin settings

2.1 Connections

Figure 2. Pin connection (through top view)



2.2 Pin description

Table 1. Pin functions

N°	Pin	Function
1	VTTGND	LDO Power Ground. Connect to negative terminal of VTT output capacitor.
2	VTTSNS	LDO Remote Sensing. Connect as close as possible to the load via a low noise PCB trace.
3	DDRSEL	DDR Voltage Selector (if MODE is tied to VCC) or Pulse-Skip/No-Audible Pulse-Skip Selector in Adjustable Mode (MODE voltage lower than 3V). See *Mode of Operation Selection* section for details.
4	VTTREF	Low Noise Buffered DDR Reference Voltage. A 22nF (minimum) ceramic bypass capacitor is required in order to achieve stability.
5	SGND	Ground Reference for analog circuitry, control logic and VTTREF buffer. Connect together with the thermal pad and VTTGND to a low impedance ground plane. See the *Application Note* for details.
6	AVCC	+5V Supply for internal logic. Connect to +5V rail through a simple RC filtering network.
7	VREF	High accuracy output Voltage Reference (1.237V) for multilevel pins setting. It can deliver up to 50µA. Connect a 100nF capacitor between VREF and SGND in order to enhance noise rejection.
8	VOSC	Frequency Selection. Connect to the central tap of a resistor divider to set the desired switching frequency. The pin cannot be left floating. See *Device Description* section for details.
9	VSNS	VDDQ Output Remote Sensing. Discharge path for VDDQ in Non-Tracking Discharge. Input for internal resistor divider that provides VDDQ/2 to VTTREF and VTT. Connect as close as possible to the load via a low noise PCB trace.
10	MODE	Mode of operation selector. If MODE pin voltage is higher than 4V, the fixed output mode is selected. If MODE pin voltage is lower than 4V, it is used as negative input of the error amplifier. See *Mode of Operation Selection* section for details.
11	COMP	DC Voltage Error Compensation Input for the switching section. Refer to *Mode of Operation Selection* section for more details.
12	DSCG	Discharge Mode Selection. Refer to *Output Discharge Selection* section for Tracking/Non-tracking Discharge or No-Discharge options.
13	S5	Switching Controller Enable. Connect to S5 system status signal to meet S0-S5 power management states compliance. See *Power Management Pins* section for details.
14	S3	Linear Regulator Enable. Connect to S3 system status signal to meet S0-S5 power management states compliance. See *Power Management Pins* section for details.
15	PG	Power-Good Signal (open drain output). High when VDDQ output voltage is within ±10% of nominal value.
16	PGND	Power Ground for the switching section.
17	LGATE	Low-side Gate Driver Output.

Table 1. Pin functions (continued)

N°	Pin	Function
18	VCC	+5V Low-side Gate Driver Supply. Bypass with a 100nF capacitor to PGND.
19	CSNS	Current Sense Input for the switching section. This pin must be connected through a resistor to the drain of the synchronous rectifier (RDSon sensing)
20	PHASE	Switch Node Connection and return path for the High-side Gate Driver.
21	HGATE	High-side Gate Driver Output
22	BOOT	Bootstrap Capacitor Connection. Positive Supply Input of the High-side Gate Driver.
23	LDOIN	Linear Regulator Input. Connect to VDDQ in normal configuration or to a lower supply to reduce the power dissipation. A 10µF bypass ceramic capacitor is suggested for noise rejection enhancement. See Device Description section for more details.
24	VTT	LDO Linear Regulator Output. Bypass with a 20µF (2x10µF MLCC) filter capacitor.

3 Electrical data

3.1 Maximum rating

Table 2. Absolute maximum ratings (1)

Symbol	Parameter	Value	Unit
V_{AVCC}	AVCC to SGND	-0.3 to 6	V
V_{VCC}	VCC to SGND	-0.3 to 6	
	PGND, VTTGND to SGND	-0.3 to 0.3	
	HGATE and BOOT to PHASE	-0.3 to 6	
	HGATE and BOOT to PGND	-0.3 to 44	
V_{PHASE}	PHASE to SGND	-0.3 to 38	
	LGATE to PGND	-0.3 to V_{VCC} +0.3	
	CSNS, PG, S3, S5, DSCG, COMP, VSNS, VOSC, VREF, MODE, DDRSEL to GND	-0.3 to V_{AVCC} + 0.3	
	VTTREF, VREF, VTT, VTTSNS to SGND	-0.3 to V_{AVCC} + 0.3	
	LDOIN, VTT, VTTREF, LDOIN to VTTGND	-0.3 to V_{AVCC} + 0.3	
P_{TOT}	Power dissipation @T_A = 25°C	2.3	W

1. Free air operating conditions unless otherwise specified. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient	42	°C/W
T_{STG}	Storage temperature range	-40 to 150	°C
T_A	Operating ambient temperature range	-40 to 85	°C
T_J	Junction operating temperature range	-25 to 125	°C

3.3 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Input voltage range	4.5		36	V
V_{AVCC}	IC supply voltage	4.5		5.5	
V_{VCC}	IC supply voltage	4.5		5.5	

4 Electrical characteristics

T_A = 0°C to 85°C , VCC = AVCC = +5V and LDOIN connected to VDDQ output if not otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
Supply section							
I_{IN}	Operating current	S3, S5, MODE and DDRSEL connected to AVCC, No Load on VTT and VTTREF Outputs. VCC connected to AVCC			0.8	2	mA
I_{STR}	Operating current in STR	S5, MODE and DDRSEL connected to AVCC, S3 tied to SGND, No Load on VTTREF. VCC connected to AVCC			0.6	1	
I_{SH}	Operating current in shutdown	S3 and S5 tied to SGND. Discharge Mode active. VCC connected to AVCC			1	10	µA
UVLO	AVCC under voltage lockout upper threshold			4.0	4.1	4.2	V
	AVCC under voltage lockout lower threshold			3.8	3.9	4.0	
	UVLO hysteresis			50			mV
ON-time (SMPS)							
t_{ON}	On-time duration	MODE and DDRSEL high, V_{VSNS} = 2V	VOSC = 300mV	650	750	850	ns
			VOSC = 500mV	390	450	510	
OFF-time (SMPS)							
t_{OFFMIN}	Minimum Off Time				300	350	ns
Voltage reference							
	Voltage accuracy	4.5V < V_{IN} < 25V		1.224	1.237	1.249	V
	Load regulation	-50µA< I_{VREF} < 50µA		-4		4	mV
	Undervoltage lockout fault threshold				800		
VDDQ output							
V_{VDDQ}	DDR3 VDDQ output voltage	MODE connected to AVCC, DDRSEL tied to SGND, No Load			1.5		V
	DDR2 VDDQ output voltage	MODE and DDRSEL connected to AVCC, No Load			1.8		
	VDDQ output accuracy	MODE connected to AVCC, No Load		-2		2	%

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Current limit and zero crossing comparator						
I_{CSNS}	CSNS input bias current		90	100	110	µA
	Comparator offset		-5		5	mV
	Positive current limit threshold	Rsense = 1kΩ V_{PGND} - V_{CSNS}		-100		mV
	Fixed negative current limit threshold			110		mV
$V_{ZC,OFFS}$	Zero crossing comparator offset		-10	-5	0	mV
High and low side gate drivers						
	HGATE driver on-resistance	HGATE high state (pull-up)		2.0	3	Ω
		HGATE low state (pull-down)		1.8	2.7	
	LGATE driver on-resistance	LGATE high state (pull-up)		1.4	2.1	
		LGATE low state (pull-down)		0.6	0.9	
UVP/OVP protections and PGOOD SIGNAL (SMPS only)						
OVP	Over voltage threshold		112	115	118	%
UVP	Under voltage threshold		67	70	73	
PGOOD	Power-good upper threshold		107	110	113	
	Power-good lower threshold		87	90	93	
$I_{PG,LEAK}$	PG leakeage current	PG forced to 5V			1	µA
$V_{PG,LOW}$	PG low-level voltage	$I_{PG,SINK}$ = 4mA		150	250	mV
Soft start section (SMPS)						
	Soft-start ramp time (4 steps current limit)		2	3	4	ms
	Soft-start current limit step			25		µA
Soft end section						
	VDDQ Discharge resistance in non-tracking discharge mode		15	25	35	Ω
	VTT discharge resistance in non-tracking discharge mode		15	25	35	
	VTTREF discharge resistance in non-tracking discharge mode		1k	1.5k	2k	
	VDDQ Output threshold synchronous for final tracking to non-tracking discharge transition		0.2	0.4	0.6	V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{TT} LDO section						
$I_{LDOIN,ON}$	LDO input bias current in full-on state	S3 = S5 = +5V, No Load on VTT		1	10	µA
$I_{LDOIN, STR}$	LDO input bias current in suspend-to-RAM state	S3 = 0V, S5 = +5V, No Load on VTT			10	
$I_{LDOIN, STD}$	LDO input bias current in suspend-to-disk state	S3 = S5 = 0V, No Load on VTT			1	
$I_{VTTSNS, BIAS}$	VTTSNS bias current	S3 = +5V, S5 = +5V, $V_{VTTSNS} = V_{VSNS}/2$			1	µA
$I_{VTTSNS, LEAK}$	VTTSNS leakage current	S3 = 0V, S5 = +5V, $V_{VTTSNS} = V_{VSNS}/2$			1	
$I_{VTT,LEAK}$	VTT leakage current	S3 = 0V, S5 = +5V, $V_{VTT} = V_{VSNS}/2$	-10		10	
V_{VTT}	LDO linear regulator output voltage (DDR2)	S3 = S5= +5V, I_{VTT} = 0A, MODE = DDRSEL = +5V		0.9		V
	LDO linear regulator output voltage (DDR3)	S3 = S5= +5V, I_{VTT} = 0A, MODE = +5V, DDRSEL = 0V		0.75		
	LDO output accuracy respect to VTTREF	S3 = S5 = MODE = + 5V, -1mA < I_{VTT} < 1mA	-20		20	mV
		S3 = S5 = MODE = +5V, -1A < I_{VTT} < 1A	-25		25	
		S3 = S5 = MODE = +5V, -2A < I_{VTT} < 2A	-35		35	
$I_{VTT,CL}$	LDO source current limit	V_{VTT} < 1.10*(V_{VSNS} /2)	2	2.3	2.6	A
		V_{VTT} > 1.10*(V_{VSNS} /2)	1	1.15	1.3	
	LDO sink current limit	V_{VTT} > 0.90*(V_{VSNS} /2)	-2.6	-2.3	-2	
		V_{VTT} < 0.90*(V_{VSNS} /2)	-1.3	-1.15	-1	
VTTREF section						
V_{VTTREF}	VTTREF output voltage	I_{VTTREF} = 0A, V_{VSNS} = 1.8V		0.9		V
	VTTREF output voltage accuracy respect to VSNS/2	-15mA < I_{VTTREF} < 15mA, V_{VSNS} = 1.8V	-2		2	%
I_{VTTREF}	VTTREF current limit	VTTREF= 0 or VSNS	-40		+40	mA

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Power management section						
S3,S5	Turn OFF level		0.4			V
	Turn ON level				1.6	
V_{MODE}	MODE pin high level threshold (1)		V_{AVCC} -0.7			
	MODE pin low level threshold (1)				V_{AVCC} - 1.3	
V_{DDRSEL}	DDRSEL pin high level threshold (1)		V_{AVCC} -0.8			
	DDRSEL pin middle level window (1)		1.0		V_{AVCC} - 1.5	
	DDRSEL pin low level threshold (1)				0.5	
V_{DSCG}	DSCG pin high level threshold (1)		V_{AVCC} -0.8			
	DSCG pin middle level window (1)		1.0		V_{AVCC} - 1.5	
	DSCG pin low level threshold (1)				0.5	
$I_{IN,LEAK}$	Logic inputs leakage current	S3, S5 = 5V			10	µA
$I_{IN3,LEAK}$	Multilevel inputs leakage current	MODE, DDRSEL and DSCG = 5V			10	µA
$I_{OSC,LEAK}$	VOSC input leakage current	VOSC = 500mV			1	µA
Thermal shutdown						
T_{SHDN}	Shutdown temperature (1)			150		°C

1. Guaranteed by design. Not production tested.

5 Block diagram

Figure 3. Functional and block diagram

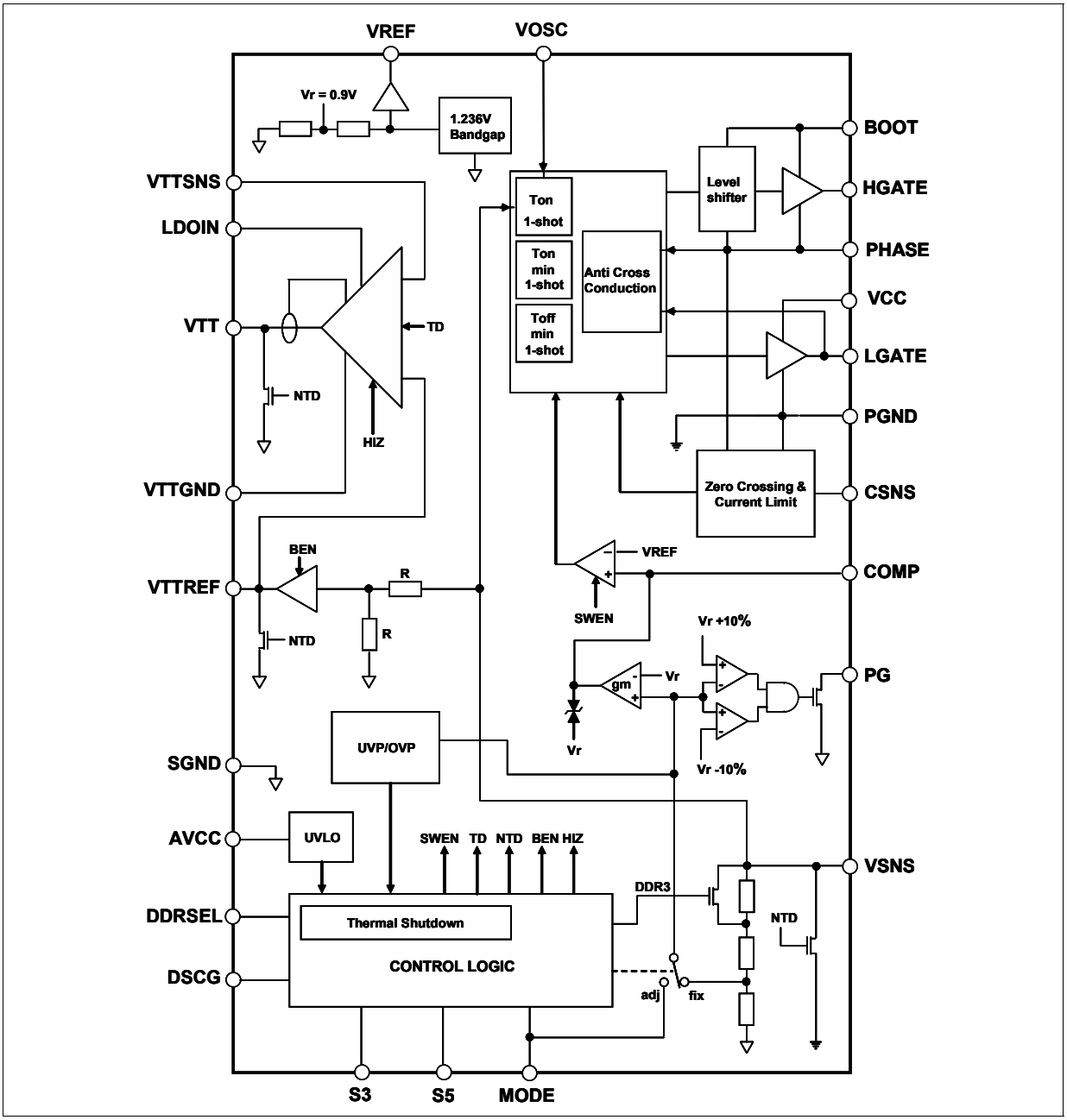


Table 6. Legend

SWEN	Switching controller enable
TD	Tracking discharge enable
NTD	Non-tracking discharge enable
BEN	VTTREF buffer enable
HIZ	LDO high impedance mode enable

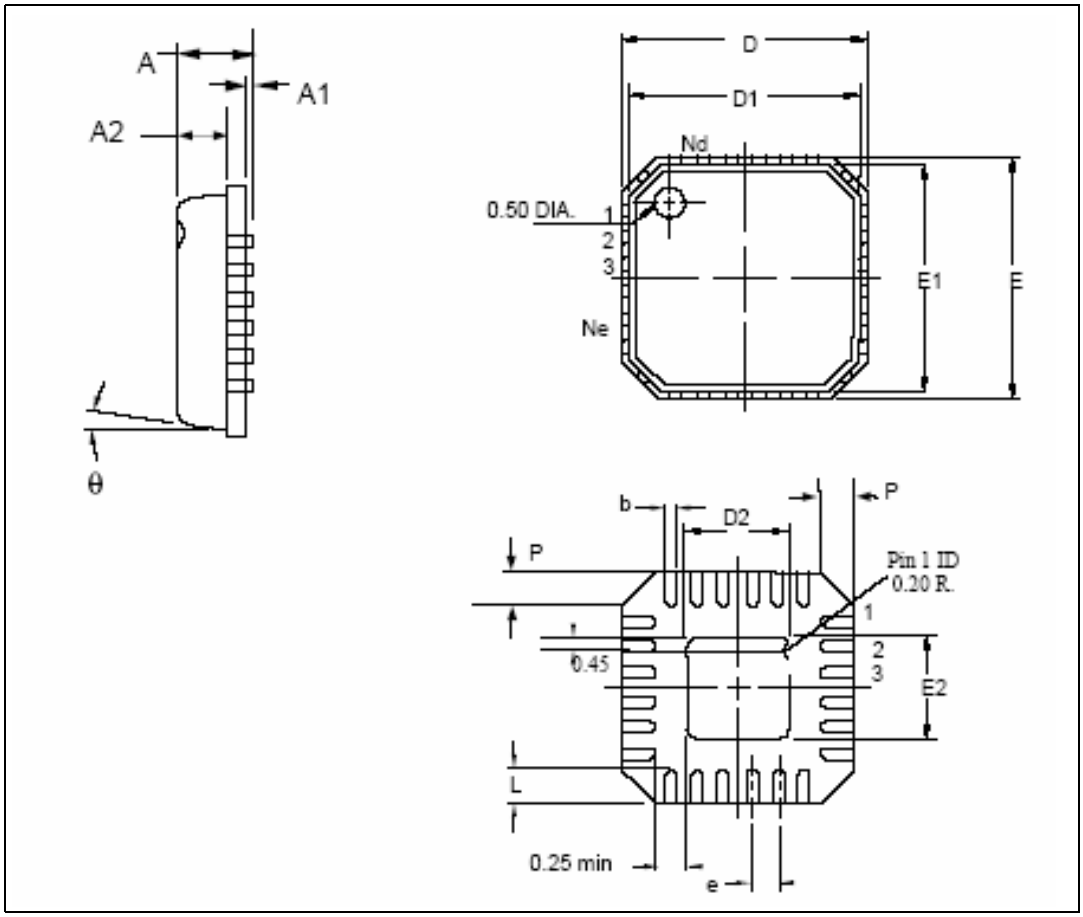
6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 7. VFQFPN-24 4mm x 4mm mechanical data

Dim.	mm.		
	Typ	Min.	Max.
A		0.80	1.00
A1	0.00	0.05	0.05
A2	0.65		0.80
D	4.00		
D1	3.75		
E	4.00		
E1	3.75		
θ			12°
P	0.42	0.24	0.60
e	0.50		
N	24.00		
Nd	6.00		
Ne	6.00		
L	0.40	0.30	0.50
b		0.18	0.30
D2	2.10	1.95	2.25
E2	2.10	1.95	2.25

Figure 4. Package dimensions



7 Revision history

Table 8. Revision history

Date	Revision	Changes
11-Oct-2006	1	Initial release.

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