PM6680A

Dual syncronous step-down controller with adjustable output voltages plus LDO

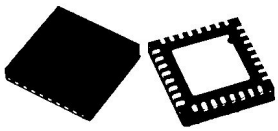
Preliminary Data

Features

- 6V to 36V input voltage range
- Adjustable output voltages
- 5V LDO delivers 100mA peak current
- 1.237V ±1% reference voltage available externally
- Current sensing using low side MOSFETs $R_{DS(on)}$
- Accurate current sense with R_{SENSE}
- Valley current sensing
- Soft-start internally fixed at 2ms
- Soft output discharge
- Latched OVP and UVP
- Selectable pulse skipping at light loads
- Selectable minimum frequency (33kHz) in pulse skip mode
- 5mW maximum quiescent power
- Independent power good signals
- Output voltage ripple compensation
- Thermal shutdown

Applications

- Embedded computer system
- FPGA system power
- Industrial applications on 24V
- High performance and high density DC/DC modules



VFQFPN-32 5X5

Description

PM6680A is a dual step-down controller specifically designed to provide extremely high efficiency conversion, with losses current sensing technique. The constant on-time architecture assures fast load transient response and the embedded voltage feed-forward provides nearly constant switching frequency operation. An embedded integrator control loop compensates the DC voltage error due to the output ripple. Pulse skipping technique increases efficiency at very light load. Moreover a minimum switching frequency of 33kHz is selectable to avoid audio noise issues. The PM6680A provides a selectable switching frequency, allowing either 200kHz/300kHz, 300kHz/400Khz or 400kHz/500kHz operation of the two switching sections. The output voltages OUT1 and OUT2 can be adjusted from 0.9V to 5V and from 0.9V to 3.3V respectively.

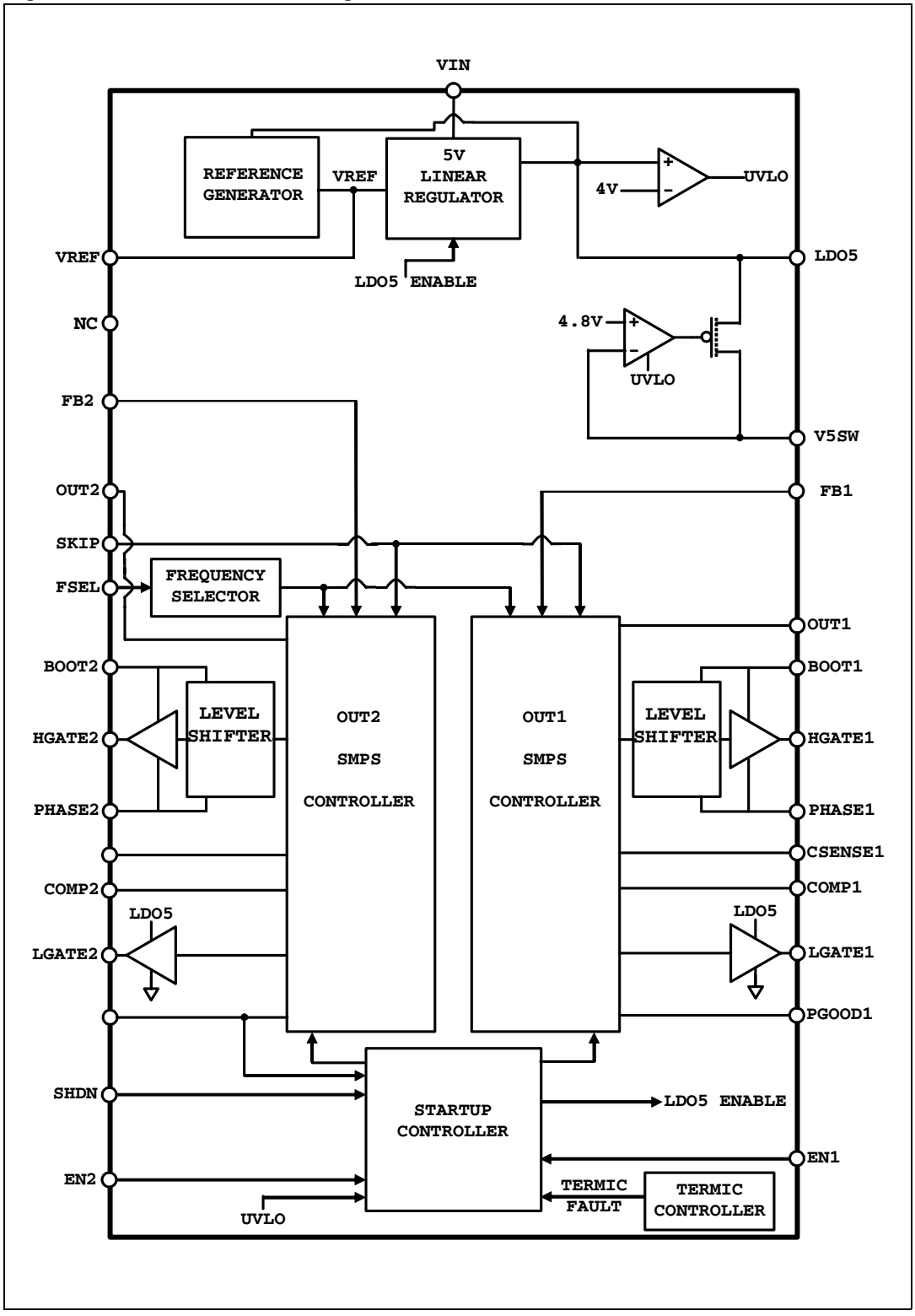
Order codes

Part number	Package	Packaging
PM6680A	VFQFPN-32 5X5 (Exposed Pad)	Tube

Contents

1 Block diagram

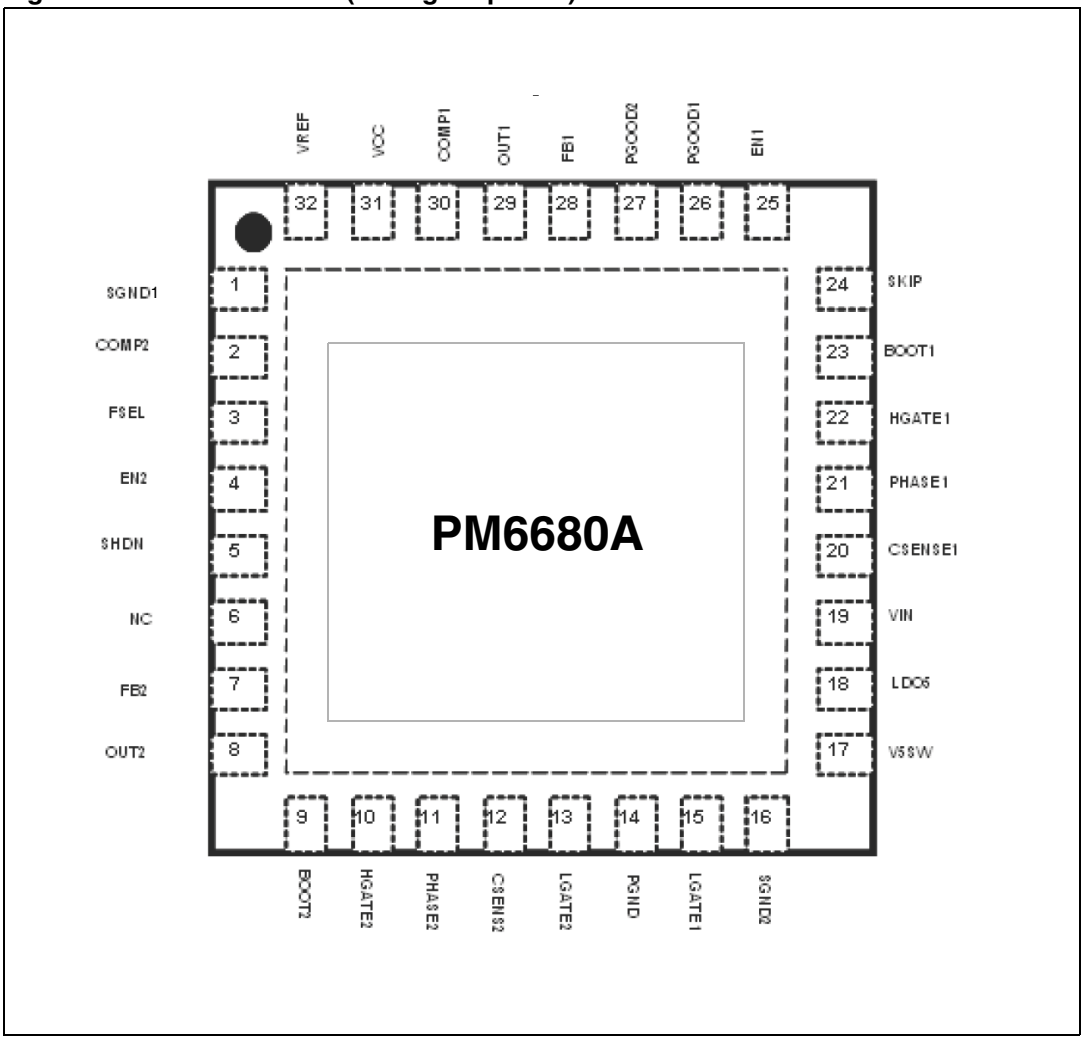
Figure 1. Functional block diagram



2 Pin settings

2.1 Connections

Figure 2. Pin connection (through top view)



2.2 Functions

Table 1. Pin functions

N°	Pin	Function
1	SGND1	Signal ground. Reference for internal logic circuitry.
2	COMP2	Static error compensation pin for the switching section 2
3	FSEL	Frequency selection pin. It provides a selectable switching frequency, allowing either 200kHz/300kHz, 300kHz/400kHz or 400kHz/500kz operation of the switching sections.
4	EN2	Enable input for the switching section 2. When a high logic level (>2.4V) is present on this pin, it enables this section, while with a low logic level (<0.8V) the device disables the switching section where HS gate driver goes low while LS gate driver goes high. Note that if both enable pins are low and SHDN is high the device enters in standby mode.
5	SHDN	Shutdown control input. The device enters in its shutdown mode with 9µA of supply current if VSHDN is less than the device off threshold and doesn't restart until VHSDN is greater then the device on threshold. Note that in shutdown mode both gate drivers of the two switching sections are in high impedance.
6	NC	Not connected.
7	FB2	Feedback input for the switching section 2 This pin is connected to a resistive voltage-divider from OUT2 to PGND to adjust the output voltage from 0.9V to 3.3V.
8	OUT2	Output voltage sense for the switching section 2.This pin must be directly connected to the output voltage of the switching section.
9	BOOT2	Bootstrap capacitor connection for the switching section 2. It supplies the high-side gate driver.
10	HGATE2	High-side gate driver output for section 2. This is the floating gate driver output.
11	PHASE2	Switch node connection and return path for the high side driver for the section 2.It is also used as negative current sense input.
12	CSENSE2	Positive current sense input for the switching section 2. This pin must be connected through a resistor to the drain of the synchronous rectifier (R_{DSON} sensing) or to the source of the synchronous rectifier (R_{SENSE} sensing) to obtain a positive current limit threshold for the power supply controller.
13	LGATE2	Low-side gate driver output for the section 2.
14	PGND	Power ground reference.
15	LGATE1	Low-side gate driver output for the section 1.
16	SGND2	Signal ground. Reference for internal logic circuitry.
17	V5SW	Internal 5V regulator bypass connection. When the main output voltage is greater than the boostrap-switchover threshold, an internal 3Ω (max) P-channel MOSFET switch connects V5SW pin to LDO5 pin shutting down the LDO5 internal linear regulator.If not used, it must be tied to ground.

Table 1. Pin functions

N°	Pin	Function
18	LDO5	5V internal regulator output. LDO5 pin supplies all gate drivers and the internal circuitry. It can provide a 100mA peak current, including MOSFET gate driver and external load requirements.
19	VIN	Device supply voltage input and battery voltage sense.
20	CSENSE1	Positive current sense input for the switching section 1. This pin must be connected through a resistor to the drain of the synchronous rectifier ($R_{DS(on)}$ sensing) or to the source of the synchronous rectifier (R_{SENSE} sensing) to obtain a positive current limit threshold for the power supply controller.
21	PHASE1	Switch node connection and return path for the high side driver for the section 1.It is also used as negative current sense input.
22	HGATE1	High-side gate driver output for section 1. This is the floating gate driver output.
23	BOOT1	Bootstrap capacitor connection for the switching section 1. It supplies the high-side gate driver.
24	SKIP	Pulse skipping mode control input. A high logic level (>2.4V)on this pin disables pulse skipping mode at light load current while a low level (<0.8V) enables it.
25	EN1	Enable input for the switching section 1. When a high logic level (>2.4V) is present on this pin, it enables this section, while with a low logic level (<0.8V) the device disables the switching section where HS gate driver goes low while LS gate driver goes high. Note that if both enable pins are low and SHDN is high the device enters in standby mode.
26	PGOOD1	Power Good output signal for the section 1. This pin is an open drain output and when the output of the switching section 1 is out of +/- 10% of its nominal value.It is pulled down.
27	PGOOD2	Power Good output signal for the section 2. This pin is an open drain output and when the output of the switching section 2 is out of +/- 10% of its nominal value.It is pulled down.
28	FB1	Feedback input for the switching section 1. This pin is connected to a resistive voltage-divider from OUT1 to PGND to adjust the output voltage from 0.9V to 5.5V.
29	OUT1	Output voltage sense for the switching section 1.This pin must be directly connected to the output voltage of the switching section.
30	COMP1	Static error compensation pin for the switching section 1.
31	VCC	IC Supply Voltage pin. This Pin must be always connected to LDO5
32	VREF	Internal 1.237V high accuracy voltage reference. It can deliver 50uA. Bypass to SGND with a 100nF capacitor to reduce noise.

3 Electrical data

3.1 Maximum rating

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{V5SW}	V5SW to PGND	-0.3 to 6	V
VIN	VIN to PGND	-0.3 to 38	V
Vcc	Vcc to PGND	-0.3 to 6	V
V_{OUT}	OUTx to PGND	-0.3 to 6	V
	HGATE and BOOT, to PHASE	-0.3 to 6	V
	HGATE and BOOT, to PGND	-0.3 to 44	V
	CSENSEx and PHASE	-0.3 to 38	V
	LGATEx to PGND	-0.3 to V_{CC} +0.3	V
	FB, COMP, SKIP, PGOOD, FSEL, LDO5, EN, VREF	-0.3 to V_{CC} +0.3	V
	SHDN	-0.3 to 6	V
	Power dissipation at T_A = 25ºC	TBD	W

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient	35	°C/W
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction operating temperature range	-25 to 125	°C

4 Electrical characteristics

T_A = -25°C to 85°C, unless otherwise specified

At negative Temperature parameters are guaranteed by design and statistical analysis.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Supply section						
VIN	Input voltage range	Vout = Vref, LDO5 in regulation	6		36	V
V_{CC}	IC Supply voltage		4.5		5.5	V
V_{V5SW}	Turn-ON voltage threshold			4.8	4.9	V
	Turn-OFF voltage threshold		4.6	4.75		V
	Hysteresis		20	50		mV
V_{V5SW}	Maximum operating range				5.5	V
$R_{DS(on)}$	LDO5 Internal bootstrap switch resistance	V5SW > 4.9		1.8	3	Ω
	OUTx,OUTx discharge-Mode On-resistance			17	25	Ω
	OUTx, OUTx discharge-Mode Synchronous rectifier Turn-on level		0.2	0.35	0.6	V
Pin	Operating power consumption	FBx > V_{REF}, Vref in regulation, V5WS to 5V			5	mW
Ish	Operating current sunk by V_{IN}	SHDN connected to GND,		20	25	µA
Isb	Operating current sunk by V_{IN}	ENx to GND, V5SW to GND		180	380	µA
Shutdown section						
V_{SHDN}	Device ON Threshold		1.2	1.5	1.7	V
	Device OFF Threshold		0.8	0.85	0.9	V
Soft start section						
	Soft start ramp time		2		6	ms
Current limit and zero crossing comparator						
I_{CSENSE}	Input bias current limit		90	100	110	µA
	Comparator offset	V_{CSENSE} - V_{PGND}	-6		6	mV
	Zero crossing comparator offset	V_{PGND} - V_{PHASE}	-1		11	mV
	Fixed negative current limit threshold	V_{PGND} - V_{PHASE}		-120		mV

Table 5. Electrical characteristics (T_A = -25°C to 85°C, unless otherwise specified
At negative Temperature parameters are guaranteed by design and statistical analysis.)

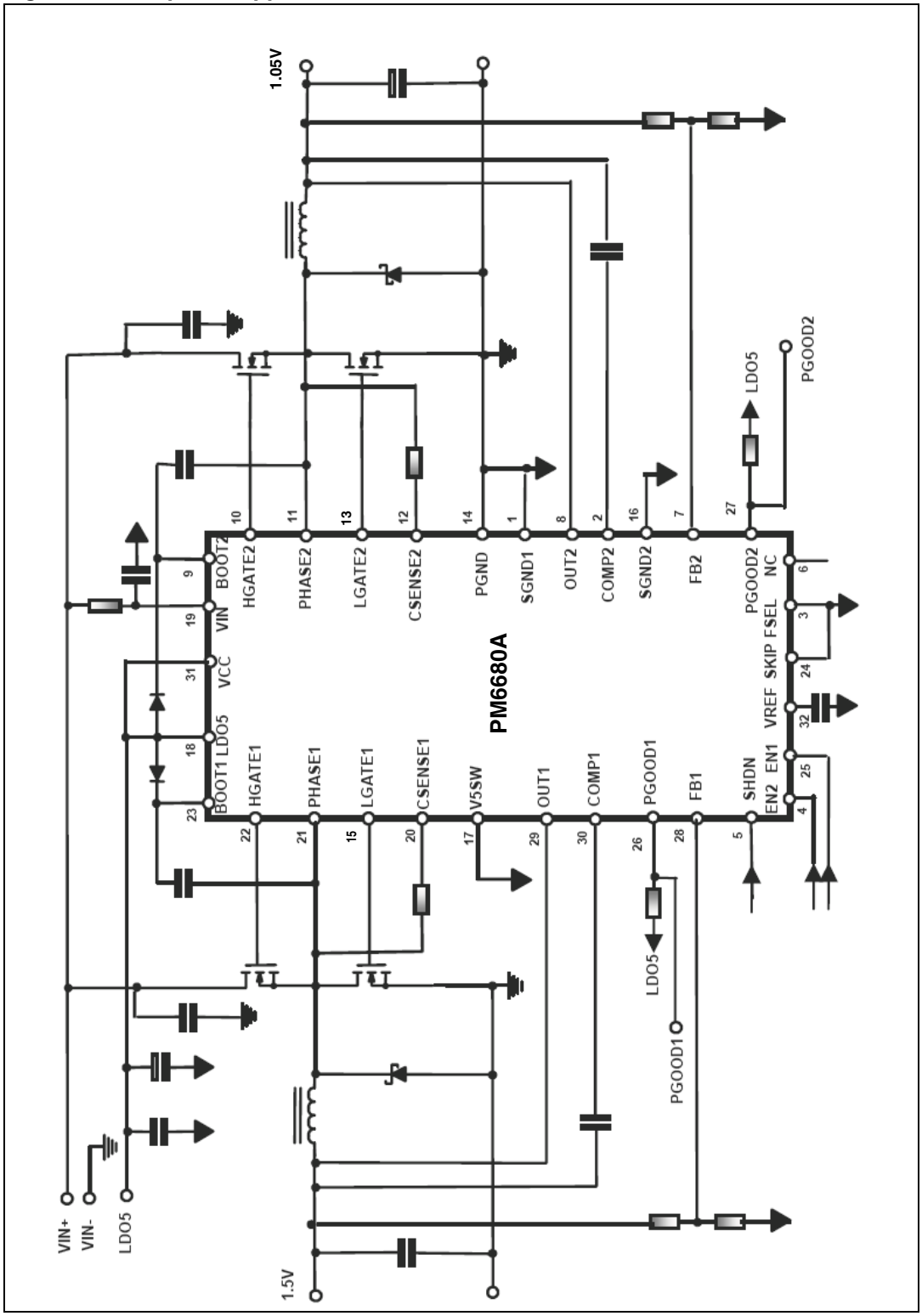
Symbol	Parameter	Test condition		Min	Typ	Max	Unit
Frequency switch							
F_{SW}	FSEL tied to GND	SMPS V_{OUT1} =1.5V			200		kHz
		SMPS V_{OUT2} = 1.05V			300		
	FSEL tied to VREF	SMPS V_{OUT1} = 1.5V			300		
		SMPS V_{OUT2} = 1.05V			400		
	FSEL tied to LDO5	SMPS V_{OUT1} = 1.5V			400		
		SMPS V_{OUT2} = 1.05V			500		
On time pulse width							
T_{ON}	On time duration V_{IN} = 12V	FSEL to GND	OUT1 = 1.5V		602		ns
			OUT2 = 1.05V		302		
		FSEL to VREF	OUT1 = 1.5V		285		
			OUT2 = 1.05V		266		
		FSEL to LDO5	OUT1 = 1.5V		303		
			OUT2 = 1.05V		276		
	On time duration V_{IN} = 24V	FSEL to GND	OUT1 = 1.5V		301		ns
			OUT2 = 1.05V		151		
		FSEL to VREF	OUT1 = 1.5V		142		
			OUT2 = 1.05V		133		
		FSEL to LDO5	OUT1 = 1.5V		151		
			OUT2 = 1.05V		138		
OFF time							
T_{OFFMIN}	Minimum off time				400	500	ns
Voltage reference							
V_{REF}	Voltage accuracy	4V<V_{LDO5}< 5.5V		1.224	1.237	1.249	V
	Load regulation	-100µA< I_{REF} < 100µA		-4		4	mV
	Undervoltage lockout fault threshold	Falling edge of REF				0.93	mV
PWM comparator							
I_{FB}	Input voltage offset			-9		9	mV
I_{FB}	Input bias current				0.1		µA
Integrator							
COMP	Over voltage clamp				250		mV
COMP	Under voltage clamp				-150		
Line regulation							
		Both SMPS, 6V < Vin < 36V				1	%

Table 5. Electrical characteristics (continued)(T_A = -25°C to 85°C, unless otherwise specified At negative Temperature parameters are guaranteed by design and statistical analysis.)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
LDO5 Linear regulation						
V_{LDO5}	LDO5 linear Output Voltage	6V < VIN < 36V, 0<I_{LDO5}<50mA	4.9	5.0	5.1	V
	LDO5 line regulation	6V < VIN < 36V, I_{LDO5} =20mA ,			0.004	%/V
I_{LDO5}	LDO5 Current limit	V_{LDO5} > UVLO	270	350	400	mA
ULVO	Under Voltage Lockout of LDO5		3.94	4	4.13	V
High and low gate drivers						
	HGATE driver on-resistence	HGATEx high state(pullup)		2.0	3	Ω
		HGATEx low state (pulldown)		1.8	2.7	Ω
	LGATE driver on-resistance	LGATEx high state(pullup)		1.4	2.1	Ω
		LGATEx low state (pulldown)		0.6	0.9	Ω
PGOOD pins UVP/OVP Protections						
OVP	Over voltage threshold	Both SMPS sections with respect to VREF.	113	116	120	%
UVP	Under voltage threshold		66	70	72	%
PGOOD1,2	Upper threshold (VFB-VREF)		107	110	113	%
	Lower threshold (VFB-VREF)		88	91	94	%
$I_{PGOOD1,2}$	PGOOD leakage current	$V_{PGOOD1,2}$ forced to 5.5V			1	uA
$V_{PGOOD1,2}$	Output Low Voltage	ISink=4mA		150	250	mV
Power management pins						
EN1,2	SMPS disabled level				0.8	V
	SMPS enabled level		2.4			
FSEL	Frequency selection range	Low level			0.5	V
		Middle level	1.0		V_{LDO5}-1.5	
		High level	V_{LDO5}-0.8			
SKIP	Pulse Skip Mode				0.5	V
	PWM Mode		1.0		V_{LDO5}-1.5	
	Ultrasonic Mode		V_{LDO5}-0.8			
	Input leakage current	$V_{EN1,2}$ = 0 to 5V			1	µA
		V_{SKIP} = 0 to 5V			1	
		V_{SHDN} = 0 to 5V			1	
		V_{FSEL} = 0 to 5V			1	

5 Application schematic

Figure 3. Simplified application schematic



6 Device description

The PM6680A is a dual step-down controller dedicated to provide logic voltages for industrial automation applications.

It is based on a Constant On Time control architecture. This type of control offers a very fast load transient response with a minimum external component count. A typical application circuit is shown in *Figure 3*.

The PM6680A regulates two adjustable output voltages: OUT1 and OUT2. The switching frequency of the two sections can be adjusted to 200/300kHz, 300/400kHz or 400/500kHz respectively. In order to maximize the efficiency at light load condition, a pulse skipping mode can be selected.

The PM6680A includes also a 5V linear regulator (LDO5) that can power the switching drivers. If the output OUT1 regulates 5V, in order to maximize the efficiency in higher consumption status, the linear regulator can be turned off and their outputs can be supplied directly from the switching outputs. The PM6680A provides protection versus overvoltage, undervoltage and over temperature as well as power good signals for monitoring purposes. An external 1.237V reference is available.

6.1 Constant On time PWM control

If the SKIP pin is tied to 5V, the device works in PWM mode. Each power section has an independent on time control.The PM6680A employees a pseudo-fixed switching frequency, Constant On Time (COT) controller as core of the switched mode section. Each power section has an independent COT control.

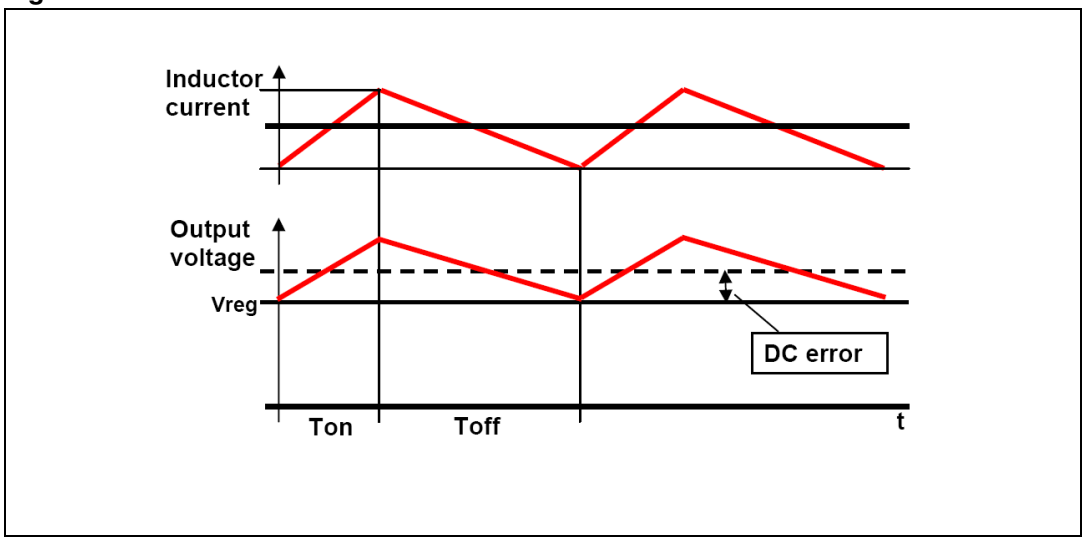
The COT controller is based on a relatively simple algorithm and uses the ripple voltage due to the output capacitor's ESR to trigger the fixed on-time one-shot generator. In this way, the output capacitor's ESR acts as a current sense resistor providing the appropriate ramp signal to the PWM comparator. On-time one-shot duration is directly proportional to the output voltage, sensed at the OUT1/OUT2 pins, and inversely proportional to the input voltage, sensed at the VIN pin, as follows:

Equation 1

$$T_{ON} = K \cdot \frac{V_{OUT}}{V_{IN}}$$

This leads to a nearly constant switching frequency, regardless of input and output voltages. When the output voltage goes lower than the regulated voltage Vreg, the on-time one shot generator directly drives the high side MOSFET for a fixed on time allowing the inductor current to increase; after the on time, an off time phase, in which the low side MOSFET is turned on, follows. *Figure 4* shows the inductor current and the output voltage waveforms in PWM mode.

Figure 4. Constant ON Time PWM Control



The duty cycle of the buck converter in steady state is:

Equation 2

$$D = \frac{V_{OUT}}{V_{IN}}$$

The PWM control works at a nearly fixed frequency f_{SW}:

Equation 3

$$f_{SW} = \frac{\frac{V_{OUT}}{V_{IN}}}{K_{on} \times \frac{V_{OUT}}{V_{IN}}} = 1 / K_{on}$$

As mentioned the steady state switching frequency is theoretically independent from input voltage and from output voltage.

Actually the frequency depends on parasitic voltage drops that are present during the charging path(high side switch resistance, inductor resistance(DCR)) and discharging path(low side switch resistance, DCR).

As a result the switching frequency increases as a function of the load current.

Standard switching frequency values can be selected for both sections by pin FSEL as shown in the following table:

Table 6. FSEL pin selection

FSEL	SMPS OUT1		SMPS OUT2	
	Frequency	K_{ON}	Frequency	K_{ON}
SGND	200KHz	5us	300kHz	3.3us
VREF	300kHz	3.3us	400kHz	2.5us
LDO5	400kHz	2.5us	500kHz	2.0us

6.2 Constant On time architecture

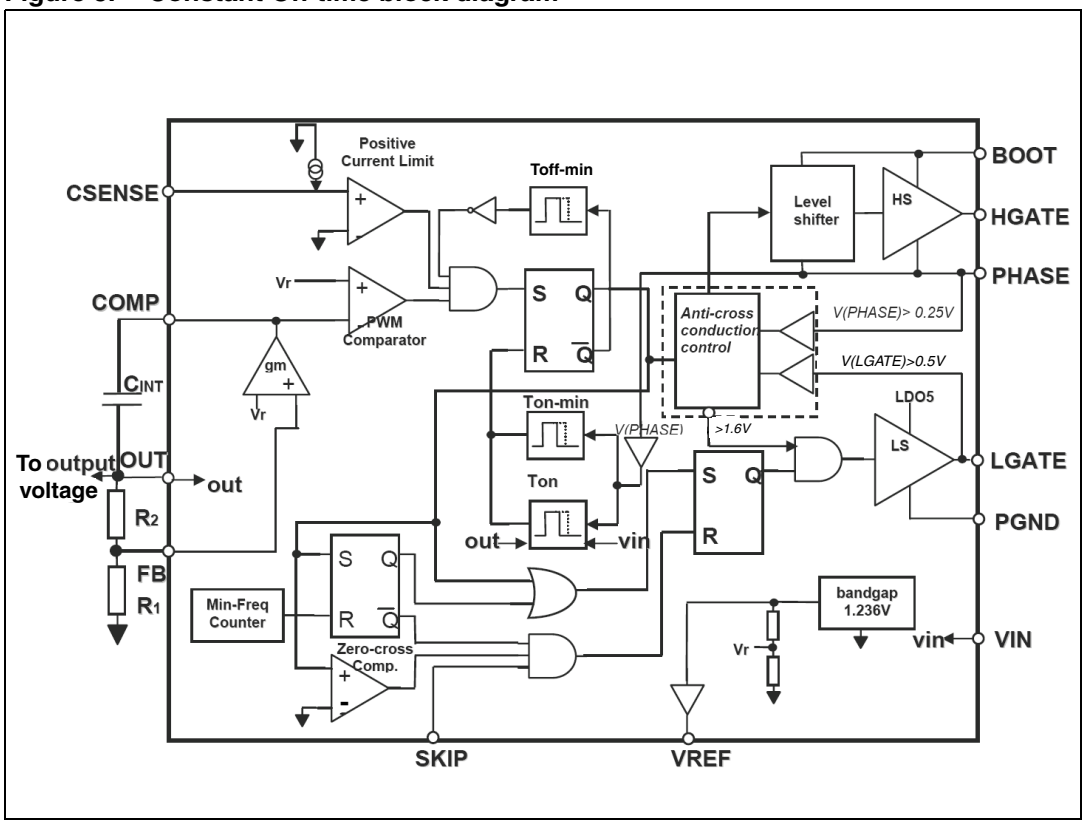
Figure 5 shows the simplified block diagram of a Constant On Time controller. A minimum off-time constrain (300ns typ.) is introduced to allow inductor valley current sensing on synchronous switch. A minimum on-time (70ns) is also introduced to assure the start-up switching sequence.

PM6680A has a one-shot generator for each power section that turns on the high side MOSFET when the following conditions are satisfied simultaneously: the PWM comparator is high, the synchronous rectifier current is below the current limit threshold, and the minimum off-time has timed out.

Once the on-time has timed out, the high side switch is turned off, while the synchronous switch is turned on according to the anti-cross conduction circuitry management.

When the negative input voltage at the PWM comparator (*Figure 5*), which is a scaled-down replica of the output voltage (see the external R1/R2 divider in *Figure 5*), reaches the valley limit (determined by internal reference Vr = 0.9V), the low-side MOSFET is turned off according to the anti-cross conduction logic once again, and a new cycle begins.

Figure 5. Constant On-time block diagram



In steady state the FB pin voltage is about Vr and the regulated output voltage depends on the external divider:

Equation 4

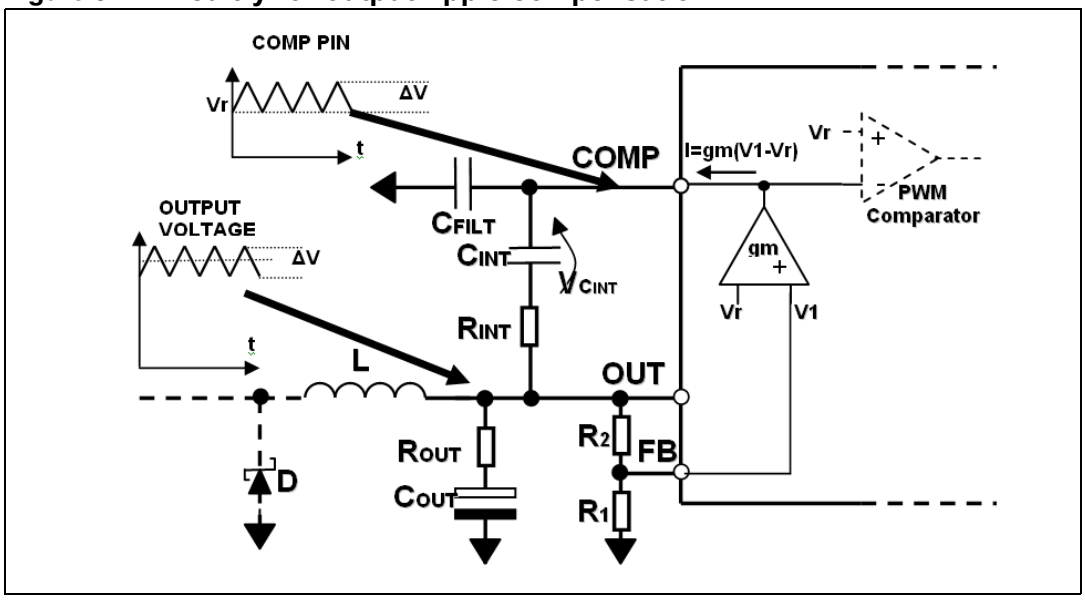
$$OUT = Vr \times \left(1 + \frac{R_2}{R_1}\right)$$

6.3 Output ripple compensation and loop stability

In a classic Constant On Time control, the system regulates the valley value of the output voltage and not the average value, as shown in *Figure 4* In this condition, the output voltage ripple is source of a DC static error.

To compensate this error, an integrator network can be introduced in the control loop, by connecting the output voltage to the COMP1/COMP2 (for the OUT1 and OUT2 sections respectively) pin through a capacitor C_{INT} as in *Figure 6*.

Figure 6. Circuitry for output ripple compensation



The integrator amplifier generates a current, proportional to the DC errors between the FB voltage and Vr, which decreases the output voltage in order to compensate the total static error, including the voltage drop on PCB traces. In addition, CINT provides an AC path for the output ripple. In steady state, the voltage on COMP1/COMP2 pin is the sum of the reference voltage Vr and the output ripple (see *Figure 6*). In fact when the voltage on the COMP pin reaches Vr, a fixed Ton begins and the output increases.

For example, we consider Vout = 5V with an output ripple of ΔV = 50mV. Considering $C_{INT} >> C_{FILT}$, the C_{INT} DC voltage drop VC_{INT} is about 5V -Vr + 25mV = 4.125V. C_{INT} assures an AC path for the output voltage ripple. Then the COMP pin ripple is a replica of the output ripple, with a DC value of Vr + 25mV = 925mV.

The design of external feedback network depends on the output voltage ripple. If the ripple is higher than approximately 30mV, the feedback network is usually enough to keep the loop stable.

The stability of the system depends firstly on the output capacitor zero frequency f_{ZOUT}. The following condition should be satisfied:

Equation 5

$$f_{SW} > K \times f_{ZOUT} = \frac{K}{2\pi \times C_{OUT} \times R_{OUT}}$$

where k is a design parameter greater than 3 and R_{out} is the ESR of the output capacitor. It determinates the minimum integrator capacitor value C_{INT}:

Equation 6

$$C_{INT} > \frac{g_M}{2\pi \times \left(\frac{f_{SW}}{K} - f_{ZOUT}\right)} \times \frac{v_r}{V_{OUT}}$$

where gm = 50µs is the integrator transconductance.

In order to reduce noise on COMP pin, it's possible to add a resistor R_{INT} and a capacitor C_{filt} that, together with C_{INT}, realize a low pass filter (see *Figure 6*). The cutoff frequency f_{CUT} must be much greater (10 or more times) than the switching frequency of the section:

Equation 7

$$R_{INT} = \frac{1}{2\pi \times f_{CUT} \times \frac{C_{INT} \times C_{filt}}{C_{INT} + C_{filt}}}$$

Due to the capacitive divider (C_{INT}, C_{filt}), the ripple voltage at the COMP pin is given by:

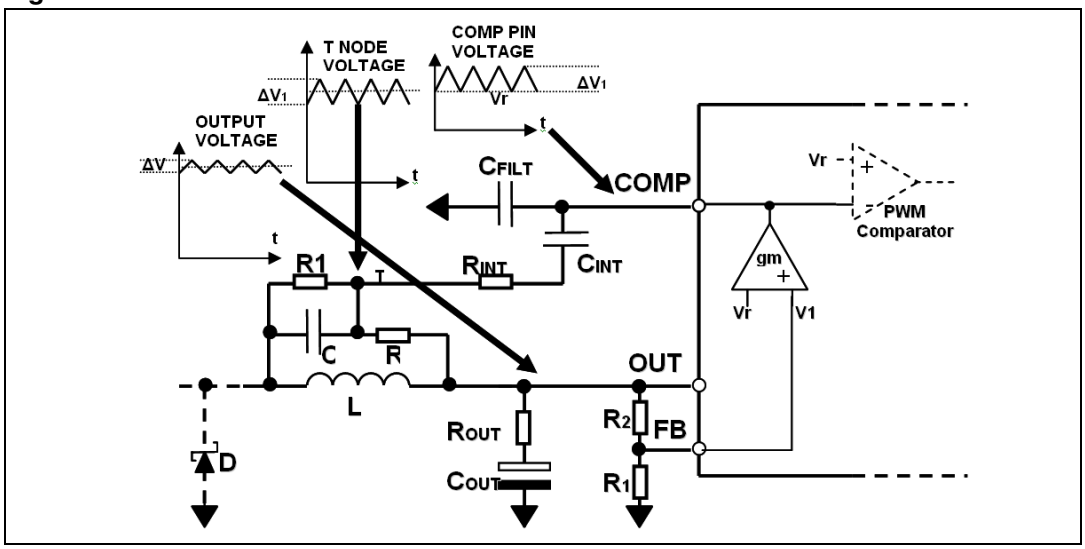
Equation 8

$$V_{RIPPLE_{INT}} = V_{RIPPLE_{OUT}} \times \frac{C_{INT}}{C_{INT} + C_{filt}} = V_{RIPPLE_{OUT}} \times q$$

Where $V_{RIPPLE_{OUT}}$ is the output ripple and q is the attenuation factor of the output ripple.

If the ripple is very small (lower than approximately 30mV), a further compensation network, named virtual ESR network, is needed. This additional part generates a triangular ripple that is added to the ESR output voltage ripple at the input of the integrator network. The complete control schematic is represented in *Figure 7.*

Figure 7. Virtual ESR network



The integrator input voltage (T node) is the sum of the output voltage and the triangular waveform generated by the virtual ESR network. In fact the virtual ESR network behaves like a further equivalent ESR RESR.

A good trade-off is to design the network in order to achieve an RESR given by:

Equation 9

$$R_{ESR} = \frac{V_{RIPPLE}}{\Delta I_L} - R_{OUT}$$

where ΔI_L is the inductor current ripple and V_{RIPPLE} is the overall ripple of the T node voltage. It should be chosen higher than approximately 30mV.

The new closed loop gain depends on C_{INT}. In order to ensure stability it must be verified that:

Equation 10

$$C_{INT} > \frac{g_m}{2\pi \times f_Z} \times \frac{V_r}{V_{OUT}}$$

Where:

Equation 11

$$f_Z = \frac{1}{2\pi \times C_{OUT} \times R_{TOT}}$$

with:

Equation 12

$R_{TOT} = R_{OUT} + R_{ESR}$

Moreover C_{INT} must meet the following condition:

Equation 13

$$f_{SW} > K \times f_Z = \frac{K}{2\pi \times C_{OUT} \times R_{TOT}}$$

where R_{TOT} is the sum of the ESR of the output capacitor (R_{out}) and the equivalent ESR given by the virtual ESR network (RESR). k is a free design parameter greater than 1 and determines the minimum integrator capacitor value C_{INT}:

Equation 14

$$C_{INT} > \frac{g_m}{2\pi \times \left(\frac{f_{SW}}{K} - f_Z\right)} \times \frac{V_r}{V_{OUT}}$$

C must be selected as shown:

Equation 15

$$C > 5 \times C_{INT}$$

R must be chosen in order to have enough ripple voltage on integrator input:

Equation 16

$$R = \frac{L}{R_{ESR} \times C}$$

R1 can be selected as follows:

Equation 17

$$R1 \times \frac{R \times \left(\frac{1}{C \times \pi \times f_Z}\right)}{R - \frac{1}{C \times \pi \times f_Z}}$$

Example:

OUT1 = 1.5V, f_{SW} = 200KHz, L = 2.5µH, Cout = 330uF with Rout ≈ 12mΩ

We design R_{ESR} = 18mΩ

We choose C_{INT} = 560pF by equations *Equation 10*, *Equation 11* and *Equation 13* and C_{filt} = 110pF, R_{INT} = 1KΩ by eq.6, 7. C = 4.7nF by *Equation 15*.

Then R = 30KΩ (eq.16) and R1 = 4.7KΩ *Equation 17*.

6.4 Pulse skip mode

If the SKIP pin is tied to ground, the device works in skip mode.

At light loads a zero-crossing comparator truncates the low-side switch on-time when the inductor current becomes negative. In this condition the section works in discontinuous conduction mode. The threshold between continuous and discontinuous conduction mode is:

Equation 18

$$ILOAD(SKIP) = \frac{V_{IN} - V_{OUT}}{2 \times L} \times T_{ON}$$

For higher loads the inductor current doesn't cross the zero and the device works in the same way as in PWM mode and the frequency is fixed to the nominal value.

Figure 8. PWM and pulse skip mode inductor current

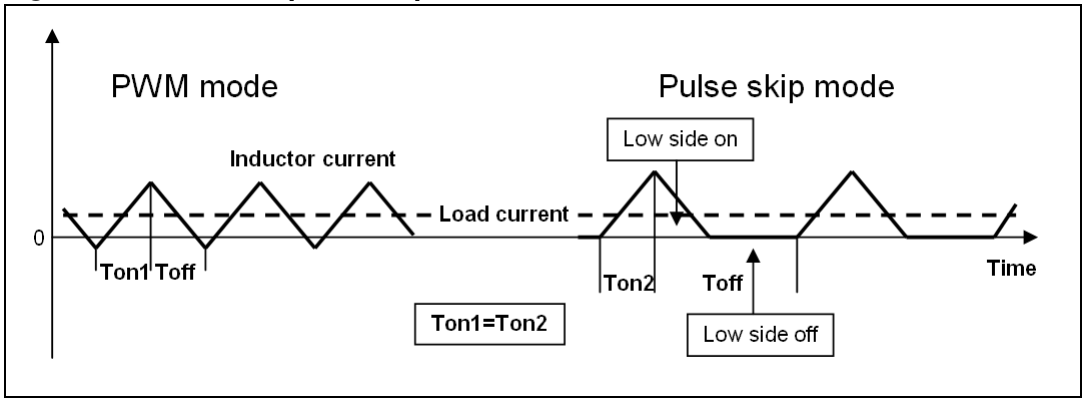


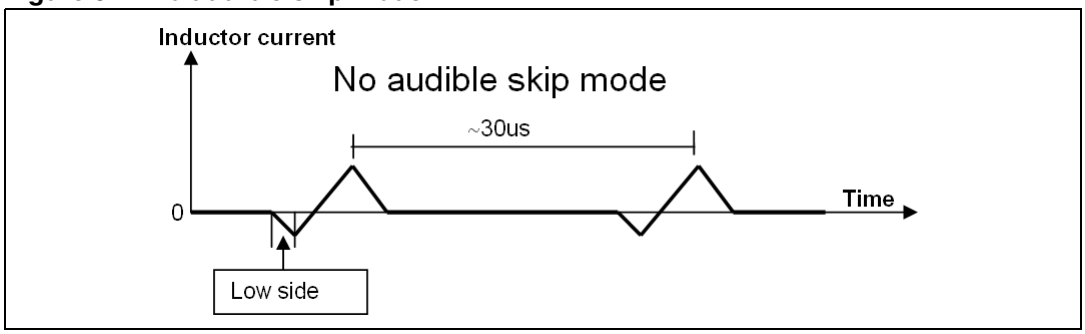
Figure 8 shows inductor current waveforms in PWM and SKIP mode. In order to keep average inductor current equal to load current, in SKIP mode some switching cycles are skipped. When the output ripple reaches the regulated voltage Vreg, a new cycle begins. The off cycle duration and the switching frequency depend on the load condition.

As a result of the control technique, losses are reduced at light loads, improving the system efficiency.

6.5 No-audible skip mode

If SKIP pin is tied to V_{REF}, a no-audible skip mode with a minimum switching frequency of 33KHz is enabled. At light load condition, If there is not a new switching cycle within a 30us (typ.) period, a no-audible skip mode cycle begins.

Figure 9. No audible skip mode



The low side switch is turned on until the output voltage crosses about Vreg + 1%. Then the high side MOSFET is turned on for a fixed on time period. Afterwards the low side switch is enabled until the inductor current reaches the zero-crossing threshold. This keeps the switching frequency higher than 33KHz. As a consequence of the control, the regulated voltage can be slightly higher than Vreg (up to 1%).

If, due to the load, the frequency is higher than 33KHz, the device works like in skip mode.

No-audible skip mode reduces audio frequency noise that may occur in pulse skip mode at very light loads, keeping the efficiency higher than in PWM mode.

6.6 Current limit

The current-limit circuit employs a “valley” current-sensing algorithm. During the conduction time of the low side MOSFET the current flowing through it is sensed. The current-sensing element can be the low side MOSFET on-resistance (*Figure 11*) or a discrete resistor in series with the source of the low side MOSFET (*Figure 10*).The first method ensures higher efficiency but lower accuracy, while with the second one ensures higher accuracy but lower efficiency.

Figure 10. Rsense sensing technique

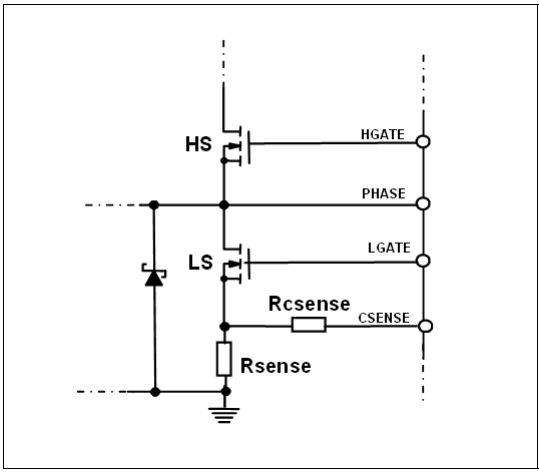
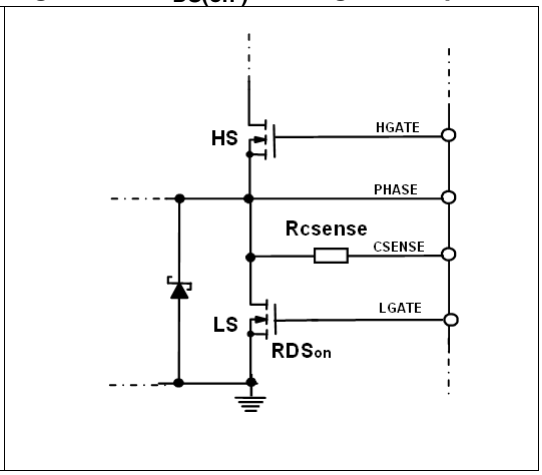


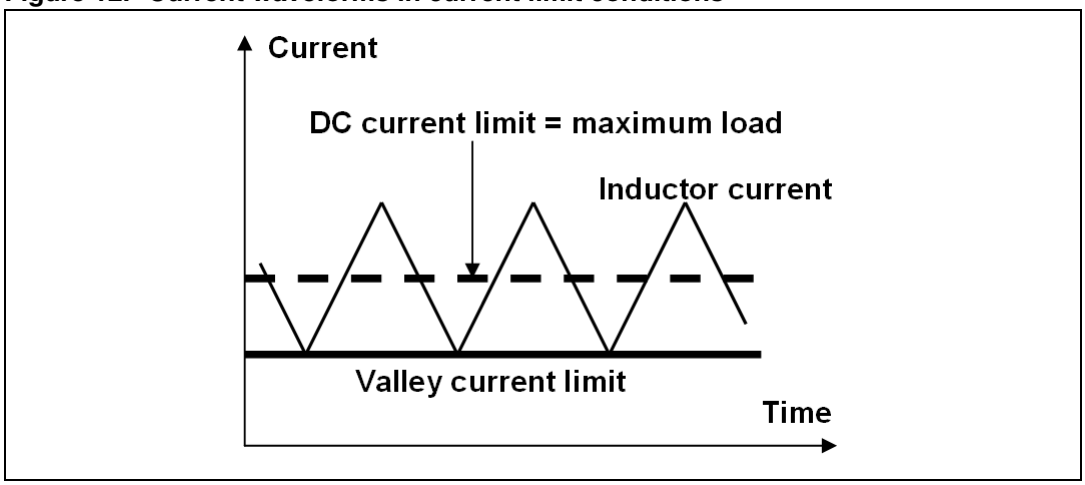
Figure 11. $R_{DS(on)}$ sensing technique



An internal 100µA current source is connected to C_{SENSE} pin and determines a voltage drop on RC_{SENSE}. If the voltage across the sensing element is greater than this voltage drop, the controller doesn't initiate a new cycle. A new cycle starts only when the sensed current goes below the current limit.

Since the current limit circuit is a valley current limit, the actual peak current limit is greater than the current limit threshold by an amount equal to the inductor ripple current. Moreover the maximum DC load is equal to the valley current limit plus half of the inductor ripple current.

Figure 12. Current waveforms in current limit conditions



The valley current limit can be set with resistor RC_{SENSE}:

Equation 19

$$R_{CSENSE} = \frac{R_{DS(on)} \times I_{Lvalley}}{100\mu A} \quad (R_{DS(on)} \text{ sensing technique})$$

Equation 20

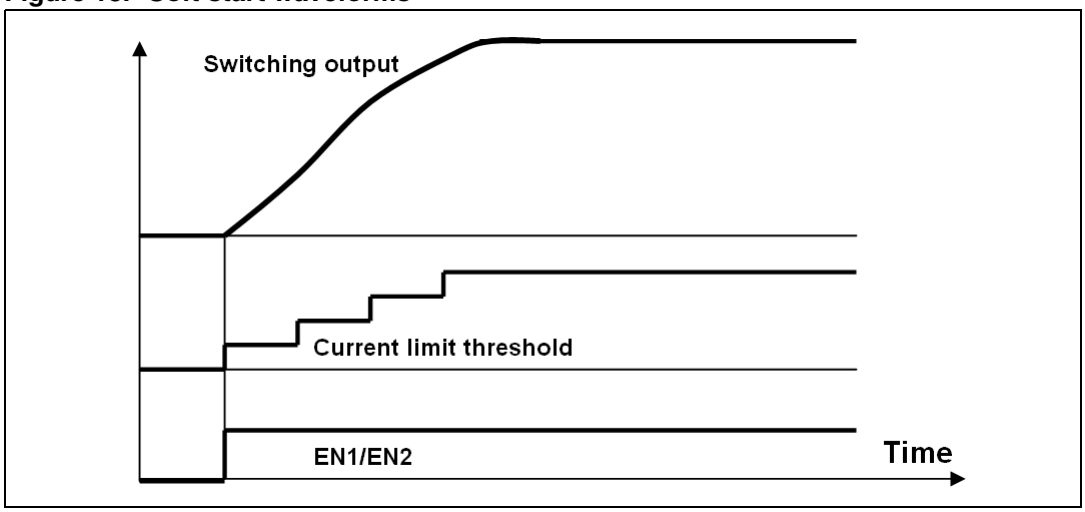
$$R_{CSENSE} = \frac{R_{SENSE} \times I_{Lvalley}}{100\mu A} \quad (R_{SENSE} \text{ sensing technique})$$

PM6680A provides also a fixed negative peak current limit to prevent an excessive reverse inductor current when the switching section sinks current from the load in PWM mode. This negative current limit threshold is measured between PHASE and SGND pins, comparing the magnitude drop on the PHASE node with an internal fixed voltage of 120mV.

6.7 Soft start and soft end

Each switching section is enabled separately by asserting high EN1/EN2 pins respectively. In order to realize the soft start, at the startup the overcurrent threshold is set 25% of the nominal value and the undervoltage protection (see related sections) is disabled. The controller starts charging the output capacitor working in current limit. The overcurrent threshold is increased from 25% to 100% of the nominal value with steps of 25% every 700µs (typ.). After 2.8ms (typ.) the undervoltage protection is enabled. The soft start time is not programmable.

Figure 13. Soft start waveforms



When a switching section is turned off (EN1/EN2 pins low), the controller enters in soft end mode.The output capacitor is discharged through an internal 10Ω p-MOSFET switch; when the output voltage reaches 0.3V, the low-side MOSFET turns on, keeping the output to ground. The soft end time also depends on load condition.

6.8 Gate drivers

The integrated high-current drivers allow to use different power MOSFETs. The high side driver MOSFET uses a bootstrap circuit which is indirectly supplied by LDO5 output. The BOOT and PHASE pins work respectively as supply and return rails for the HS driver.

The low side driver uses the internal LDO5 output for the supply rail and PGND pin as return rail.

An important feature of the gate drivers is the adaptive anti-cross conduction protection, which prevents high side and low side MOSFETs from being on at the same time. When the high side MOSFET is turned off the voltage at the phase node begins to fall. The low side MOSFET is turned on when the voltage at the phase node reaches an internal threshold. When the low side MOSFET is turned off, the high side remains off until the LGATE pin voltage goes approximatively under 1V.

The power dissipation of the drivers is a function of the total gate charge of the external power MOSFETs and the switching frequency, as shown in the following equation:

Equation 21

$$P_{driver} = V_{driver} \times Q_g \times f_{SW}$$

6.9 Reference voltage and bandgap

The 1.237V (typ.) internal bandgap voltage is accurate to ±1% over the temperature range. It is externally available (VREF pin) and can supply up to ±100µA and can be used as a voltage threshold for the multifunction pins FSEL and SKIP to select the appropriate working mode. Bypass VREF to ground with a 100nF minimum capacitor.

If VREF goes below 0.87V (typ.) , the system detects a fault condition and all the circuitry is turned off. A toggle on the input voltage (power on reset) or a toggle on SHDN pin is necessary to restart the device.

An internal divider of the bandgap provides a voltage reference Vr of 0.9V. This voltage is used as reference for the linear and the switching regulators outputs. The overvoltage protection, the undervoltage protection and the power good signals are referred to Vr.

6.10 Internal linear regulator

The PM6680A has an internal linear regulator providing 5V (LDO5) at ±2% accuracy. High side drivers, low side drivers and most of internal circuitry are supplied by LDO5 output through VCC pin (an external RC filter may be applied between LDO5 and VCC). The linear regulator can provide an average output current of 50mA and a peak output current of 100mA. Bypass LDO5 output with a minimum 1µF ceramic capacitor and a 4,7µF tantalum capacitor (ESR ≤2Ω). If the 5V output goes below 4V, the system detects a fault condition and all the circuitry is turned off. A power on reset or a toggle on SHDN pin is necessary to restart the device.

V5SW pin allows to keep the 5V linear regulator always active or to enable the internal bootstrap-switchover function: if the 5V switching output is connected to V5SW, when the voltage on V5SW pin is above 4.8V, an internal 3.0Ω max p-channel MOSFET switch connects V5SW pin to LDO5 pin and simultaneously LDO5 shuts down. This configuration allows to achieve higher efficiency. V5SW can be connected also to an external 5V supply.

LDO5 regulator turns off and LDO5 is supplied externally. If V5SW is connected to ground, the internal 5V regulator is always on and supplies LDO5 output.

Table 7. V5SW multifunction pin

V5SW	Description
GND	The 5V linear regulator is always turned on and supplies LDO5 output.
Switching 5V output	The 5V linear regulator is turned off when the voltage on V5SW is above 4.8V and LDO5 output is supplied by the switching 5V output.
External 5V supply	The 5V linear regulator is turned off when the voltage on V5SW is above 4.8V and LDO5 output is supplied by the external 5V.

6.11 Power up sequencing and operative modes

Let us consider SHDN, EN1 and EN2 low at the beginning. An external voltage is applied as input voltage. The device is in shutdown mode.

When the SHDN pin voltage is above the shutdown device on threshold (1.5V typ.), the controller begins the power-up sequence. All the latched faults are cleared. LDO5 undervoltage control is blanked for 4ms and the internal regulator LDO5 turns on. If the LDO5 output is above the UVLO threshold after this time, the device enters in standby mode. The switching outputs are kept to ground by turning on the low side MOSFETs.

When EN1 and EN2 pins are forced high the switching sections begin their soft start sequence.

Table 8. Operatives modes

Mode	Conditions	Description
Run	SHDN is high, *EN1/EN2* pins are high	Switching regulators are enabled; internal linear regulators outputs are enabled.
Standby	Both *EN1/EN2* pins are low and *SHDN* pin is high	Internal Linear regulators active (LDO5 is always on). In Standby mode *LGATE1/LGATE2* pins are forced high while *HGATE1/HGATE2* pins are forced low.
Shutdown	*SHDN* is low	All circuits off.

7 Monitoring and protections

Power good signals

The PM6680A provides three independent power good signals: one for each switching section (PGOOD1/PGOOD2).

PGOOD1/PGOOD2 signals are low if the output voltage is out of ±10% of the designed set point or during the soft-start, standby and shutdown mode.

Thermal protection

The PM6680A has a thermal protection to preserve the device from overheating. The thermal shutdown occurs when the die temperature goes above +150°C. In this case all internal circutry is turned off and the power sections are turned off after the discharge mode.

A power on reset or a toggle on the SHDN pin is necessary to restart the device.

Overvoltage protection

When the switching output voltage is about 115% of its nominal value, a latched overvoltage protection occurs. In this case, the synchronous rectifier immediately turns on while the high-side MOSFET turns off. The output capacitor is rapidly discharged and the load is preserved from being damaged. The overvoltge protection is also active during the soft start. Once an overvoltage protection has been detected, a toggle on SHDN, EN1/EN2 pins or a power on reset is necessary to exit from the latched state.

Undervoltage protection

When the switching output voltage is below 70% of its nominal value, a latched undervoltage protection occurs. In this case the switching section is immediately disabled and both switches are open. The controller enters in soft end mode and the output is eventually kept to ground, turning low side MOSFET on. The undervoltage circuit protection is enabled only at the end of the soft-start. Once an overvoltage protection has been detected, a toggle on SHDN, EN1/EN2 pin or a power on reset is necessary to clear the undervoltage fault and starts with a new soft-start phase.

Table 9. Protections and operatives modes

Mode	Conditions	Description
Overvoltage protection	OUT1/OUT2>115% of the nominal value	*LGATE*1/LGATE2 pin is forced high, LDO5 remains active. Exit by a power on reset or toggling *SHDN* or *EN1/EN2*
Undervoltage protection	OUT1/OUT2<70% of the nominal value	*LGATE1/LGATE2* is forced high after the soft end mode, LDO5 remains active. Exit by a power on reset or toggling *SHDN* or *EN1/EN2*
Thermal shutdown	T_J> +150°C	All circuitry off. Exit by a POR on *VIN* or toggling *SHDN.*

8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 10. VFQFPN 5x5 mechanical data (mm)

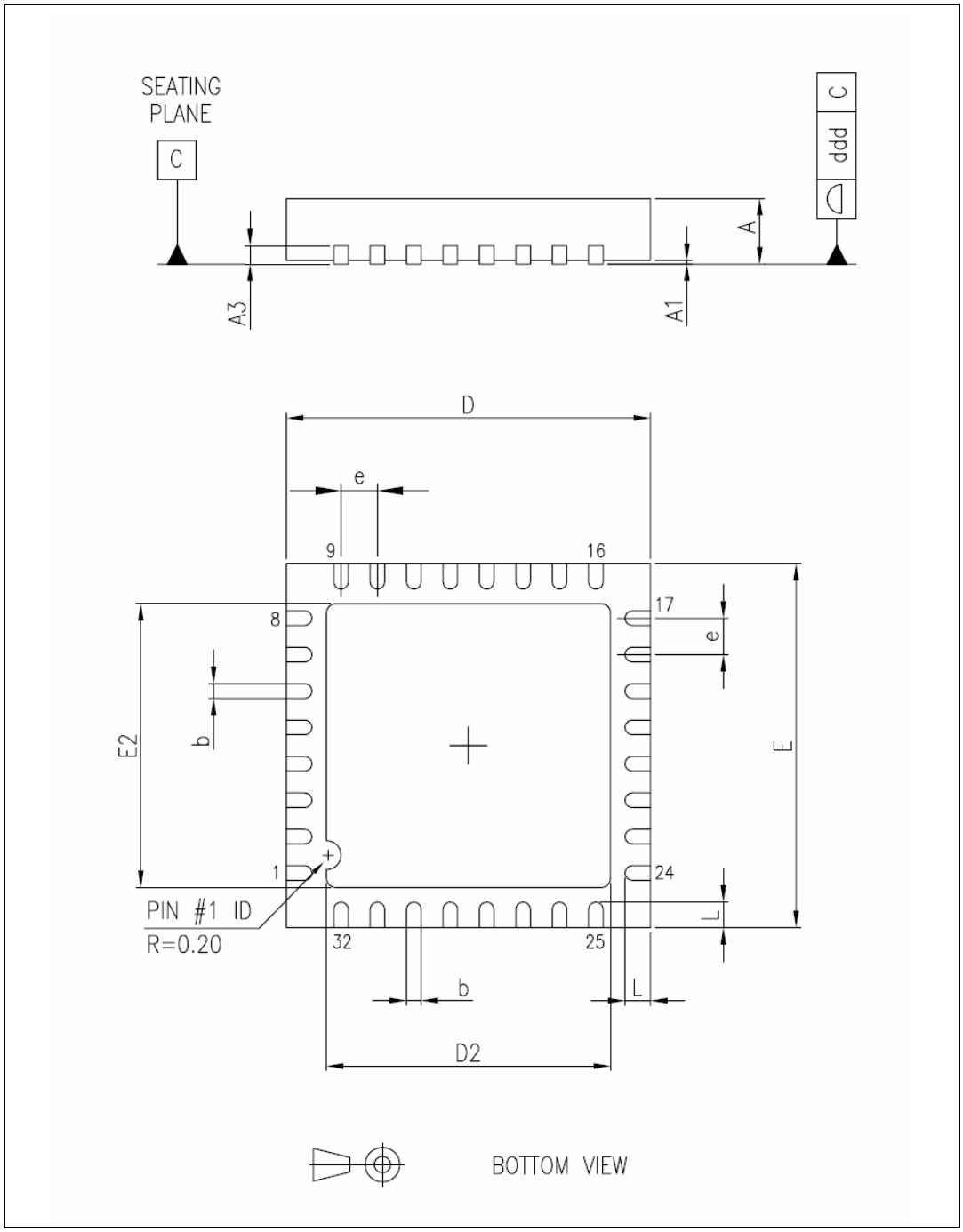
Dim.	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20	
b	0.18	0.25	0.30
D	4.85	5.00	5.15
D2	See exposed pad variations (1)		
E	4.85	5.00	5.15
E2	See exposed pad variations (1)		
e		0.50	
L	0.30	0.40	0.50
ddd			0.05

1. Dimensions D2 & E2 are not in accordance with JEDEC.

Table 11. Exposed pad variations

D2			E2		
Min.	Typ.	Max.	Min.	Typ.	Max.
2.90	3.10	3.20	2.90	3.10	3.20

Figure 14. Package dimensions



9 Revision history

Table 12. Revision history

Date	Revision	Changes
12-Oct-2006	1	Initial release.

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