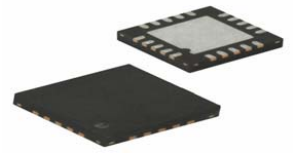
PM6697H

Datasheet

VR13 single-phase controller



VFQFPN20 3x3 mm

Product status link
PM6697H

Product summary	
Order code	PM6697H TR
Package	VFQFPN20 3x3mm
Packing	Tape & reel

Features

- Single-phase controller Intel® VR13 compliant with 25 MHz SVID bus rev 1.7
- High performance digital control loop STVCOT™
- Selectable PWM switching frequency, maximum current, DVID slew rate, load-line
- External power MOSFET support
- Remote sense; 0.5% V_{out} accuracy with calibration
- Ultrasonic mode at light loads
- Programmable voltage positioning
- OV, UV and FB disconnection protection
- Package VFQFPN20 3x3mm

Application

- Power regulation for VR13 based Intel® based microprocessors
- Power regulation for Denverton Intel® based systems

Description

The PM6697H is a high performance single-phase controller designed to power Intel's VR13 power rails. All required parameters are programmable through dedicated pin strapping.

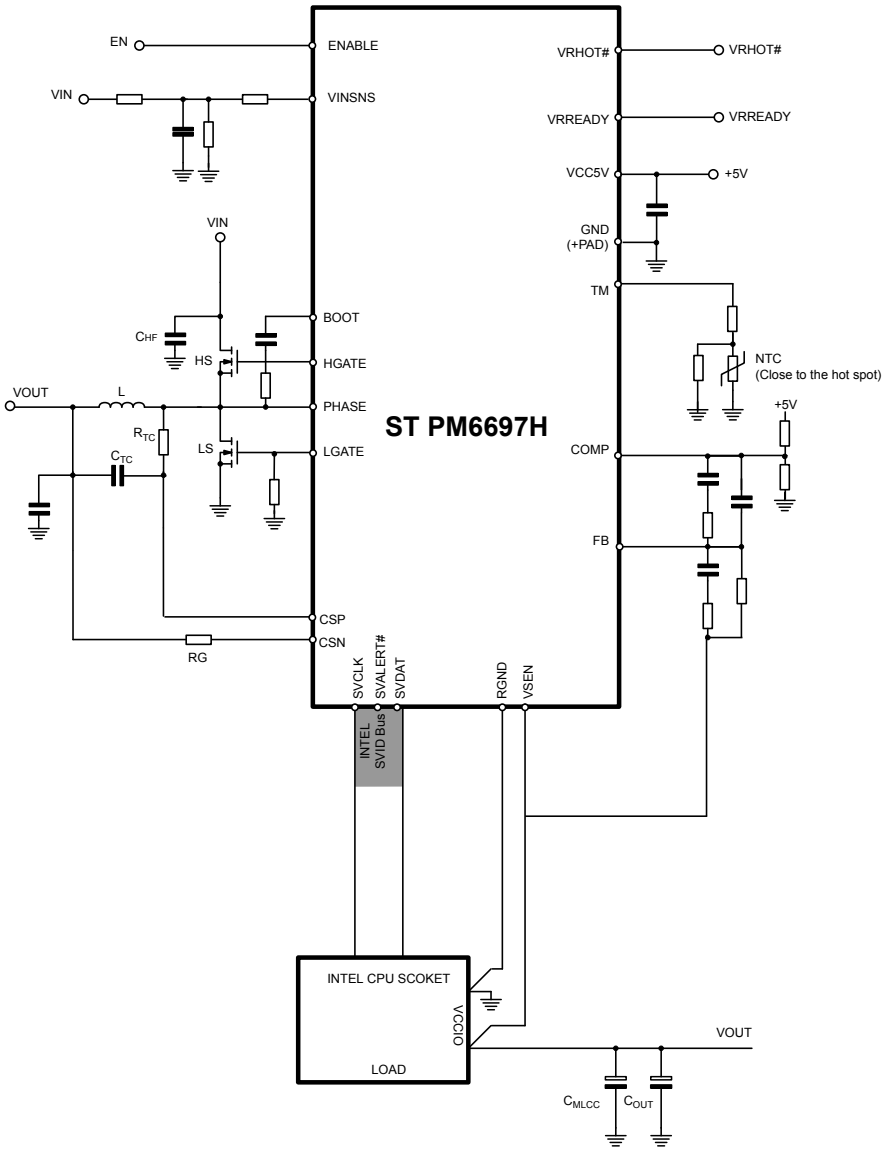
STVCOT™ control loop provides fast load transient response, minimizing and optimizing the output filter composition.

The device assures fast and independent protection against load overcurrent, under/overvoltage and feedback disconnections. The device is available in VFQFPN20 3x3mm package.

1 Typical application circuit and block diagram

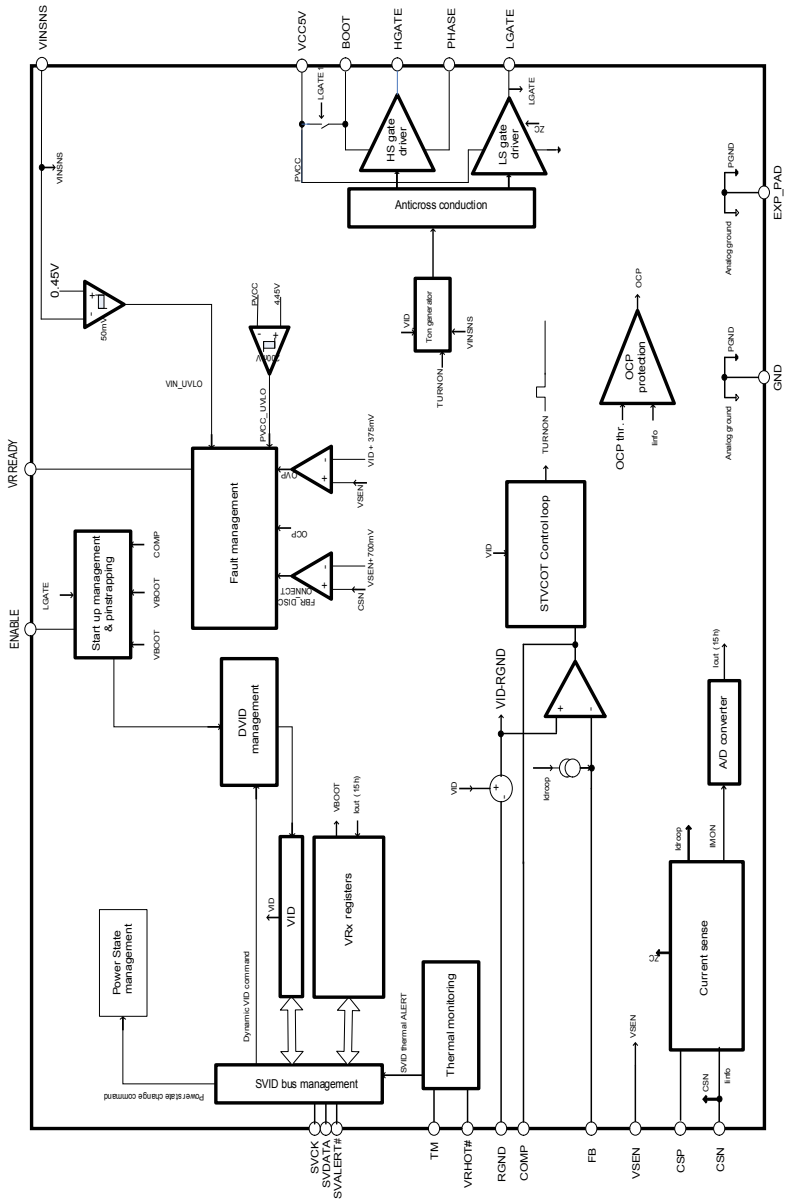
1.1 Application circuit

Figure 1. Typical PM6697H application circuit with MOSFETs



1.2 Block diagram

Figure 2. **PM6697H block diagram**



2 Pin description and connection diagram

Figure 3. **PM6697H pin connection (top view)**

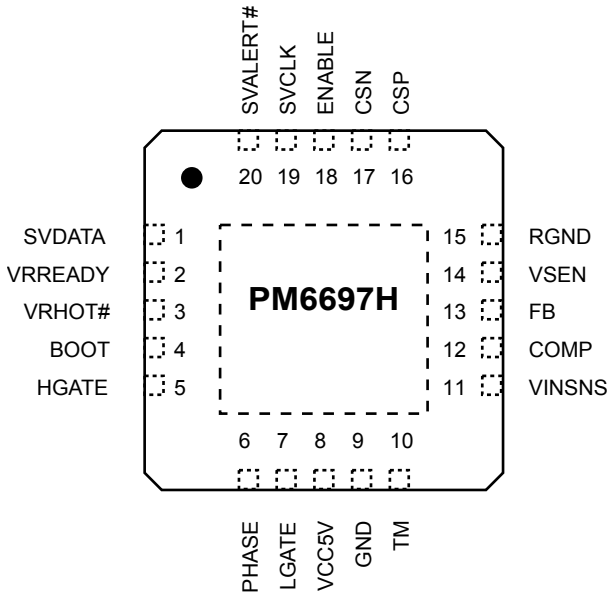


Table 1. **Pin description**

No.	Name	I/O	Type	Function
1	SVDAT	I/O	Open drain	SVIBus serial data.
2	VRREADY	O	Open drain	VRREADY indicator. Pull-up to an external voltage (3.3V typ.), if not used it can be left floating.
3	VRHOT#	O	Open drain	Voltage regulator HOT. This is an alarm signal asserted by the controller when the temperature sensed through the TM pin exceeds T_{MAX} (Active Low).
4	BOOT	I	Analog	Bootstrap capacitor connection. Input for the supply voltage of the high-side gate driver.
5	HGATE	O	Analog	High-side gate driver output. This is the floating gate driver output.
6	PHASE	I/O	Analog	Switch node connection and return path for the high-side gate driver.
7	LGATE	O	Analog	Low-side gate driver output. A resistor to GND can be used to set the VBOOT (startup) voltage.
8	VCC5V	I	Supply	Main IC analog power supply. Operative voltage is 5V ±5%. Filter with 1µF MLCC to GND (typ.).
9	GND			GND connection. All internal references and logic are referenced to this pin. Filter to VCC5V with proper MLCC capacitor and connect to the PCB GND plane.
10	TM	I	Analog	Thermal monitor sensor. Connect with proper network embedding NTC to the multi-phase power section. The IC senses the power section temperature and uses the information to define the VR_HOT signal and temperature monitoring.
11	VINSNS	I	Analog	Input voltage sense. It is used by the on-time generator and by the UVLO VIN monitor. Connect with a 1/10 resistor divider to the regulator input voltage and mount 22nF resistor in parallel to the low resistor of the divider. A series resistor allows to set the switching frequency.

No.	Name	I/O	Type	Function
12	COMP	O	Analog	Error amplifier output. Connect with a (R_F+C_F)//C_P network to the FB pin. The device cannot be disabled by pulling low this pin. This pin is also used to program the working mode of the regulator (max. load Icc MAX, load-line on/off, DVID slew rate).
13	FB	I	Analog	Load-line error amplifier inverting input. Connect with a resistor R_{FB} to VSEN and with a (R_F+C_F)//C_P network to COMP pin.
14	VSEN	I	Analog	Remote buffer positive sense of output voltage. Connect to the positive side of the load to perform remote sense. Anti-aliasing filter embedded.
15	RGND	I	Analog	Remote buffer positive sense of the ground of output rail. Connect to the negative side of the load to perform remote sense. Anti-aliasing filter embedded.
16	CSP	I	Analog	Current sense positive input. Connect through an R-C filter to the phase-side of the inductor.
17	CSN	I	Analog	Current sense negative input. Connect to the output-side of the inductor. Filter with 100nF (typ.) to GND.
18	ENABLE	I	CMOS	Level sensitive enable pin (3.3V compatible). Pull low to disable the device, pull up above the turn-on threshold to enable the controller.
19	SVCK	I/O	Open drain	SVI Bus serial clock.
20	SVALERT#	O	Open drain	SVI Bus alert.
	EXPOSED PAD			Thermal pad connection, internally connected to silicon GND. Connect to the PCB GND plane.

3 Absolute maximum ratings

Absolute maximum ratings are those values beyond which damage to the device may occur. These are stress ratings only and functional operation of the device at these conditions is not implied. Operating outside maximum recommended conditions for extended periods of time may impact product reliability and result in device failures.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
PHASE	to GND	-5 to 35	V
BOOT	to GND	-0.3 to 40	V
HGATE	to GND	-0.3 to 40	V
BOOT, HGATE	to PHASE	-0.3 to 7	V
LGATE	to GND	-0.3 to 7	V
VCC5V, COMP	to GND	-0.3 to 7	V
All other Pins	to GND	-0.3 to 4.6	V

Table 3. Recommended operating conditions

Symbol	Parameter	Value	Unit
VIN - input voltage of the switching regulator	to GND	4.5 to 13.2	V
VCC5V	to GND	4.2 to 5.5	V
COMP	to GND	-0.3 to 5.5	V
PHASE, t < 50ns	to GND	-3 to 30	V
BOOT, HGATE	to PHASE	-0.3 to 5.5	V
All other Pins	to GND	-0.3 to 3.6	V
TOPERATING	Operating temperature range	0 to 85	°C

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{THJA}	Thermal Resistance Junction to Ambient (Device soldered on 2s2p PC Board)	45	°C/W
T_{MAX}	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-40 to 150	°C
T_J	Junction Temperature Range	-5 to125	°C

4 Electrical characteristics

Table 5. Electrical characteristics

(VCC5= 5 V ± 5%, ENABLE = 3.3 V, VID = 1 V, T_{amb}= 25°C, unless otherwise specified).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current and power-on						
VCC5V	Supply current	ENABLE = high, FB = COMP		7.9		mA
		ENABLE = low, FB = COMP		5.9		mA
	UVLO turn-ON	VCC5 voltage rising		4.2		V
	UVLO turn-OFF	VCC5 voltage falling		3.8		V
IBOOT	Boot input current	BOOT = 19 V, phase = 14 V		0.6		mA
VINSNS	UVLO turn-ON	VINSNS rising		0.45		V
	UVLO turn-OFF	VINSNS falling		0.4		V
Oscillator, startup, enable						
FSW	Switching frequency	VINSNS pinstrap = 500 kHz	450	500	550	kHz
		VINSNS pinstrap = 600 kHz	540	600	660	
		VINSNS pinstrap = 800 kHz	720	800	880	
		VINSNS pinstrap = 400 kHz	360	400	440	
TOFFMIN	Minimum off-time			120		ns
TONMIN	Minimum on-time			60		ns
TA		Delay time from ENABLE high to VR startup			160	µs
ENABLE	Input high voltage	EN voltage rising			0.8	V
	Input low voltage	EN voltage falling	0.3			V
	Leakage current				1	µA
SVI serial bus						
SVCLK, SVDAT	Input high voltage		0.65			V
	Input low voltage				0.45	V
SVDAT, SVALERT#	Output low voltage	I_{SINK} = -5 mA			65	mV
Reference and current reading						
k_{VID}	V_{OUT} setpoint accuracy	FB to RGND, VID = 1.0 V to 1.52 V	-0.5		+0.5	%
		FB to RGND, VID = 0.8 V to 1.0 V	-5		+5	mV
		FB to RGND, VID <= 0.8 V			+8	mV
□ DROOP	LL accuracy 0 to full load	I_{INFO} = 0 µA	-1		+1	µA
		I_{INFO} = 25 µA	24		26	µA
IMON ADC	15h register accuracy 0 to full load	I_{INFO} = 1.27 µA		0D		HEX
		I_{INFO} = 25 µA		FF		HEX
DVID	Slew - rate fast		10			mV/µs
	Slew - rate slow	Slew - rate fast / 4	2.5			mV/µs
Drivers						
HGATE	R_{ON_HPCH}	BOOT - PHASE = 5 V, I = 100 mA		1.4		Ω

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
HGATE	R_{ON_HNCH}	BOOT - PHASE = 5 V, I = 100 mA		1.5		Ω
LGATE	R_{ON_LPCH}	Pull-up, I = 100 mA		1.6		Ω
	R_{ON_LNCH}	Pull-up, I = 100 mA		0.7		Ω
BOOT	Switch on resistance	VCC5V = 5.0 V, I_BOOT = 5 mA		20		Ω
Thermal throttling						
TM trip point	VR_HOT_assertion			1.8		V
	VR_HOT_deassertion			1.9		V
Protections						
OVP	Overvoltage protection	(VSEN-RGND) Rising above setpoint		375		mV
UVP	Undervoltage protection	Only for VCCIO applications (see Table 7)		650		mV
FB DISC	FB disconnection	V_{CSN} rising, above (VSEN-RGND)		700		mV
OC	OC threshold	I_{INFO}	28	33.25	39	uA
VRREADY	Output low voltage	I = 4 mA			150	mV
VRHOT#	Output low voltage	I = 20 mA			260	mV

5 Device configuration and pin strapping tables

The PM6697H is fully compliant with Intel VR13 SVID Protocol rev1.7. To guarantee proper device and CPU operations, refer to this document for bus design and layout guidelines.

Different platforms may require different pull-up impedance on the SVI bus. Impedance matching and spacing among SVDATA, SVCLK and SVALERT# must be followed.

Once VCC5V is above the UVLO (under voltage lock-out) threshold (see Chapter Start-up sequence), the device reads the voltage on COMP, LGATE, VINSNS pins to detect the application configuration, according to the following tables (Table 6,Table 7,Table 8):

Table 6. Voltage regulator switching frequency pinstrapping

Resistor R_{VINs} [kOhm]	Switching frequency [kHz]
0	500
8.2	600
16	800
24	400

Table 7. Application type pin strapping

COMP pull up resistor [kOhm] (1)	COMP pull down resistor [kOhm] (1)	SVID ADDR [HEX]	APPLICATION	Icc MAX [A]	Load line	BOOT [V]	DVID Slew rate [mV/us]
820	20	00h	Denverton CPU VR13 - 1	35	ON	1.0 /0	10
220	20	00h	Denverton CPU VR13 - 2	20	ON	1.0 /0	10
130	20	01h	Denverton VNN VR13 - 1	14	OFF	1.0 /0	10
91	20	01h	Denverton VNN VR13 - 2	7	OFF	1.0 /0	10
68	20	02h	Denverton DDR VR13 - 1	32	OFF	1.0 /0	10
51	20	02h	Denverton DDR VR13 - 2	32	OFF	1.2 /0	10
51	27	03h	Denverton VCCRAM VR13 - 1	9	OFF	1.0 /0	10
51	33	03h	Denverton VCCRAM VR13 - 2	5	OFF	1.0 /0	10
51	39	00h	Denverton CPU VR13 - 3	10	ON	1.0 /0	10
51	51	00h	Denverton CPU VR13 - 4	5	ON	1.0 /0	10
51	62	01h	VCCSA VR13- 1	15	ON	0.9 /0	10
51	75	01h	VCCSA VR13 -2	15	OFF	1.0 /0	10
51	91	02h	VCCIO VR13 -1	26	OFF	0.9 /0	10
51	120	02h	VCCIO VR13 -2	26	OFF	1.0 /0	10
51	150	03h	VMCP VR13 - 1	15	OFF	0.9 /0	10
51	200	03h	VMCP VR13 -2	15	OFF	1.0 /0	10

1. CF < 10nF

Table 8. **VBOOT pin strapping**

LGATE (PM6697H) pulldown resistor [kOhm]	VBOOT voltage [V]
–	1.2, 1 and 0.9 (see Table 7)
10	0 (see Table 7)

6 Device description

The PM6697H is a high performance single-phase controller designed to power Intel's VR13 power rails. All required parameters are programmable through dedicated pin strapping. The STVCOT^{TM} control loop provides fast load transient response, minimizing and optimizing the output filter composition.

The device assures fast and independent protection against load overcurrent, under/overvoltage and feedback disconnections.

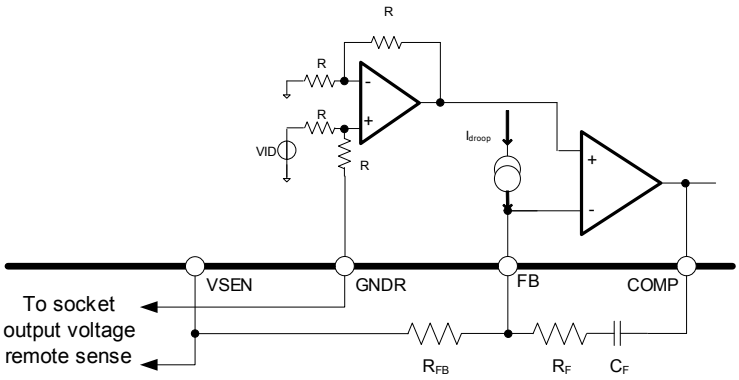
The device is available in a VFQFPN20 3x3 mm package.

6.1 Output voltage positioning

The controller reads the current delivered by each switching section by monitoring the voltage drop across the DCR inductor. The current I_{droop} sourced from the FB pin is directly proportional to the read current, and it causes the output voltage to vary according to the external RFB resistor (connected remotely to the output voltage), so implementing the desired load-line effect (see Figure 4).

The PM6697H embeds a ground remote-sense to sense remotely the ground of the regulated output without any additional external components. In this way, the programmed output voltage is regulated compensating for board and socket losses. Keeping the sense traces parallel and guarded by a power plane results in common mode coupling for any picked-up noise.

Figure 4. Output voltage remote sense



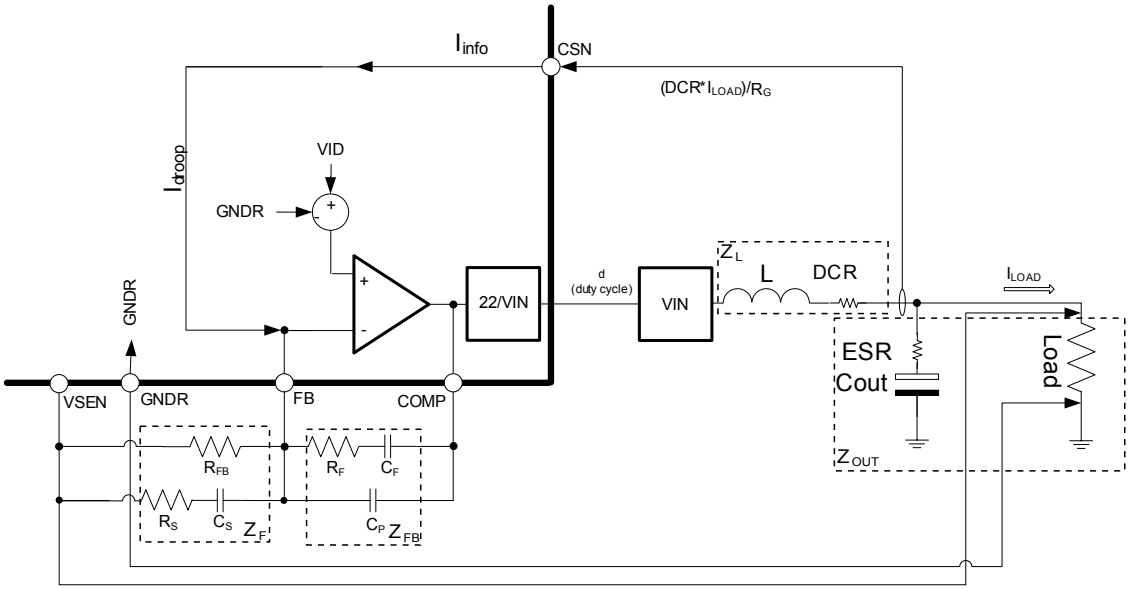
6.2 Active regulation

The PM6697H controller implements the proprietary STVCOT™ architecture.

During operation, the output voltage is sensed differentially and compared to a voltage reference at the input of an error amplifier. The resulting error amplifier error is then used to generate the PWM pulses of the controller.

The STVCOT™ architecture can be modeled with an equivalent analog control loop of a single-phase converter (see Figure 5).

Figure 5. Equivalent control loop



The equivalent transfer function of the control loop is:

$$G_{LOOP}(s) = -GAIN \cdot \frac{Z_{OUT}(s)}{Z_{OUT}(s) + Z_L(s)} \cdot \frac{Z_F(s)}{Z_{FB}(s)} \cdot \left[1 + \frac{DCR}{R_G} \cdot \frac{R_{DROOP}(s)}{Z_{OUT}(s)}\right] \quad (1)$$

Where:

- $Z_{OUT}(s)$ is the impedance resulting by the parallel of the output capacitor (and its ESR) and the applied load R_O
- $Z_F(s)$, $Z_{FB}(s)$ are the compensation network impedances
- $Z_L(s)$ is the equivalent inductor impedance
- GAIN is the PWM transfer function. It is a constant value (=22)

A dedicated support worksheet can be used to properly design the compensation network. Ask your ST representative for the proper design aid material.

6.3 DCR current reading loop

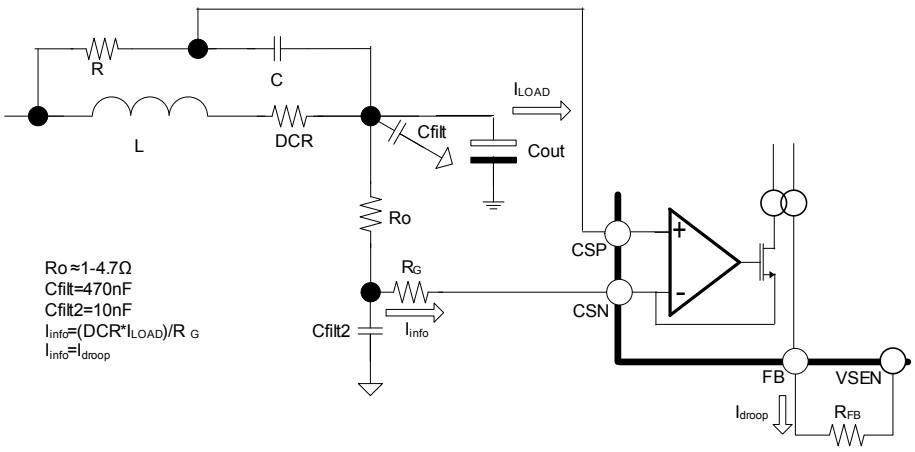
The PM6697H can read the current delivered by the switching section by monitoring the voltage drop across the inductor DCR or across a sense resistor placed in series to the inductor element. The fully-differential current reading rejects noise and allows placing sensing elements in different locations without affecting the measurement's accuracy. The transconductance ratio is issued by the external resistor R_G placed outside the chip between CSN pin toward the reading points. The current sense circuit always tracks the current information, the pin CSP is used as a reference keeping the CSN pin to this voltage. To correctly reproduce the inductor current an R-C filtering network must be introduced parallel to the sensing element. The current that flows from the CSN pin is then given by the following equation (see Figure 6):

$$I_{info} = \frac{DCR}{R_G} \cdot \frac{1 + s \cdot L/DCR}{1 + s \cdot R \cdot C} \cdot I_{PHASE} \quad (2)$$

Considering now to match the time constant between the inductor and the R-C filter applied (Time constant mismatches cause the introduction of poles into the current reading network causing instability. In addition, it is also important for the load transient response and to let the system show resistive equivalent output impedance) it results:

$$\frac{L}{DCR} = R \cdot C \Rightarrow I_{info} = \frac{R_L}{R_G} \cdot I_{PHASE} = I_{Droop} \quad (3)$$

Figure 6. DCR current reading

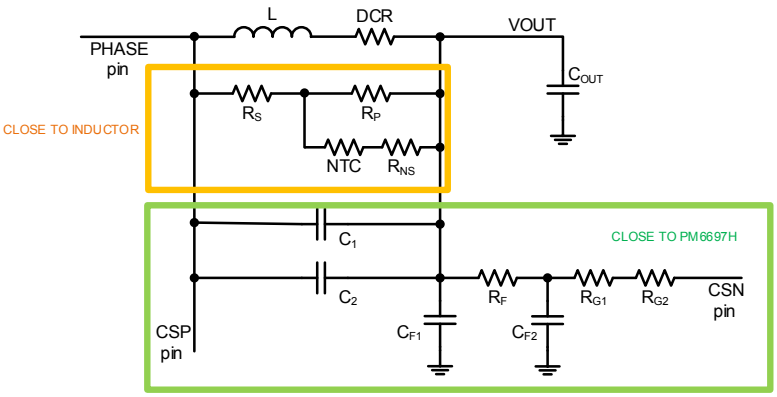


The current read through the CSP / CSN pairs is mirrored into a current I_{droop} proportional to the current delivered by the regulator.

Refer to worksheet for proper design of the R-C fillter and of the NTC needed to thermally compensate the DCR drift overtemperature.

For a compact board layout keep the current sensing signals directly from the current sensing element terminals (inductor pads). Route the current sensing nets coupled and far from analog switching/digital high speed nets. Place all the resistors of the R-C filter and the NTC close to the inductor and place the capacitors of the R-C filter and the RG resistors close to PM6697H (see Figure 7). Use the GND plane for shielding.

Figure 7. **DCR current reading layout suggestion**



6.4 Load-line definition

When load-line is enabled (COMP pin strapping), the PM6697H introduces a dependence of the output voltage on the load current recovering part of the drop due to the output capacitor ESR in the load transient. Introducing a dependence of the output voltage on the load current, a static error, proportional to the output current, causes the output voltage to vary according to the sensed current.

Figure 6 shows the Current Sense Circuit used to implement the load-line. The current I_{droop} is sourced by the FB pin. R_{FB} gives the final gain to program the desired load-line slope. The output voltage characteristic vs. load current is then given by:

$$V_{OUT} = VID - R_{FB} \cdot I_{DROOP} = VID - R_{FB} \cdot \frac{DCR}{R_G} \cdot I_{OUT} = VID - R_{LL} \cdot I_{OUT} \quad (4)$$

Where R_{LL} is the resulting load-line resistance implemented by the switching regulator.

The R_{FB} resistor can be then designed according to the RLL specifications as follows:

$$R_{FB} = R_{LL} \cdot \frac{R_G}{DCR} \quad (5)$$

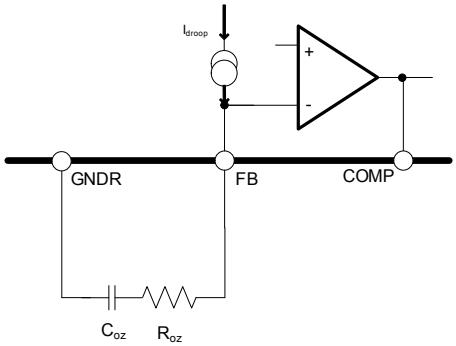
6.5 Dynamic VID transitions

The integrated 8-bit digital-to-analog converter (DAC) can change its output voltage, with 5 mV step, according to INTEL VR13 VID table. The PM6697H manages Dynamic VID Transitions (DVID) that allow the output voltage to change according to DVID commands sent through SVID bus.

When the controller receives a DVID command, the internal VID reference steps up or down with the proper voltage slew rate until the final VID value is reached. If a new DVID command is issued during the transition, the device updates the final VID value and performs the dynamic transition to the new final VID. The voltage slew rate in DVID can be fast (10 mV/us) or slow (SR-slow, programmable value in the range 1/2 to 1/16 of SR-fast), according to the SVID bus command (SetVID Fast and SetVID Slow respectively).

The PM6697H properly adds offset to the output voltage in order to avoid any undershoot in DVID transitions. When needed, it is possible to further compensate the undershoot in DVID transition by designing a R_{OZ} - C_{OZ} network as shown in Figure 8:

Figure 8. DVID undershoot compensation



Refer to worksheet for R_{OZ} - C_{OZ} network design.

During DVID transitions the protections are managed as follows:

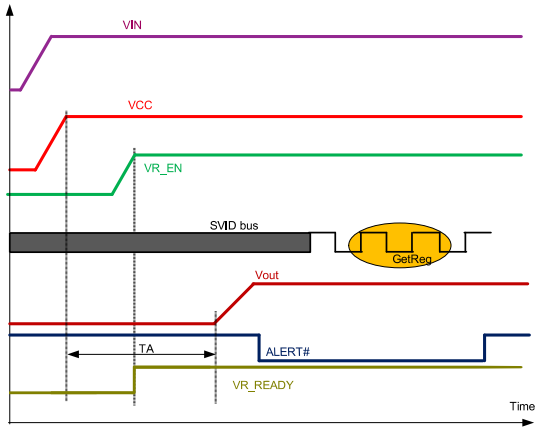
- During every positive and negative DVID, OVP is disabled and it is re-enabled at the end of the DVID.
- During positive DVID, OCP is disabled.

6.6 Start-up sequence

The start-up sequence occurs only when VCC5V is above VCC5V UVLO rising threshold and VIN is above UVLO threshold. At this point the controller sets its internal register based on the pin strapping configuration (see section Device configuration and pin strapping tables). The procedure lasts TA = 2.5 ms max. After this time, if the ENABLE pin is over the EN turn-ON threshold, the controller can start up and the SVID bus is set active and idle.

VR then ramps to the programmed boot voltage (VBOOT, see Table 8) and asserts VRREADY. SVALERT# is asserted at the end of VBOOT ramp. During startup OVP and OCP are enabled.

Figure 9. **Start-up sequence (VBOOT = 0V)**

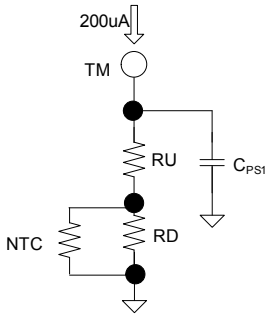


6.7 SVID thermal alert and VRHOT#

In DCR current sense mode, PM6697H TM pin is used as a source of a precise current (200 µA typ.) which is injected into an NTC-based resistor network (refer to Figure 10). The NTC should be placed close to the hottest spot of the power stage in order to sense the regulator temperature. As the temperature of the power stage increases, the NTC resistive value decreases so reducing the voltage observable at the TM pin. The voltage observed at the TM pin is internally compared with the following thresholds:

- 1.8 V: the temperature of the voltage regulator power stage has reached 100% of the allowed maximum temperature (TMAX). VRHOT# is asserted (low).
- 1.9 V: the temperature of the voltage regulator power stage has reached 97% of the allowed maximum temperature. VRHOT# is de-asserted but SVID thermal alert is asserted.
- 2.0 V: the temperature of the voltage regulator power stage is <= 94% of the allowed maximum temperature. SVID thermal alert is de-asserted

Figure 10. **PM6697H TM network in DCR current sense mode**



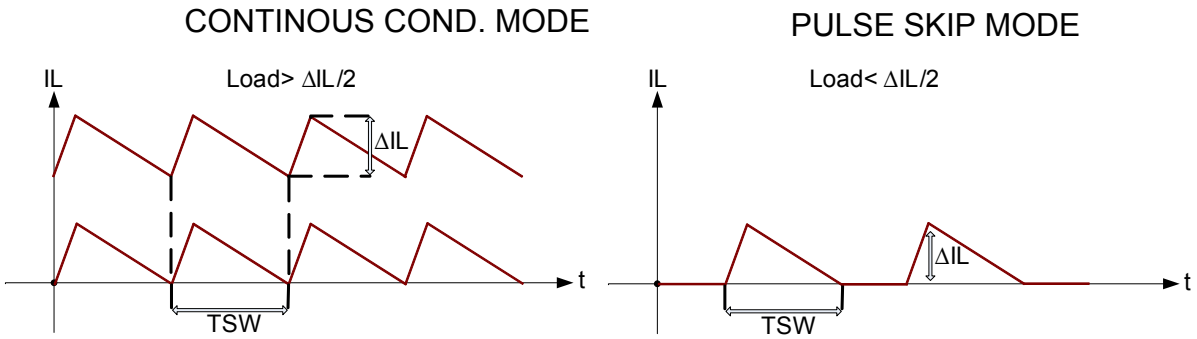
The allowed maximum temperature (TMAX) is design dependent and can be easily programmed by designing the network on the TM pin. Refer to worksheet for RU and RD design.

6.8 Efficiency optimization

The PM6697H can skip switching cycles at light loads in order to optimize the conversion efficiency without losing responsiveness to load transients.

In all power states (PS0, PS1, PS2, PS3) the switching regulator is forced to work in discontinuous conduction mode (see Figure 11): at light load the low-side MOSFET is turned off when the inductor current becomes equal to zero or lower than zero (by driving SMOD# signal). This feature is performed by a zero crossing comparator of the voltage between CSP and CSN pins. This management is commonly known as PULSE SKIP mode. When the load current goes higher than half of the inductor ripple, the controller works in continuous conduction mode.

Figure 11. Pulse skip and continous conduction mode



6.9 Monitoring and protections

6.9.1 Overvoltage protection

The PM6697H provides an overvoltage protection when Vout > VID + 375 mV typ. In this case the Voltage Regulator (VR) stops switching and the output voltage reference is brought to 250 mV with a DVID fast down transition; during this transition, the low-side MOSFET is turned on when Vout > VID + 375 mV typ. and turned off when Vout < VID, discharging the output voltage without any output voltage undershoot.

Latched protection. VCC5V or EN toggle is needed to restart.

6.9.2 Undervoltage protection (VCCIO application only)

If the PM6697H works in VCCIO VR13 mode (see Table 7), then an undervoltage protection is enabled.

When Vout < 650 mV typ., the Voltage Regulator (VR) stops switching and VRREADY signal is pulled low.

Latched protection. VCC5V or EN toggle is needed to restart.

6.9.3 Overcurrent protection

The PM6697H performs a total overcurrent protection: Overcurrent protection occurs when the current I_{info} overcomes OCTHR = 33.5 uA typ. for a time > 2 ms typ. In case of overcurrent, the switching controller stops switching and the output is left in high impedance (Hi-Z).

This is a latched protection, so VCC5V or EN toggle is needed to restart.

As a general rule, RG resistor can be designed in order to have I_{info}=25 uA when the load is about IccMAX:

$$R_G = \frac{IccMAX \cdot DCR}{25\mu A} \quad (6)$$

As a result the OCP load is:

$$I_{LOADOCP} = \frac{OCTHR}{25uA} \cdot IccMAX = 1.3 \cdot IccMAX \quad (7)$$

6.9.4 FB disconnection

This protection is enabled only in DCR current sensing mode.

If CSN voltage goes over VSEN + 700 mV typ., FB disconnection protection is triggered. In this case the Voltage Regulator (VR) stops switching and the output is left in high impedance (Hi-Z), in order to protect the load from overvoltage due to remote feedback network disconnection.

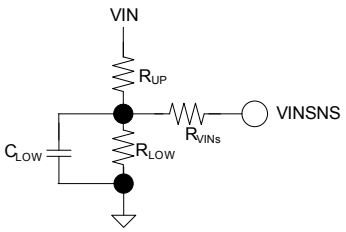
This is a latched protection, so VCC5V or EN toggle is needed to restart.

6.9.5 VIN monitor

When the pin VINSNS, that senses the input voltage with a ratio 1:10, goes lower than 0.40 V, the controller shuts down immediately. VINSNS > 0.45 V is needed to restart (refer to start-up procedure). This protection is always enabled.

Caution: in order to ensure proper behavior, the VIN monitor protection and the stability of the control loop, a 1:10 divider must be used between the input voltage and the VINSNS pin, as shown in Figure 12.

Figure 12. VINSNS network



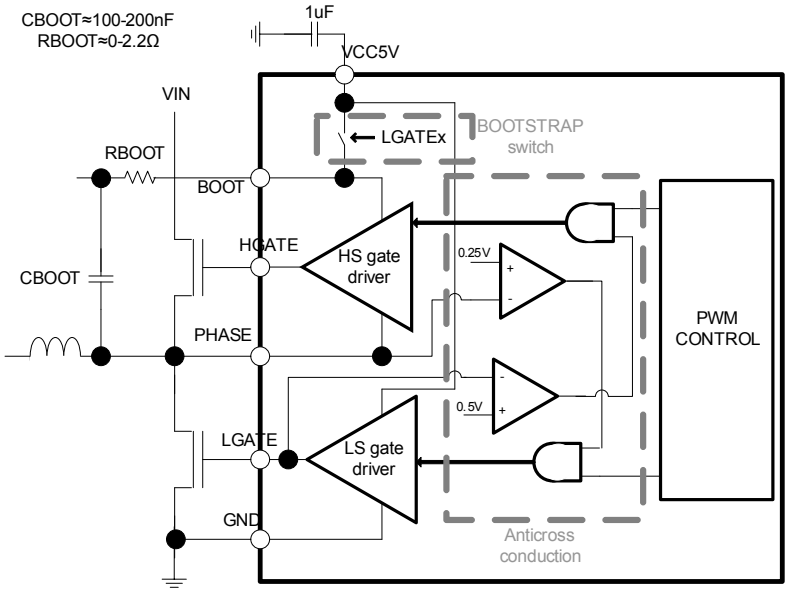
Recommended values are R_{UP} = 910 kOhm, R_{LOW} = 100 kOhm. A capacitor C_{LOW} = 22 nF in parallel to R_{LOW} is also recommended. R_{VINs} series resistance is used to program the maximum slew rate (see Table 7).

6.9.6 VCC5V monitor

When the VCC5V voltage goes lower than VCC5V UVLO falling threshold (3.8 V typ.), the controller shuts down immediately. VCC5V above the VCC5V UVLO rising threshold (4.2 V typ.) is needed to restart (refer to start-up procedure). This protection is always enabled.

6.10 Embedded gate drivers

Figure 13. **Embedded gate drivers**



The integrated high-current drivers allow the use of different power MOSFETs. High-side driver is supplied with a bootstrap circuit with an integrated bootstrap switch. The BOOT and the PHASE pins work respectively as supply and return rails for the HS driver. The VCC5V pin is the input for the supply of the low-side driver and GND is the pin used as return rail.

The PM6697H implements an anti-cross conduction protection which prevents high-side and low-side MOSFET from being on at the same time.

Place 1 uF capacitors near VCC5V pin to filter switching noise. Use 100 - 200 nF bootstrap capacitor between BOOT and the PHASE pins.

7 Mechanical data & package dimensions

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

Table 9. PM6697H mechanical data

DIM	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.0
A1	0	0.02	0.05
b	0.15	0.2	0.25
D		3.00	
D2	1.55	1.70	1.80
E		3.00	
E2	1.55	1.70	1.80
e		0.40	
k	0.15		
L	0.3	0.4	0.5
N		20	
ND		5	
NE		5	
aaa		0.07	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

Figure 14. **PM6697H package dimensions**

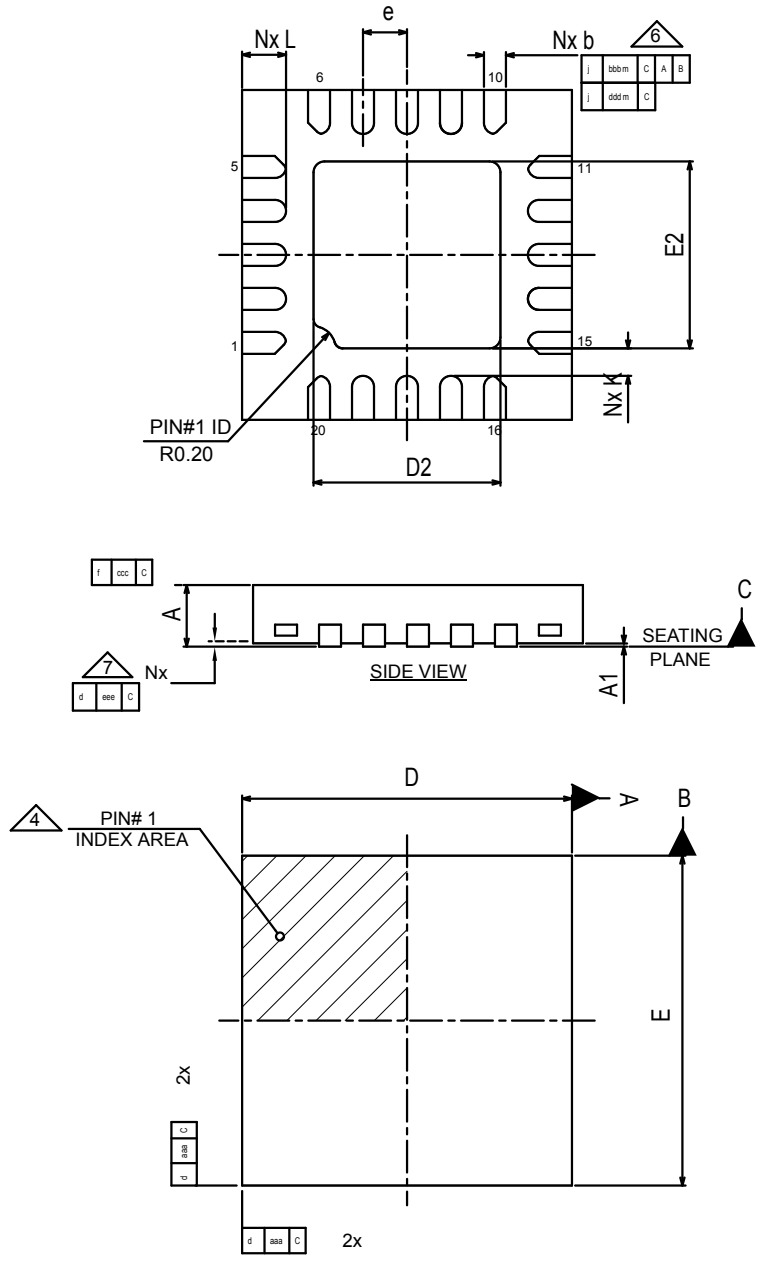
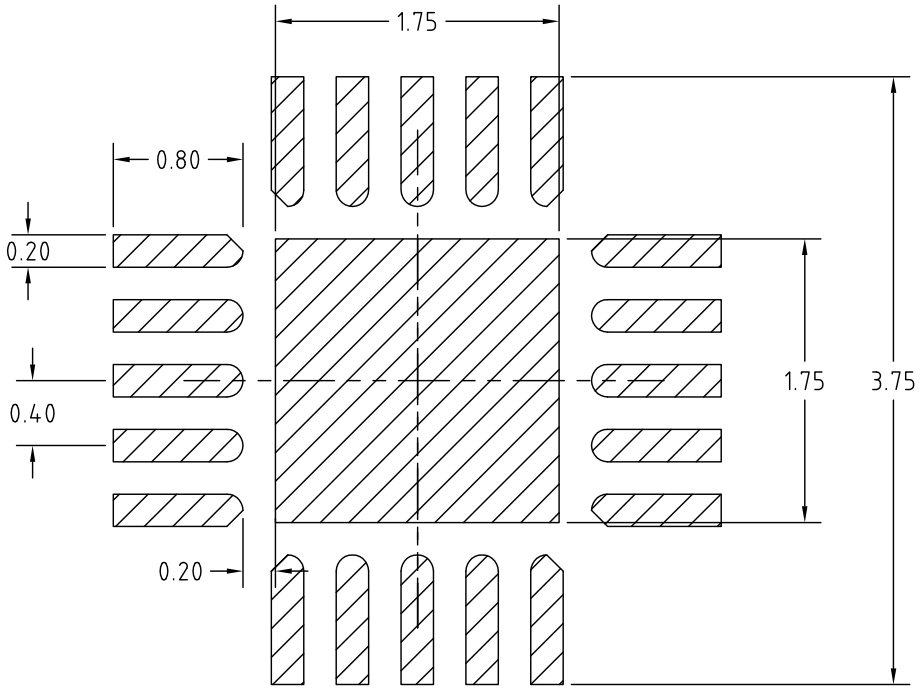


Figure 15. **PM6697H footprint recommended**



Revision history

Table 10. **Document revision history**

Date	Version	Changes
17-Jun-2014	1	Initial release
13-Mar-2017	2	Updated Applications
16-Nov-2021	3	Added Section 1 Typical application circuit and block diagram,Section 4 Electrical characteristics, and Section 7 Mechanical data & package dimensions.

Contents

List of tables

List of figures