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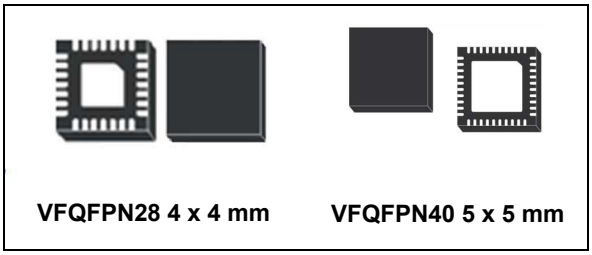
PM6766-PM6764

VR12.5™ digital multiphase controller with PMBus™

Datasheet - custom data



VFQFPN28 4 x 4 mm **VFQFPN40 5 x 5 mm**

Features

- PM6764: 4-phase compact digital controller
- PM6766: 6-phase compact digital controller
- Compliant to VR12.5 / 25 MHz SVID bus with programmable IMAX, TMAX, VBOOT, ADDRESS
- High-performance digital control loop (digital STVCOT™)
- Fully configurable through PMBus™
- Flexible driver/DrMOS support
- Single NTC design for TM, LL and IMON thermal compensation
- DPM - dynamic phase management
- Remote sense; 0.5% V_{OUT} accuracy with calibration
- Current sense across DCR with calibration
- Autocalibration capability for current and voltage sense
- Programmable voltage positioning
- OV, UV and FB disconnection protection
- Embedded non-volatile memory (NVM)
- Black box recorder
- PM6764: VFQFPN28 4 x 4 mm package
- PM6766: VFQFPN40 5 x 5 mm package

Applications

- High current power regulation for VR12.5 based Intel® based microprocessors
- DDR memory power regulation for VR12.5 based Intel® based systems

Description

The PM6764/66 is a high performance digital controller designed to power Intel's VR12.5 processors (PM6766) and memories (PM6764): all required parameters are programmable through a PMBus™ interface.

The device utilizes digital technology to implement all control and power management functions to provide maximum flexibility and performance. The NVM is embedded to store custom configurations.

The PM6764/66 features up to 4/6-phase programmable operation. The PM6764/66 supports power state transitions featuring VFDE, and programmable DPM maintaining the best efficiency over all loading conditions without compromising transient response. The device assures fast and independent protection against load overcurrent, under/overvoltage and feedback disconnections. The devices are available in VFQFPN28 4 x 4 mm (PM6764) and VFQFPN40 5 x 5 mm (PM6766) packages.

Table 1. Device summary

Order code	Package	Packing
PM6764TR	VFQFPN28 4 x 4 mm	Tape and reel
PM6766TR	VFQFPN40 5 x 5 mm	Tape and reel

Contents

1 Typical application circuit and block diagram

1.1 Application circuit

Figure 1. Typical PM6764 phase application circuit

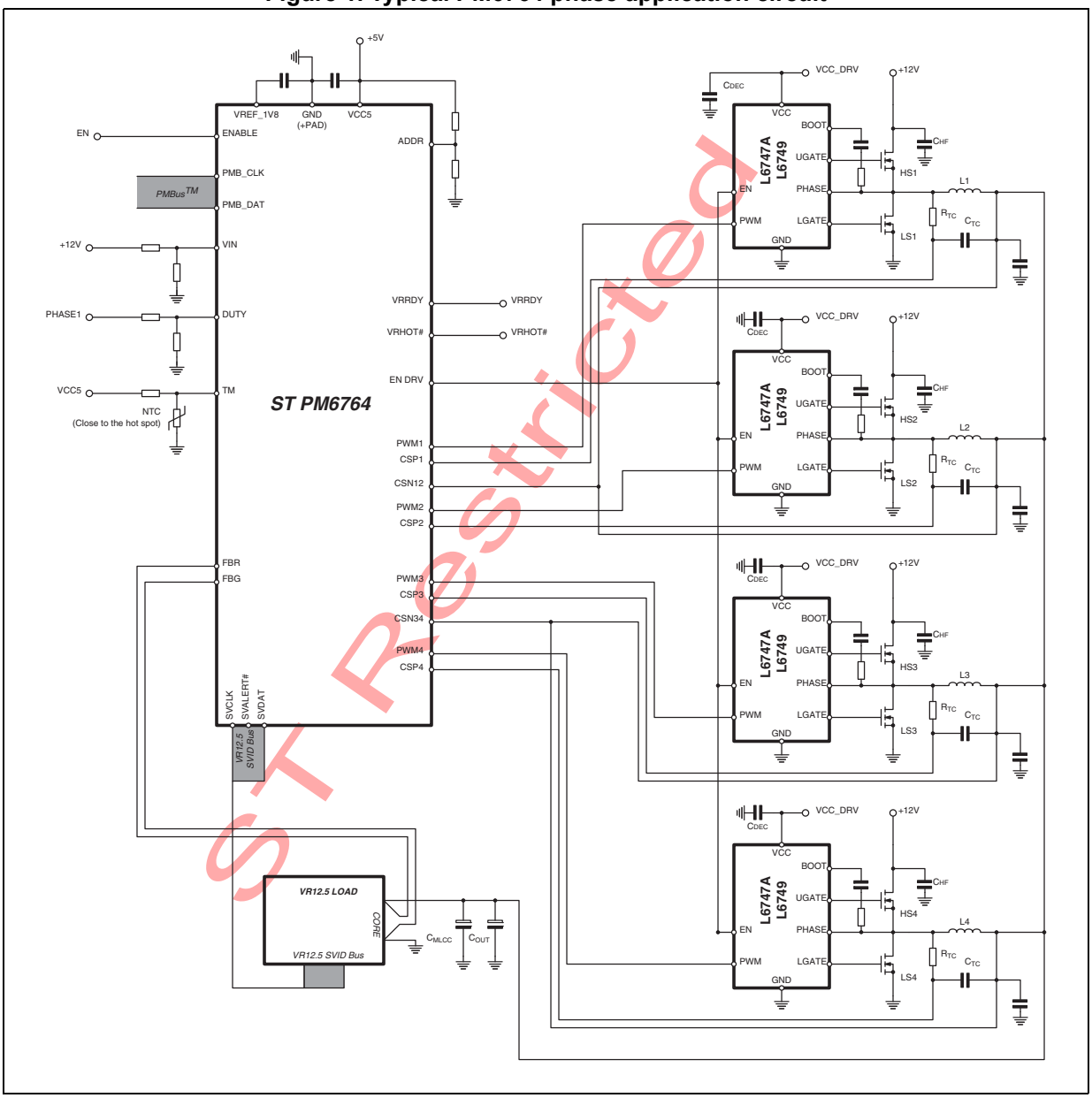
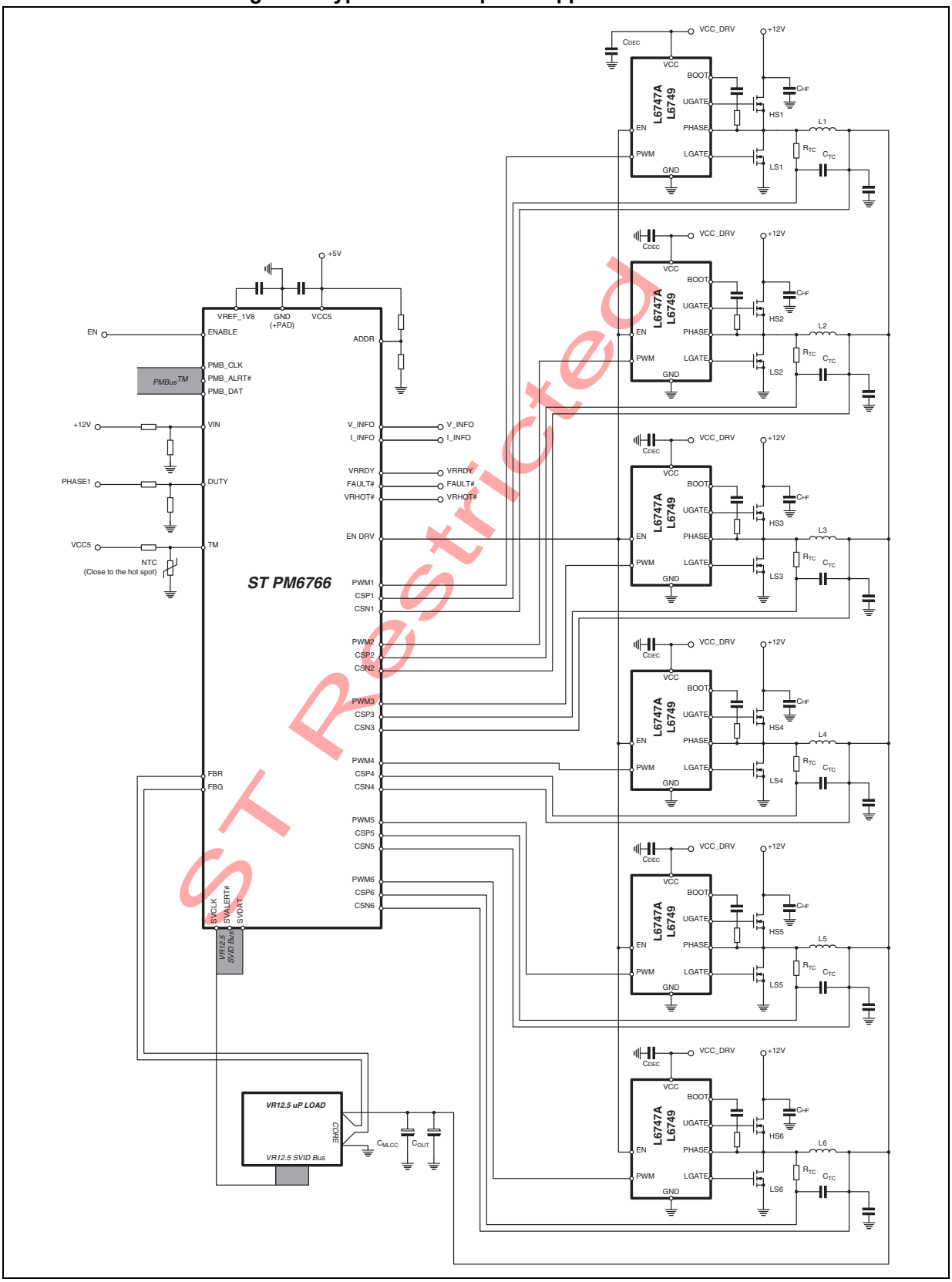


Figure 2. Typical PM6766 phase application circuit



1.2 Block diagram

Figure 3. PM6766 block diagram

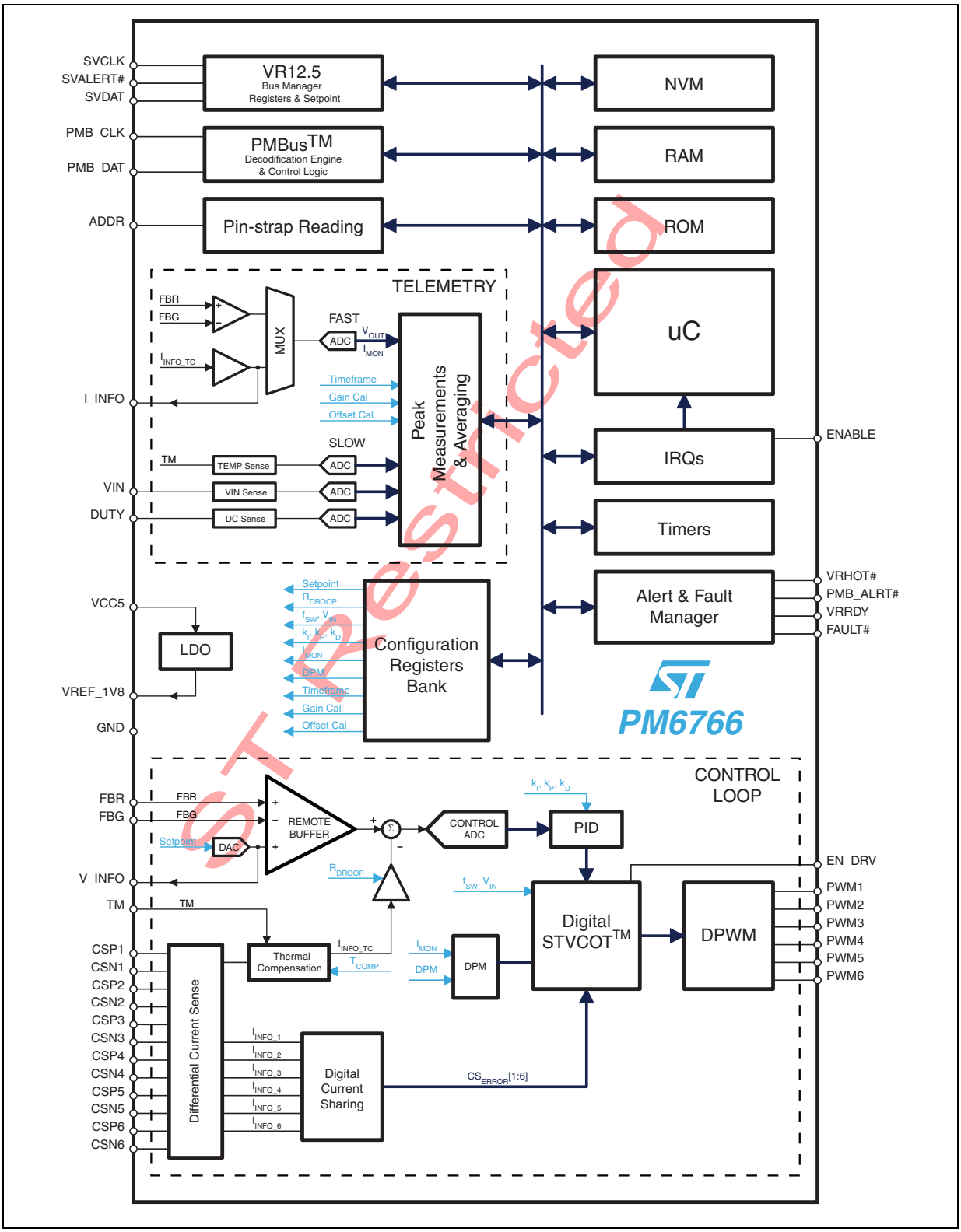
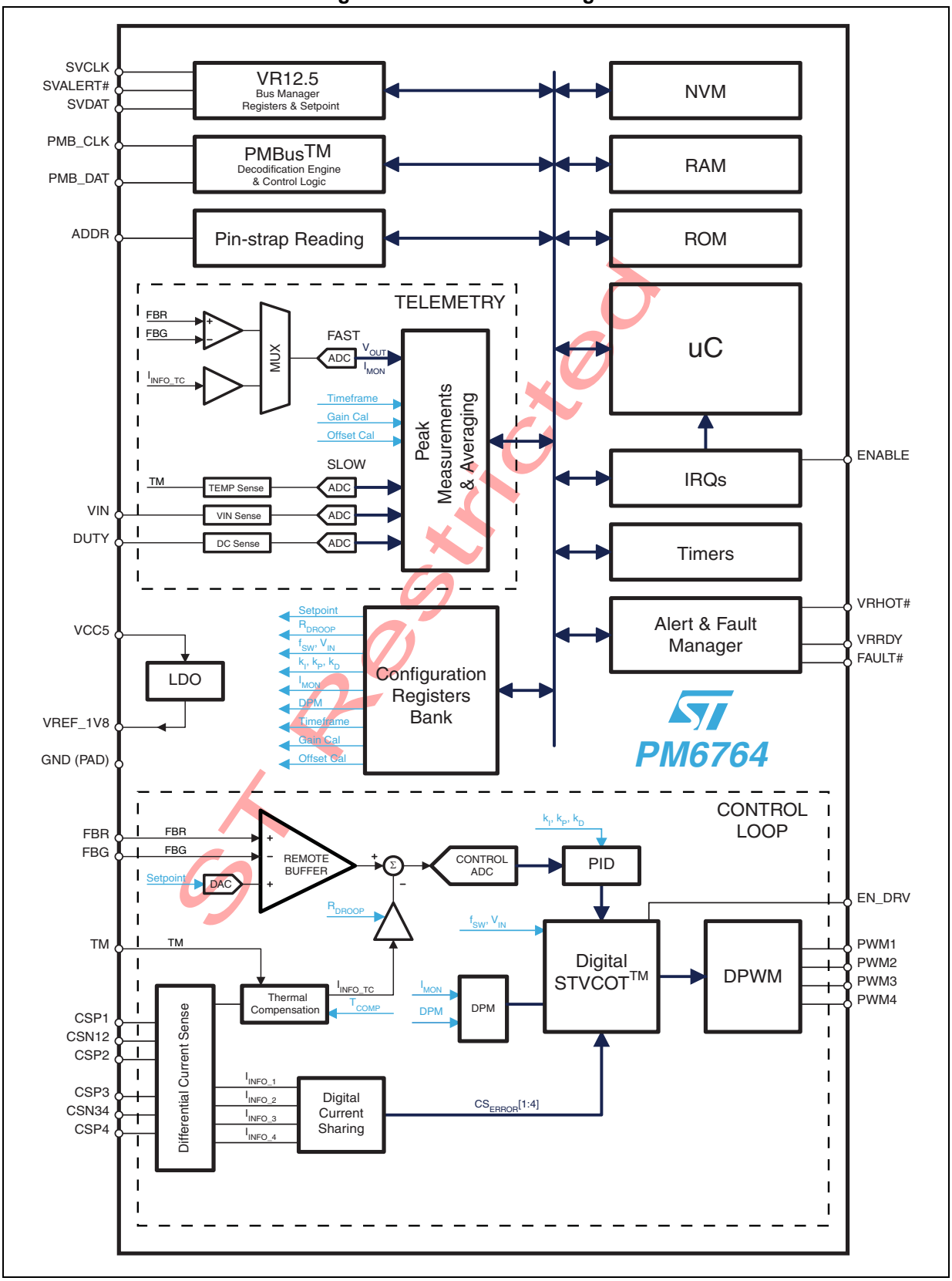
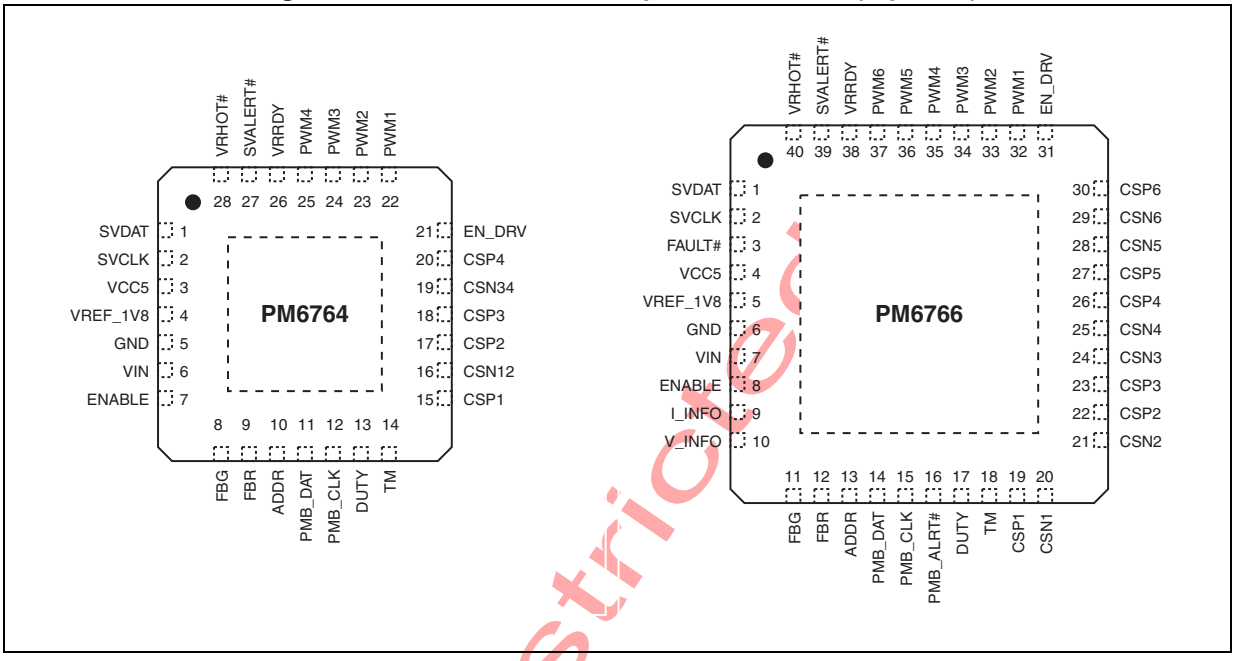


Figure 4. PM6764 block diagram



2 Pin description and connection diagrams

Figure 5. PM6764 and PM6766 pin connections (top view)



2.1 Pin descriptions

Table 2. Pin description

Pin no.		Name	I/O	Type	Function
PM6766	PM6764				
1	1	SVDAT	I/O	Open drain	VR12.5 bus serial data. Pull-up to an external voltage equal or lower than VREF_1V8.
2	2	SVCLK	I	Analog	VR12.5 bus serial clock. Pull-up to an external voltage equal or lower than VREF_1V8.
3	N/A	FAULT#	O	Open drain	Programmable fault indicator. Pulled low when triggering any selected fault. See *Section 6 on page 31* for details. Pull-up to an external voltage equal or lower than VCC5, if not used it can be left floating.
4	3	VCC5	I	Supply	Main IC analog power supply. Operative voltage is 5 V ± 5%. Filter with 1 µF MLCC to GND (typ.).
5	4	VREF_1V8	--	Internal supply	Main IC digital power supply (LDO output). It is the output of the internal LDO generating 1.8 V to supply the digital portion of the IC. Filter with 0.1 µF MLCC to GND (typ.).

Table 2. Pin description (continued)

Pin no.		Name	I/O	Type	Function
PM6766	PM6764				
6	5	GND	--	Ground	GND connection. All internal references and logic are referenced to this pin. Filter to VCC5 and VREF_1V8 with the proper MLCC capacitor and connect to the PCB GND plane.
7	6	VIN	I	Analog	Input voltage monitor. Connect to the input voltage monitor point through a divider R_{VUP} / R_{VDWN} to perform VIN sense through PMBus™ (R_{UP} = 121 kΩ; R_{DOWN} = 10.7 kΩ typ.).
8	7	ENABLE	I	CMOS	Level sensitive enable pin (3.3 V compatible). Pull-low to disable the device, pull-up above the turn-on threshold to enable the controller.
9	N/A	I_INFO	O	Analog	Total output current monitor (thermally compensated). This pin is only for monitoring purposes, leave it floating or read with at least 1 MΩ impedance.
10	N/A	V_INFO	O	Analog	Output voltage setpoint monitor. This pin is only for monitoring purposes, leave it floating or read with at least 1 MΩ impedance.
11	8	FBG	I	Analog	Remote ground sense. Connect to the negative side of the load to perform remote sense.
12	9	FBR	I	Analog	Remote buffer positive sense. Connect to the positive side of the load to perform remote sense. An anti-aliasing filter embedded.
13	10	ADDR	I	Analog	Connect a resistor divider to VCC5/GND in order to define PMBus™ and VR12.5 addressing. See *Section 4.1 on page 16* for details.
14	11	PMB_DAT	I/O	Open drain	PMBus™ data. Pull-up to an external voltage equal or lower than VCC5.
15	12	PMB_CLK	I	CMOS	PMBus™ clock. Pull-up to an external voltage equal or lower than VCC5.
16	N/A	PMB_ALRT#	O	Open drain	PMBus™ alert. Pull-up to an external voltage equal or lower than VCC5.
17	13	DUTY	I	Analog	Duty cycle detection. Connect through the resistor divider to the multiphase channel 1 switching node. The voltage on this pin must be equal or lower than VCC5.

Table 2. Pin description (continued)

Pin no.		Name	I/O	Type	Function
PM6766	PM6764				
18	14	TM	I	Analog	Thermal monitor sensor. Connect with the proper network the embedding NTC to the multiphase power section. The IC senses the power section temperature and uses the information to define the VR_HOT signal and temperature monitoring. By programming the proper TCOMP gain through the PMBus™, the IC also implements the load line and IMON thermal compensation. The voltage on this pin must be equal or lower than VCC5. Pull-up to VCC5 with 1 kΩ to disable the thermal sensor. See *Section 5.5 on page 26* for details.
19	15	CSP1	I	Analog	Channel 1 current sense positive input. Connect through an R-C filter to the phase-side of the channel 1 inductor.
20	16	CSN1	I	Analog	Channel 1 current sense negative input. Connect to the output-side of the channel 1 inductor. Filter with 100 nF (typ.) to GND. In the PM6764, the connection is shared with the channel 2 (CSN12).
21		CSN2	I	Analog	Channel 2 current sense negative input. Connect to the output-side of the channel 2 inductor. Filter with 100 nF (typ.) to GND. In the PM6764, the connection is shared with the channel 1 (CSN12).
22	17	CSP2	I	Analog	Channel 2 current sense positive input. Connect through an R-C filter to the phase-side of the channel 2 inductor.
23	18	CSP3	I	Analog	Channel 3 current sense positive input. Connect through an R-C filter to the phase-side of the channel 3 inductor. When working at < 3-phase, short to the regulated voltage.
24	19	CSN3	I	Analog	Channel 3 current sense negative input. Connect to the output-side of the channel 3 inductor. Filter with 100 nF (typ) to GND. In the PM6764, the connection is shared with the channel 4 (CSN34).
25		CSN4	I	Analog	Channel 4 current sense negative input. Connect to the output-side of the channel 4 inductor. Filter with 100 nF (typ.) to GND. In the PM6764, the connection is shared with the channel 3 (CSN34).
26	20	CSP4	I	Analog	Channel 4 current sense positive input. Connect through an R-C filter to the phase-side of the channel 4 inductor. When working at < 4-phase, short to the regulated voltage.

Table 2. Pin description (continued)

Pin no.		Name	I/O	Type	Function
PM6766	PM6764				
27	n/a	CSP5	I	Analog	Channel 5 current sense positive input. Connect through an R-C filter to the phase-side of the channel 5 inductor. When working at < 5-phase, short to the regulated voltage.
28	n/a	CSN5	I	Analog	Channel 5 current sense negative input. Connect to the output-side of the channel 5 inductor. Filter with 100 nF (typ.) to GND.
29	n/a	CSN6	I	Analog	Channel 6 current sense negative input. Connect to the output-side of the channel 6 inductor. Filter with 100 nF (typ.) to GND.
30	n/a	CSP6	I	Analog	Channel 6 current sense positive input. Connect through an R-C filter to the phase-side of the channel 6 inductor. When working at < 6-phase, short to the regulated voltage.
31	21	EN_DRV	O	CMOS	Enable driver. CMOS output driven high when the IC commands the drivers. Used in conjunction with the HiZ window on the PWMx pins to optimize the overall efficiency. Connect directly to the external driver enable pin.
32	22	PWM1	O	Tristate	PWM output. Connect to related external driver PWM input. During normal operations the device is able to manage HiZ status by setting and holding the PWMx pin to fixed voltage defined before.
33	23	PWM2	O	Tristate	
34	24	PWM3	O	Tristate	
35	25	PWM4	O	Tristate	
36	n/a	PWM5	O	Tristate	
37	n/a	PWM6	O	Tristate	
38	26	VRRDY	O	Open drain	VR ready. Set free after SS has finished and pulled low when triggering any protection. Pull-up to an external voltage equal or lower than VCC5. If not used it can be left floating.
39	27	SVALERT#	O	Open drain	VR12.5 bus alert. Pull-up to an external voltage equal or lower than VREF_1V8.
40	28	VRHOT#	O	Open drain	Voltage regulator HOT. This is an alarm signal asserted by the controller when the temperature sensed through the TM pin exceeds TMAX (active low). Pull-up to an external voltage equal or lower than VCC5. See *Section 5.5.1 on page 27* for details.
PAD	PAD	GND			GND connection. All internal references and logic are referenced to this pin. Filter to VCC5 and VREF_1V8 with the proper MLCC capacitor and connect to the PCB GND plane.

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{THJA}	PM6766 - thermal resistance junction to ambient (device soldered on demonstration board)	35	°C/W
	PM6764 - thermal resistance junction to ambient (device soldered on demonstration board)	40	
R_{THJC}	Thermal resistance junction to case	2	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction temperature range	0 to 125	°C

3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings(1)

Symbol	Notes	Value	Unit
VCC5		-0.3 to 7	V
VREF_1V8	(2)	-0.3 to 2.1	V
SVDAT, SVCLK	(3)	-0.3 to 2.1	V
CSPx, CSNx	(2), (4)	-0.3 to 2.5	V
VIN, ENABLE, ADDR, PMB_DAT, PMB_CLK, DUTY, TM, VRHOT#	(2)	-0.3 to 7	V

1. All voltages referenced to GND unless otherwise specified.
2. Need to be lower than VCC5 under any condition.
3. Need to be lower than VREF_1V8 under any condition.
4. Max. differential voltage to be limited within 100 mV.

Table 5. Recommended operative conditions(1)

Symbol	Parameter	Value	Unit
VCC5		5 +/- 10%	V
VID (max)	Programmed	2.3	V

1. All voltages referenced to GND unless otherwise specified.

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. These are stress ratings only and functional operation of the device at these conditions is not implied. Operating outside maximum recommended conditions for extended periods of time may impact product reliability and result in device failures.

3.2 Electrical characteristics

Table 6. Electrical characteristics

(VCC5 = 5 V, Tamb = 25 °C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
Supply current and power-on						
VCC5	Supply current			60		mA
	UVLO turn-on	VCC5 rising			4.2	V
	UVLO turn-off	VCC5 falling	3.5			V
VREF_1V8	Voltage accuracy		1.760		1.860	V
	Load regulation	I = 50 mA	25		55	mV
	Current capability				50	mA
Enable						
ENABLE	Input high voltage	ENABLE voltage rising			0.7	V
	Input low voltage	ENABLE voltage falling	0.4			V
	Leakage current	V_{EN} = 1.1 V			1	µA
SVI serial bus						
SVCLK, SVDAT	Input high voltage		0.65			V
	Input low voltage				0.45	V
SVALERT#	Output low voltage	I_{SINK} = 5 mA			125	mV
PMBus™						
PMB_CLK, PMB_DAT	Input high voltage		1.75			V
	Input low voltage				1.45	V
PMB_ALRT#	Output low voltage	I_{SINK} = 5 mA			70	mV
Reference and ADC						
k_{VID}	V_{OUT} setpoint accuracy	FBR to V_{CORE}, FBG to GND_{CORE}; VID = 1.50 V to 2.30 V	-0.5	-	0.5	%
		FBR to V_{CORE}, FBG to GND_{CORE}; VID = 1.00 V to 1.49 V	-8	-	8	mV
		FBR to V_{CORE}, FBG to GND_{CORE}; VID < 0.99 V	-10	-	10	mV
k_{DROOP}	LL Accuracy MFR_VOUT_LL = 0x4D	V_{OUT} error; I_{LOAD} = 0 A;	-6.5	-	6.5	mV
		N_{PH} = 6; VCSNx - VCSPx = 10 mV	1.00	1.05	1.10	-
		N_{PH} = 4; VCSNx - VCSPx = 10 mV	1.07	1.13	1.19	-

Table 6. Electrical characteristics (continued)
(VCC5 = 5 V, Tamb = 25 °C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit

I_{MON} ADC	GetReg(15h)	N_{PH} = 6, (VCSPx-VCSNx) = 10 mV
		`IMON = 0x08,`
		`TEL_IOUTMAX = 0xFF,`
		`MFR_IOUT_CAL_GAIN = 0xB4`
		`IOUT_CAL_OFFSET = 0xF72A`
			C2	C8	CE	Hex

	GetReg(15h)	N_{PH} = 4, (VCSPx-VCSNx) = 8 mV
		`IMON = 0x16,`
		`TEL_IOUTMAX = 0xCA,`
		`MFR_IOUT_CAL_GAIN = 0x9C,`
		`IOUT_CAL_OFFSET = 0xF750`
			47	4A	4D	Hex

VIN ADC	`READ_VIN`	Accuracy; VIN = 1 V	11.9	12.3	12.7	V
DUTY ADC	`READ_DUTY_CYCLE` accuracy	DUTY = 25%	-1		1	%
DVID	Slew rate fast, min	`DVID_SR_FAST_STEP = 0x0A`		20		mV/µs
	Slew rate slow, min	`DVID_SR_SLOW_STEP = 0x28`		5		mV/µs
k_{CK}	Time base accuracy		-5		5	%
PWM outputs and ENDRV						
HiZ	PWM high impedance	`PWM_HIZ = 0x00`	1.35	1.40	1.45	V
		`PWM_HIZ = 0x01`	1.55	1.60	1.65	V
EN_DRV	Voltage low	I_{ENDRV} = -4 mA			0.4	V
Protections						
OVP	Overvoltage protection	(FBR-FBG) rising; above setpoint	350		450	mV
FBR DISC	FBR disconnection	V_{CSN1} rising, above (FBR-FBG)		700		mV
FBG DISC	FBG disconnection	Remote buffer output, above FBR		700		mV
V_{OC_TOT}	OC threshold, CSPx - CSNx	N = 6; `IMON = 0x06`	17.1	21.4	25.7	mV
		N = 4; `IMON = 0x09`				
VRRDY	Output low voltage	I_{SINK} = 4 mA			110	mV
VRHOT#	Output low voltage	I_{SINK} = 4 mA			75	mV
FAULT#	Output low voltage	I_{SINK} = 4 mA			150	mV

4 Device configuration and pin strapping tables

The full digital architecture of the PM6766 and PM6764 devices allow to configure the behavior of the control loop, the power management and the fault handling. The configuration is stored in the embedded non-volatile memory (NVM) and can be modified using the PMBus™ and VR12.5 interfaces.

The PM6764, PM6766 devices are fully compliant with the PMBus™ specification part I and part II, revision 1.2 *(www.pmbus.org)*. Devices are fully compatible with the PMBus™ specification for read/write access in the byte, word, block mode.

The PM6764, PM6766 devices are fully compliant with the Intel® VR12.5 SVID protocol Rev1.2, document # 453513. To guarantee proper device and CPU operations, refer to this document for bus design and layout guidelines. Different platforms may require different pull-up impedance on the SVI bus. Impedance matching and spacing between SVDAT, SVCLK, and SVALERT# must be followed.

4.1 Device address configuration

The PMBus™ and the VR12.5 slave addresses are configured at the startup of the device by reading the voltage on the ADDR pin. The proper resistor divider must be connected from the ADDR pin to the GND and VCC5 pins (see *Figure 1 on page 4* and *Figure 2 on page 5*) as per *Table 7*.

Table 7. PM6764, PM6766 address pin-strap

R_{UP} [kΩ]	R_{DOWN} [kΩ]	PM6764		PM6766	
		PMBus™ address	VR12.5 address	PMBus™ address	VR12.5 address
12	13	0xE0	0x02	0xC0	0x00
10	12	0xE4			
5.6	7.5	0xE8			
4.3	6.8	0xEC			
4.7	8.2	0xE2	0x04	0xC4	
3.9	8.2	0xE6			
5.1	12	0xEA			
4.3	12	0xEE			
6.8	22	0xD0	0x06	0xC8	
5.6	22	0xD4			
4.7	22	0xD8			
3.6	22	0xDC			
2.7	22	0xD2	0x08	0xCC	
1.8	22	0xD6			
1	22	0xDC			
0	Open	0xDE			

4.2 Non-volatile memory

The PM6764, PM6766 devices have an on-board non-volatile memory that allows storing the actual configuration of the device. Furthermore, additional user data can be stored into the NVM using USER_DATA_00 and USER_DATA_01 commands (see *Table 14 on page 37*). Storing/restoring the configuration data to/from the memory is performed by the single standard PMBus™ command STORE/RESTORE_DEFAULT_ALL. Any unintended writing can be prevented using the write protection capability enabled by the custom MFR_PROTECT_DEFAULT command.

During the design and the fine-tuning of the application, using the PM6764/66 graphical user interface, each configuration written into the device is uniquely identified by:

- An incremental revision number, MFR_PMBUSCFG_REVISION custom command
- A digital timestamp in ISO 8601:2004 format (YYYYMMDDHHMM), MFR_PMBUSCFG_TIMESTAMP_L&H custom commands
- A user ID identifier, MFR_PMBUSCFG_USERID custom command

The embedded NVM is also used to store the status of the device when a critical fault occurs (black box recorder function).

Memory cells are qualified for 1000 read/erase/write cycles and 5 years at 85 °C data retention.

4.3 Device initialization and startup

When power supply voltage greater than the UVLO threshold is applied to the device, the steps illustrated in the diagram of *Figure 6* are performed.

As soon as the supply voltage on the pin VCC5 is greater than the UVLO, the analog circuitry is started and stabilized and all the digital blocks are initialized.

Then, the voltage on the pin ADDR is read and both the PMBus™ and the VR12.5 slave addresses are calculated as per *Table 7*.

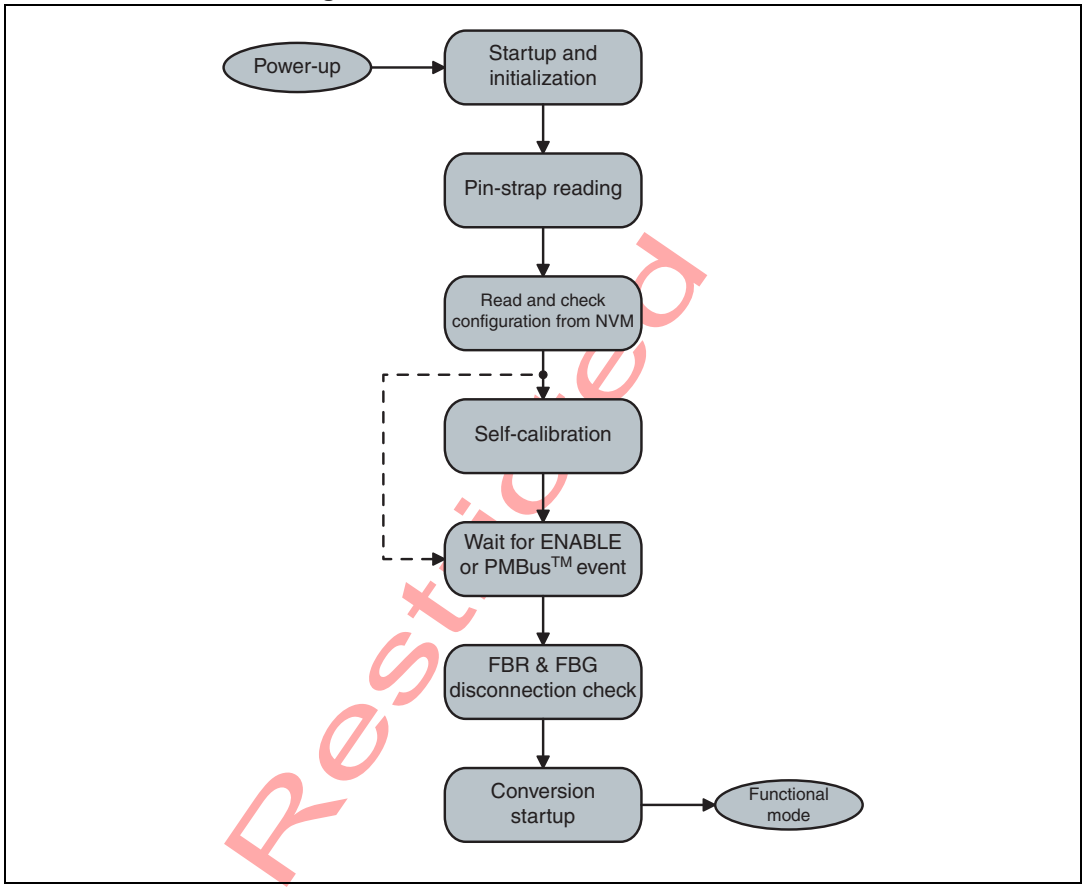
At this stage, the configuration of the device is read from the embedded NVM and written to the operating (volatile) memory. In order to ensure the validity of the current configuration, thus avoiding dangerous operating conditions, a CRC check is performed over the whole content of the non-volatile memory. If any error is detected, the power conversion is not started and the status flag "*Memory fault detected*" in the STATUS_CML register is set.

The self-calibration nulls out any error due to the residual offsets in the output voltage and in the output current readings, resulting in improved voltage positioning and current telemetry accuracies. This procedure is fully automated and does not require neither intervention by the user, nor additional external components. If desired, the self-calibration can be disabled by setting the corresponding parameter in the configuration of the device.

The conversion startup can now be requested asserting the ENABLE pin, sending the PMBus™ command OPERATION or configuring the device to the startup regardless of the previous two events. During the startup sequence, a feedback disconnection check is performed. In order to prevent possible damage to the load, the device checks if the FBR or the FBG pins are not connected to the output stage of the converter. In this case, the power conversion is stopped and the "*FB disconnection*" flag in the STATUS_MFR_SPECIFIC register is set.

After the completion of the soft-start, the device is fully functional and is able to manage any command sent via the PMBus™ or VR12.5 digital interfaces.

Figure 6. Device initialization flowchart



4.4 Device configuration

The PM6764/66 devices have a dedicated system register, stored in the NVM memory, to customize the device behavior for each specific application. These registers can be programmed using dedicated PMBus™ commands. The main functions of system registers are:

- Program the IMON resistor to define the overcurrent threshold (see *Section 6.1.2 on page 33*)
- Program the HiZ levels for HiZ on PWMx guaranteeing flexibility in driving different external drivers as well as the DrMOS ICs
- Program the DVID optimization features (See *Section 5.7 on page 29*)
- Program the BOOT voltage
- Program the thermal compensation of the monitored output current (See *Section 5.5.2 on page 27* and following)
- Program the power managements features like phase numbers, phase shedding behavior and light load efficiency optimizations
- Calibration of the monitored input and output rails

The list of supported registers is detailed in *Table 8*.

Table 8. System registers

Register	Address	Data bytes	Description
Application setup			
IMON	0x00B002	1	Used to change the current monitoring resistor. See *Section 6.1.2 on page 33*. $IMON[7:0] = R_{IMON} \cdot \frac{63}{95984}$
PWM_HIZ	0x00B004	1	Used to set the voltage of the PWMx when in the hi-impedance state (HiZ). The supported values are: 0x00: 1.4 V 0x01: 1.6 V 0x02: 1.8 V 0x03: 2.0 V
TCOMP	0x00B005	1	Used to thermally compensate the device. See *Section 5.5 on page 26*.
VR12_VBOOT	0x0200DA	1	Used to set the BOOT voltage.
DVID_OPT_PARAM	0x00B00F to 0x00B014	6	Used to set the DVID optimization parameters. See *Section 5.6 on page 28*.
Power management			
PFM_ENA_PS	0x00B006	1	Used to enable the PFM working mode vs. power states (PSx). The supported values are: 0x00: PFM disabled 0x01: PFM enabled in PS0 only 0x02: PFM enabled in PS1 only 0x03: PFM enabled in PS1, PS0 0x04: PFM enabled in PS2 only 0x05: PFM enabled in PS2, PS0 0x06: PFM enabled in PS2, PS1 0x07: PFM enabled in PS2, PS1, PS0 0x08: PFM enabled in PS3 only 0x09: PFM enabled in PS3, PS0 0x0A: PFM enabled in PS3, PS1 0x0B: PFM enabled in PS3, PS1, PS0 0x0C: PFM enabled in PS3, PS2 0x0D: PFM enabled in PS3, PS2, PS0 0x0E: PFM enabled in PS3, PS2, PS1 0x0F: PFM enabled in PS3, PS2, PS1, PS0
DISABLE_OCP	0x00B007	1	Used to enable [0x00] or disable [0x01] the HW OCP fault detection.
DPM_HYSTERESIS	0x00B008	1	Used to set the dynamic phase management current hysteresis [A].
DPM_NPH_PS0	0x00B009	1	Used to set the nominal number of active phases in PS0 when DPM is enabled.

Table 8. System registers (continued)

Register	Address	Data bytes	Description
DPM_NPH_PS1	0x00B00A	1	Used to set the nominal number of active phases in PS1 when DPM is enabled.
DPM_NPOP	0x00B00B	1	Used to set the number of phases populated on the board.
DISABLE_OVP	0x00B00C	1	Used to enable [0x00] or disable [0x01] the HW OVP fault detection.
EN_PGOOD	0x00B015	1	Used to enable [0x00] or disable [0x01] the PGOOD pin output.
EN_VRRDY	0x00B016	1	Used to enable [0x00] or disable [0x01] the VRRDY pin output.
Monitoring calibration			
TEL_IOUT_EXP	0x00B019	1	Used to set the output current readings exponent.
TEL_IIN_GAIN	0x00B01A	1	Used to set the input current readings gain correction.
TEL_PIN_GAIN	0x00B01B	1	Used to set the input power readings gain correction.
TEL_POUT_GAIN	0x00B01C	1	Used to set the output power readings gain correction.
TEL_VIN_GAIN	0x00B01D	1	Used to set the input voltage readings gain correction.
TEL_IOUT_MAX	0x00B01E	1	Used to set the output current overcurrent threshold [A].
TEL_IIN_OFFSET	0x00B01F - 0x00B020	2	Used to set the input current readings offset correction [A]
TEL_PIN_OFFSET	0x00B021 - 0x00B022	2	Used to set the input power readings offset correction [W].
TEL_POUT_OFFSET	0x00B023 - 0x00B024	2	Used to set the output power readings offset correction [W].
TEL_VIN_OFFSET	0x00B025 - 0x00B026	2	Used to set the input voltage readings offset correction [V].
TEL_VIN_EXP	0x00B027	1	Used to set the input voltage readings exponent.
TEL_VOUT_EXP	0x00B028	1	Used to set the output voltage readings exponent.

4.5 Device configuration procedure

To program the system registers the following basic procedures can be used:

READ procedure

- Write the memory location address to be read using the *MFR_MEMORY_RD* PMBus™ command.
- Read the memory location addressed using the *MFR_MEMORY_WORD* PMBus™ command

WRITE procedure

- Write the data to written into the memory using the *MFR_MEMORY_WORD* PMBus™ command
- Write the memory location address to be written using the *MFR_MEMORY_WR* PMBus™ command.

See *Table 14 on page 37* for details about the *MFR_MEMORY_RD, MFR_MEMORY_WR and MFR_MEMORY_WORD commands.*

5 Device description

The PM6764, PM6766 devices are single rail controllers with a complete control logic and protections to realize a high performance step-down DC-DC voltage regulator optimized for the advanced microprocessor and memories power supply.

The controllers are based on the high performances digital STVCOT™ architecture, allowing to have fast load transient response, linear with the load frequency sweep, while maintaining
a nearly constant switching frequency in the steady state allowing to minimize the output filter components.

The PM6764, PM6766 devices implement current reading across the inductor in the differential mode.
A sense resistor in series to the inductor can be also considered to improve reading precision. The current information read corrects the PWM output in order to equalize the average current carried by each phase.

In order to guarantee the load to be safe under all circumstances, a complete set of protection is available on the output voltage/current, input voltage/current, feedback disconnection, temperature, input/output powers and catastrophic fails.

Special power management features like DPM and VFDE modify the phase number and switching frequency to optimize the efficiency over the load range.

All the required parameters of both the control loop and power management features are programmable through dedicated PMBus™ commands.

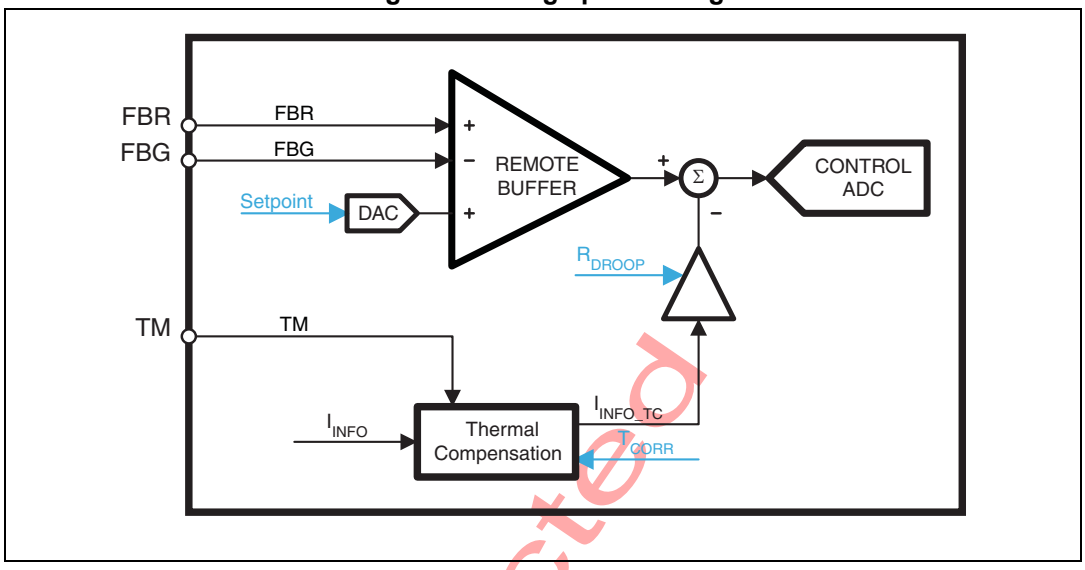
The PM6764, PM6766 devices are available in VFQFPN28 4 x 4 mm and VFQFPN40 5 x 5 mm packages.

5.1 Output voltage positioning

Output voltage positioning is performed by programming the digital control loop parameters and droop function effect (see *Figure 7*) using the dedicated PMBus™ commands (see *Section 7.1 on page 44*). The controller reads the current delivered by monitoring the voltage drop across the DCR inductors. The total current (I_{INFO}) is internally compensated vs. temperature variations (I_{INFO_TC}), converted into a direct proportional voltage using the PMBus™ programmable resistor (R_{DROOP}) and added to the remote buffer output voltage causing the output voltage to vary accordingly, thus implementing the desired load line effect. This voltage is finally converted into digital value and used by the digital control loop for the regulation.

The PM6674, PM6766 devices embed a remote-sense buffer to sense remotely the regulated voltage without any additional external components. In this way, the output voltage programmed is regulated compensating for board and socket losses. Keeping the sense traces parallel and guarded by a power plane results in the common mode coupling for any picked-up noise.

Figure 7. Voltage positioning



5.2 Active regulation

The PM6764/66 controllers implement the proprietary digital STVCOT™ architecture.

During operation, the output voltage is sensed differentially and digitized by a fast analog-to-digital converter (ADC). The resultant digital error signal is then fed into a digital PID compensator and then processed by the digital STVCOT™ control logic.

The output of the digital loop is converted into a PWM pulse using a digital pulse width modulator (DPWM).

The digital STVCOT™ architecture can be modeled with an equivalent analog control loop and with a single-phase converter, which only difference is the equivalent inductor L/N (where each phase has an L inductor and N is the number of the configured phases). See *Figure 8*. The user can adjust the parameter for the control loop compensation by working in the digital environment or, as more convenient, working in the corresponding analog equivalent environment.

The equivalent transfer function of the control loop is:

Equation 1

$$G_{LOOP}(s) = -GAIN \cdot \frac{Z_{OUT}(s)}{Z_{OUT}(s)+Z_L(s)} \cdot \frac{Z_F(s)}{Z_{FB}(s)} \cdot \left[1 + \frac{DCR}{R_G} \cdot \frac{R_{DROOP}(s)}{Z_{OUT}(s)}\right]$$

Where:

- $Z_{OUT}(s)$ is the impedance resulting by the parallel of the output capacitor (and its ESR) and the applied load R_O
- $Z_F(s)$, $Z_{FB}(s)$ are the compensation network impedances
- $Z_L(s)$ is the equivalent inductor impedance
- GAIN is the PWM transfer function. It is a constant value (= 4) once programmed the application input voltage (V_{IN}) in the `SYS_CONFIG` PMBus™ register, see *Table 15 on page 44*.

The analog equivalent transfer function allows to design the control loop using the analog well known techniques and then to transform them into digital coefficients using these formulas:

Equation 2

$$K_p = \frac{R_F \cdot C_F + C_I \cdot (R_I + R_{FB})}{R_{FB} \cdot (C_P + C_F)}$$

Equation 3

$$K_i = \frac{1}{R_{FB} \cdot (C_P + C_F)}$$

Equation 4

$$K_d = \frac{R_F \cdot C_F \cdot C_I \cdot R_{FB}}{R_{FB} \cdot C_F}$$

Equation 5

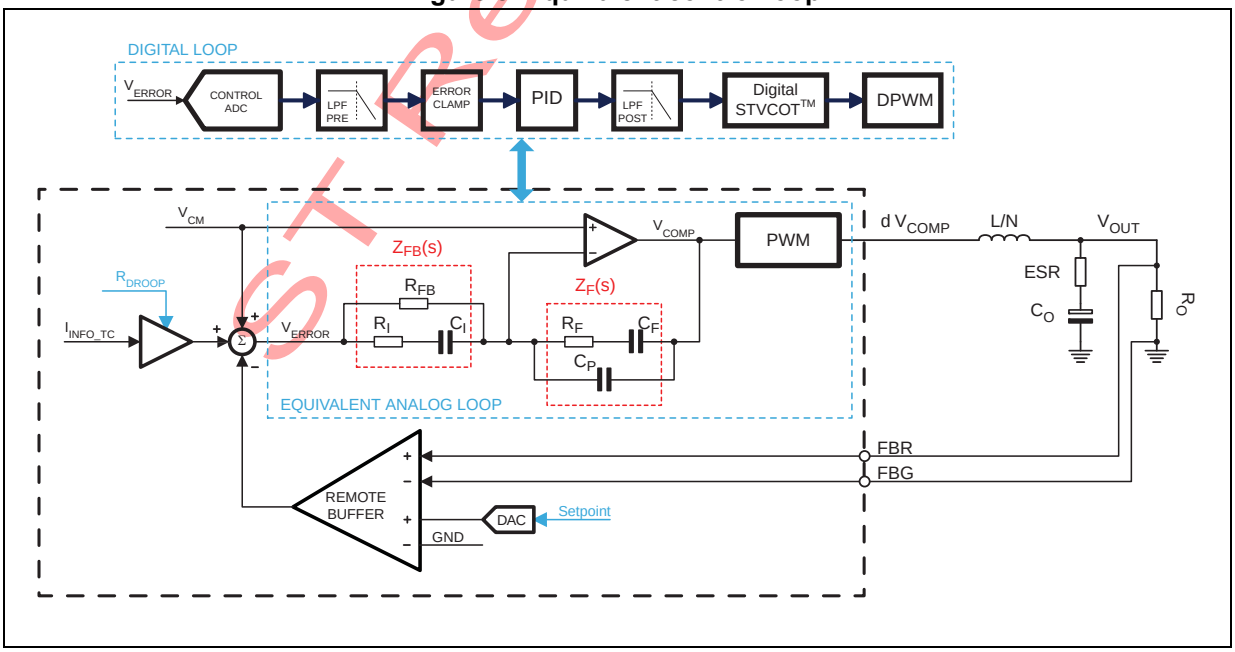
$$\tau_{PRE} = R_I \cdot C_I$$

Equation 6

$$\tau_{POST} = R_F \cdot \left(\frac{C_F \cdot C_P}{C_F + C_P}\right)$$

These coefficients are programmed into the PM6764/66 using the `MFR_PID` and `MFR_PRECONDITIONING` PMBus™ registers, see *Table 16 on page 45* and *Table 17 on page 46*.

Figure 8. Equivalent control loop.



5.3 Inductors current reading

The PM6764/66 devices embed a flexible, differential current sense circuitry that is able to read across the inductor parasitic resistance or across a sense resistor placed in series to the inductor element. The differential current reading rejects noise and allows placing the sensing element in different locations without affecting the measurement's accuracy. The transconductance ratio is issued by the internal resistor R_G = 560Ω. The current sense circuit always tracks the current information; to correctly reproduce the inductor current an R-C filtering network must be introduced in parallel to the sensing element. The current that flows from the CSNx pin is then given by the following equation (see *Figure 9*):

Equation 7

$$I_{CSNx} = \frac{DCR}{R_G} \cdot \frac{1 + s \cdot L/DCR}{1 + s \cdot R \cdot C} \cdot I_{PHASEx}$$

Considering now to match the time constant between the inductor and the R-C filter applied (time constant mismatches cause the introduction of poles into the current reading network causing instability. In addition, it is also important for the load transient response and to let the system show resistive equivalent output impedance) it results:

Equation 8

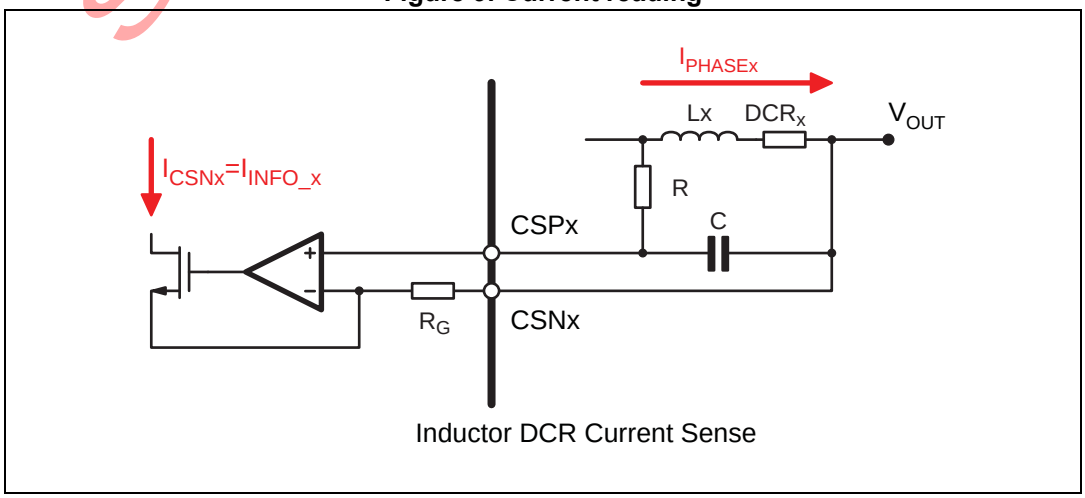
$$\frac{L}{DCR} = R \cdot C \quad \Rightarrow \quad I_{CSNx} = \frac{DCR}{R_G} \cdot I_{PHASEx} = I_{INFO\_X}$$

The current read through the CSPx / CSNx pairs is converted into a current I_{INFO_x} proportional to the current delivered by each phase and the information about the average current $I_{AVG} = \Sigma I_{INFO\_x} / N$ is internally built into the device (*N* is the number of working phases).

The error between the read current I_{INFO_x} and the reference I_{AVG} is then used to adjust the ON time of the PWMx signals in order to equalize the current carried by each phase.

The current sharing loop bandwidth can be adjusted with the `SYS_CONFIG` PMBus™ register, see *Table 15 on page 44*. It is recommended to use R resistors not exceeding 200 kΩ.

Figure 9. Current reading



5.4 Load line definition

The PM6764/66 devices introduce a dependence of the output voltage on the load current recovering a part of the drop due to the output capacitor ESR in the load transient. Introducing a dependence of the output voltage on the load current, a static error, proportional to the output current, causes the output voltage to vary according to the sensed current.

Figure 9 shows the current sense circuit used to implement the load line. The current flowing across the inductor(s) is read through the R - C filter across the CSPx and CSNx pins. The integrated R_G resistors program a transconductance gain and generate a current I_{INFO_X} proportional to the current of the phase. The sum of the I_{INFO_x} currents ($I_{INFO)}$ is first thermally compensated using TM information (I_{INFO_TM}) and then converted into a direct proportional voltage using the PMBus™ programmable resistor (R_{DROOP}). The R_{DROOP} gives the final gain to program the desired load line slope (see *Figure 7*).

Time constant matching between the inductor (L / DCR) and the current reading filter (RC) is required to implement a real equivalent output impedance of the system, so avoiding over and/or undershoot of the output voltage as a consequence of a load transient.

The output voltage characteristic vs. load current (see *Section 5.5.2* for details on thermal compensation), is then given by:

Equation 9

$$V_{OUT} = VID - R_{DROOP} \cdot I_{INFO\_TC} = VID - R_{DROOP} \cdot \frac{DCR}{R_G} \cdot I_{OUT} = VID - R_{LL} \cdot I_{OUT}$$

Where R_{LL} is the resulting load line resistance implemented by the device. The R_{DROOP} resistor can be then designed according to the R_{LL} specifications as follow:

Equation 10

$$R_{DROOP} = R_{LL} \cdot \frac{R_G}{DCR}$$

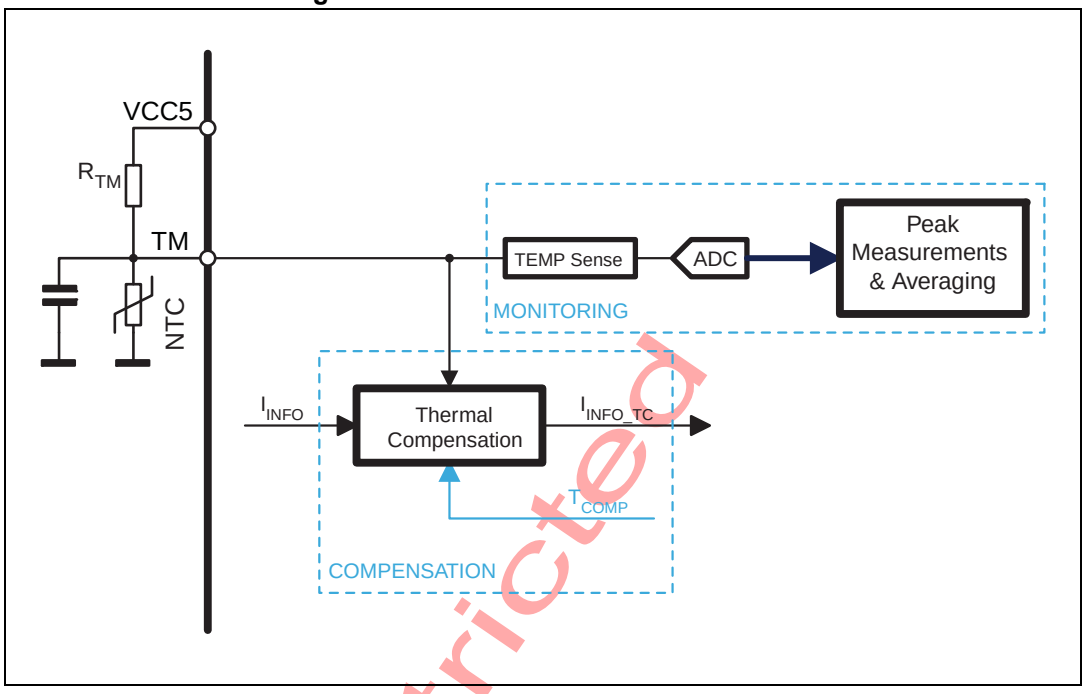
The digital droop function is programmed into the PM6764/66 using the `MFR_VOUT_LL` PMBus™ register, see *Table 14 on page 37*.

5.5 Thermal monitor and compensation

The PM6764/66 devices feature a single NTC for thermal sensing for both thermal monitoring and compensation (see *Figure 10*), allowing to optimize the overall application cost without compromising the performances:

- The thermal monitor consists in monitoring the converter temperature eventually reporting alarm by asserting the VR_HOT signal. This is the base for the temperature reporting.
- Thermal compensation consists in compensating the inductor DCR derating with temperature so preventing drifts in any variable correlated to the DCR: voltage positioning, overcurrent and current reporting.

Figure 10. Thermal monitor connections



5.5.1 Thermal monitor and VR_HOT

The diagram for the thermal monitor is reported in *Figure 10*. The NTC should be placed close to the power stage hotspot in order to sense the regulator temperature. As the temperature of the power stage increases, the NTC resistive value decreases, so reducing the voltage observable at the TM pin.

A recommended NTC is the NTHS0805N02N6801HE for accurate temperature sensing and thermal compensation. A different NTC may be used: to reach the requested accuracy in temperature reporting, a proper resistive network must be used in order to match the resulting characteristic with the one coming from the recommended NTC; furthermore the internal look up table (LUT) can be reprogrammed using custom PMBus™ commands.

The voltage observed at the TM pin is internally converted and then used for the temperature reporting. When the temperature observed on the thermal sensors exceeds TMAX (programmed using the dedicated PMBus™ command), the PM6764/66 devices assert VR_HOT (active low as long as the overtemperature event lasts).

5.5.2 Thermal compensation

The PM6764/66 devices support DCR sensing for output voltage positioning: the same current information used for voltage positioning is used to define the overcurrent protection and the current reporting. Having imprecise and temperature dependent information leads to violation of the specification and misleading information: a positive thermal coefficient specific from the DCR needs to be compensated to get stable behavior of the converter as temperature increase. Uncompensated systems show temperature dependencies on the regulated voltage, overcurrent protection and current reporting.

The same temperature information available on the TM pin used for the thermal monitor is also used for this purpose, see *Figure 10*. The voltage on the TM pin is compensated changing the T_{COMP} digital value using the dedicated PMBus™ commands, allowing to

correct the I_{INFO} current used for voltage positioning (see *Section 5.4*) thus recovering the DCR temperature deviation.

Equation 11

$$I_{INFO\_TC} = I_{INFO} \cdot k_{TC}$$

Where K_{TC} is a function of T_{COMP}.

Depending on the NTC location and distance from the inductors and the available airflow, the correlation between NTC temperature and DCR temperature may be different.

T_{COMP} adjustment allows to modify the gain between the sensed temperature and the correction made upon the I_{INFO} current. Set T_{COMP} value to 0 to disable the thermal compensation (no correction is given and $I_{DROOP\_TC} = I_{DROOP}$).

5.5.3 Thermal compensation design

To thermally compensate the device use this procedure:

1. Choose the resistive network to be connected to the TM pin in order to have a voltage equal to 4 V when ambient temperature is equal to 25 °C.
2. Power on the converter and load the thermal design current (TDC) with the desired cooling conditions. Record the output voltage regulated as soon as the load is applied.
3. Wait for the thermal steady state. Adjust the T_{COMP} value in order to get the same output voltage recorded at the point no. 2.

5.6 Dynamic VID transition support

The PM6764/66 manages dynamic VID transitions that allow the output voltage to modify during normal device operation for power management purposes. OV, UV and OC signals are masked during every DVID transition and they are reactivated with proper delay to prevent from false triggering.

When changing dynamically the regulated voltage (DVID), the system needs to charge or discharge the output capacitor accordingly. This means that an extra-current I_{DVID} needs to be delivered (especially when increasing the output regulated voltage) and it must be considered when setting the overcurrent threshold of both sections. This current results:

Equation 12

$$I_{DVID} = C_{OUT} \cdot \frac{dV_{OUT}}{dT_{VID}}$$

where dV_{OUT} / dT_{VID} depends on the specific command issued (20 mV/µsec. for `SetVID_Fast` and 5 mV/µsec. for `SetVID_Slow`).

As soon as the controller receives a new valid command to set the VID level, the setpoint steps up or down according to the target - VID with the programmed slope until the new code is reached. If a new valid command is issued during the transition, the device updates the target - VID level and performs the dynamic transition up to the new code.

5.7 DVID optimization

High slew rate for dynamic VID transitions cause overshoot and undershoot on the regulated voltage, causing violation in the microprocessor requirement. To compensate for this behavior and to remove any undershoot in the transition, the PM6764/66 implement DVID optimization features.

The optimization features allow the user to program a fixed offset voltage for that is applied to the nominal setpoint voltage during the DVID events. This offset is applied immediately once the DVID event start and softly removed when the target VID is reached (see *Figure 11*).

The fixed offset voltage can be positive or negative with a maximum value 155 mV and a minimum value of -160 mV; moreover it can be different for:

- DVID rising with fast slope
- DVID rising with slow slope
- DVID falling with fast slope
- DVID falling with slow slope

The time constant τ_{DVID} of the removal of the DVID offset can be also programmed (with a minimum value of 25 ns) and considering that it depends on the output filter capacitance and its ESR value:

Equation 13

$$\tau_{DVID} = C_{OUT} \cdot ESR_{OUT}$$

Furthermore during the transition to a new valid VID code OCP is masked and reactivated with proper delay after the end of the transition to prevent from false triggering. This delay T_{OCP} can be also programmed simply considering that T_{OCP} must be greater than τ_{DVID}.

The DVID optimization values are stored in the system register `DVID_OPT_PARAM` (see *Table 8 on page 19* and *Table 9* for details) and programmed using dedicated PMBus™ commands. The `DVID_OPT_PARAM` is composed by 43 bits, distributed among 6 bytes, as per following *Table 9*.

Figure 11. DVID optimization features

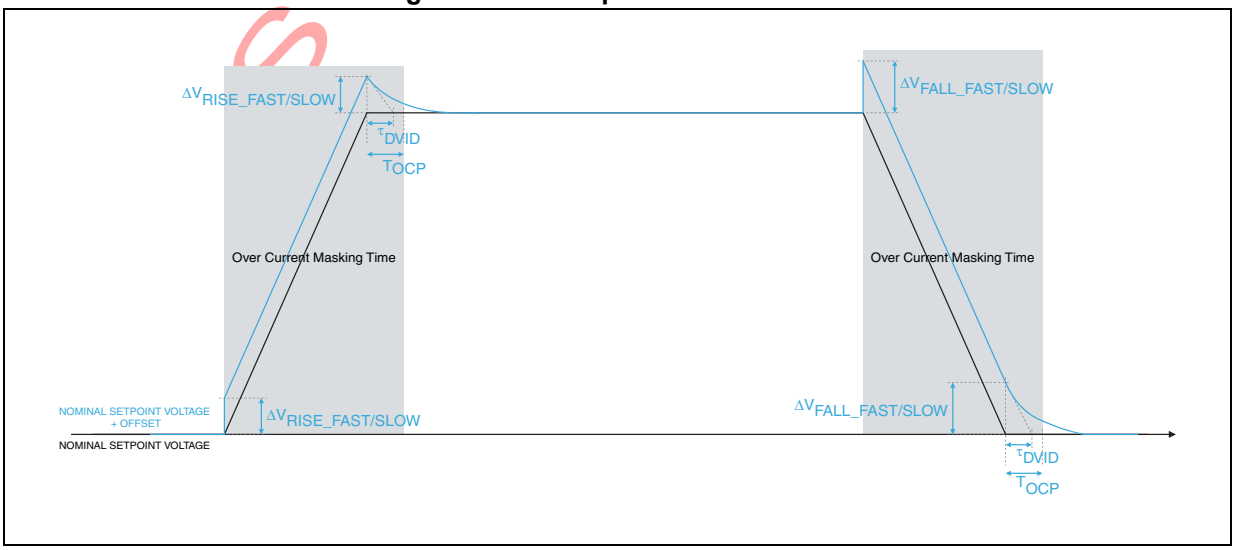


Table 9. DVID_OPT_PARAM register

bit	Symbol	Description
9 - 0	T_OCP [9:0]	**OCP time constant** This value is used to program the intervention time delay of the OCP after DVID events. $T\_OCP[9:0] = \frac{T_{OCP}[ns]}{25}$
23 - 10	TAU_DVID [13:0]	**DVID time constant** This value is used to program the time constant of the DVID offset removing. $TAU\_DVID[13:0] = \frac{25}{\tau_{DVID}[ns]} \cdot 2^{14}$
29 - 24	OFF_FALL_SLOW [5:0]	**OFFSET during SLOW_DVID falling** This value is used to program the offset during the slow DVID falling events. When the offset is positive: $OFF\_FALL\_SLOW[5:0] = \frac{\Delta V_{FALL\_SLOW}[mV]}{5}$ and when the offset is negative: $OFF\_FALL\_SLOW[5:0] = \frac{\Delta V_{FALL\_SLOW}[mV]}{5} + 64$
35 - 30	OFF_FALL_FAST [5:0]	**OFFSET during FAST_DVID falling** This value is used to program the offset during the fast DVID falling events. When the offset is positive: $OFF\_FALL\_FAST[5:0] = \frac{\Delta V_{FALL\_FAST}[mV]}{5}$ and when the offset is negative: $OFF\_FALL\_FAST[5:0] = \frac{\Delta V_{FALL\_FAST}[mV]}{5} + 64$
41 - 36	OFF_RISE_SLOW [5:0]	**OFFSET during SLOW_DVID rising** This value is used to program the offset during the fast DVID falling events. When the offset is positive: $OFF\_RISE\_SLOW[5:0] = \frac{\Delta V_{RISE\_SLOW}[mV]}{5}$ and when the offset is negative: $OFF\_RISE\_SLOW[5:0] = \frac{\Delta V_{RISE\_SLOW}[mV]}{5} + 64$
47 - 42	OFF_RISE_FAST [5:0]	**OFFSET during FAST_DVID rising** This value is used to program the offset during the fast DVID falling events. When the offset is positive: $OFF\_RISE\_FAST[5:0] = \frac{\Delta V_{RISE\_FAST}[mV]}{5}$ and when the offset is negative: $OFF\_RISE\_FAST[5:0] = \frac{\Delta V_{RISE\_FAST}[mV]}{5} + 64$

6 Monitoring and protections

The PM6764/66 devices monitor input/output voltages and currents in order to manage OV, UV and OC events and to provide telemetry data to the PMBus™ interface.

The complete list of the monitored signal available as telemetry data through the PMBus™ interface is summarized in *Table 10*.

Moreover, the PM6764/66 provides an Intel® VR12.5 compliant load current monitor digital signal (DIMON) through the SVID interface with an averaging time frame of 200 µs.

The PM6764/66 allows the user to select which monitored inputs can trigger a fault event and in that case it is possible to select how to respond (i.e.: latched, writing the BBR, asserting the FAULT# signal, etc.).

The mapping of protections implemented is summarized in *Table 11*.

According to standard PMBus™ implementation, protections feature warning and fault limits and actions are programmable as detailed in the following subsections. Protections can additionally be configured to trigger special features such as the FAULT# signal (see *Section 6.1.3*), the SMB_ALERT# assertion (see *Section 6.1.4*) and the black box recorder (BBR, see *Section 6.1.5*).

Table 10. PMBus™ telemetry data

Input signal			PMBus™ command	LSB weight	Range	Averaging time (programmable)
Input	Voltage (average)		*READ_VIN*	15.63 mV	0 V - 15 V	1.2 ms - 1.23 s
	Current (average)		*READ_IIN*	0.25 A	0 A - 255.75 A	1.2 ms - 1.23 s
	Power (average)		*READ_PIN*	0.5 W	0 W - 511.5 W	1.2 ms - 1.23 s
Output	Voltage	Average	*MFR_READ_VOUT*	3.9 mV	0 V - 3.996 V	1.2 ms - 1.23 s
		Max.	*MFR_READ_VOUT_MINMAX*	3.9 mV	0 V - 3.996 V	1.2 ms - 1.23 s
		Min.				1.2 ms - 1.23 s
	Current	Average	*READ_IOUT*	0.25 A	0 A - 255.75 A	1.2 ms - 1.23 s
		Max.	*MFR_READ_IOUT_MINMAX*	0.25 A	0 A - 255.75 A	1.2 ms - 1.23 s
		Min.				1.2 ms - 1.23 s
	Power (average)		*READ_POUT*	1 W	0 W - 1023 W	1.2 ms - 1.23 s
Duty cycle (average)			*READ_DUTY_CYCLE*	0.25%	0% - 100%	1.2 ms - 1.23 s
Power losses (average)			*MFR_READ_PLOSS*	1 W	0 W - 1023 W	1.2 ms - 1.23 s
Temperature (average)			*MFR_READ_TEMPERATURE*	0.25 °C	0 A - 255.75 °C	1.2 ms - 1.23 s

Table 11. Protections map features and programmabilities

Input signal		Programmability					
		Fault limit	Warning limit	Response type programmability	Triggering		
					FAULT# (PM6766 only)	SMB_ALERT	BBR
Input	Overvoltage	Yes	Yes	Yes	Yes	Yes	Yes
	Undervoltage	Yes	Yes	Yes	Yes	Yes	Yes
	Overcurrent	Yes	Yes	Yes	Yes	Yes	Yes
	Overpower	No	Yes	Yes	Yes	Yes	No
Output	Overvoltage	Yes	No	Yes	Yes	Yes	Yes
	Undervoltage	Yes	Yes	Yes	Yes	Yes	Yes
	Overcurrent peak	Yes	No	Yes	Yes	Yes	Yes
	Overcurrent average	Yes	No	Yes	Yes	Yes	Yes
	Overpower	Yes	Yes	Yes	Yes	Yes	Yes
FB disconnection		No	No	No	Yes	Yes	Yes
Catastrophic fault		Yes	No	Yes	Yes	Yes	Yes
Overtemperature		Yes	Yes	Yes	Yes	Yes	Yes

6.1 Input voltage

The input voltage (V_{IN}) is sensed through an external resistor divider network (R_{UP}/R_{DOWN}) as shown in *Figure 1 on page 4* and *Figure 2 on page 5*. The divided down voltage is digitized through an internal ADC and accessible using the `READ_VIN` PMBus™ command.

Using the suggested resistors values (R_{UP}/= 121 kΩ, R_{DOWN}= 10.7 kΩ) the maximum VIN that can be read is about 15 V.

The over/undervoltage fault and warning threshold can be programmed using the PMBus™ commands:

- `VIN_OV_FAULT_LIMIT`
- `VIN_OV_WARN_LIMIT`
- `VIN_UV_FAULT_LIMIT`
- `VIN_UV_WARN_LIMIT`

The device response to a fault detected can be programmed using the PMBus™ commands:

- `VIN_OV_FAULT_RESPONSE`
- `VIN_UV_FAULT_RESPONSE`

The allowable values for fault response commands are:

- 0x80 - latched shutdown
- 0x00 - ignore fault

Both warning and faults events are recorded into the PMBus™ STATUS_INPUT register, they can assert the SMB_ALERT# and/or FAULT# pin and trigger the BBR (see *Table 18 on page 46* and *Table 19 on page 48* for details).

6.1.1 Output voltage

The output voltage (V_{OUT}) is sensed differentially between the FBR and FBG pins and it is digitized through an internal ADC and accessible using the *MFR_READ_VOUT* PMBus™ command.

The over/undervoltage fault and warning threshold can be programmed using the PMBus™ commands:

- MFR_VOUT_OV_FAULT_LIMIT
- VOUT_UV_FAULT_LIMIT
- VOUT_UV_WARN_LIMIT

The device response to a fault detected can be programmed using the PMBus™ commands:

- VOUT_OV_FAULT_RESPONSE
- VOUT_UV_FAULT_RESPONSE

The allowable values for fault response commands are:

- 0x80 - latched shutdown
- 0x00 - ignore fault

Both warning and faults events are recorded into the PMBus™ STATUS_VOUT register, they can assert the SMB_ALERT# and/or FAULT# pin and trigger the BBR (see *Table 18* and *Table 19* for details).

6.1.2 Output current

The current flowing across the inductor(s) is read through the R - C filter across the CSPx and CSNx pins. The integrated R_G resistors program a transconductance gain and generate a current I_{INFO_X} proportional to the current of the phase. The sum of the I_{INFO_X} currents is first thermally compensated using TM information and then converted into a direct proportional voltage using the PMBus™ programmable resistor (R_{IMON}), see *Table 8 on page 19*. The R_{IMON} gives the final gain to program the desired overcurrent protection (see *Figure 12*):

Equation 14

$$V_{IMON} = I_{INFO\_TC} \cdot R_{IMON} = I_{OUT} \cdot \frac{DCR}{R_G} \cdot R_{IMON}$$

The R_{IMON} has to be designed considering that the OC protection is triggered when V_{IMON} crosses the V_{IMON_OCP} threshold ($V_{IMON\_OCP} = V_{OC\_TOT} - 0.9\ V = 2.1\ V$):

Equation 15

$$R_{IMON} = \frac{2.1V \cdot R_G}{I_{OC\_TOT} \cdot DCR}$$

The voltage on the $R_{IMON}$is digitized through an internal ADC and accessible using the READ_IOUT PMBus™ command and through the SVID interface.

To have an accurate reading of the output current, the system register TEL_IOUTMAX must be programmed with the overcurrent value I_{OC_TOT}.

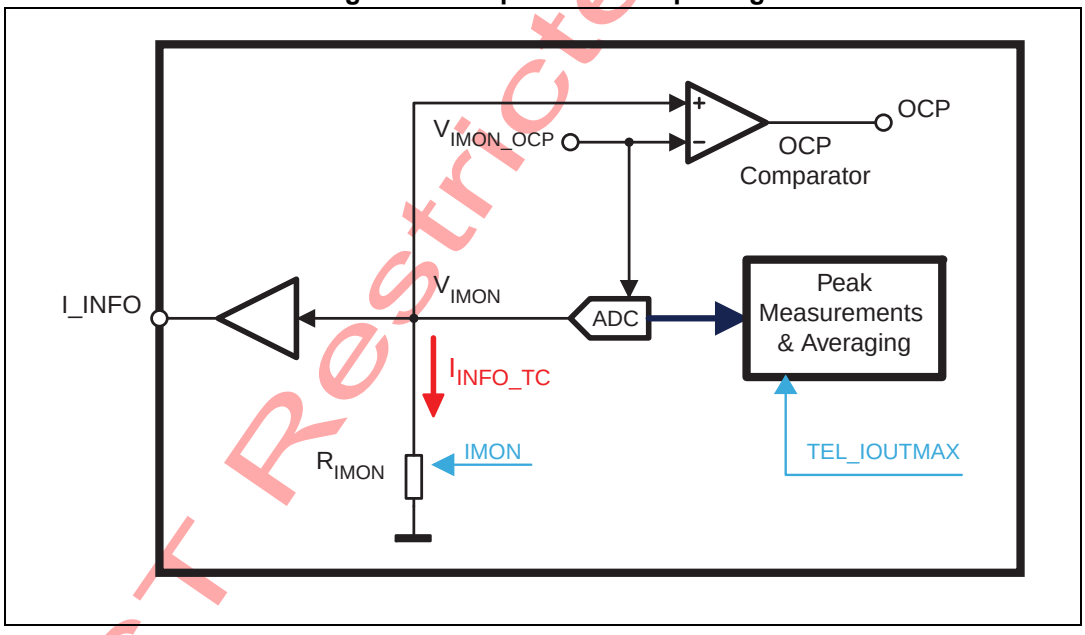
A second level overcurrent protection, using the digital current information, can be programmed using the PMBus™ commands IOUT_OC_FAULT_LIMIT and the device response to an OCP fault detected can be programmed using the PMBus™ commands IOUT_OC_FAULT_RESPONSE.

The allowable values for fault response commands are:

- 0x80 - latched shutdown
- 0x00 - ignore fault

The output overcurrent faults event is recorded into the PMBus™ STATUS_IOUT register, it can assert the SMB_ALERT# and/or FAULT# pin and trigger the BBR (see *Table 18 on page 46* and *Table 19 on page 48* for details).

Figure 12. Output current reporting



6.1.3 Configurable FAULT# indicator (PM6766 only)

The FAULT# pin can be configured to be asserted when selected protections trigger in order to perform custom and specific power management by properly configuring the MFR_FAULT_CONFIG register (see *Table 19*).

6.1.4 Configurable SMB_ALERT#

The PMBus™ alert signal can be programmed so that only selected protection can trigger its assertion. The SMB_ALERT_MASK register needs to be configured by issuing the proper SMBALERT_MASK PMBus™ command (see *Table 18*).

6.1.5 Black box recorder (BBR)

Black box features is aimed to picture precisely the status of the device before any fault occurs. When at least one of the programmed events is verified, the device records the

most significant bit of the PMBus™ status registers before (OLD) and after (NEW) an event occurred into the device NVM, in order to preserve these data even in case of power cycling and/or retrigger of the same protection (see *Table 12* for the complete list of the events recored by the BBR).

The first step to correctly use BBR function is to configure which fault events can trigger the BBR recording procedure using the *MFR_CONFIG_BBR* PMBus™ command (see *Table 12*).

BBR data can be stored into NVM only when it is empty, thus *MFR_CLEAR_BBR* PMBus™ command must be sent to clear the BBR content and wait for one of the programmed events to be detected.

When the BBR is full, to review BBR data stored into the NVM, first the *MFR_READ_BLACKBOX* PMBus™ command must be sent in order to copy the content of the NVM that contains BBR data into internal registers, and then using the *MFR_BLACKBOX* PMBus™ command to receive BBR data (see *Table 12*). These data can be reviewed according to the following cases:

- If OLD = 1 and NEW = 1 then the fault has not triggered the BBR because the fault was triggered before.
- If OLD = 0 and NEW = 1 then the fault has triggered the BBR.
- If OLD = 0 and nNEW = 0 then the fault has not triggered the BBR.

Table 12. MFR_CONFIG_BBR register

Bit	Signal	Values
0	OT	0: ignore fault 1: trigger BBR
1	VIN_OV	
2	VIN_UV	
3	IIN_OC	
4	POUT_OP	
5	IOUT_OC (average)	
6	VOUT_UV	
7	-	
8	CATASTROPHIC	
9	-	
10	Feedback disconnection	
11	IOUT_OC	
12	VOUT_OV	

Table 13. MFR_BLACKBOX register

Fault	OLD bit	NEW bit	Values
Reserved	0 - 63		Reserved
PIN_OP_WARNING	64	96	0: not triggered 1: triggered
IIN_OC_WARNING	65	97	
IIN_OC_FAULT	66	98	
Unit OFF for insufficient VIN	67	99	
VIN_UV_FAULT	68	100	
VIN_UV_WARNING	69	101	
VIN_OV_WARNING	70	102	
VIN_OV_FAULT	71	103	
Feedback disconnection	72	104	0: not triggered 1: triggered
OFF	73	105	
PATCH_CODE_DOWNLOAD(0)	74	106	
PATCH_CODE_DOWNLOAD(1)	75	107	
NVM_STATUS(0)	76	108	
NVM_STATUS(1)	77	109	
CATASTROPHIC_FAULT	78	110	
BLACKBOX_FULL	79	111	
POUT_OP_WARNING	80	112	0: not triggered 1: triggered
POUT_OP_FAULT	81	113	
IOUT_OC_FAULT	82	114	
VUOT_MAX_WARNING	83	115	
VOUT_UV_FAULT	84	116	
VOUT_UV_WARNING	85	117	
-	86	118	
VOUT_OV_FAULT	87	119	
BUSY	88	120	0: not triggered 1: triggered
OT_WARNING	89	121	
OT_FAULT	90	122	
PROCESSOR_FAULT_DETECT	91	123	
MEMORY_FAULT_DETECT	92	124	
PEC_FAIL	93	125	
INVALID/UNSUPPORTED_DATA_RECEIVED	94	126	
INVALID/UNSUPPORTED_COMMAND_RECEIVED	95	127	

7 PMBus™ support

The PM6674, PM6766 device is compatible with the PMBus™ standard revision 1.2, refer to PMBus™ standard documentation for further information (www.pmbus.org).

An embedded microcontroller manages the PM6674, PM6766 PMBus: thanks to its power and flexibility, more than 110 commands are implemented, covering all the basic and advanced functions of the device.

In order to improve reliability, the PM6674, PM6766 support optional PEC (packet error checking), both for incoming and outgoing data packets.

Table 14. PMBus™ supported commands

Command	Code	Packet	Comments
Device control			
OPERATION	0x01	RW byte	Used to turn the controller on/off in conjunction with the input from the control pin. Also used to set margin voltages. Soft-off is not supported.
ON_OFF_CONFIG	0x02	RW byte	Used to configure how the controller responds when power is applied.
Output voltage positioning			
VOUT_MODE	0x20	RW byte	Used to define the data format for output voltage related commands. See the PMBus™ 1.1 specifications.
VOUT_COMMAND	0x21	RW word	Used to set the converter's output voltage to the commanded value - VID mode.
VOUT_TRIM	0x22	RW word	Used to apply a fixed offset voltage to the value set by the VOUT_COMMAND (in Volts).
VOUT_MAX	0x24	RW word	Used to set the upper limit on the output voltage regardless of any other command.
VOUT_MARGIN_HIGH	0x25	RW word	Used to set the voltage to which the output is to be changed when the OPERATION command is set to “margin high”.
VOUT_MARGIN_LOW	0x26	RW word	Used to set the voltage to which the output is to be changed when the OPERATION command is set to “margin low”.
MRF_DEBUG_MODE	0xD2	RW byte	DEBUG_MODE. [01/10] switches [ON/OFF] the VOUT control on the PMBus domain.
MFR_VOUT_TRIM	0xD5	RW byte	Used to apply a fixed offset voltage to the value set by the VOUT_COMMAND (in Volts). This offset is applied only if MFR_DEBUG_MODE = 0x01.

Table 14. PMBus™ supported commands (continued)

Command	Code	Packet	Comments
MFR_VOUT_LL	0xD8	RW byte	VOUT_LL. Used to change the VOUT load line. $R\_DROOP[7:0] = R_{DROOP} \cdot \frac{255}{7678}$
MFR_DAC_VID	0xF2	R byte	Used to read the VR12.5 vid code.
Monitoring calibration			
IOUT_CAL_OFFSET	0x39	RW word	Used to add a calibration offset for the IOUT monitoring, READ_IOUT command.
MFR_VOUT_CAL_GAIN	0xD9	RW byte	Used to apply a calibration gain for the VOUT monitoring, READ_VOUT command.
MFR_VOUT_CAL_OFFSET	0xE0	RW word	Used to add a calibration offset for the VOUT monitoring, READ_VOUT command.
MFR_IOUT_CAL_GAIN	0xE1	RW byte	Used to apply a calibration gain for the IOUT monitoring, READ_IOUT command.
Application setup, power management and digital CTRL			
MFR_MANUAL_PHASE_SHED	0xF3	RW byte	MANUAL PHASE SHEDDING. Used to manage the phase shedding manually.
MFR_DPM12_THR	0xFA	RW byte	DPM12 THRESHOLD. Used to set the DPM12 threshold [A].
MFR_DPM23_THR	0xFB	RW byte	DPM23 THRESHOLD. Used to set the DPM23 threshold [A].
MFR_DPM34_THR	0xFC	RW byte	DPM34 THRESHOLD. Used to set the DPM34 threshold [A].
MFR_DPM45_THR	0xFD	RW byte	DPM45 THRESHOLD. Used to set the DPM45 threshold [A].
MFR_DPM56_THR	0xF4	RW byte	DPM56 THRESHOLD. Used to set the DPM56 threshold [A].
MFR_SYS_CONFIG	0xEB	RW block	7 bytes - used to setup the control loop system parameters.
MRF_PID	0xEC	RW block	8 bytes - used to setup the control loop PID filter parameters.
MFR_PRECONDITIONING	0xED	RW word	Used to setup the control loop preconditioning filter parameters.
MFR_OPEN_LOOP	0xEE	RW word	Used to setup the open loop mode parameters and to enable/disable.
MFR_PGOOD_HI	0xDD	RW word	Used to setup the PGOOD upper threshold [V].
MFR_PGOOD_LO	0xDE	RW word	Used to setup the PGOOD lower threshold [V].
MFR_FAULT_CONFIG	0xEF	RW word	Used to setup the FAULT# pin behavior.

Table 14. PMBus™ supported commands (continued)

Command	Code	Packet	Comments
Sequencing management			
TON_DELAY	0x60	RW word	Used to setup the time delay between the enable signal assertion and the beginning of the soft-start.
TOFF_DELAY	0x64	RW word	Used to setup the time delay between the enable signal de-assertion and the stop of conversion.
Fault threshold and management			
VOUT_OV_FAULT_RESPONSE	0x41	RW byte	Used to set the VOUT overvoltage fault response type.
VOUT_UV_WARN_LIMIT	0x43	RW word	Used to set the VOUT overvoltage warning threshold [V].
VOUT_UV_FAULT_LIMIT	0x44	RW word	Used to set the VOUT overvoltage fault threshold [V].
VOUT_UV_FAULT_RESPONSE	0x45	RW byte	Used to set the VOUT overvoltage fault response type.
IOUT_OC_FAULT_LIMIT	0x46	RW word	Used to set the IOUT overcurrent fault threshold [A].
IOUT_OC_FAULT_RESPONSE	0x47	RW byte	Used to set the IOUT overcurrent fault response type [A].
OT_FAULT_LIMIT	0x4F	RW word	Used to set the overtemperature fault threshold [°C].
OT_FAULT_RESPONSE	0x50	RW byte	Used to set the overtemperature fault response type.
OT_WARN_LIMIT	0x51	RW word	Used to set the overtemperature warning threshold [°C].
VIN_OV_FAULT_LIMIT	0x55	RW word	Used to set the VIN overvoltage fault threshold [V].
VIN_OV_FAULT_RESPONSE	0x56	RW byte	Used to set the VIN overvoltage fault response type.
VIN_OV_WARN_LIMIT	0x57	RW word	Used to set the VIN overvoltage warning threshold [V].
VIN_UV_WARN_LIMIT	0x58	RW word	Used to set the VIN overvoltage warning threshold [V].
VIN_UV_FAULT_LIMIT	0x59	RW word	Used to set the VIN overvoltage fault threshold [V].
VIN_UV_FAULT_RESPONSE	0x5A	RW byte	Used to set the VIN overvoltage fault response type.
IIN_OC_FAULT_LIMIT	0x5B	RW word	Used to set the IIN overcurrent fault threshold [A].
IIN_OC_FAULT_RESPONSE	0x5C	RW byte	Used to set the IIN overcurrent fault response type.
IIN_OC_WARN_LIMIT	0x5D	RW word	Used to set the IIN overcurrent warning threshold [A].
POUT_OP_FAULT_LIMIT	0x68	RW word	Used to set the POUT over power fault threshold [W].

Table 14. PMBus™ supported commands (continued)

Command	Code	Packet	Comments
POUT_OP_FAULT_RESPONSE	0x69	RW byte	Used to set the POUT over power fault response type.
POUT_OP_WARN_LIMIT	0x6A	RW word	Used to set the POUT over power warning threshold [W].
PIN_OP_WARN_LIMIT	0x6B	RW word	Used to set the PIN over power warning threshold [W].
MFR_CAT_FAULT_LIMIT	0xDB	RW word	Used to set the catastrophic fault threshold, evaluated on power losses [W].
MFR_CAT_FAULT_RESPONSE	0xDC	RW byte	Used to set the catastrophic fault response type.
MFR_VOUT_OV_FAULT_LIMIT	0xF6	RW byte	Used to set the VOUT overvoltage fault threshold: 0x00: +400 mV 0x01: +450 mV 0x02: +500 mV 0x03: +550 mV.
Status			
CLEAR_FAULT	0x03	Send byte	Used to clear any fault bits that have been set.
SMBALERT_MASK	0x1B	W word / R block	Used to set which status registers affect the assertion of the SMB_ALRT# pin. This command uses the “block write - block read process call”.
STATUS_BYTE	0x78	RW byte	One byte with information on the most critical faults.
STATUS_WORD	0x79	RW word	Two bytes with information on the units fault condition.
STATUS_VOUT	0x7A	RW byte	Status information on the output voltage warnings and faults.
STATUS_IOUT	0x7B	RW byte	Status information on the output current warnings and faults.
STATUS_INPUT	0x7C	RW byte	Status information on the input warning and fault.
STATUS_TEMPERATURE	0x7D	RW byte	Status information on the temperature warnings and faults.
STATUS_CML	0x7E	RW byte	Status information on the units communication, memory and logic.
STATUS_MRF_SPECIFIC	0x80	RW byte	Manufacturer specific status.
Monitoring			
READ_VIN	0x88	R word	Used to read the measured input voltage [V].
READ_IIN	0x89	R word	Used to read the measured input current [A].
READ_IOUT	0x8C	R word	Used to read the measured output current [A].
READ_TEMPERATURE_1	0x8D	R word	Used to read the measured temperature [°C].
READ_DUTY_CYCLE	0x94	R word	Used to read the measured duty cycle [%].

Table 14. PMBus™ supported commands (continued)

Command	Code	Packet	Comments
READ_POUT	0x96	R word	Used to read the measured output power [W].
READ_PIN	0x97	R word	Used to read the measured input power [W].
MFR_AVERAGE_TIME_SCALE	0xD1	RW byte	Used to set the time period between two measurements [ms].
MFR_READ_VOUT	0xD4	R word	Used to read the measured output voltage [V].
MRF_READ_PIN_POUT	0xE4	R block	4 bytes - used to read the measured input power [W].
MRF_READ_VOUT_MINMAX	0xE5	R block	4 bytes - used to read the measured minimum and maximum values of VOUT [V].
MRF_READ_IOUT_MINMAX	0xE7	R block	4 bytes - used to read the measured minimum and maximum values of IOUT [A].
MFR_RESET_MINMAX	0xEA	Send byte	Used to reset minimum and maximum values of VOUT/IOUT.
MFR_READ_PLOSS	0xF5	RW word	Used to read the measured power losses [W].
Communication and memories manteinance			
WRITE_PROTECT	0x10	RW byte	Used to control writing access to PMBus™ registers in order to prevent accidental changes.
STORE_DEFAULT_ALL	0x11	Send byte	Used to copy the values of PMBus™ registers into the NVM memory. Written data is then verified and the PMB_ALRT# signal is asserted if an error occurs and the "*Memory Fault Detected*" bit is asserted in the STATUS_CML register.
RESTORE_DEFAULT_ALL	0x12	Send byte	Used to reload the values of PMBus™ registers from the NVM memory. This command is rejected if the conversion is enabled.
CAPABILITY	0x19	R byte	Returns the PMBus™ capabilities of the device. 0xA0 (PEC supported, SMBus ARA not supported, bus speed 400 kHz max.).
PMBUS_REVISION	0x98	R word	Used to read the revision of the PMBus™ which the device is compliant to (The device is compliant to PMBus specification part I and part II, rev 1.2).
MFR_ID	0x99	R block	3 bytes - used to read the manufacturers ID (ASCII: STM).
MFR_MODEL	0x9A	R block	7 bytes - used to read manufacturer model number (ASCII: PM676xA).
MFR_REVISION	0x9B	R block	5 bytes - used to read the device revision number (ASCII: x/x/x).
USER_DATA_00	0xB0	RW block	4 bytes - used to read/write custom specific data (4 bytes).
USER_DATA_01	0xB1	RW block	4 bytes - used to read/write custom specific data (4 bytes).

Table 14. PMBus™ supported commands (continued)

Command	Code	Packet	Comments
ST_MODEL_ID	0xE9	R word	Used to read STM internal reference code (0x1DEA).
MFR_PROTECT_DEFAULT	0xFE2E	Ext. RW byte	Protects the non-volatile memory from writing. If a write access to the non-volatile memory is detected while in the protected mode, the PMB_ALRT# signal is asserted and the "*other ML flag*" bit in the STATUS_CML register is set.
MFR_PMBUSCFG_REVISION	0xFE30	Ext. RW word	Used to read/write the revisioning of the current PMBus™ configuration.
MFR_PMBUSCFG_TIMESTAMP_L	0xFE31	Ext. RW block	L: 8 bytes, H: 4 bytes - used to read/write the revisioning of the current PMBus™ time-stamp. Timestamp in the ISO 8601:2004 format (YYYYMMDDHHMM): L: MMDDHHMM H: YYYY
MFR_PMBUSCFG_TIMESTAMP_H	0xFE32	Ext. RW block	
MFR_PMBUSCFG_USERID	0xFE33	Ext. RW word	Used to read/write the revisioning of the current PMBus™ user ID.
Low level access			
MFR_BREAKPOINT	0xD0	RW word	Used to set the new breakpoint access. This command must be unlocked using the command MFR_UNLOCK.
MFR_UNLOCK	0xF0	W word	Used to unlock the access to low level commands.
MFR_LOCK	0xF1	Send byte	Used to lock the access to low level commands.
MFR_SECT_L	0xFE20	Ext. RW block	8 bytes - used to read/write the registers used as an image of the specified NVM sector. This command must be unlocked using the command MFR_UNLOCK.
MFR_SECT_H	0xFE21	Ext. RW block	
MFR_SECT_RD	0xFE24	Ext. W byte	Used to copy the content of the specified NVM sector into PMBus™ accessible registers. This command must be unlocked using the command MFR_UNLOCK.
MFR_SECT_WR	0xFE25	Ext. W byte	Used to copy the content of PMBus™ accessible registers into the specified NVM sector. This command must be unlocked using the command MFR_UNLOCK.
MFR_MEMORY_WORD	0xFE26	Ext. RW block	8 bytes - used to read/write the registers used as an image of the specified memory location. This command must be unlocked using the command MFR_UNLOCK.
MFR_MEMORY_RD	0xFE27	Ext. R block	3 bytes - used to copy 8 bytes of the specified memory location into PMBus™ accessible registers (using the MFR_MEMORY_WORD command). This command must be unlocked using the command MFR_UNLOCK.

Table 14. PMBus™ supported commands (continued)

Command	Code	Packet	Comments
MFR_MEMORY_WR	0xFE28	Ext. W block	4 bytes - used to copy the content of PMBus™ accessible registers (using the MFR_MEMORY_WORD command) into the specified memory location. The Byte#4 is used to set the number of bytes to be written. This command must be unlocked using the command MFR_UNLOCK.
BBR features			
MFR_READ_BLACKBOX	0xFE22	Ext. send byte	Used to copy the content of the NVM that contains BBR data into PMBus™ registers.
MFR_BLACKBOX	0xFE29	Ext. R block	16 bytes - read the registers that contains BBR data.
MFR_CLEAR_BBR	0xFE2B	Ext. send byte	Clear the content of the NVM that contains BBR data.
MFR_CONFIG_BBR	0xFE2C	Ext. RW word	Select which events trigger the writing of the BBR in the NVM.
VR12.5			
MFR_VR12_TEMPZONE	0xFE02	Ext. RW byte	VR12.5 register 0x12: temperature zone register
MFR_VR12_IOUT	0xFE03	Ext. RW byte	VR12.5 register 0x15: output current register
MFR_VR12_ICCMAX_CORE	0xFE08	Ext. RW byte	VR12.5 register 0x21: ICC max.
MFR_VR12_TEMPMAX	0xFE09	Ext. RW byte	VR12.5 register 0x22: temp max.
MFR_VR12_SRFAST	0xFE0A	Ext. RW byte	VR12.5 register 0x24: slew rate fast
MFR_VR12_SRSLOW	0xFE0B	Ext. RW byte	VR12.5 register 0x25: slew rate slow
MFR_VR12_VOUTMAX	0xFE0D	Ext. RW byte	VR12.5 register 0x30: VOUT max.
MFR_VR12_VIDSETTING	0xFE0E	Ext. RW byte	VR12.5 register 0x31: VID setting
MFR_VR12_PWRSTATE	0xFE0F	Ext. RW byte	VR12.5 register 0x32: pwr state
MFR_VR12_OFFSET	0xFE10	Ext. RW byte	VR12.5 register 0x33: offset
MFR_VR12_MULTI_VR_CONFIG	0xFE11	Ext. RW byte	VR12.5 register 0x34: multi VR config.
MFR_VR12_REGLOCK	0xFE1F	Ext. RW byte	V12.5 registers are by default accessible only with read operations (locked). This command allows to lock (0x01) or unlock (0x00) V12.5 registers.

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7.1 Digital control loop registers

Table 15. SYS_CONFIG register

bit	Symbol	Description
3 - 0	T_{ON_MIN} [3:0]	**Minimum TON** Used to program the minimum T_{ON} that can be generated by the control loop. $T_{ON\_MIN}[3:0] = \frac{T_{ON\_MIN}[ns]}{25ns}$
7 - 4	T_{OFF_MIN} [3:0]	**Minimum TOFF** Used to program the minimum T_{OFF} that can be generated by the control loop. $T_{OFF\_MIN}[3:0] = \frac{T_{OFF\_MIN}[ns]}{25ns}$
17 - 8	k_{FF} [9:0]	**Feed forward constant** Used to program the feed forward of the control loop, this is a function of the input voltage and it is a constant of a specific platform. $K_{FF}[9:0] = \frac{5mV}{V_{IN}[V]} \cdot 2^{19}$
27 - 18	BW_{SW_CORR} [9:0]	**Switching time correction bandwidth** Used to program the bandwidth of the loop that fine adjusts the switching frequency. This frequency must be lower than the system loop bandwidth. $BW_{SW\_CORR}[9:0] = 2\pi \cdot \frac{BW_{SW\_CORR}[kHz]}{f_{SW}[kHz]} \cdot \frac{V_{OUT\_MIN}[V]}{V_{IN}[V]} \cdot 2^{10}$
36 - 28	T_{SW} [8:0]	**Switching frequency** Used to program the switching frequency of the conversion. The minimum programmable frequency is 79 kHz. $T_{SW}[8:0] = \frac{40000}{f_{SW}[kHz]}$
44 - 37	BW_{CSH_CORR} [7:0]	**Current sharing correction bandwidth** Used to program the bandwidth of the current sharing loop. This frequency must be lower than the system loop bandwidth. $BW_{CSH\_CORR}[7:0]=$ $= 2\pi \cdot \frac{BW_{CSH\_CORR}[kHz]}{f_{SW}[kHz]} \cdot \frac{V_{OUT\_MIN}[V]}{V_{IN}[V]} \cdot \frac{1 - V_{OUT\_MIN}[V]}{V_{IN}[V]} \cdot 2^{12}$

Table 15. SYS_CONFIG register (continued)

bit	Symbol	Description
51 - 45	STRATEGY [6:0]	**Strategy bits** Used to program power management strategy: STRATEGY [6:5]: UNUSED, 11b. STRATEGY [4]: disable DPM protection – 1: disable DPM protection; – 0: enable DPM protection. STRATEGY [3:2]: multi-pulse strategy – 00b: restart ASAP (during T_{ON}); restart ASAP (during T_{OFF}); – 01b: restart now (during T_{ON}); restart ASAP (during T_{OFF}); – 10b: skip (during T_{ON}); restart ASAP (during T_{OFF}); – 11b: skip (during T_{ON}); skip (during T_{OFF}). STRATEGY [1:0]: T_{ON} correction limits – 00b: T_{ON_NOM} (both positive and negative); – 01b: nominal T_{ON_NOM}/2 (both positive and negative); – 10b: nominal T_{ON_NOM}/4 (both positive and negative); – 11b: no limit (positive); T_{ON_NOM} (negative).
55 - 52	--	Unused.

Table 16. MRF_PID register

bit	Symbol	Description
6 - 0	PID_LP_POST [6:0]	**PID low pass filter post PID coefficient** Used to program the low pass filter coefficient after the PID. See *Section 5.2: Active regulation on page 23* for definitions of τ_{POST}. $PID\_LP\_POST[6:0] = \frac{25ns}{25ns + \tau_{POST}} \cdot 2^7$
22 - 7	PID_C3 [15:0]	**PID coefficient C3** Used to program the PID loop coefficient C3. See *Section 5.2: Active regulation on page 23* for definitions of K_i, K_p and K_d. $PID\_3[15:0] = \frac{K_d}{25ns}$
38 - 23	PID_C1_F [15:0]	**PID coefficient C1_F** Used to program the PID loop coefficient C1_F. See *Section 5.2: Active regulation on page 23* for definitions of K_i, K_p and K_d. $PID\_C1\_F[15:0] = K_i \cdot 25ns \cdot 2^{16}$
57 - 39	PID_C1_I [18:0]	**PID coefficient C1_I** Used to program the PID loop coefficient C1_I. See *Section 5.2: Active regulation on page 23* for definitions of K_i, K_p and K_d. $PID\_C1\_I[18:0] = \left(K_p + \frac{K_d}{25ns}\right) \cdot 8$
63 - 58	--	Unused.

Table 17. MFR_PRECONDITIONING register

bit	Symbol	Description
6 - 0	V_ERR_CLAMP [6:0]	**ERROR voltage clamp** Used to program the clamp of the error voltage before the PID. $V\_ERR\_CLAMP[6:0] = 64 - \frac{V_{ERR\_CLAMP}[mV]}{2mV}$
14 - 7	PID_LP_PRE [7:0]	**PID low pass filter pre PID coefficient** Used to program the low pass filter coefficient before the PID. See *Section 5.2: Active regulation on page 23* for definitions of τ_{PRE}. $PID\_LP\_PRE[7:0] = \frac{25ns}{25ns + \tau_{PRE}} \cdot 2^8$
15	--	Unused.

7.2 Fault and monitoring registers

Table 18. STATUS and SMBALERT_MASK registers

	STATUS registers			SMBALERT_MASK	
	bit	Signal	Description	bit	Description
STATUS BYTE	7	BUSY	Asserted (1) when the input condition is true	7	Enable/disable the assertion of the SMBALERT# pin when one or more of the input condition(s) are true: 0: = NOT MASKED 1: = MASKED
	6	OFF		-	
	5	VOUT_OV		-	
	4	IOUT_OC		-	
	3	VIN_UV		-	
	2	Temperature	These bits are set to 1 when at least one bit in the dedicated status register is set to 1.	-	
	1	CML		-	
	0	None of above		-	
STATUS WORD (byte 1)	7	VOUT	These bits are set to 1 when at least one bit in the dedicated status register is set to 1.	-	
	6	IOUT/POUT		-	
	5	INPUT		-	
	4	MFR		-	

Table 18. STATUS and SMBALERT_MASK registers (continued)

STATUS registers				SMBALERT_MASK	
	bit	Signal	Description	bit	Description
STATUS VOUT	7	VOUT OV fault	Asserted (1) when the input condition is true	7	Enable/disable the assertion of the SMBALERT# pin when one or more of the input condition(s) are true: 0: = NOT MASKED 1: = MASKED
	5	VOUT UV warning		5	
	4	VOUT UV fault		4	
	3	VOUT_MAX warning		3	
STATUS IOUT	7	IOUT OC fault	Asserted (1) when the input condition is true	7	Enable/disable the assertion of the SMBALERT# pin when one or more of the input condition(s) are true: 0: = NOT MASKED 1: = MASKED
	1	POUT OP fault		1	
	0	POUT OP warning		0	
STATUS IINPUT	7	VIN OV fault	Asserted (1) when the input condition is true	7	Enable/disable the assertion of the SMBALERT# pin when one or more of the input condition(s) are true: 0: = NOT MASKED 1: = MASKED
	6	VIN OV warning		6	
	5	VIN UV fault		5	
	4	VIN UV warning		4	
	3	VIN UVLO		3	
	2	IIN OC fault		2	
	1	IIN OC warning		1	
	0	PIN OP warning		0	
STATUS TEMPERATURE	7	OT fault	Asserted (1) when the input condition is true	7	Enable/disable the assertion of the SMBALERT# pin when one or more of the input condition(s) are true: 0: = NOT MASKED 1: = MASKED
	6	OT warning		6	

Table 18. STATUS and SMBALERT_MASK registers (continued)

STATUS registers				SMBALERT_MASK	
	bit	Signal	Description	bit	Description
STATUS CML	7	Invalid or unsupported command received	Asserted (1) when the input condition is true	7	Enable/disable the assertion of the SMBALERT# pin when one or more of the input condition(s) are true: 0: = NOT MASKED 1: = MASKED
	6	Invalid or unsupported data received		6	
	5	PEC failed		5	
	4	Memory fault detected		4	
	3	Processor fault detected		3	
	0	Other memory or logic fault		0	
STATUS MFR SPECIFIC	7	BBR full	Asserted (1) when the input condition is true	7	Enable/disable the assertion of the SMBALERT# pin when one or more of the input condition(s) are true: 0: = NOT MASKED 1: = MASKED
	6	Catastrophic fault		6	
	5	NVM status (1)	11 - NVM is blank 00 - no error detected	5	
	4	NVM status (0)		4	
	3	Patch download (1)	11 - timeout detected 10 - EEPROM not present 01 - CRC error detected 00 - no error detected	3	
	2	Patch download (0)		2	
	1	Rail_OFF	Asserted (1) when the input condition is true	1	
	0	FB_disconnection		0	

Table 19. MFR_FAULT_CONFIG register

bit	Input signal	Description
10	VOUT OV	Enable/disable the assertion of the FAULT# pin when one or more of the input condition(s) are true (fault detected): – 0: = disable – 1: = enable
9	IOUT OC	
8	Catastrophic fault	
7	-	
6	VOUT UV	
5	IOUT OC (average)	
4	POUT OP	
3	IIN OC	
2	VIN UV	
1	VIN OV	
0	Overtemperature	

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 13. PM6766 package outline (VFQFPN40 5 x 5 mm)

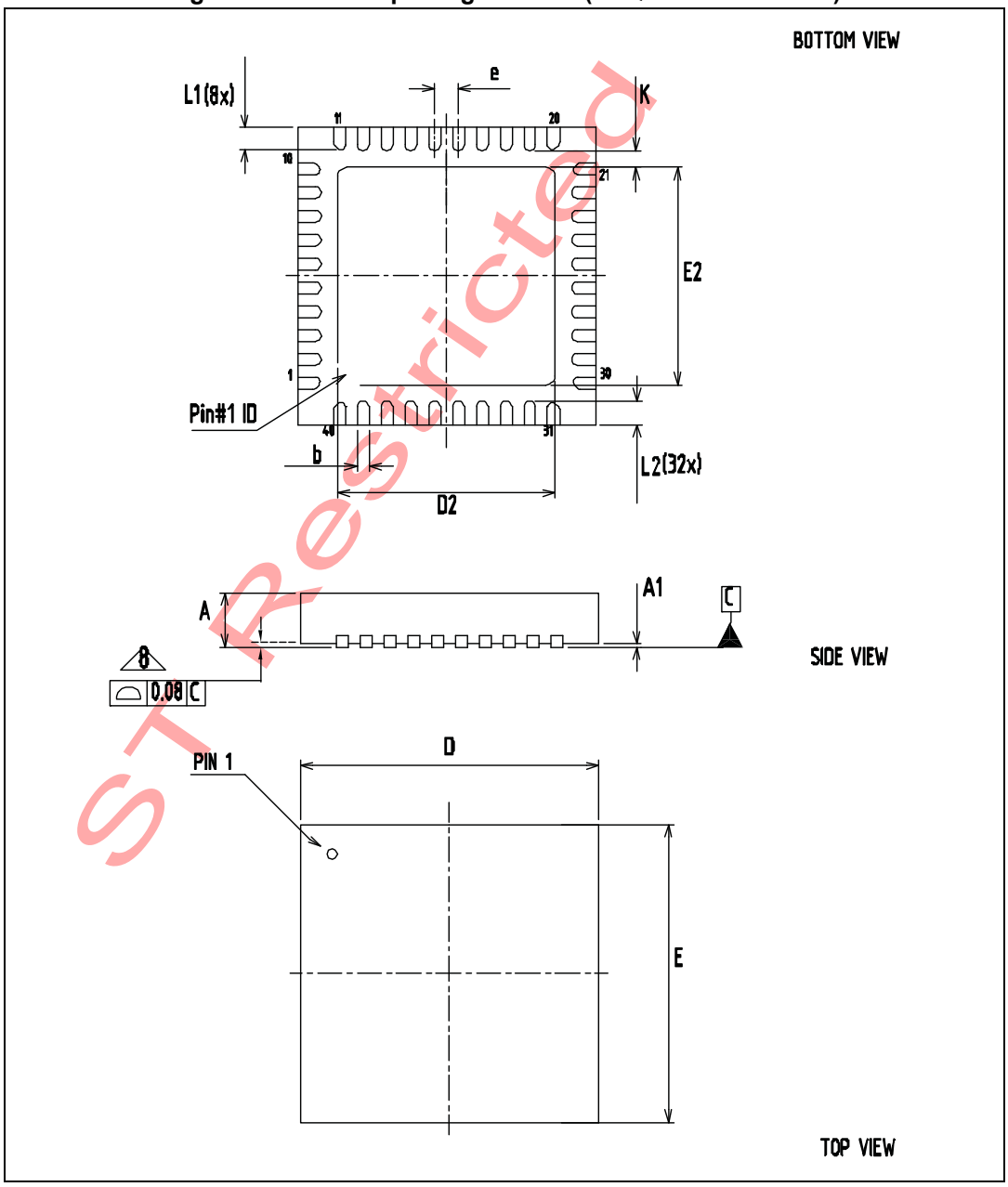


Table 20. PM6766 package mechanical data (VFQFPN40 5 x 5 mm)

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0	0.02	0.05
b	0.15	0.20	0.25
D		5.00	
E		5.00	
D2	3.50	3.65	3.75
E2	3.50	3.65	3.75
e		0.40	
L1	0.277	0.377	0.477
L2	0.30	0.40	0.50
K		0.20	

Figure 14. PM6766 recommended footprint (VFQFPN40 5 x 5 mm)

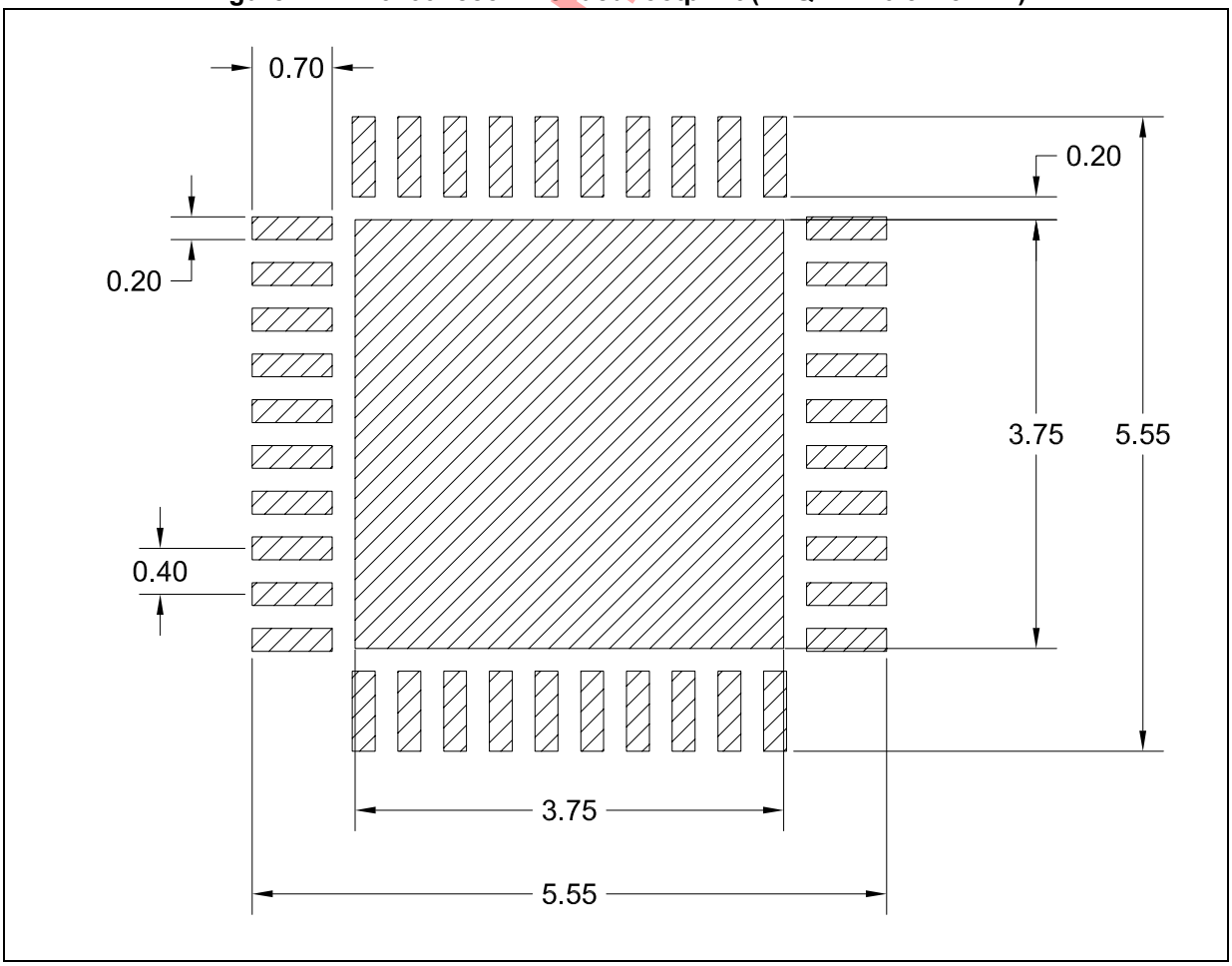


Figure 15. PM6764 package outline (VFQFPN28 4 x 4 mm)

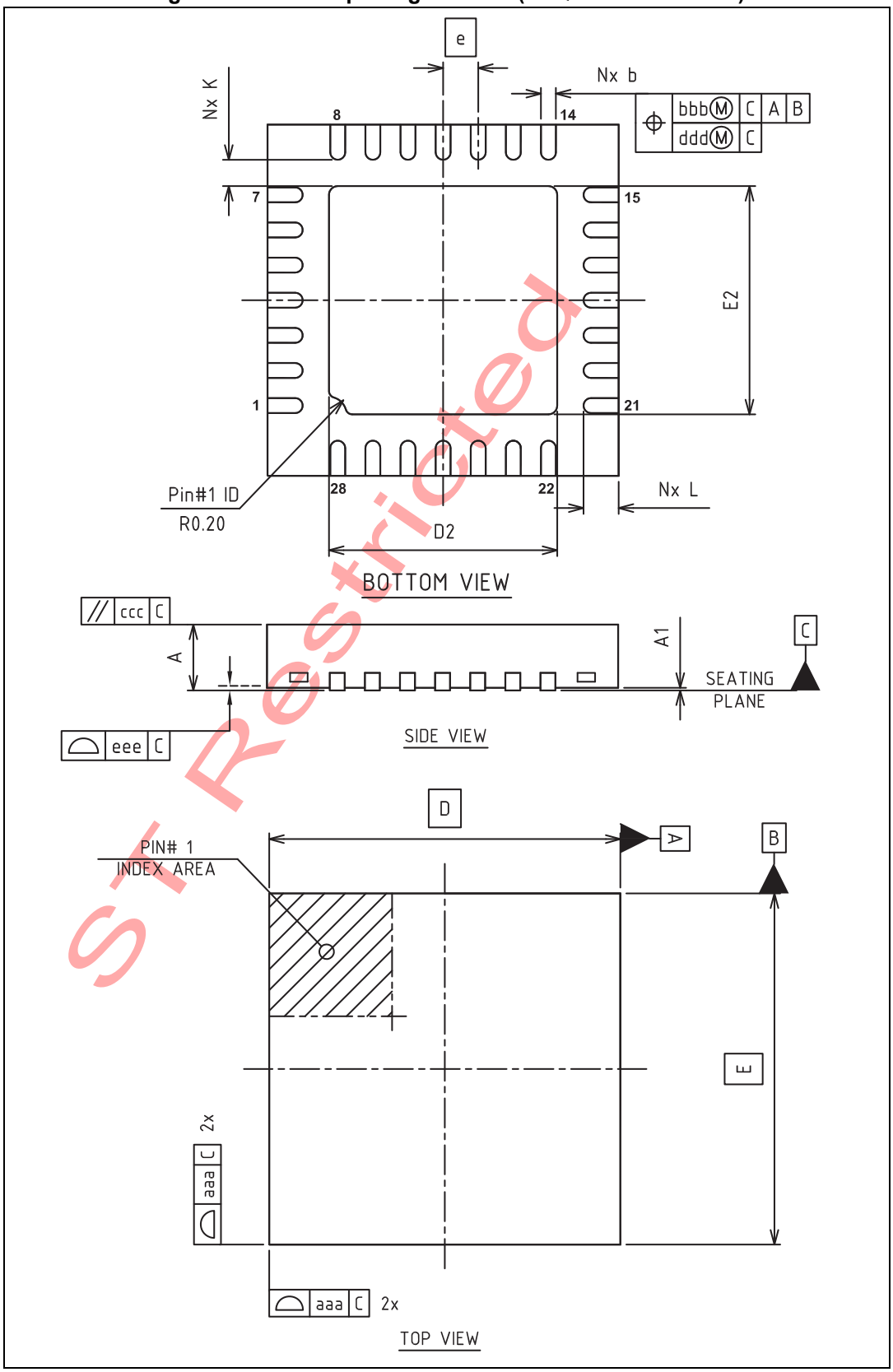
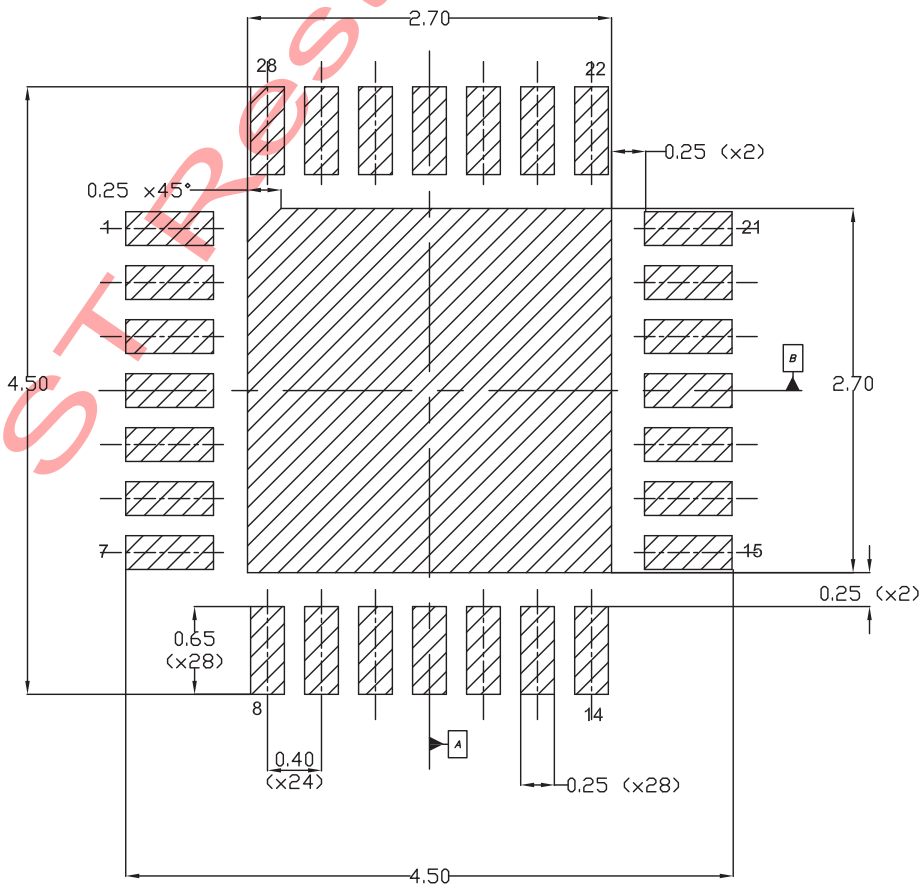


Table 21. PM6764 package mechanical data (VFQFPN28 4 x 4 mm)

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
D		4.00	
E		4.00	
D2	2.45	2.60	2.70
E2	2.45	2.60	2.70
e		0.40	
L	0.30	0.40	0.50
K		0.20	

Figure 16. PM6764 recommended footprint (VFQFPN28 4 x 4 mm)



9 Revision history

Table 22. Document revision history

Date	Revision	Changes
16-Jun-2014	1	Initial release.
15-Sep-2014	2	Updated typo in PID_LP_POST equations of *Table 16 on page 45* and *Table 17 on page 46*). Minor modifications throughout document.
11-Feb-2015	3	Updated *Figure 14 on page 50* (replaced by new figure). Minor modifications throughout document.