PMC *PMC-Sierra,Inc.*

Quad J2, E3 and DS-3 Framer

FEATURES

- Quad DS-3, E3 (G.751 and G.832), and J2 framers.
- Each channel can be independently configured to be a DS-3, E3, or J2 Framer.
- Gapped transmit and receive clocks can be optionally generated for interface to devices which only need access to payload data bits.
- Provides programmable pseudo-random test pattern generation, detection, and analysis features.
- Provides integral transmit and receive HDLC controllers with 128-byte FIFO depths.
- Provides performance monitoring counters suitable for accumulation periods of up to 1 second.
- Provides an 8-bit microprocessor interface for configuration, control and status monitoring.
- Provides a standard five signal P1149.1 JTAG test port for boundary scan board test purposes.
- Low power 3.3 V CMOS technology with 5 V tolerant inputs.
- Available in a high density 256-pin SBGA package (27 mm x 27 mm).

RECEIVER SECTION

- Provides frame synchronization for the M23 or C-bit parity DS3 applications, alarm detection, and accumulates line code violations, framing errors, parity errors, path parity errors and FEBE events. In addition, far end alarm channel codes are detected, and an integral HDLC receiver is provided to terminate the path maintenance data link.
- Provides frame synchronization for the G.751 or G.832 E3 applications, alarm detection, and accumulates line code violations, framing errors, parity errors, and FEBE events. In addition, in G.832, the Trail Trace is detected, and an integral HDLC receiver is provided to terminate either the Network Requirement or the General Purpose data link.
- Provides frame synchronization for G.704 and NTT 6.312 Mbit/s J2 applications, alarm detection, and accumulates line code violations, framing errors, and CRC parity errors. An integral HDLC receiver is provided to terminate the data link.
- Provides a receive HDLC controller with a 128-byte FIFO to accumulate data link information.
- Provides detection of yellow alarm and loss of frame (LOF), and accumulates BIP-8 errors, framing errors and FEBE events.
- Provides programmable pseudo-random test-sequence detection (up to $2^{32}-1$ bit length patterns conforming to ITU-T O.151 standards) and analysis features.

TRANSMITTER SECTION

- Provides frame insertion for the M23 or C-bit parity DS3 applications, alarm

BLOCK DIAGRAM
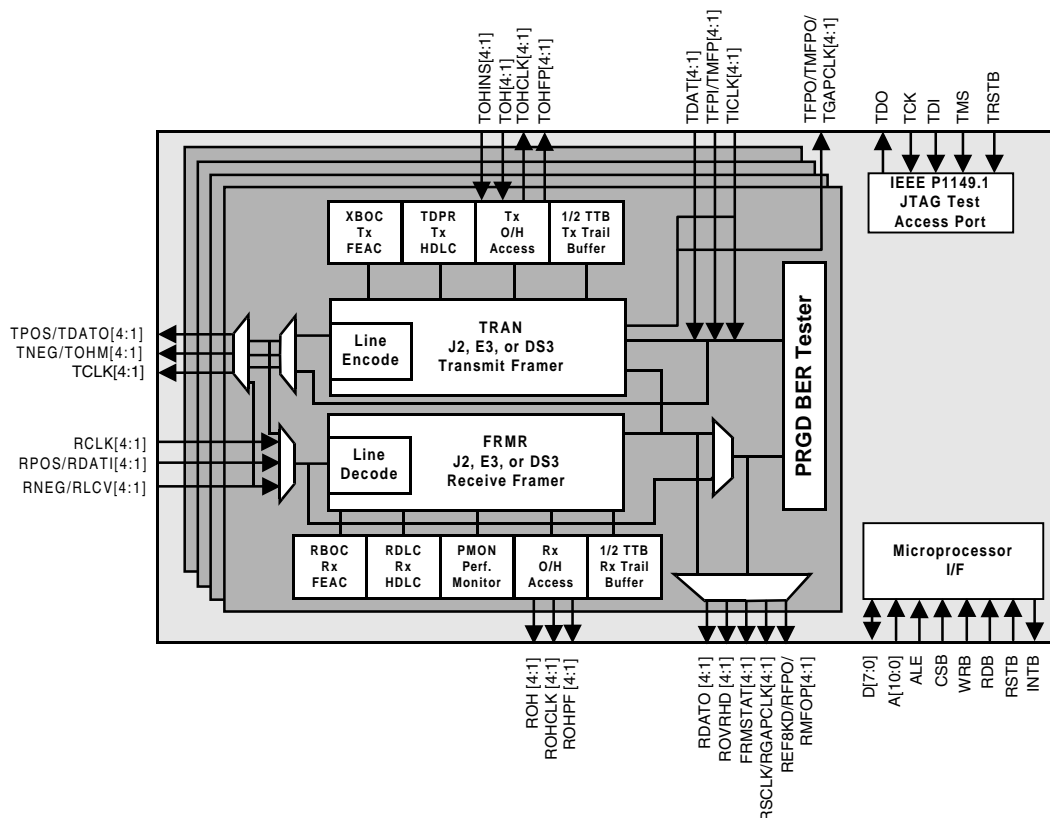
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insertion, and diagnostic features. In addition, far end alarm channel codes may be inserted, and an integral HDLC transmitter is provided to insert the path maintenance data link.

- Provides frame insertion for the G.751 or G.832 E3 applications, alarm insertion, and diagnostic features. In addition, for G.832, the Trail Trace is inserted, and an integral HDLC transmitter is provided to insert either the Network Requirement or the General Purpose data link.

- Provides frame insertion for G.704 6.312 Mbit/s J2 applications, alarm

insertion, and diagnostic features. An integral HDLC transmitter is provided to insert the path maintenance data link.

- Provides a transmit HDLC controller with a 128-byte FIFO.

- Provides programmable pseudo-random test sequence generation (up to 232-1 bit length sequences conforming to ITU-T O.151 standards). Diagnostic abilities include single bit error insertion or error insertion at bit error rates ranging from 10^{-1} to 10^{-7}.
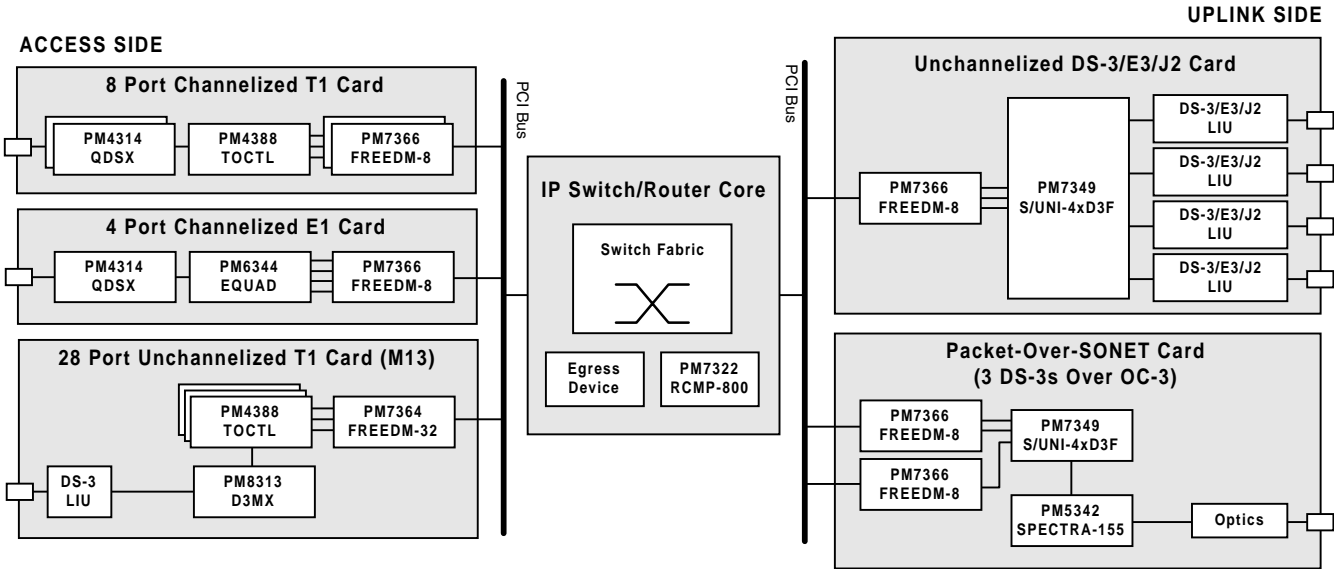
LOOPBACK FEATURES
- Provides for diagnostic loopbacks, line loopbacks, and payload loopbacks.
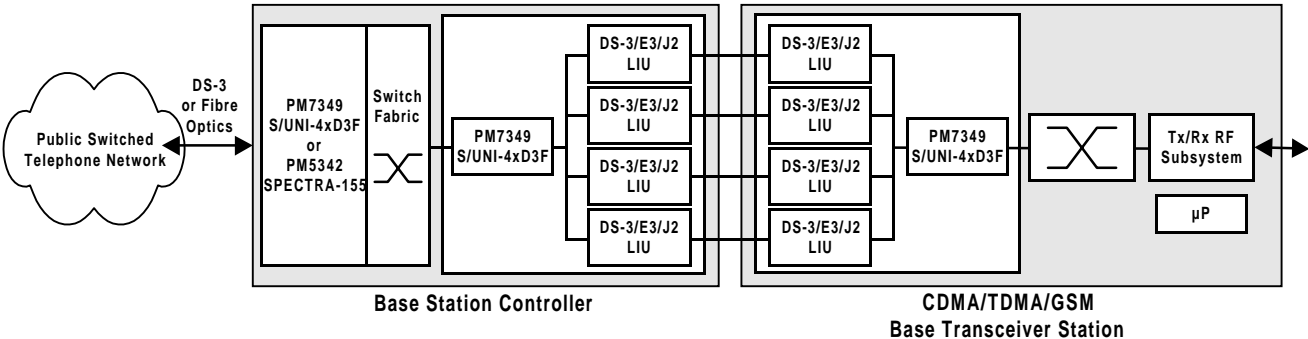
APPLICATIONS
- SONET/SDH Mux E3/DS-3 Tributary Interfaces.
- PDH Mux J2/E3/DS-3 Line Interfaces.
- DS-3/E3/J2 Digital Cross Connect Interfaces.
- DS-3/E3/J2 PPP Internet Access Interfaces.
- DS-3/E3/J2 Frame Relay Interfaces.

TYPICAL APPLICATIONS

FRAME RELAY SWITCH/ROUTER

WIRELESS BASE STATION APPLICATION