White LED Driver with PWM Brightness Control

Features

- **2.7V to 15V Input Voltage Range**
- **200mV Reference Voltage With ±2% Accuracy**
- **PWM Brightness Control**
- **Built-in Soft Start**
- **Up to 90% Efficiency**
- **2mm × 2mm × 0.8mm 6-pin QFN Package With Thermal Pad**
- **<1㎃A Quiescent Current during Shutdown**

APPLICATIONS

- **Cellular Phones**
- **Portable Media Players**
- **Ultra Mobile Devices**
- **GPS Receivers**
- **White LED Backlighting for Media Form Factor Display**

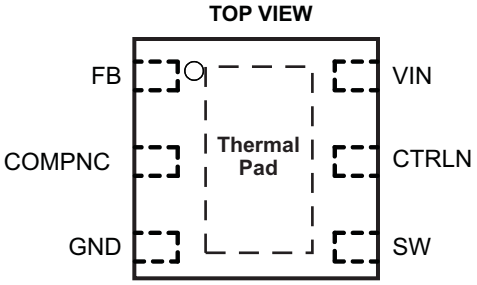
General Description

The PM8001D is a current-mode and fixed frequency 600kHz boost converter with an integrated N-FET to drive white LEDs.

The series connection allows the LED current to be identical for uniform brightness. Its low on-resistance of NFET and low feedback voltage reduce power loss and achieve high efficiency. 600kHz Constant switching frequency allows using small-size inductor and both of input and output capacitors. An over voltage protection function, which monitors the output voltage via LX pin, stops switching of the IC if the LX voltage exceeds the over voltage threshold. An internal soft-start circuit eliminates the inrush current during start-up.

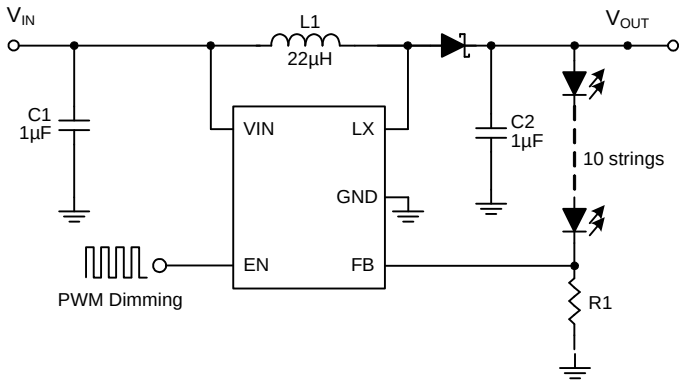
PM8001D also intergates under-voltage lockout and over-temperature protection to protect the IC in abnormal conditions. The PM8001D is available in TDFN2x2-6 package.

Pin Configuration



6-PIN 2mm x 2mm x 0.8mm QFN

Simplified Application Circuit



Pin Description

PIN.		FUNCTION
TDFN-2x2-6	NAME	
1	FB	Feedback Pin. Connect this pin to cathode of the lowest LED and current-sense resistor (R1). Calculate resistor value according to $R1=V_{REF}/I_{LED}$.
2	NC	No Commend.
3	GND	Power and signal ground pin.
4	LX	Switch pin. Connect this pin to inductor/diode here.
5	EN	Enable Control Input. Forcing this pin above 1.0V enables the device, or forcing this pin below 0.4V to shut it down. In shutdown, all functions are disabled to decrease the supply current below 1μA.
6	VIN	Main Supply Pin. Must be closely decoupled to GND with a 1μF or greater ceramic capacitor.
Exposed Pad	GND	Connecting this pad to GND.

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN Pin to GND	-0.3 to 15	V
	FB and EN to GND	-0.3 ~ V_{IN}	V
V_{LX}	LX Pin to GND	-0.3 to 40	V
P_D	Power Dissipation	Internally Limit	W
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Thermal Characteristics

Symbol	Parameter		Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	TDFN2x2-6	165	°C/W
θ_{JC}	Junction-to-Case Resistance	TDFN2x2-6	20	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	VIN Input Voltage	2.7 ~ 15	V
C_{IN}	Input Capacitor	1 ~	µF
C_{OUT}	Output Capacitor	1 ~	µF
L1	Converter Output Inductor	4.7 ~ 22	µH
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Please refer to the typical application circuit.

Electrical Characteristics

Refer to the typical application circuits. These specifications apply over. V_{IN}=3.6V, T_A=25°C.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY VOLTAGE AND CURRENT						
V_{IN}	Input Voltage Range		2.7	-	6	V
I_{DD1}	Input DC Bias Current	V_{FB} = 0.4V, no switching	-	-	420	µA
I_{DD2}		V_{FB} = GND, switching	-	1.2	1.8	mA
I_{SD}		EN = GND	-	-	1	µA
UNDER-VOLTAGE LOCKOUT						
	UVLO Threshold Voltage	V_{IN} Rising	2.0	2.2	2.4	V
	UVLO Hysteresis Voltage	V_{IN} Falling	50	100	150	mV
REFERENCE AND OUTPUT VOLTAGES						
V_{REF}	Regulated Feedback Voltage	V_{IN}=2.7V ~ 6V, T_A= 25°C	0.196	0.2	0.204	V
		V_{IN}=2.7V ~ 6V, T_A= 50°C	0.192	0.2	0.208	
I_{FB}	FB Input Current	V_{FB}=1.23V	-50	-	50	nA
INTERNAL POWER SWITCH						
F_{SW}	Switching Frequency		540	600	660	kHz
R_{ON}	Power Switch On Resistance	VIN=3.6V	-	0.3	0.7	Ω
		VIN=3V	-	-	0.7	
	LX Leakage Current	V_{EN}=0V, V_{LX}=6V, V_{IN} = 6V	-1	-	1	µA
		V_{EN}=0V, V_{LX}=35V, V_{IN} = 6V	-	-	10	µA
D_{MAX}	LX Maximum Duty Cycle		92	95	98	%
OUTPUT OVER VOLTAGE PROTECTION						
V_{LX_OVP}	Over Voltage Threshold	V_{LX} Rising	36	38	40	V
POWER SWITCH CURRENT LIMIT						
I_{LIM}	N-Channel MOSFET Current Limit	Duty = D_{MAX}	1.5	-	-	A

Electrical Characteristics(Cont.)

Refer to the typical application circuits. These specifications apply over. V_{IN}=3.6V, T_A=25°C.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ENABLE AND TDOWN						
	Enable Voltage Threshold	V_{EN} Rising	1	-	-	V
	Shutdown Voltage Threshold	V_{EN} Falling	-	-	0.4	V
	EN Pulled Low Resistance		400	800	1200	kΩ
	EN Dimmimg Minimum Enable Pulsed Width	In Normal Operation	100	-	-	ns
	EN Minimum On Pulsed Width	Use VEN=3V to enable to device, PWM Dimmimg Frequency=5kHz to 100 k Hz	-	1	-	μs
OVER-TEMPERATURE PROTECTION						
T_{OTP}	Over-Temperature Protection (Note 4)	T_J Rising	-	150	-	°C
	Over-Temperature Protection Hysteresis (Note 4)	T_J Falling	-	40	-	°C

Note 4: Guaranteed by design, not production tested.

Typical Application Circuits

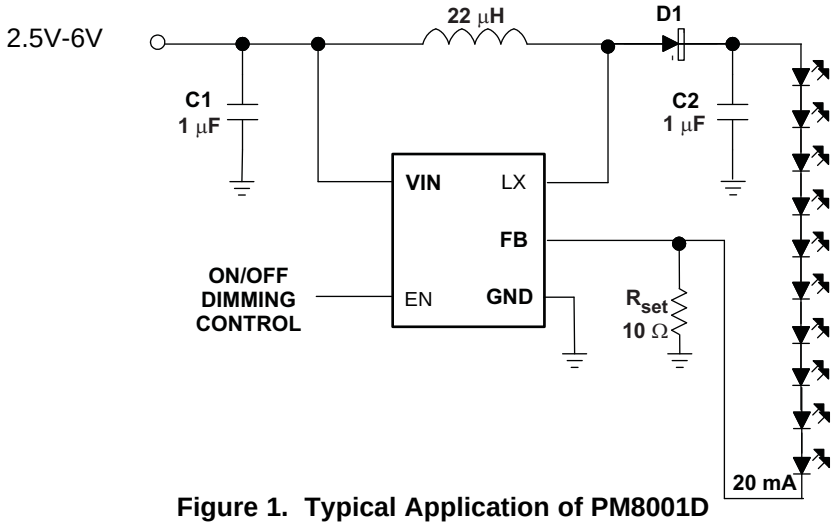


Figure 1. Typical Application of PM8001D

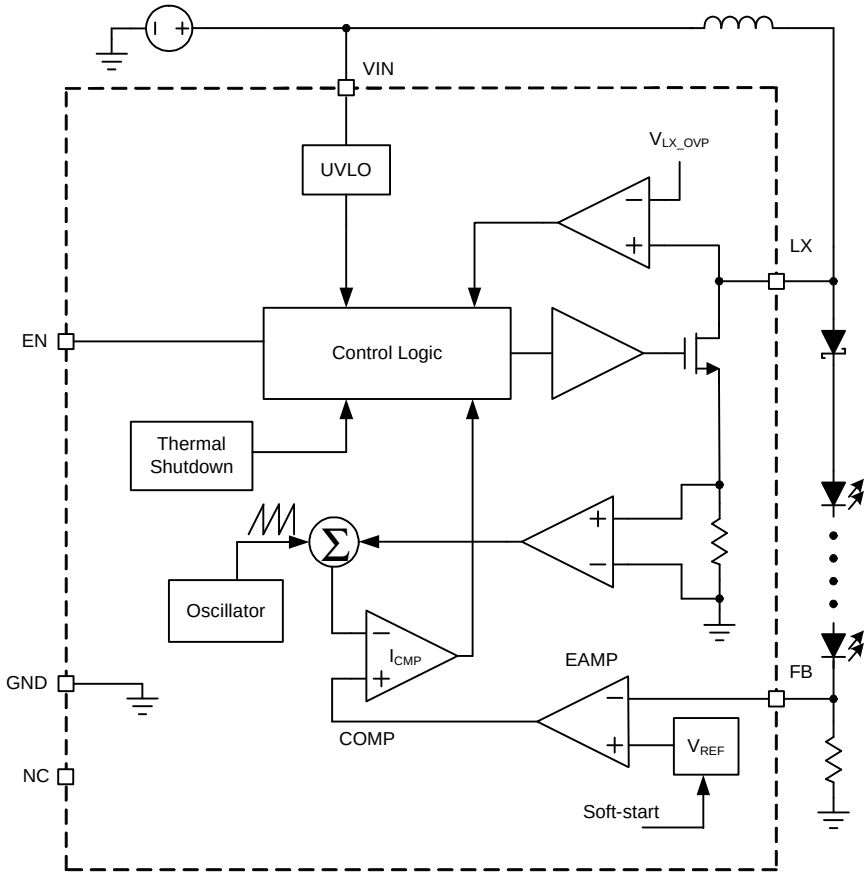
Output Voltage Setting

In figure 1, the converter regulates the voltage on FB pin, current- sense resistor R1 at V_{REF}. Therefore, the current (I_{LED}), flowing via the LEDs and the R1, is calculated by the following equation:

connected with the cathode of the lowest LED and the

$$I_{LED} = \frac{V_{REF}}{R1}$$

Block Diagram



Function Description

Main Control Loop

The PM8001D is a constant frequency current-mode switching regulator. During normal operation, the internal N-channel power MOSFET is turned on each cycle when the oscillator sets an internal RS latch and turned off when an internal comparator (ICMP) resets the latch. The peak inductor current at which ICMP resets the RS latch is controlled by the voltage on the internal COMP node, which is the output of the error amplifier (EAMP). An external current-sense resistor connected between cathode of the lowest LED and ground allows the EAMP to receive a current feedback voltage VFB at FB pin. When the LEDs voltage decreases to cause the LEDs current to decrease, it causes a slightly decrease in V_{FB} relative to the reference voltage, which in turn causes the internal COMP voltage to increase until the LEDs current reaches the set point.

VIN Under-Voltage Lockout (UVLO)

The Under-Voltage Lockout (UVLO) circuit compares the input voltage at VIN with the UVLO threshold (2.2V rising, typical) to ensure the input voltage is high enough for reliable operation. The 100mV (typ) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the UVLO rising threshold, startup begins. When the input voltage falls below the UVLO falling threshold, the controller turns off the converter.

Soft-Start

The PM8001D has a built-in soft-start to control the N channel MOSFET current raises during start-up. During soft-start, an internal ramp voltage connected to one of the inverting inputs of the current limit comparator. The inductor current limit is proportional to the voltage. When the threshold voltage of the internal soft-start comparator is reached, the full current limit is released.

Current-Limit Protection

The PM8001D monitors the inductor current flowing through the N-channel MOSFET, and limits the current peak at current-limit level to prevent loads and the device from damages in overload conditions.

Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the PM8001D When the junction temperature exceeds 150°C, a thermal sensor turns off the power MOSFET, allowing the device to cool. The thermal sensor allows the converter to start a soft-start process and regulate the LEDs current again after the junction temperature cools by 40°C. The OTP is designed with a 40°C hysteresis to lower the average Junction Temperature (T_J) during continuous thermal overload conditions, increasing the lifetime of the device.

Enable/Shutdown

Driving EN to ground places the PM8001D in shutdown mode. When in shutdown, the internal power MOSFET turns off, all internal circuitry shuts down and the quiescent supply current reduces to 1mA maximum. This pin also could be used as a digital input allowing brightness controlled by using a PWM signal with frequency from 5kHz to 100kHz. The 0% duty cycle of PWM signal corresponds to zero LEDs current and 100% corresponds to full one. If use EN Pin to enable the device, suggestion dimmimg duty range is from 15% to 100% at 100kHz dimmimg frequency.

Open-LED Protection

In driving LED applications, the feedback voltage on FB pin falls down if one of the LEDs, in series, is failed. Meanwhile, the converter unceasingly boosts the output voltage like an open-loop operation. Therefore, an over-voltage protection monitoring the output voltage via LX pin prevents the LX and the output voltages from exceeding their maximum voltage ratings. Once the voltage on the LX pin rises above the OVP threshold, the converter stops switching and prevents the output voltage from rising. The converter can work again when the LX voltage falls below the falling of OVP voltage threshold.

Application Information

Input Capacitor Selection

The input capacitor (C_{IN}) reduces the ripple of the input current drawn from the input supply and reduces noise injection into the IC. The reflected ripple voltage will be smaller when an input capacitor with larger capacitance is used. For reliable operation, it is recommended to select the capacitor with maximum voltage rating at least 1.2 times of the maximum input voltage. The capacitors should be placed close to the VIN and the GND.

Inductor Selection

Selecting an inductor with low dc resistance reduces conduction losses and achieves high efficiency. The efficiency is moderated whilst using small chip inductor which operates with higher inductor core losses. Therefore, it is necessary to take further consideration while choosing an adequate inductor. Mainly, the inductor value determines the inductor ripple current: larger inductor value results in smaller inductor ripple current and lower conduction losses of the converter. However, larger inductor value generates slower load transient response. A reasonable design rule is to set the ripple current, ΔI_L, to be 30% to 50% of the maximum average inductor current, $I_{L(AVG)}$. The inductor value can be obtained as below,

$$L \geq \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \times \frac{V_{OUT} - V_{IN}}{F_{SW} \cdot I_{OUT(MAX)}} \times \frac{\eta}{\left(\frac{\Delta I_L}{I_{L(AVG)}}\right)}$$

where

V_{IN} = input voltage

V_{OUT} = output voltage

F_{SW} = switching frequency in MHz

I_{OUT} = maximum output current in amp.

η = Efficiency

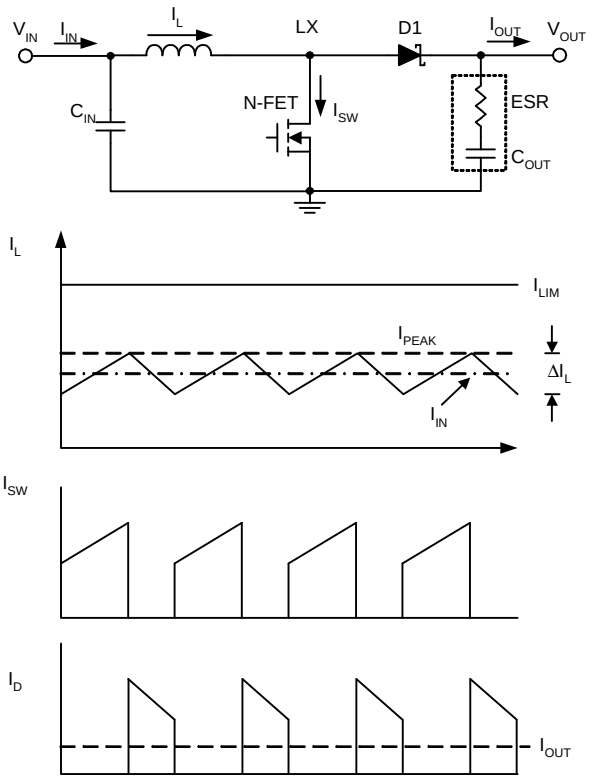
$\Delta I_L / I_{L(AVG)}$ = inductor ripple current/average current (0.3 to 0.5 typical)

To avoid the saturation of the inductor, the inductor should be rated at least for the maximum input current of the converter plus the inductor ripple current. The maximum input current is calculated as below:

$$I_{IN(MAX)} = \frac{I_{OUT(MAX)} \cdot V_{OUT}}{V_{IN} \cdot \eta}$$

The peak inductor current is calculated as the following equation:

$$I_{PEAK} = I_{IN(MAX)} + \frac{1}{2} \cdot \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{V_{OUT} \cdot L \cdot F_{SW}}$$



Output Capacitor Selection

The current-mode control scheme of the PM8001D allows the usage of tiny ceramic capacitors. The higher capacitor value provides good load transients response. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. If required, tantalum capacitors may be used as well. The output ripple is the sum of the voltages across the ESR and the ideal output capacitor.

$$\Delta V_{OUT} = \Delta V_{ESR} + \Delta V_{COUT}$$

$$\Delta V_{COUT} \approx \frac{I_{OUT}}{C_{OUT}} \cdot \left(\frac{V_{OUT} - V_{IN}}{V_{OUT} \cdot F_{SW}}\right)$$

$$\Delta V_{ESR} \approx I_{PEAK} \cdot R_{ESR}$$

where I_{PEAK} is the peak inductor current.

PWM BRIGHTNESS DIMMING

When the EN pin is constantly high, the FB voltage is regulated to 200mV typically. However, the EN pin allows a PWM signal to reduce this regulation voltage therefore, it achieves LED brightness dimming. The relationship between the duty cycle and FB voltage is given by Equation 2.

$$V_{FB} = Duty \times 200\ mV$$

Where

Duty = duty cycle of the PWM signal

200 mV = internal reference voltage

(2)

The IC chops up the internal 200mV reference voltage at the duty cycle of the PWM signal, The pulse signal is then filtered by an internal low pass filter. The output of the filter is connected to the error amplifier as the reference voltage for the FB pin regulation.

Therefore, although a PWM signal is used for brightness dimming, only the LED current is modulated, which is often referred as analog dimming. This eliminates the audible noise which often occurs when the LED current is pulsed in replica of the frequency and duty cycle of PWM control. Unlike other scheme which filters the PWM signal for analog dimming, PM8001D regulation voltage is independent of the PWM logic voltage level which often has large variations.

For optimum performance, use the PWM dimming frequency in the range of 5kHz to 100kHz The requirement of minimum dimming frequency comes from the Easy Scale detection delay and detection time specification in the dimming mode selection. Since the CTRL pin is logic only pin, adding external RC filter applied to the pin does not work

TYPICAL PERFORMANCE CHARACTERISTICS (Cont')

OPEN LED PROTECTION

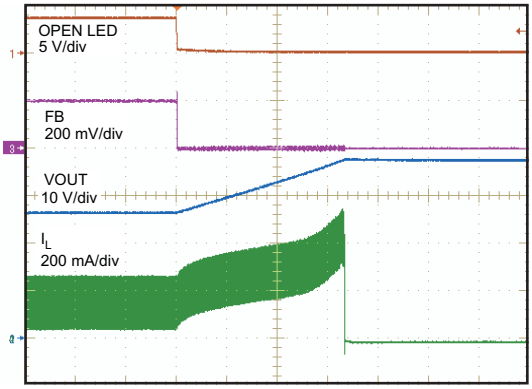


Figure 12.
Figure 8.

OUTPUT RIPPLE at PWM DIMMING

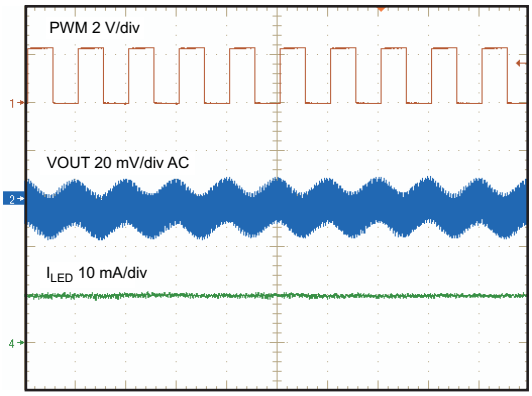


Figure 9.

SWITCHING WAVEFORM

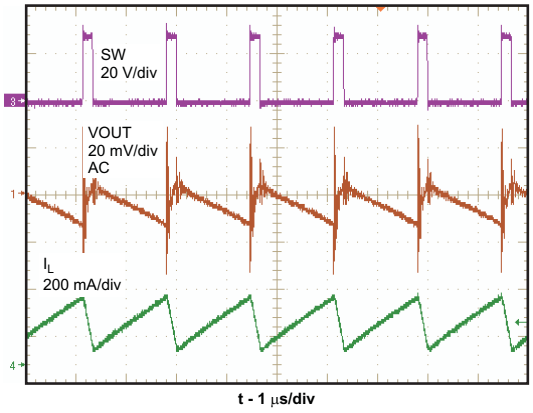


Figure 10.

START-UP

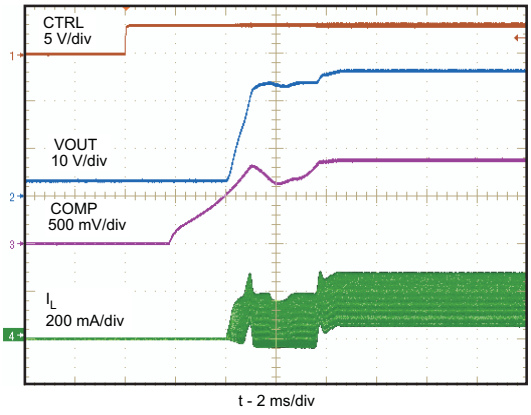
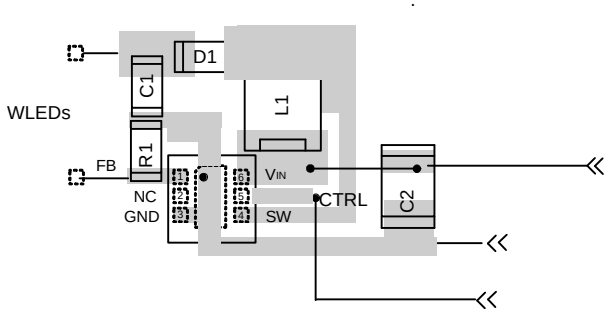


Figure 11.

Layout Consideration

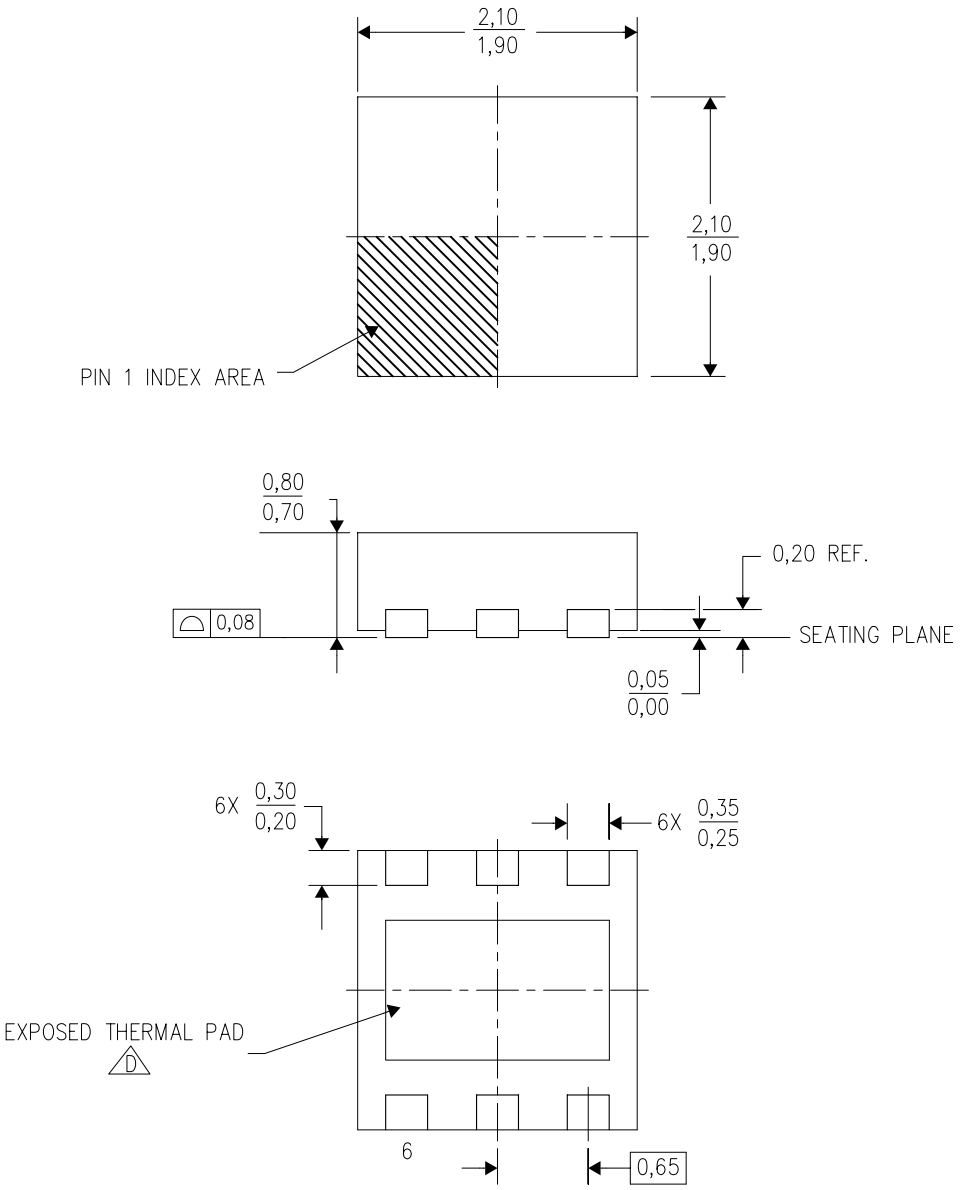
For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The input capacitor should be placed close to the VIN and GND. Connecting the capacitor with VIN and GND pins by short and wide tracks without using any vias for filtering and minimizing the input voltage ripple.
2. The inductor should be placed as close as possible to the SW pin to minimize length of the copper tracks as well as the noise coupling into other circuits.
3. Since the feedback pin and network is a high impedance circuit, the feedback network should be routed away from the inductor. The feedback pin and feedback network should be shielded with a ground plane or track to minimize noise coupling into this circuit.
4. A star ground connection or ground plane minimizes ground shifts and noise is recommended.

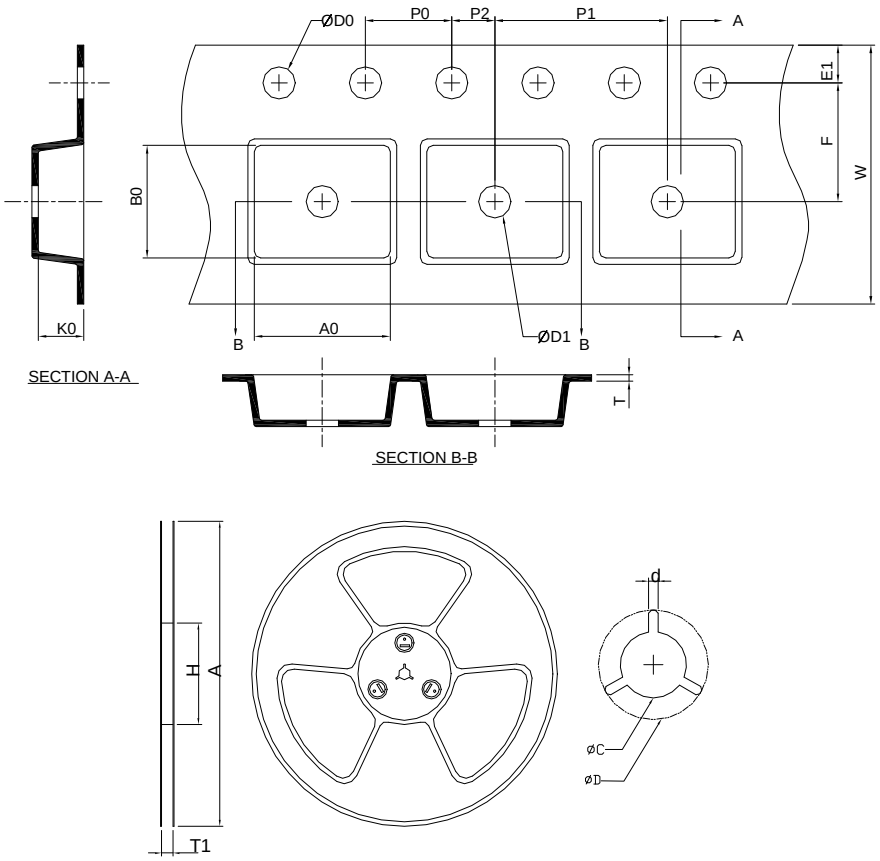


Package Information

TDFN2x2-6



Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TDFN2x2-6	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	2.35±0.20	2.35±0.20	1.30±0.20

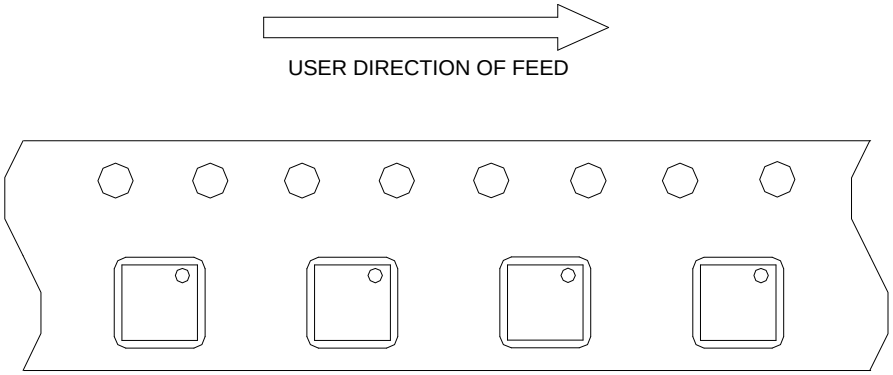
(mm)

Devices Per Unit

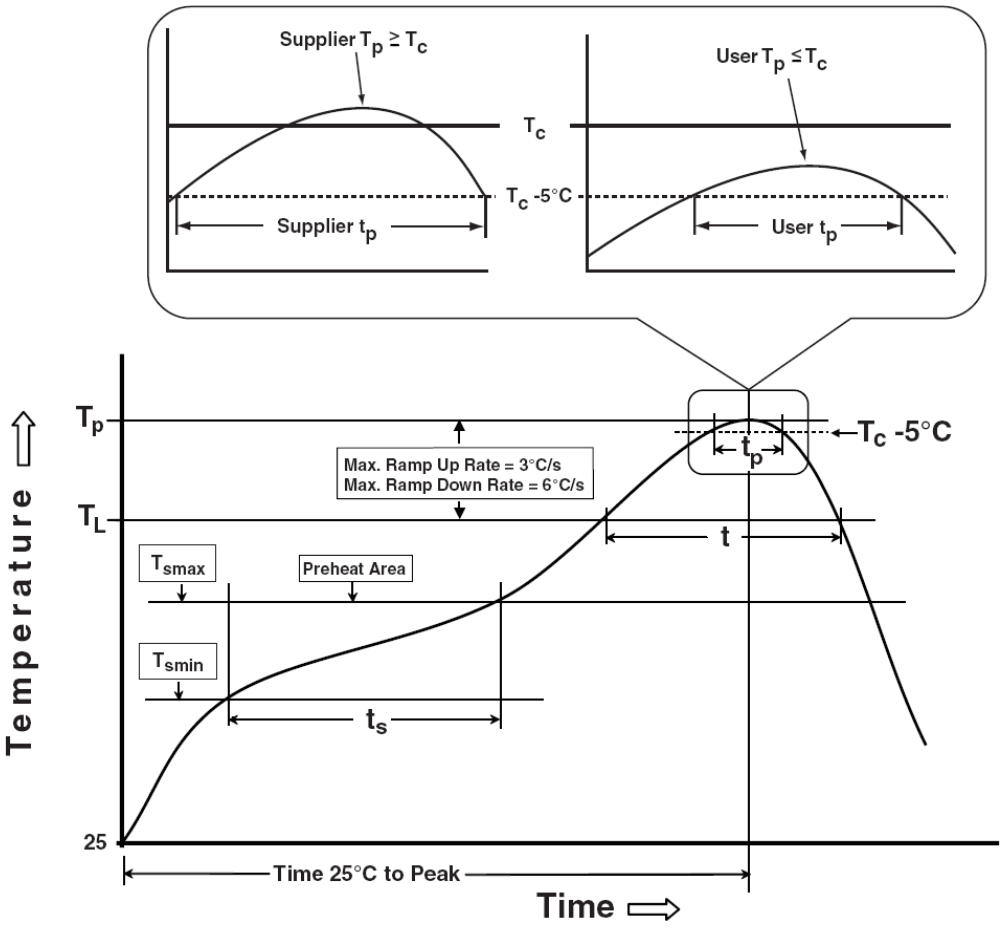
Package Type	Unit	Quantity
TDFN2x2-6	Tape & Reel	3000

Taping Direction Information

TDFN2x2-6



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA