PM8172 System Controller

FEATURES

The PM8172 system controller is ideal for various designs of advanced set-top boxes, DVD players, game stations, and Internet terminal appliances. The PM8172 interfaces to PMC-Sierra's RM5231A, RM7035C and RM7935 MIPS RISC processors.

CPU INTERFACE

- Connects to PMC-Sierra's RM5231A, RM7035C, and RM7935 64-bit MIPS RISC microprocessors.
- Supports CPU bus frequencies up to 100 MHz.

SDRAM CONTROLLER

- 32-bit data bus interface.
- Supports two banks of SDRAM, up to 128 Mbytes in size.
- Provides a deep buffer for CPU to SDRAM burst transfers and for PCI to SDRAM burst transfers.
- Supports bus frequencies up to 100 MHz.

FLASH/ROM INTERFACE

- Supports Flash memory area up to 64 Mbytes, with 8-bit, 16-bit, and 32-bit data access capability.
- Supports a ROM area size up to 4 Mbytes, with 8-bit, 16-bit, and 32-bit data access capability.
- Supports a maximum of 12 chip-select signals.
- Shared with a 68K-like peripheral bus.

PERIPHERAL BUS CONTROLLER

- Provides a 68K-like bus interface.
- Does not require an external latch for addressing.
- Provides an 8-bit and 16-bit data bus interface.
- Shared with the Flash/ROM interface.
- Supports up to four DMA channels.
- Provides cycle posting to avoid performance hits from slower devices.

PCI BUS CONTROLLER

- Provides CPU to PCI buffers for burst transfers.
- Provides a PCI arbiter that supports up to five individual bus master devices.
- Supports 33 MHz bus frequency.
- Provides a 32-bit data bus interface.

INTERRUPT CONTROLLER

- Supports a maskable interrupt to the CPU and a non-maskable interrupt to the CPU for severe events.
- The priority order of interrupt request lines can be assigned by software.
- Module interrupts can be masked on/off independently by setting the corresponding mask registers.

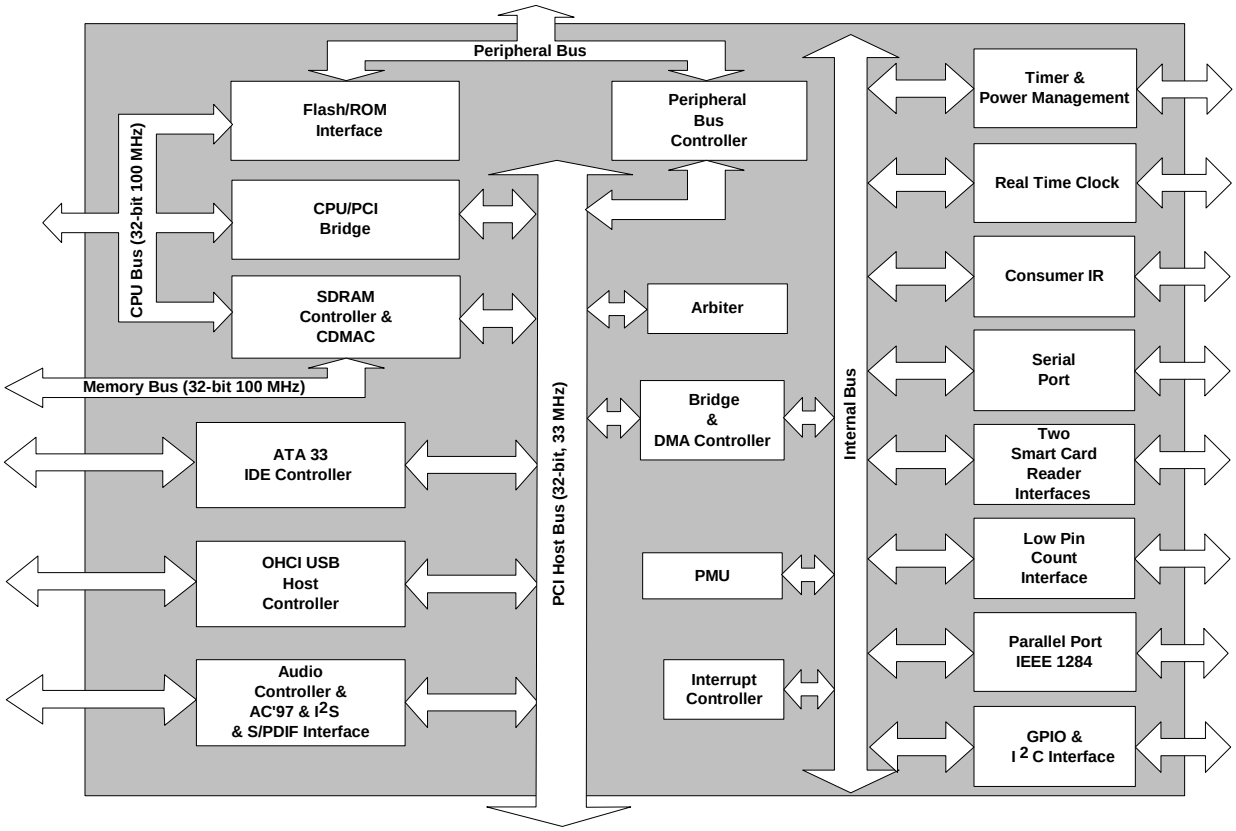
DMA CONTROLLER

- Supports four channel requests for LPC or ECP DMA mode data transfers.
- Supports PCI bus master accessing to the SDRAM.

CHAINING DMA CONTROLLER

- Supports four independent software DMA channels for transferring data between SDRAM and PCI devices.

BLOCK DIAGRAM



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- Supports chaining and non-chaining modes.
- Supports rotating and fixed priority types.

TIMERS

- Provides two 16-bit auto-reload counters with pre-scale (1,1/4,1/8, 1/16) from division of the CPU clock.
- Supports interrupt generation upon the timer time-out.
- Provides one Watchdog timer to monitor the VALIDOUT# signal.

SMART CARD INTERFACE

- Compliant with the Personal Computer Smart Card (PC/SC) Working Group standard.
- Compliant with Smart Card (ISO 7816) protocols.
- Provides card present detection.
- Supports Smart Card insertion power-on.
- Supports one programmable clock frequency, and 7.1 MHz and 3.5 MHz (default) card clocks.
- Supports two channels of the Smart Card interface.
- Supports the T=0, T=1 protocol.

ATA 33 IDE BUS CONTROLLER

- Provides one channel IDE controller for two devices.
- Supports master/DMA/slave mode IDE.
- Supports any 16-bit and 32-bit ordering access to the IDE data port in bus-slave access mode.
- Provides an integrated 8-level 32-bit post-write buffer and a 16-level 16-bit pre-fetch buffer.
- Compatible with ATA/ATAPI-4.
- Compatible with the ANSI ATA proposed PIO modes 0, 1, 2, 3, 4 with flow control, DMA modes 0, 1, 2 and UDMA modes 0, 1, 2.

CONSUMER IR

- Supports 27-58 KHz, 400 - 500 KHz devices.
- Supports up to two CIR channels.
- Channel 0 (CIR0) supports a remote power-on switch and Channel 1 (CIR1) is shared with the GPIO pins.

AUDIO DIGITAL CONTROLLER

- Directly interfaced to AC97 CODEC for controlling voice data to the speaker or from the microphone.
- Provides sample rate conversion.
- Supports an FM synthesizer.
- Supports a digital mixer.
- Supports S/PDIF output.
- Supports I2S input.

16C550 UART

- Supports one standard serial port.

IEEE 1284 PARALLEL PORT

- Standard mode - Bi-directional SPP.
- Enhanced mode - EPP V. 1.7 and EPP V. 1.9 compliant.
- High speed mode - ECP, IEEE 1284 compliant.
- Provides back-drive current reduction.
- Provides printer power-on damage reduction.

USB HOST CONTROLLER

- Supports two USB host ports.
- Supports device bandwidth of 12 Mbps or 1.5 Mbps.
- Supports a power management mode to protect USB Bus power, and over-current detector to protect USB bus from abnormal over-current load.
- Fully compatible with version 1.1. of the USB specification and register-compatible with version 1.0 of the OHCI specification issued by Microsoft, Compaq and NS.

GENERAL PURPOSE I/O (GPIO) FUNCTIONS

- GPIO pins can be programmed as inputs, outputs, or as interrupt inputs.
- Interrupt events can be independently programmed to rising edge or falling edge trigger.
- Maximum 21 pins.

LOW PIN COUNT (LPC) HOST CONTROLLER

- Compliant with the Intel LPC Interface specification Rev. 1.0 (Sept. 29, 1997).
- Supports the Serial IRQ protocol.
- Supports the Encoded DMA protocol.
- For system expansion.

POWER MANAGEMENT

- Provides software controllable power management.
- Provides intelligent power management reducing power consumption for lower power system.
- Provides function wake up through the interrupt, GPIO pins or remote control interface Clock Oscillator and DLL.
- Provides a clock oscillator of 32.768 KHz for the RTC and a clock oscillator of 24.576 MHz for the audio controller.
- Provides two DLLs for reducing clock skew of 100 MHz host processor clock and 33 MHz PCI clock.
- Each clock oscillator and DLL can be programmed to STANDBY mode.

REAL TIME CLOCK

- Compatible with MC146818.
- Provides 241-byte battery-backed CMOS SRAM.
- Provides a daylight saving function.
- Provides 12/24 hour format and BCD/digital format.
- Includes one date alarm and one year alarm

PACKAGE

- 400-pin BGA package.

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All product documentation is available on our web site at: http://www.pmc-sierra.com For corporate information, send email to: info@pmc-sierra.com

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