4-Channel 2.125, 2.5 and 3.125 Gbit/s Transceiver with Half-rate Support

GENERAL DESCRIPTION

The QuadPHY-II is a physical layer transceiver ideal for systems requiring high speed point-to-point communication links. It is applicable for PMA-PMD connections in 10 GE, Infiniband 1 or 4 x 2.5 Gbit/s links, 1 and 2 Gbit/s Fibre Channel, as well as high speed serial backplanes for high capacity systems.

FEATURES

GENERAL

- 10Gbit/s, bi-directional, XAUI to XGMII link supporting the proposed IEEE 802.3ae (the standard is draft and is subject to change).
- Four independent 2.125, 2.5 and 3.125 Gbit/s Serdes for Fibre Channel, Infiniband, 10 GE line cards and high-speed backplane applications.
- Half/Full rate mode selectable per channel.
- Integrated serializer/ deserializer, clock synthesis, clock recovery and 8B/10B encode/decode logic.
- Under 2 Watts typical power.

SERIAL I/O

- Redundant high speed serial I/O channels for convenient switching to redundant fabric.
- High speed outputs with optional pre-emphasis to drive longer backplanes.
- High speed I/O with on-chip termination resistors to directly drive dual-terminated 50 Ohm lines.

PARALLEL I/O

- 10-bit Dual Data Rate (DDR) parallel interface.
- Selectable source simultaneous or source synchronous transmit and receive parallel interfaces.
- Convenient output clock for user friendly ASIC timing.
- Interoperates with SSTL2 and 1.8V LVCMOS standard.

TRUNKING &TIMING

- Integrated Receive FIFO synchronizes incoming data to local clock domain.
- Trunking feature de-skews and aligns all four channels to form a single 10 Gbit/s logical link.

TEST FEATURES

- Extensive control of loopback, BIST, and operating modes via 802.3 compliant MDC/MDIO serial interface.
- On-chip packet generator/checker-provides at-speed diagnostics.
- Built-in error counters per channel.
- Support for IEEE 1149.1 JTAG testing on all pins.

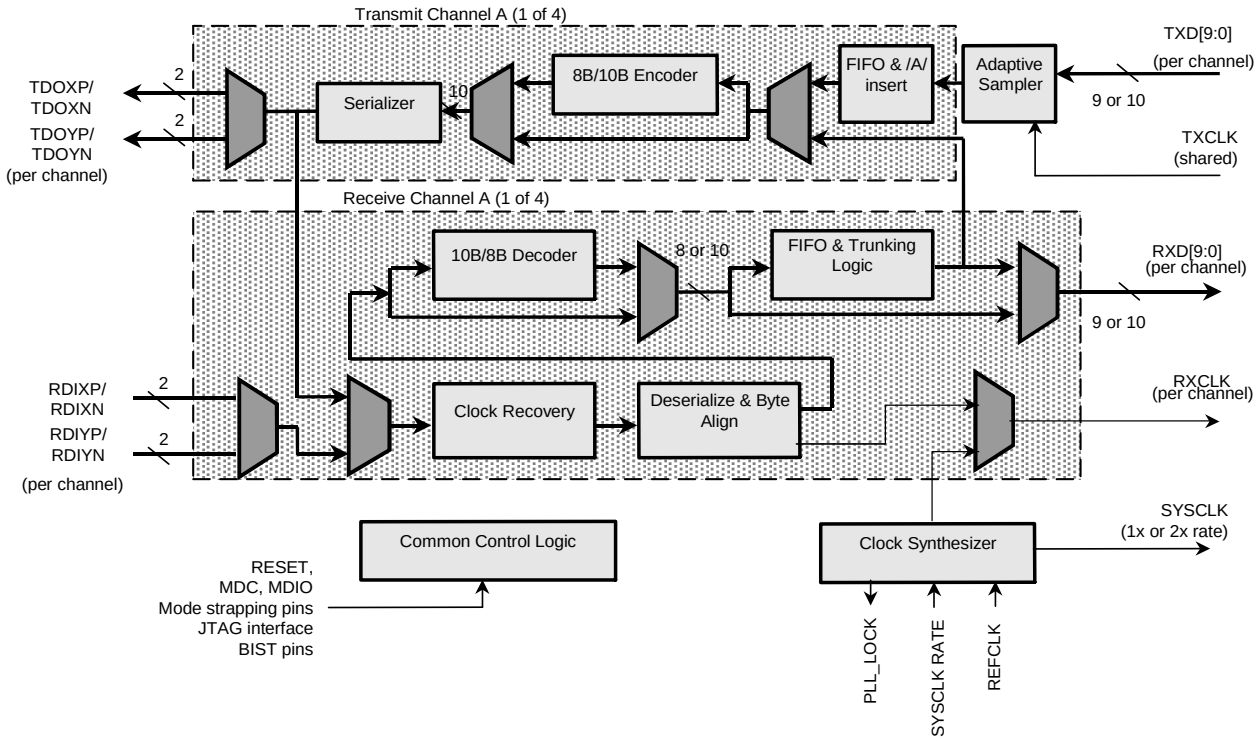
PHYSICAL

- 1.8V, 0.18 micron standard CMOS technology with 2.5V tolerant I/O.
- 289-ball PBGA (19mm x 19mm package).

APPLICATIONS

- High speed serial backplanes
- 10 GE links
- Fibre Channel transceivers
- Infiniband transceivers
- XAUI retimers
- Intra-system interconnect

BLOCK DIAGRAM



EXAMPLE ARCHITECTURE

The figure below shows a multi-service switching platform using QuadPHY-II devices for backplane interconnect and client signal physical interfaces.

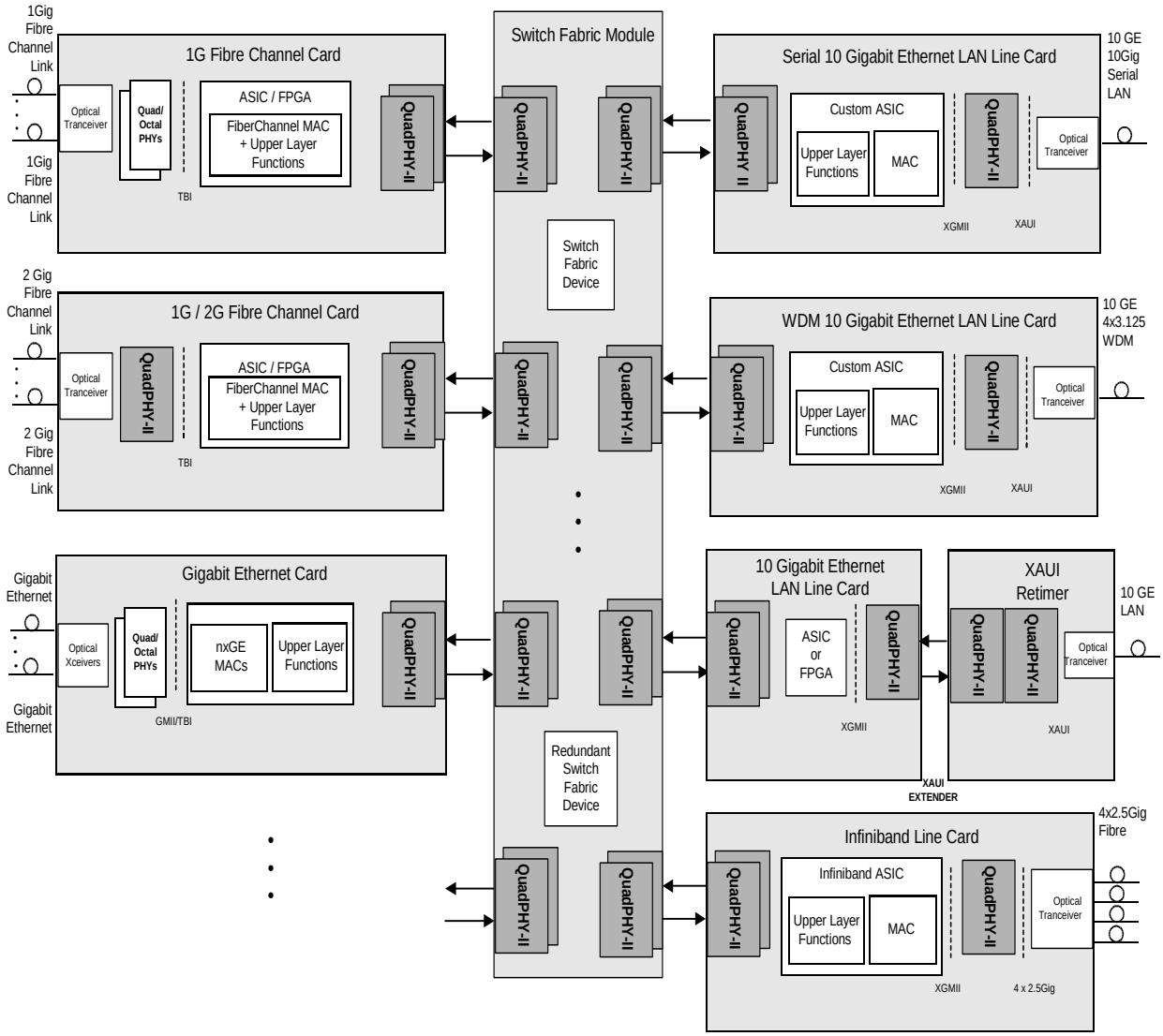
As a serial backplane transceiver, the redundant high-speed links simplify the interface to a working and protect fabric.

The 10GE line cards use the QuadPHY-II as a PHY supporting XAUI on the line side and mating to a 10GE MAC using XGMII.

Infiniband and Fibre Channel line cards applications are also shown. The half-rate mode of the QuadPHY-II enables 1 and 2 Gbit/s support using the same device.

The other applications shown are a XAUI retimer and an XGMII extender where the MAC and Optics module separated by longer distance.

APPLICATION EXAMPLE - MULTI-SERVICE SWITCHING PLATFORM



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