Never stop thinking

SmartLEWIS™ MCU

Smart Low Energy Wireless Systems with a Microcontroller Unit

PMA51xx

RF Transmitter ASK/FSK 315/434/868/915 MHz,
Embedded 8051 Microcontroller,
10-bit ADC,
125 kHz ASK LF Receiver

PMA5110 Version 1.0
PMA5105 Version 1.0

Data Sheet

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Wireless Control

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Revision History: 2010-06-02, Revision 2.1

Previous Revision: 2.0

Page	Subjects (major changes since last revision)
101, 86	Added note to use Library function LFSensitivityCalibration() for LF Carrier Detector Threshold Level Selection.

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1 Product Description

1.1 Overview

The SmartLEWIS™ MCU family comprises an ASK/FSK multiband transmitter for the sub 1GHz ISM frequency bands with an embedded 8051 microcontroller as base functionality. Additionally, the highly integrated single chip family has internal sensors and optional peripheral functions like an analog to digital converter (ADC) and a LF Receiver on chip. The operating voltage range of 1.9 to 3.6 V, the high efficiency Power Amplifier and an advanced power control system make the PMA51xx family ideal for battery operated applications where low current consumption is necessary. The pin-compatible product family requires only a few external components and is the basis for flexible wireless control transmitter platforms enabling applications for different frequency bands, output power levels and feature sets based on only one design - just through different mounting options.

The multiband ASK/FSK transmitter for 315/434/868/915 MHz frequency bands contains a fully integrated VCO, a PLL synthesizer, an ASK/FSK modulator and a high efficiency Power Amplifier with selectable output power. Fine tuning of the center frequency can be done by an on-chip capacitor bank.

The integrated microcontroller is instruction set compatible to the standard 8051 processor. It can be clocked with an internal 12 MHz RC HF or an external oscillator. 6 clock cycles are needed for the execution of one instruction. This results in 2 MIPS[1)] when using the 12 MHz RC HF oscillator. The microcontroller is equipped with various peripherals like a hardware Manchester/BiPhase Encoder/Decoder and a CRC Generator/Checker. To store the microcontroller application program code, a 6 kbyte on-chip FLASH memory is integrated. This FLASH memory is also used for saving the unique ID-number of the chip. A comprehensive software function library with high level commands in ROM allows easy and fast time to market development. The library provides many powerful functions like AES-encryption and EEPROM emulation, what helps to reduce the user code size.

Additional peripherals are an integrated temperature sensor and a low battery voltage sensor. Measurements via these internal sensors and reading signals from analog inputs (e.g. from an external analog sensor) are performed under software control.

Depending on the product variant, PMA51xx offers an embedded multi-channel 10-bit analog to digital converter with flexible high-gain settings as interface for a broad variety of analog sensors and an integrated 125 kHz LF Receiver. The LF Receiver enables wireless wake-up in battery operated applications with ultra-long-lifetime or even contactless configuration of the device.

1) MIPS .. Million Instructions Per Second

1.2 PMAx1xx Product Family

The PMAx1xx product family contains various product variants listed in **Table 1 “PMA51xx and PMA71xx Family” on Page 14**.

Note: This data sheet documents the full feature set of the PMA5110, which has the full feature set of the PMA51xx product family available. When using the PMA51xx family data sheet for product variants other than the PMA5110, please keep in mind that not all of the features and data described are relevant for these other members of the family.

Following table shows the functional differences of the PMA51xx and PMA71xx family members:

Table 1 PMA51xx and PMA71xx Family

Product Name	Ordering Code	RF Transmitter	Embedded 8051 MCU	ADC	125 kHz LF Receiver	Automotive Qualified
PMA7110	SP000430596	X	X	X	X	no
PMA7107	SP000450412	X	X		X	no
PMA7106	SP000450410	X	X	X		no
PMA7105	SP000450408	X	X			no
PMA5110	SP000373573	X	X	X	X	yes
PMA5105	SP000463432	X	X			yes

The PMA51xx products are supporting a temperature range from -40 to +125°C and are full automotive qualified, tailored for automotive applications and industrial applications in harsh environment. Additionally, Infineon offers the PMA71xx product family with a temperature range of -40 to +85°C, tailored for consumer and industrial applications.

1.3 Applications

- Remote Keyless Entry (RKE)
- Security and alarm systems requiring high quality standards
- Industrial controls in harsh environments
- Wireless sensing

1.4 Key Features

General:

- Supply voltage range from 1.9 V up to 3.6 V
- Operating temperature range from -40 to +125°C
- Low power down current consumption < 0.6 µA
- Advanced power control system for lowest system current consumption, switching the microcontroller or transmitter part into POWER DOWN or IDLE state whenever possible
- PG-TSSOP-38 package

Transmitter:

- Multiband RF Transmitter for ISM frequency band 315/434/868/915 MHz
- SW configurable transmit power of 5/8/10 dBm into 50 Ohm load
- Selectable transmit data rates up to 32 kbit/s (64 kchips/s) for the temperature range -40°C to +85°C and 20 kbit/s (40 kchips/s) for temperatures above +85°C
- RF Encoder supporting Manchester-, BiPhase- or NRZ coded data (Chip Mode)

- ASK/FSK modulation capability
- FSK frequency deviation up to 100 kHz
- Fully integrated VCO and PLL synthesizer
- Crystal oscillator tuning on chip

Microcontroller:

- 8051 instruction set compatible microcontroller (cycle-optimized)
- 6 kbyte free programmable FLASH code memory
- 2 blocks of 128 byte FLASH data memory, alternatively usable as 31 byte emulated EEPROM
- ROM embedded software function library with preprogrammed functions and high level commands for easy programming
- 128 bit AES (Advanced Encryption Standard) embedded as software function
- 256 bytes RAM (128 bytes configurable to keep content in POWER DOWN state)
- 16 bytes XData memory (supplied in POWER DOWN state)
- 2 MIPS when using internal 12 MHz RC HF oscillator

Peripherals:

- 125 kHz ASK LF Receiver
- LF Receiver data rate for typical 3.9 kbit/s (Manchester/BiPhase coded)
- 10 bit ADC with 3 pair differential channels and flexible high-gain settings (e.g. as inputs for external sensors)
- 10 free programmable bidirectional General Purpose Input Output pins (GPIO) with on-chip pull-up/pull-down resistors. 8 of them have wake-up functionality
- On-chip temperature sensor
- On-chip voltage sensor for low battery voltage measurement
- Brownout Detector
- Manchester/BiPhase Encoder and Decoder
- 16 bit hardware CRC Generator
- 8 bit Pseudo Random Number Generator
- I^2C bus interface
- SPI bus interface

Miscellaneous:

- Watchdog Timer
- 4 independent 16 bit timers
- Wake-up from POWER DOWN state possible by different sources: Interval Timer, Watchdog Timer, LF Receiver or external wake-up sources connected to GPIOs
- On-chip debugging via I^2C interface
- 48 bit unique-ID on chip

1.5 Pin Diagram

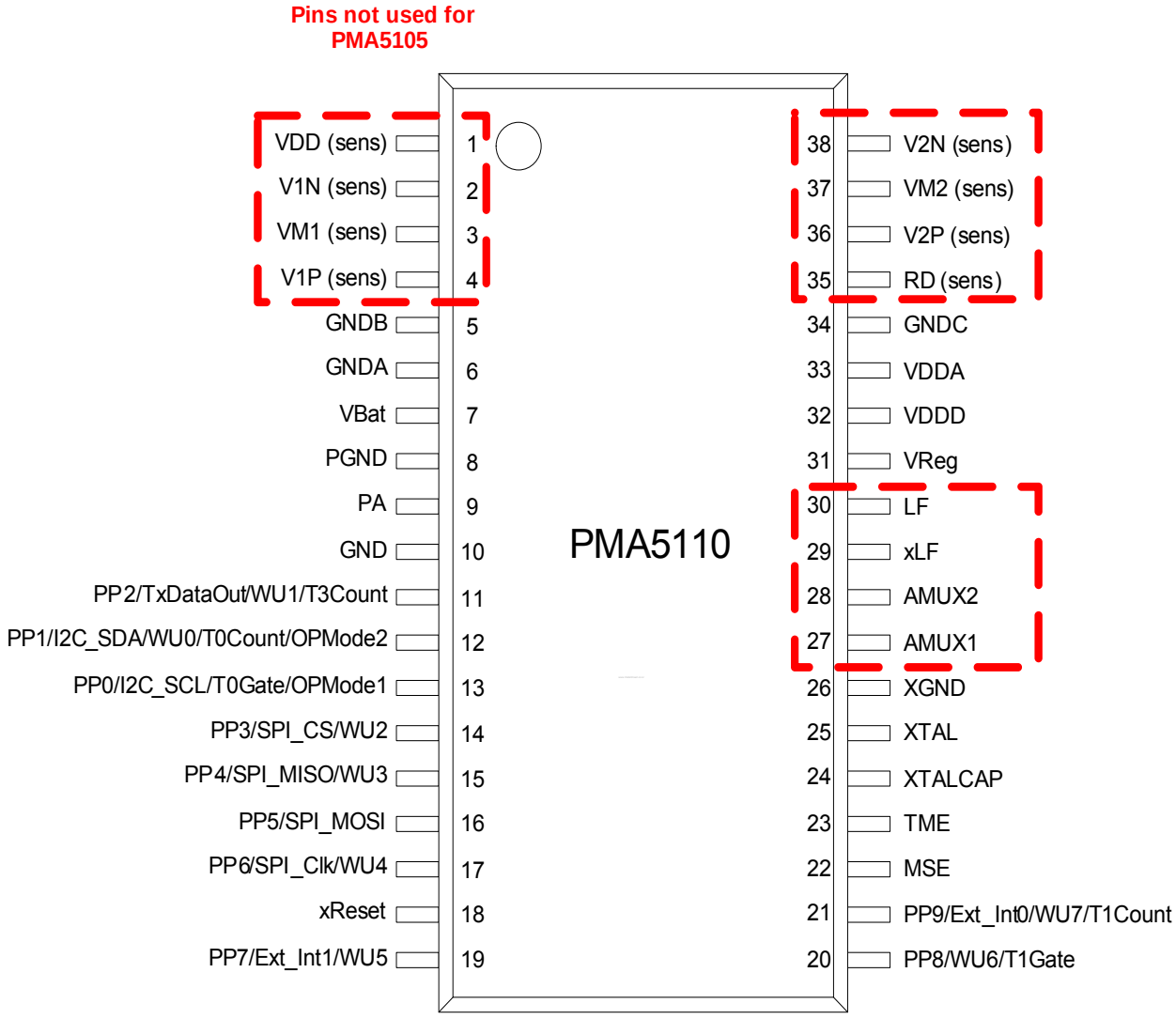


Figure 1 Pin-outs of PMA51xx

1.6 Pin Description

Abbreviations

Standard abbreviations for I/O are shown in **Table 2**.

Table 2 Abbreviations for Pin Type

Abbreviations	Description
I	Standard input-only pin. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
AO	Output. Analog levels.
AI/O	Input or Output. Analog levels.
PWR	Power
GND	Ground

Table 3 Pin Description

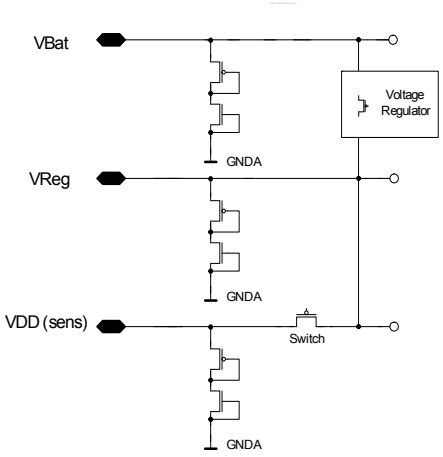
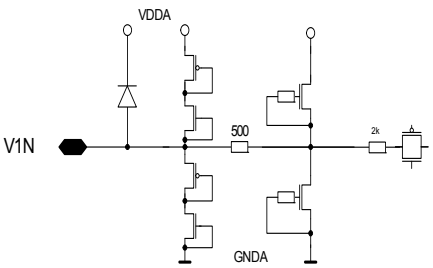
Pin No.	Name	Pin Type	Buffer Type	Function
1	VDD_sens	AO	Supply_output 	**Sensor Bridge Positive Supply** Output of V_{Reg} during measurement.
2	V1N_sens	AI	Analog 	**Channel 6, High-gain ADC Input** Negative input connect to sensor bridge. Output of wheatstone bridge sensor

Table 3 Pin Description (cont'd)

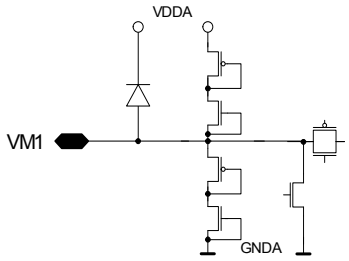
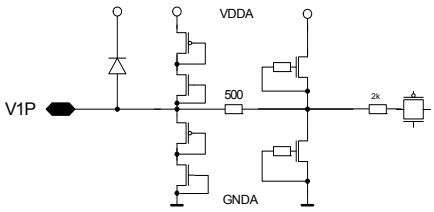
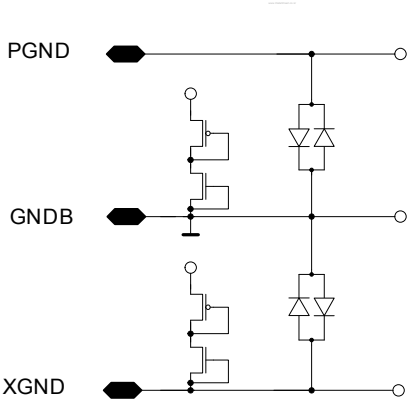
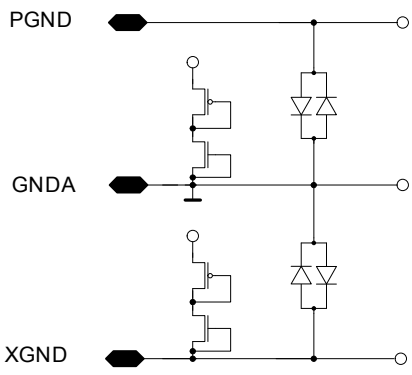
Pin No.	Name	Pin Type	Buffer Type	Function
3	VM1_sens	GND	Supply 	**Channel 6, High-gain ADC Input** Sensor bridge negative supply. Same voltage as chip GND.
4	V1P_sens	AI	Analog 	**Channel 6, High-gain ADC Input** Positive input connect to sensor bridge. Output of wheatstone bridge sensor
5	GNDB	GND	Supply 	**Ground**
6	GNDA	GND	Supply 	**Ground**

Table 3 Pin Description (cont'd)

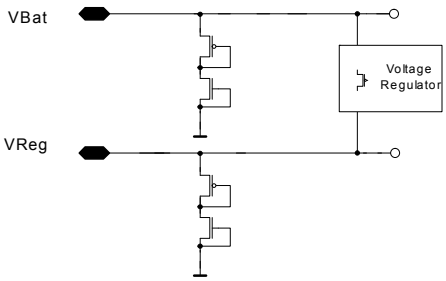
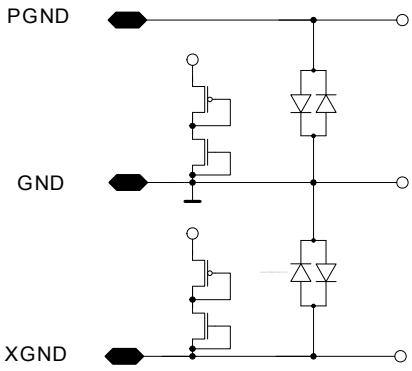
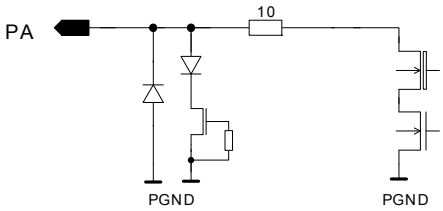
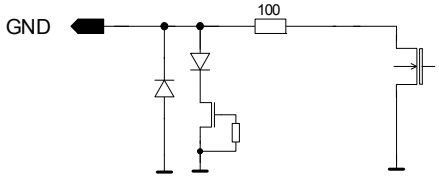
Pin No.	Name	Pin Type	Buffer Type	Function
7	VBat	PWR	Supply 	**Battery Supply Voltage Regulators**
8	PGND	GND	Supply 	**Power Amplifier Ground** Double bond
9	PA	AO	Analog 	**Power Amplifier Output Stage**
10	GND	GND	Supply(Analog) 	**Ground**

Table 3 Pin Description (cont'd)

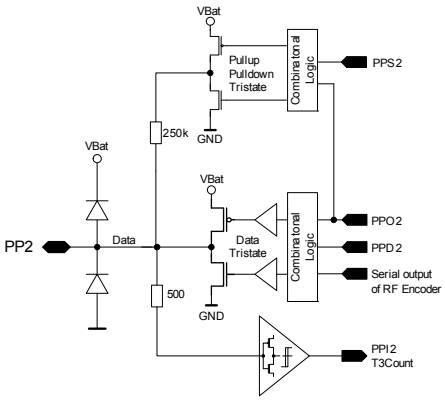
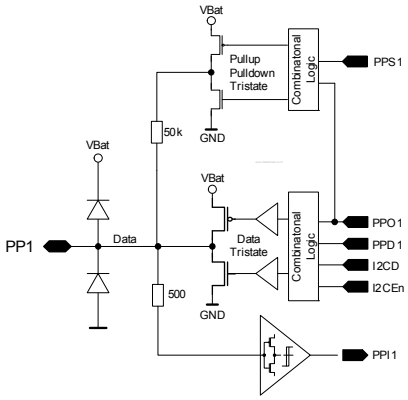
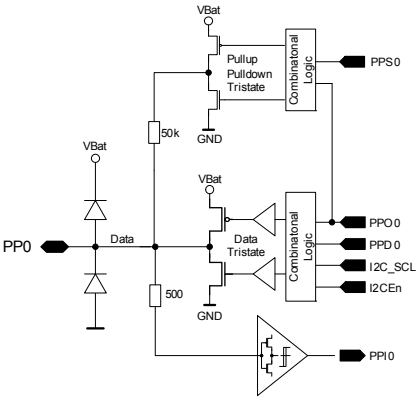
Pin No.	Name	Pin Type	Buffer Type	Function
11	PP2/TxDataOut/ WU1/T3Count/	I/O	Digital 	**PP2** -) Serial output of Manchester / Biphase encoded data. -) GPIO -) External wake-up source 1 -) Clock source for Timer 3 -) Internal, switchable pull-up/pull-down.
12	PP1/I2C_SDA/ WU0/T0Count/ OPMode2	I/O	Digital 	**PP1** -) I2C bus interface data -) GPIO -) External wake-up source 0 -) Clock source for Timer 0 -) Select operation mode -) Internal, switchable pull-up/pull-down.
13	PP0/I2C_SCL/ T0Gate/OPMode1	I/O	Digital 	**PP0** -) I2C bus interface clock -) GPIO -) External enable for Timer 0 -) Select operation mode -) Internal, switchable pull-up/pull-down.

Table 3 Pin Description (cont'd)

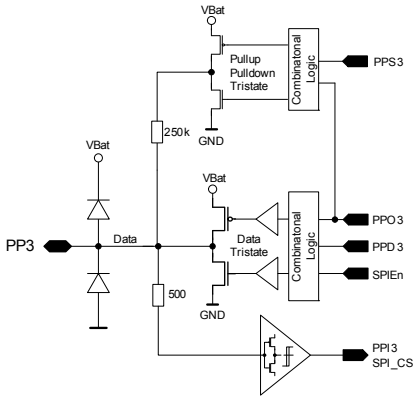
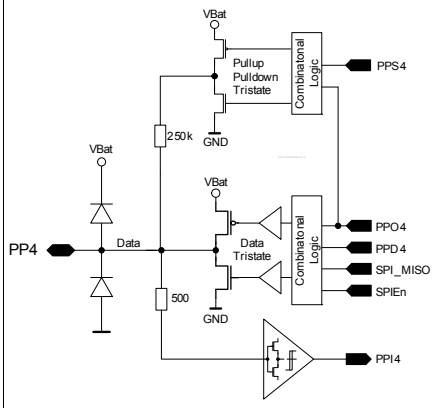
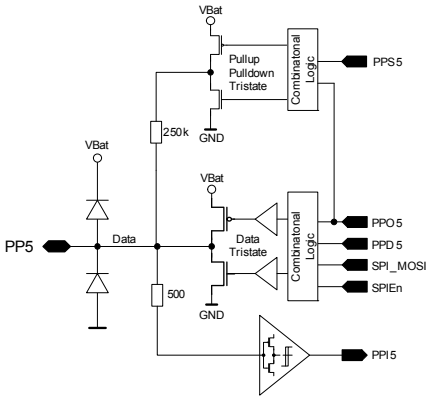
Pin No.	Name	Pin Type	Buffer Type	Function
14	PP3/SPI_CS/WU2	I/O	Digital 	**PP3** -) SPI bus interface chip select -) GPIO -) External wake-up source 2 -) Internal, switchable pull-up/pull-down.
15	PP4/SPI_MISO/ WU3	I/O	Digital 	**PP4** -) SPI bus interface master in slave out -) GPIO -) External wake-up source 3 -) Internal, switchable pull-up/pull-down.
16	PP5/SPI_MOSI	I/O	Digital 	**PP5** -) SPI bus interface master out slave in -) GPIO -) Internal, switchable pull-up/pull-down.

Table 3 Pin Description (cont'd)

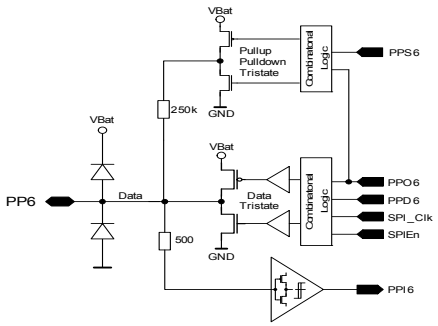
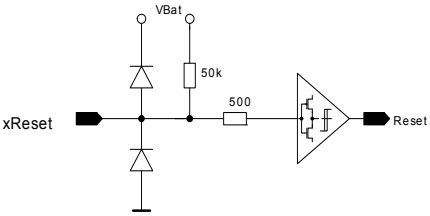
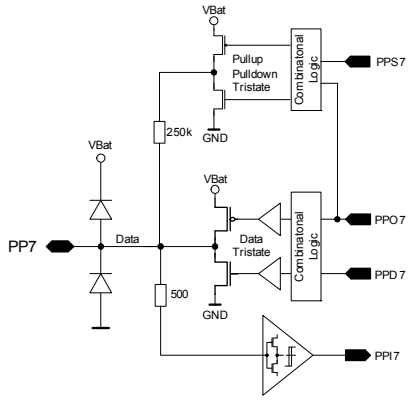
Pin No.	Name	Pin Type	Buffer Type	Function
17	PP6/SPI_Clk/WU4	I/O	Digital 	**PP6** -) SPI bus interface clock -) GPIO -) External wake-up source 4 -) Internal, switchable pull-up/pull-down.
18	xReset	I	Digital 	**External Reset** Low active
19	PP7/Ext_Int1/WU5	I/O	Digital 	**PP7** -) GPIO -) External interrupt source 1 -) External wake-up source 5 -) Internal, switchable pull-up/pull-down.

Table 3 Pin Description (cont'd)

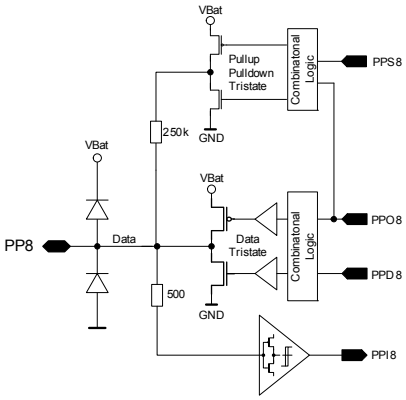
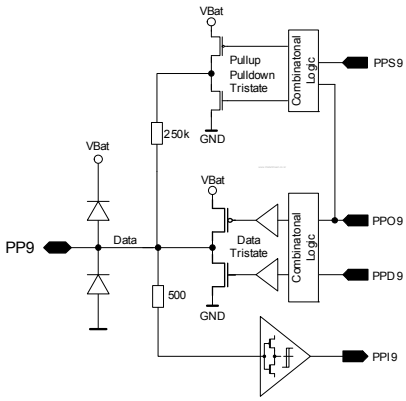
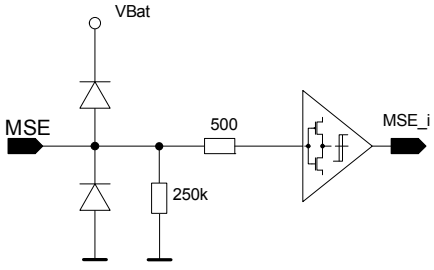
Pin No.	Name	Pin Type	Buffer Type	Function
20	PP8/WU6/T1Gate	I/O	Digital 	**PP8** -) GPIO -) External wake-up source 6 -) External enable for Timer 1 -) Internal, switchable pull-up/pull-down.
21	PP9/Ext_Int0/WU7 /T1Count	I/O	Digital 	**PP9** -) GPIO -) External interrupt source 0 -) External wake-up source 7 -) Clock source for Timer 1 -) Internal, switchable pull-up/pull-down.
22	MSE	I	Digital 	**Mode Select Enable** High active, set to GND in NORMAL Mode.

Table 3 Pin Description (cont'd)

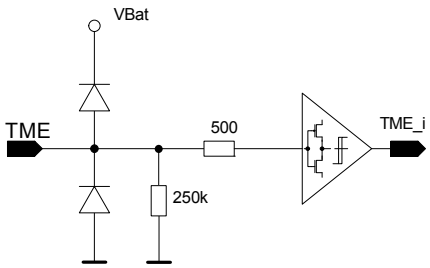
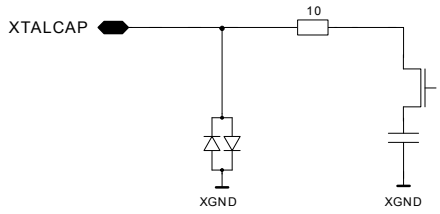
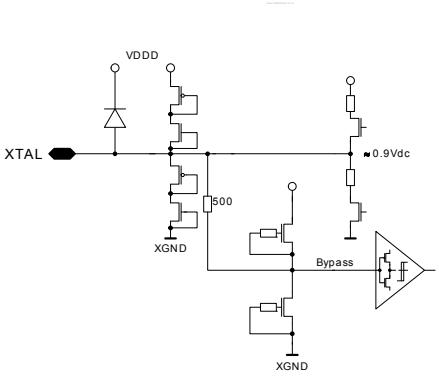
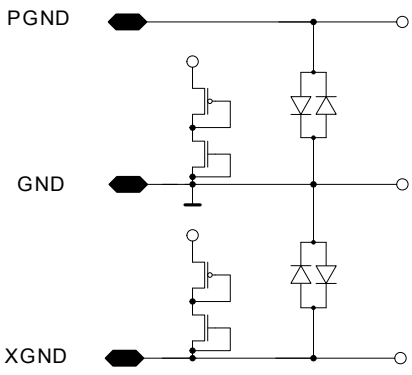
Pin No.	Name	Pin Type	Buffer Type	Function
23	TME	I	Digital 	**Test Mode Enable, n.a. for Normal Application** Has to be set to GND in NORMAL Mode
24	XTALCAP	AI	Analog 	**Crystal Oscillator Load Capacitance**
25	XTAL	AI	Analog 	**Crystal Oscillator Input**
26	XGND	GND	Supply 	**Crystal Oscillator Ground**

Table 3 Pin Description (cont'd)

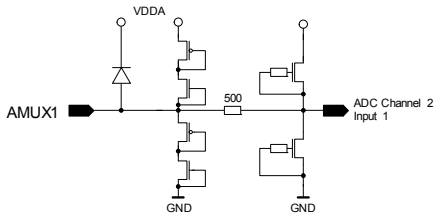
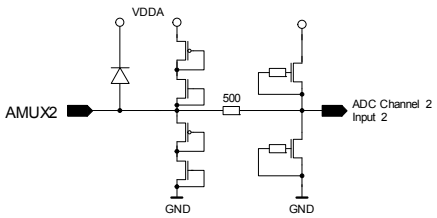
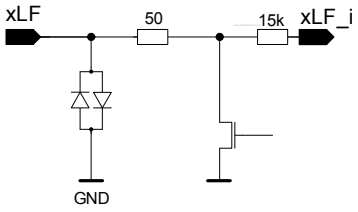
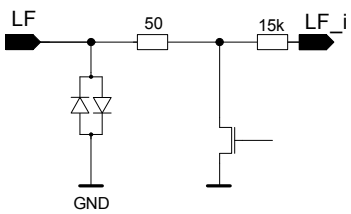
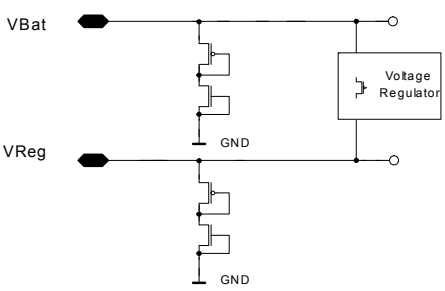
Pin No.	Name	Pin Type	Buffer Type	Function
27	AMUX1	AI	Analog 	**Additional Differential ADC Standard Input1 for External Sensor** Connect to GND if not use.
28	AMUX2	AI	Analog 	**Additional Differential ADC Standard Input2 for External Sensor** Connect to GND if not use.
29	xLF	AI	Analog 	**Differential LF Receiver Input2** 125kHz Input.
30	LF	AI	Analog 	**Differential LF Receiver Input1**
31	VReg	AO	Supply 	**Internal Voltage Regulator Output** Connect to decoupling capacitor (C_{BCAP}=100 nF) Regulated Power supply.

Table 3 Pin Description (cont'd)

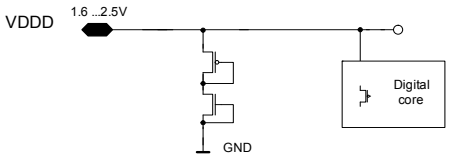
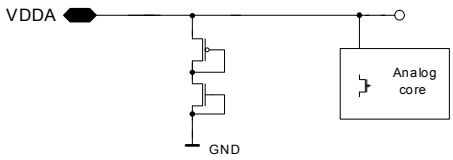
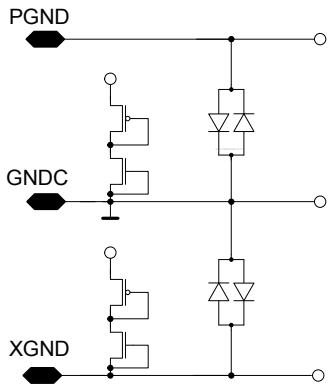
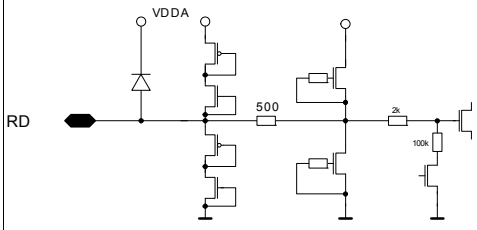
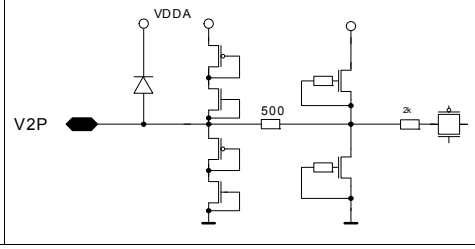
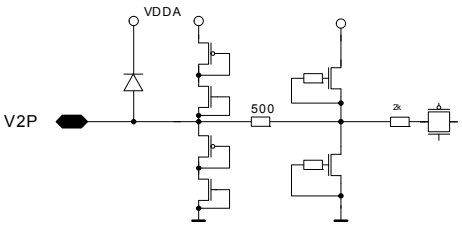
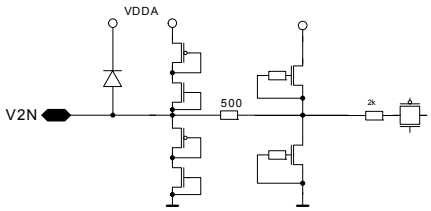
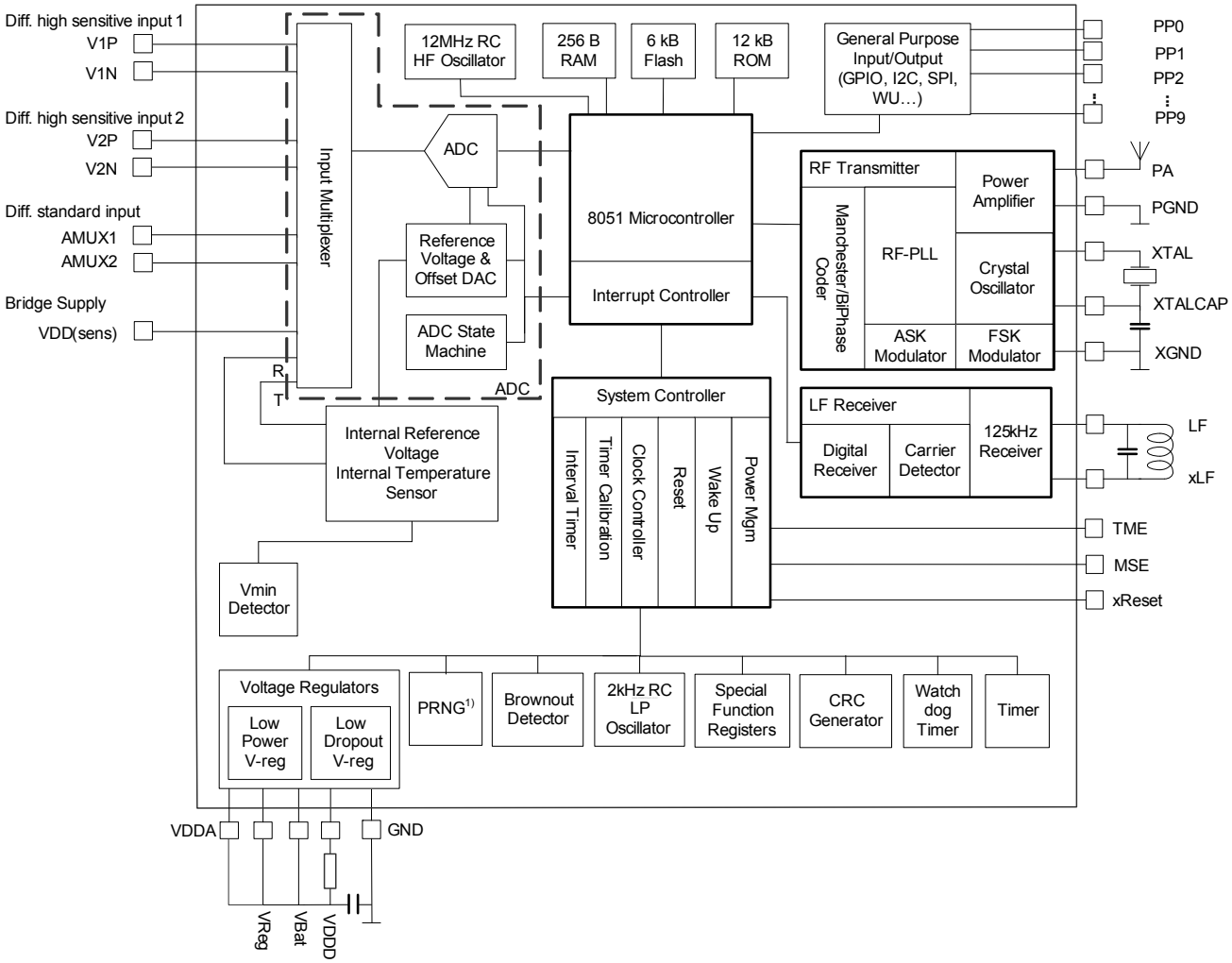
Pin No.	Name	Pin Type	Buffer Type	Function
32	VDDD	PWR	Supply 	**Digital Supply**
33	VDDA	PWR	Supply 	**Analog Supply**
34	GNDC	GND	Supply 	**Ground**
35	RD_sens	AI	Analog 	**Diagnostic Resistor** Use only by having diagnostic resistor on sensor bridge for high-gain ADC input, otherwise no connection
36	V2P_sens	AI	Analog 	**Channel 7, High-gain ADC Input** Positive input connect to sensor bridge. Output of Wheatstone bridge sensor.

Table 3 Pin Description (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
37	VM2_sens	GND	Supply 	**Channel 7, High-gain ADC Input** Sensor bridge negative supply. Same voltage as chip GND.
38	V2N_sens	AI	Analog 	**Channel 7, High-gain ADC Input** Negative input connect to sensor bridge. Output of Wheatstone bridge sensor.

1.7 Functional Block Diagram



1) PRNG .. Pseudo Random Number Generator

Figure 2 PMA51xx Block Diagram

2 Functional Description

2.1 Operating Modes and States

The PMA51xx can be operated in three different operating modes.

- NORMAL mode
- PROGRAMMING mode
- DEBUG mode

2.1.1 Operating Mode Selection

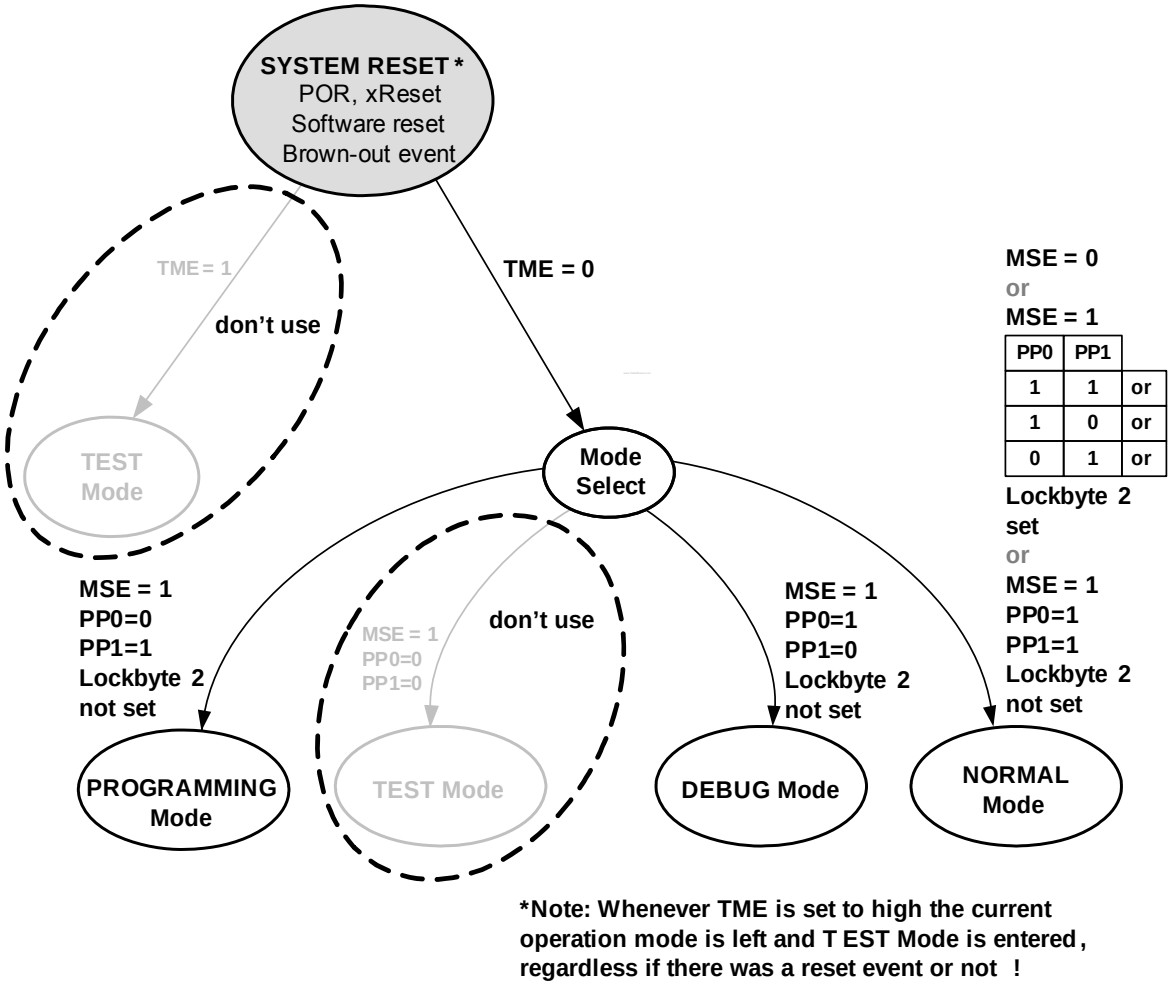


Figure 3 Operating Mode Selection of the PMA51xx after Reset

The Mode Select is entered after the System Reset expires. The levels on the I/O pins PP0 and PP1 are latched by the System Controller and read by the operating system to determine the mode of operation of the device according to **Table 4 "Operating Mode Selection after Reset" on Page 30**. **Figure 3 "Operating Mode Selection of the PMA51xx after Reset" on Page 29** shows how the MSE and Lockbyte 2 are also checked to determine the operating mode. The MSE, PP0, and PP1 levels must not change after reset release during the whole t_{MODE} period (see **Figure 5 "Power On Reset - Operating Mode Selection" on Page 31**).

Table 4 Operating Mode Selection after Reset

TME	MSE	Lockbyte 2	PP0	PP1	Operating Mode	Device Control	Hardware Restrictions
0	0	x	x	x	NORMAL	CPU executing from 4000_H	FLASH write access depends on Lockbyte setting
0	1	x	0	0	TEST[1)]		
0	1	Not set	0	1	PROGRAMMING	PROGRAMMING mode handler	None
0	1	Set	0	1	NORMAL	CPU executing from 4000_H	FLASH write restriction[2)]
0	1	Not set	1	0	DEBUG	DEBUG mode handler	FLASH write disabled
0	1	Set	1	0	NORMAL	CPU executing from 4000_H	FLASH write restriction[2)]
0	1	x	1	1	NORMAL	CPU executing from 4000_H	FLASH write restriction[2)]

1) Do not use

2) FLASH programming and erasing is possible via Library functions

Note: FLASH protection is done by hardware.

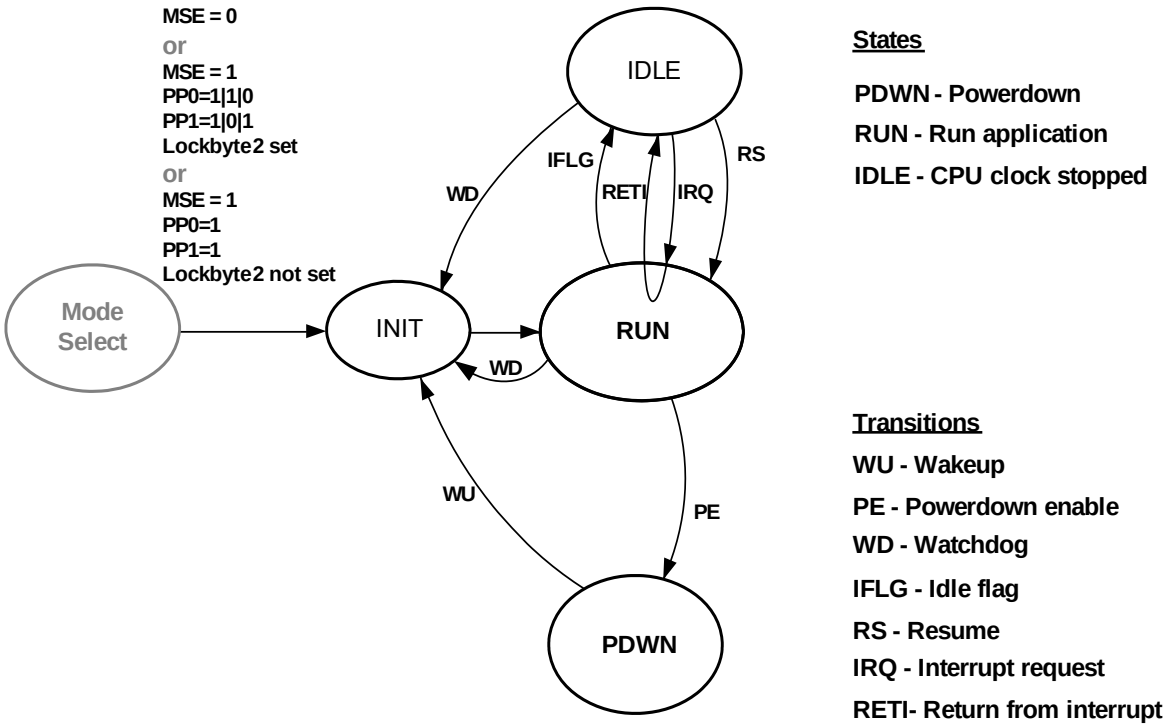


Figure 4 NORMAL mode - State Transition Diagram

For low power consumption the PMA51xx supports different operating states - RUN state, IDLE state and POWER DOWN state. The device operation in these states is as described below.

Transitions between these states are either controlled by application software or managed automatically by the System Controller.

- PDWN: Power down (CPU and peripherals are not supplied)
- IDLE: CPU clock stopped, peripherals are still running

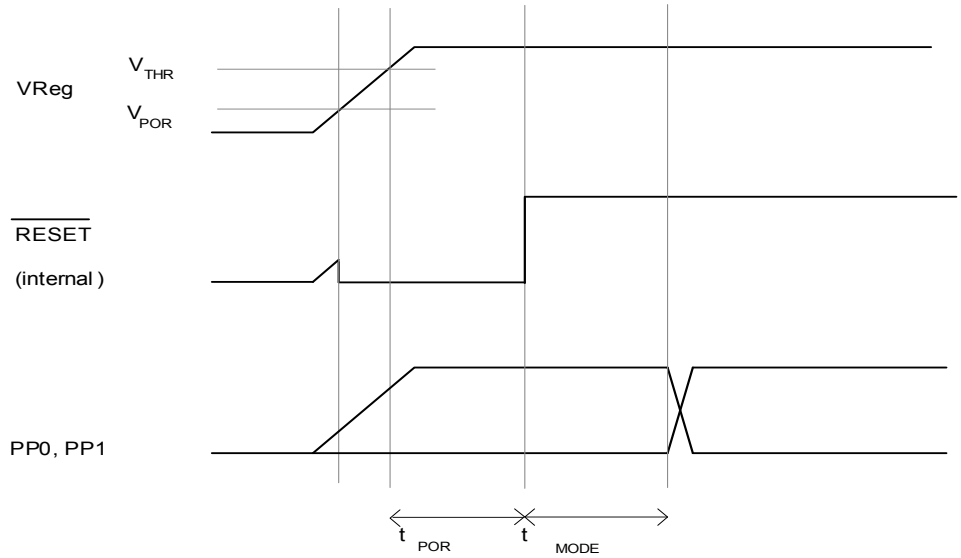


Figure 5 Power On Reset - Operating Mode Selection

During the time interval t_{MODE}, the levels of PP0, PP1 and MSE are read, and the operation mode of the device determined according to **Table 4 “Operating Mode Selection after Reset” on Page 30**. The levels on these pins must be stable during the whole t_{MODE} period.

The PMA51xx's Power-On Reset circuit is activated if V_{reg} rises above V_{POR}. The internal blocks are held in Reset state until Vreg exceeds the level of V_{THR}.

When this Reset state is released, a further time of t_{MODE} is needed for reading the levels on PP0, PP1, and MSE. After t_{MODE} has elapsed, the device starts operation in the selected mode.

*Note: See **Table 44 “Power On Reset” on Page 193** for details on Power-On Reset characteristics.*

2.1.2 State Description

2.1.2.1 INIT state

This is a transient state after the System Reset, which is entered when the settings of PP0, PP1, MSE, TSE, and the Lockbyte 2 lead to NORMAL mode (please refer to **Table 4 “Operating Mode Selection after Reset” on Page 30**). It is also a transient state in NORMAL mode before the state change between PDWN and RUN or when a watchdog reset occurs in IDLE or RUN state. In INIT state, the relevant SFRs get reset to their default values. Then the application program in FLASH is started at 4000_H and the device enters RUN state.

2.1.2.2 RUN state

In the RUN state, the CPU executes the FLASH code. Peripherals are on or off according to the application program and the Watchdog Timer is active. All wake-up events except in ExtWUFs are ignored in the RUN state but the corresponding wake-up flags get set and can be read and cleared. Activity on the external wake-up pins can be monitored in the corresponding SFR P1In or P3In.

2.1.2.3 IDLE state

In the IDLE state, the CPU clock is disabled but peripherals (Timers, ADC, RF-TX, LF-RX, SPI and I^2C interface) continue normal operation. If a resume event occurs, the RUN state is reentered immediately. The Watchdog Timer is active and reset automatically when entering IDLE state. All wake-up events are ignored in IDLE state, but the corresponding flags are set if a wake-up occurs and can be evaluated once the device returns to the RUN state.

If a peripheral requests an interrupt or an external interrupt occurs, the IDLE state is left for RUN state, the interrupt service routine is executed, and on the next RETI (return from interrupt) instruction the IDLE state is re-entered in case no resume event has occurred in between.

Resume events

The resume source can be identified by reading the Resume Event Flag, REF. Resume events may occur on the following events:

- RF Transmitter buffer empty
- RF transmission finished
- LF Receiver buffer full
- Timer 2 underflow
- A/D conversion finished
- 2 kHz RC LP oscillator calibration finished
- Clock change from 12 MHz RC HF oscillator to crystal oscillator finished

Interrupt requests

Interrupts during IDLE state may be requested by embedded peripherals or external events.

- External (pin) interrupt 0/1
- Timer 0/1/2/3
- I2C interface
- SPI interface
- LF Receiver
- Manchester/Biphase Encoder

2.1.2.4 POWER DOWN state (PDWN)

In the POWER DOWN state, the CPU and its peripherals are powered down. The System Controller, the XData memory, and optionally the lower 128-byte internal RAM are kept powered. Furthermore some SFRs are kept powered in the POWER DOWN state (see **Table 12 “Special Function Registers Overview” on Page 61**). The LF Receiver will be switched on periodically if the LF On/Off Timer is enabled. Wake-up flags are cleared automatically when going to POWER DOWN.

Wake-up Events

A wake-up event occurs when a peripheral or external source causes the system to power up again. The wake-up source can be identified by reading SFRs WUF and ExtWUF. Wake-up Events may occur on following events:

- At least one of the External wake-up pins changed its state to the configured one
- Interval Timer underflow occurred
- LF Receiver carrier detected
- LF Receiver pattern matched
- LF Receiver sync matched

2.1.2.5 State Transitions

With reference to **Figure 4 “NORMAL mode - State Transition Diagram” on Page 30**, the following state transitions can occur:

Table 5 State Transitions in NORMAL mode

State Transition	Description
RUN state => IDLE state (IFLG)	The application program sets SFR bit CFG0.5[IDLE][1] to enter IDLE state. (see **Configuration Register 0 on page 46**) *Note: If no peripheral that can create a RESUME event is active, IDLE state will not be entered and the application will continue operation.*
IDLE state => RUN state (RS, IRQ)	**RS:** A peripheral unit (Timer 2, ADC, RF Transmitter, LF Receiver, system clock source switch) creates a resume event. The application continues with the instruction after the Idle bit setting (see **Resume Event Flag Register on page 39**). **IRQ:** An interrupt occurs. This interrupt allows the immediate execution of the interrupt service routine. With the return from interrupt instruction, the device returns to IDLE state if no resume event has been generated in between.
IDLE state => INIT state (WD[2]) RUN state => INIT state (WD)	If the Watchdog Timer elapsed, the application will restart by initialization of some SFRs. Only the SFRs which are not supplied in POWER DOWN state are initialized after the Watchdog Timer elapsed (see **Table 12 “Special Function Registers Overview” on Page 61**). The Watchdog Timer wake-up may be identified by **Wake-up Flag Register on page 40**
RUN state => POWER DOWN state (PDWN)	Entering this state is always software-controlled by setting CFG0.7[PDWN]. The application program calls a Library function to enter POWER DOWN state whenever needed.
POWER DOWN state => INIT state	A wake-up event will restart the application and set the SFR WUF resp. ExtWUF accordingly. The Watchdog Timer is re-initialized (see **External Wake-up Flag Register on page 37**).
INIT state => RUN state	This state change is initiated automatically by the System Controller as soon as INIT state is finished.

1) It is mandatory that the instruction setting the CFG0.5[IDLE] is followed by a NOP instruction.

2) WD .. Watchdog Timer

Wake-up duration from POWER DOWN state through INIT state to RUN state typically lasts 1410 µs. The time is the sum of the time for the power supply to get stable (100 µs), the startup time of the oscillator (1150 µs) and the time for the operating system to get initialized (160 µs @ 12-MHz CPU clock).

2.1.2.6 Status of PMA5110 Blocks in Different States

Depending of the actual state in NORMAL mode, the internal blocks of the PMA5110 are active, inactive or have no supply to reduce power consumption. The next table gives an overview of the various blocks in the different device states.

Table 6 Status of Important PMA5110 Blocks in Different States

Peripheral Unit	RUN state	IDLE state	POWER DOWN state
Power-On Reset	Active	Active	Active
Brown-Out Detector	Active	Active	Inactive; power down
Low-Power voltage supply	Active	Active	Active
System Controller	Active	Active	Active
Wake-up Logic	Active	Active	Active
CPU	Active	Inactive	No supply
Non-volatile SFRs (System Controller)	Active	Inactive; content not lost	Inactive; content not lost
Manchester/Biphase Coder, Timer	Software selectable	Software selectable	No supply
Peripheral modules: CRC, MLFSR	Software selectable	Inactive	No supply
Peripheral modules: I2C, SPI, ADC	Software selectable	Software selectable	No supply
Watchdog Timer	Active	Active	No supply
RAM Lower 128 byte	Active	Inactive; content not lost	Selectable power down (content lost) or inactive (content not lost)
RAM Upper 128 byte	Active	Inactive; content not lost	No supply; content lost
XData 16 byte	Active	Inactive; content not lost	Inactive; content not lost
FLASH memory	Active	Inactive; content not lost	No supply; content not lost
crystal oscillator	Software selectable	Software selectable	No supply
2 kHz RC oscillator	Active	Active	Active
12 MHz RC HF oscillator	Software selectable	Software selectable	Power down (Remark: automatically enabled after Carrier Detect WU)
Interval Timer	Active	Active	Active
LF Receiver	Software selectable	Software selectable	Software selectable
RF Transmitter	Software selectable	Software selectable	No supply
Vmin Detector	Software selectable	Software selectable	No supply

*Note: **Active**: Block is powered, is active and keeps its register contents. Power consumption is high*
***Inactive**: Block is powered, cannot be used, but keeps its register contents. Power consumption is low*
***No supply**: Block is not powered, power consumption is very low.*

2.2 System Controller

While the microcontroller controls PMA51xx in the RUN state, the System Controller takes over control in the POWER DOWN state and the IDLE state.

The System Controller handles the system clock, wake-up events, and system resets.

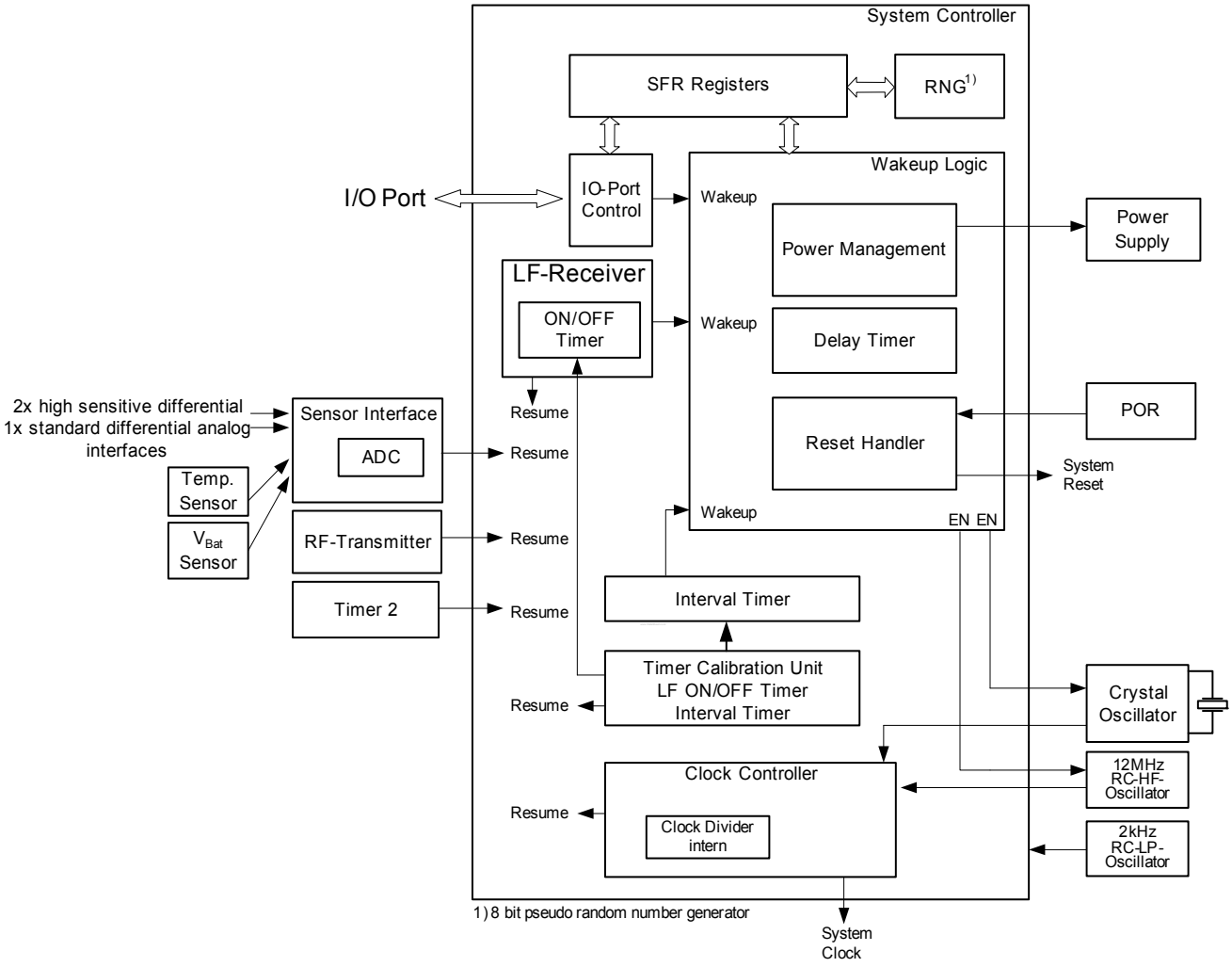


Figure 6 Block Diagram of the System Controller

2.2.1 Wake-up Logic

One of the key elements within the System Controller is the Wake-up Logic, which is responsible for transitions from the POWER DOWN state to the RUN state via the INIT state.

The difference between Reset and Wake-up

- **Reset** - Either via Software Reset, Brownout Reset, Power-On Reset or Reset pin, the digital circuit is reset. Program execution starts at address 0000_H to perform reset initialization routines (including operation mode selection), and will jump to the FLASH at address 4000_H in NORMAL mode to execute the application program.
- **Wake-up** - Only the microcontroller and its peripheral units are reset. Program execution starts at address 0000_H to perform wake-up initialization routines (for evaluating the wake-up source), and jumps to the FLASH at 4000_H to execute the application program.

Wake-up Event Handling

Whenever a wake-up event occurs, the PMA51xx leaves the POWER DOWN state and enters the RUN state to execute the application code. This transition can be initiated by various sources. The wake-up source can be identified by reading SFR WUF and SFR ExtWUF, which are cleared on read out. On every wake-up SFR bit DSR.1[WUP] is set to 1_B.

A wake-up source can be enabled or disabled by setting the appropriate bits in SFR WUM and SFR ExtWUM. For security reasons, the Interval Timer wake-up cannot be masked and the Interval Timer cannot be disabled in NORMAL mode.

The wake-up source (except the Watchdog Timer) is available during the whole RUN state. If an additional wake-up event occurs during the RUN state, the appropriate flag will be set, but the device won't be forced through INIT state.

Watchdog Timer Event

A Watchdog Timer event occurs after the Watchdog Timer has elapsed. The Watchdog Timer, which is only active in RUN and IDLE state cannot be masked.
See **Chapter 2.4.1** for details about the Watchdog Timer.

LF Receiver Wake-up Event

The LF Receiver wake-up can be enabled by setting one of these bits:

- SFR bit WUM.5 [LFCD] or
- SFR bit WUM.4 [LFSY] or
- SFR bit WUM.3 [LFPM1] and/or SFR bit WUM.2 [LFPM0]

The wake-up source can be read in the SFR WUF.

*Note: The LF Receiver has to be configured appropriately for the particular wake-up modes. See **Chapter 2.10.4** for details.*

External Wake-up Event

I/O Port PP1-PP4 and PP6-PP9 can be configured to wake up the PMA51xx from the POWER DOWN state by an external source.

*Note: PP1-PP4 and PP6-PP9 have to be configured according to **Chapter 2.15.3** for this feature. The appropriate bits in SFR ExtWUF are only set when the PMA51xx leaves the POWER DOWN state. In RUN state and IDLE state these bits are not set.*

Interval Timer Wake-up Event

When the Interval Timer elapses, a wake-up event is generated and the POWER DOWN state is left. The wake-up can be identified by the application software reading SFR bit WUF.0 [ITIM].

The Interval Timer is reloaded automatically with actual values from register ITPR and immediately restarted, so the Interval Timer is even working in the RUN state.

Note: The Interval Timer is not maskable in NORMAL mode, so the application will get Interval Timer wake-up events periodically. If these wake-up events occur during the RUN state, they will set the appropriate flag but not force the device through the INIT state.

IDLE state and Resume Event Handling

If switched to the IDLE state by setting SFR bit CFG0.5 [IDLE], the system clock to the microcontroller is gated off. This reduces the chip current consumption and simultaneously improves ADC resolution due to the lower noise level during the time that microcontroller is not clocked.

Note: The IDLE state will only be entered if one of the units providing a resume event is enabled and active. Otherwise, the system will continue executing code in the RUN state without entering the IDLE state.

Only few peripheral components are still active in the IDLE state. The Watchdog Timer is active and will be initialized automatically before entering the IDLE state; thus the IDLE state has a maximum duration of approx. 1 second before a Watchdog Timer wake-up occurs.

The system clock to the microcontroller is re-enabled when a resume event occurs.

The program code continues working where it was suspended. SFR bit CFG0.5 [IDLE] is automatically cleared after a resume event. The resume event source is available in SFR REF.

The IDLE state will be left in case an interrupt event occurs. After completion of the Interrupt service, the IDLE state will be re-entered in case no resume event is pending.

2.2.1.1 Register Description

Table 7 Registers Overview

Register Short Name	Register Long Name	Offset Address	Wakeup Value	Page Number
WUF	Wake-up Flag Register	$C0_H$	$XXXXXX0X_B$	40
WUM	Wake-up Mask Register	$C1_H$	$UUUUUUUU_B$	41
REF	Resume Event Flag Register	$D1_H$	00_H	39
ExtWUF	External Wake-up Flag Register	$F1_H$	$XXXXXXXX_B$	37
ExtWUM	External Wake-up Mask Register	$F2_H$	$UUUUUUUU_B$	38

External Wake-up Flag Register

ExtWUF	Offset	Wakeup Value	Reset Value
External Wake-up Flag Register	**$F1_H$**	**$XXXXXXXX_B$**	**00_H**

7	6	5	4	3	2	1	0
EXTWU7	**EXTWU6**	**EXTWU5**	**EXTWU4**	**EXTWU3**	**EXTWU2**	**EXTWU1**	**EXTWU0**
rc	rc	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
EXTWU7	7	rc	**External Wake-up event on PP9**
EXTWU6	6	rc	**External Wake-up event on PP8**
EXTWU5	5	rc	**External Wake-up event on PP7**
EXTWU4	4	rc	**External Wake-up event on PP6**
EXTWU3	3	rc	**External Wake-up event on PP4**

Field	Bits	Type	Description
EXTWU2	2	rc	**External Wake-up event on PP3**
EXTWU1	1	rc	**External Wake-up event on PP2**
EXTWU0	0	rc	**External Wake-up event on PP1**

External Wake-up Mask Register

ExtWUM	Offset	Wakeup Value	Reset Value
External Wake-up Mask Register	**$F2_H$**	**$UUUUUUUU_B$**	**FF_H**

7	6	5	4	3	2	1	0
MEXTWU7	**MEXTWU6**	**MEXTWU5**	**MEXTWU4**	**MEXTWU3**	**MEXTWU2**	**MEXTWU1**	**MEXTWU0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
MEXTWU7	7	rw	**Mask External Wake-up 7 (on PP9)** 0_B External wake-up 7 allowed 1_B External wake-up 7 disabled
MEXTWU6	6	rw	**Mask External Wake-up 6 (on PP8)** 0_B External wake-up 6 allowed 1_B External wake-up 6 disabled
MEXTWU5	5	rw	**Mask External Wake-up 5 (on PP7)** 0_B External wake-up 5 allowed 1_B External wake-up 5 disabled
MEXTWU4	4	rw	**Mask External Wake-up 4 (on PP6)** 0_B External wake-up 4 allowed 1_B External wake-up 4 disabled
MEXTWU3	3	rw	**Mask External Wake-up 3 (on PP4)** 0_B External wake-up 3 allowed 1_B External wake-up 3 disabled
MEXTWU2	2	rw	**Mask External Wake-up 2 (on PP3)** 0_B External wake-up 2 allowed 1_B External wake-up 2 disabled
MEXTWU1	1	rw	**Mask External Wake-up 1 (on PP2)** 0_B External wake-up 1 allowed 1_B External wake-up 1 disabled
MEXTWU0	0	rw	**Mask External Wake-up 0 (on PP1)** 0_B External wake-up 0 allowed 1_B External wake-up 0 disabled

Resume Event Flag Register

REF	Offset	Wakeup Value	Reset Value
Resume Event Flag Register	**$D1_H$**	**00_H**	**00_H**

7	6	5	4	3	2	1	0
REXTG	Res	**READC**	**RELFO**	**RERFF**	**RERFU**	**RERC**	**RET2**
rc	r	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
REXTG	7	rc	**Clock changed to Xtal clock**
Res	6	r	**For future use**
READC	5	rc	**A/D conversion complete**
RELFO	4	rc	**LF receive buffer full**
RERFF	3	rc	**RF transmission finished**
RERFU	2	rc	**RF transmit buffer empty**
RERC	1	rc	**RC calibration complete**
RET2	0	rc	**Timer 2 underflow**

Wake-up Flag Register

WUF	Offset	Wakeup Value	Reset Value
Wake-up Flag Register	**$C0_H$**	**$XXXXXX0X_B$**	**00_H**

7	6	5	4	3	2	1	0
WDOG	Res	**LFCD**	**LFSY**	**LFPM1**	**LFPM0**	Res	**ITIM**
rc		rc	rc	rc	rc		rc

Field	Bits	Type	Description
WDOG	7	rc	**Watchdog Timer Event**
Res	6		**Reserved**
LFCD	5	rc	**LF RX carrier-detect Wake-up**
LFSY	4	rc	**LF RX sync-match Wake-up**
LFPM1	3	rc	**LF RX pattern 1-match Wake-up**
LFPM0	2	rc	**LF RX pattern 0-match Wake-up**
Res	1		**Reserved**
ITIM	0	rc	**Interval Timer Wake-up**

Wake-up Mask Register

WUM	Offset	Wakeup Value	Reset Value
Wake-up Mask Register	$C1_H$	$UUUUUUUU_B$	FF_H

7	6	5	4	3	2	1	0
MWDOG	Res	**MLFCD**	**MLFSY**	**MLFPM1**	**MLFPM0**	Res	**MITIM**
rw		rw	rw	rw	rw	r	rw

Field	Bits	Type	Description
MWDOG	7	rw	**Mask Watchdog Timer** This bit does only have effect in TEST -, DEBUG - and PROGRAMMING mode. 0_B Watchdog Timer event allowed. Always allowed in NORMAL mode! 1_B Watchdog Timer event disabled
Res	6		**Reserved**
MLFCD	5	rw	**Mask LF RX carrier detected** 0_B LF RX carrier wake-up allowed 1_B LF RX carrier wake-up disabled
MLFSY	4	rw	**Mask LF RX sync match** 0_B LF RX sync match wake-up allowed 1_B LF RX sync match wake-up disabled
MLFPM1	3	rw	**Mask LF RX pattern 1 match** 0_B LF RX pattern 1 match wake-up allowed 1_B LF RX pattern 1 match wake-up disabled
MLFPM0	2	rw	**Mask LF RX pattern 0 match** 0_B LF RX pattern 0 match wake-up allowed 1_B LF RX pattern 0 match wake-up disabled
Res	1	r	**For future use**
MITIM	0	rw	**Mask Interval Timer Wake-up** This bit does only have effect in TEST -, DEBUG - and PROGRAMMING mode. 0_B Interval Timer wake-up allowed. Always allowed in NORMAL mode! 1_B Interval Timer wake-up disabled

2.2.2 Interval Timer

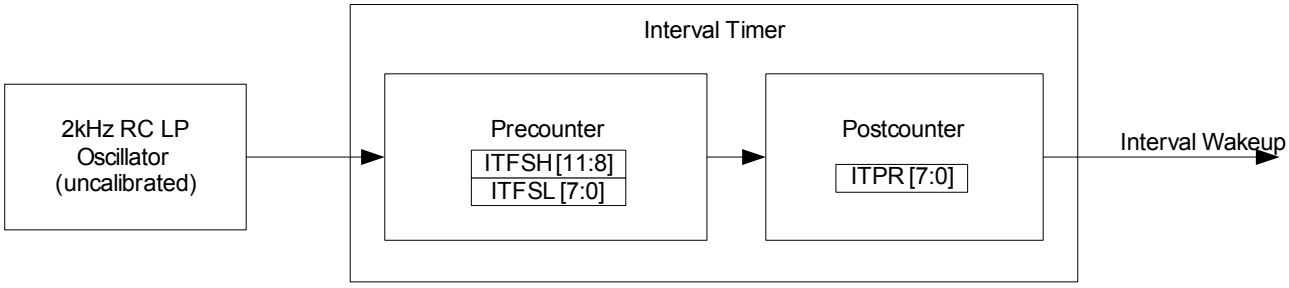


Figure 7 Interval Timer Block Diagram

The Interval Timer is responsible for waking up the PMA51xx from the POWER DOWN state after a predefined time interval. It is clocked by the 2 kHz RC LP oscillator and incorporates two dividers:

- Precounter: Can be calibrated to the system clock and represents the time base.
- Postcounter: Configures the Interval Timer duration. It can be set from 1-256_{dec}.

Timing accuracy can be ensured by using a Library function that calibrates the precounter with the accurate system clock (see **[1]**).

The Interval Timer duration is determined by the SFR ITPR. This value is calculated by using the following equation:

$$Interval\,Timer\,period[s] = \frac{precounter}{f_{2kHz\,RC\,LP\,Oscillator}\left[\frac{1}{s}\right]} \cdot postcounter$$

Figure 8 Calculation of Interval Timer period

The Postcounter (ITPR) is an 8-bit register. The maximum interval duration corresponds to 00_H (multiplication with 256_{dec}). 01_H up to FF_H corresponds to a multiplication with 1_{dec} up to 255_{dec}.

Note: After writing SFR ITPR, some clock cycles are needed to activate the new setting. SFR bit CFG1.1 [ITInit] is cleared automatically when the new setting is activated.

Interval Timer calibration

Due to the deviation of the 2 kHz RC LP oscillator frequency calibration is necessary and done by counting clock cycles from the crystal oscillator or the 12 MHz RC HF oscillator (depending on the current system clock) during one 2 kHz RC LP oscillator period. The counted clock cycles are used to calculate the appropriate configuration values.The calibration is performed automatically by a Library function (see **[1]**).

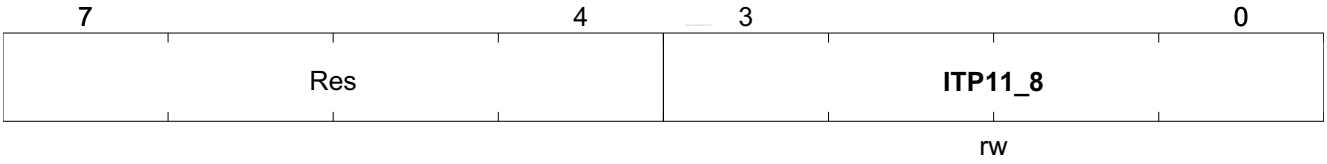
2.2.3 Register Description

Table 8 Registers Overview

Register Short Name	Register Long Name	Offset Address	Wakeup Value	Page Number
ITPL	Interval Timer Precounter Register Low Byte	BA_H	$UUUUUUUU_B$	44
ITPH	Interval Timer Precounter Register High Byte	BB_H	$0000UUUU_B$	43
ITPR	Interval Timer Period Register	BC_H	$UUUUUUUU_B$	44

Interval Timer Precounter Register High Byte

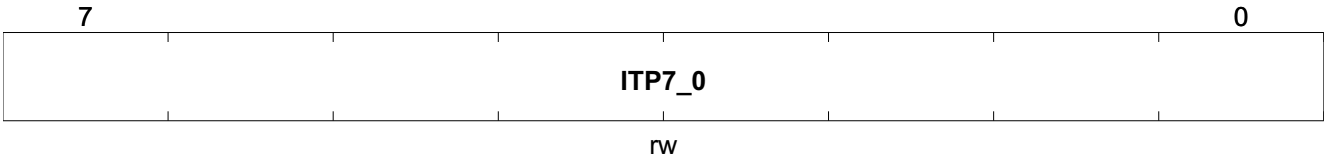
ITPH	Offset	Wakeup Value	Reset Value
Interval Timer Precounter Register High Byte	**BB_H**	**$0000UUUU_B$**	**03_H**



Field	Bits	Type	Description
Res	7:4		**Reserved**
ITP11_8	3:0	rw	**Interval Timer Precounter Register bit 11 down to bit 8**

Interval Timer Precounter Register Low Byte

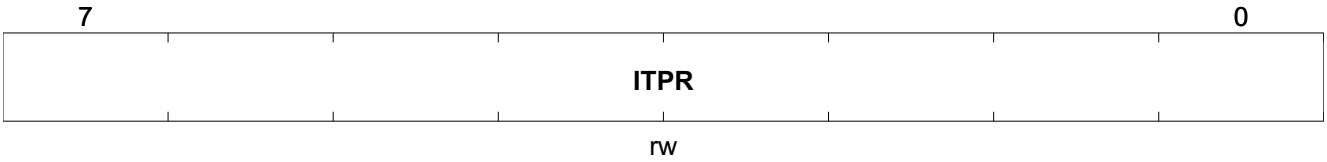
ITPL	Offset	Wakeup Value	Reset Value
Interval Timer Precounter Register Low Byte	BA_H	$UUUUUUUU_B$	$E8_H$



Field	Bits	Type	Description
ITP7_0	7:0	rw	**Interval Timer Precounter Register bit 7 down to bit 0**

Interval Timer Period Register

ITPR	Offset	Wakeup Value	Reset Value
Interval Timer Period Register	BC_H	$UUUUUUUU_B$	01_H



Field	Bits	Type	Description
ITPR	7:0	rw	**Interval Timer Period Register**

Note: These SFRs can be modified manually as well for using other (uncalibrated) precounter values. If the Interval Timer function is not needed for the application, it is recommended to set the registers ITPR, ITPL, ITPH to their maximal value of FF_H to save power. In this case, the wake-up interval will be extended to maximal interval.

2.3 System Configuration Registers

The system configuration registers are used for:

- Initiating state transitions
- System software reset
- Enabling or disabling peripherals
- Monitoring the operation mode, the system state, and peripherals

2.3.1 Register Description

Table 9 Registers Overview

Register Short Name	Register Long Name	Offset Address	Wakeup Value	Page Number
CFG2	Configuration Register 2	$D8_H$	$000U1000_B$	48
DSR	Diagnosis and Status Register	$D9_H$	$0XUU00XU_B$	49
CFG1	Configuration Register 1	$E8_H$	$000U000U_B$	47
CFG0	Configuration Register 0	$F8_H$	$0000U000_B$	46

Configuration Register 0

CFG0	Offset	Wakeup Value	Reset Value
Configuration Register 0	$F8_H$	$0000U000_B$	00_H

7	6	5	4	1	0
PDWN	Res	**IDLE**	Res		**CLKSel0**
rw		rw			rw

Field	Bits	Type	Description
PDWN	7	rw	**POWER DOWN state Enable** POWER DOWN state is entered, if this bit is set to 1_B. This bit is automatically reset to 0_B by the system controller after wake-up from POWER DOWN state. 0_B RUN state 1_B POWER DOWN state
Res	6		**Reserved** Must be set to 0_B.
IDLE	5	rw	**IDLE state Enable** IDLE state is entered, if this bit is set to 1_B. This bit is automatically reset to 0_B by the system controller after a resume event occurred. 0_B RUN state 1_B IDLE state
Res	4:1		**Reserved**
CLKSel0	0	rw	**Clock Source Select** 0_B 12 MHz RC HF oscillator (internal) 1_B Crystal oscillator is selected (external)

Configuration Register 1

CFG1	Offset	Wakeup Value	Reset Value
Configuration Register 1	$E8_H$	$000U000U_B$	01_H

7	6	5	4	3	2	1	0
PMWEn	**I2CEn**	Res	**RfTXPEn**	**ADCEn**	**SPIEn**	**ITInit**	**ITEn**
rw	rw		rw	rw	rw	r	r

Field	Bits	Type	Description
PMWEn	7	rw	**Program Memory Write Enable** 0_B Write access to Flash program memory not allowed 1_B Write access to Flash program memory allowed Note: Write operation to program memory is not feasible on standard 8051 microcontroller, thus write access has to be allowed explicitly
I2CEn	6	rw	**I2C Enable** 0_B I^2C-Interface disabled. Port Pins PP0 and PP1 are used as GPIOs 1_B I^2C-Interface enabled. Port Pins PP0 and PP1 are used for I^2C communication
Res	5		**Reserved**
RfTXPEn	4	rw	**RF TX Port Out Enable** 0_B PP2 is used as GPIO 1_B PP2 is used for serial output of Manchester/BiPhase coded RF TX data
ADCEn	3	rw	**ADC Enable** 0_B ADC disabled 1_B ADC enabled
SPIEn	2	rw	**SPI Enable** 0_B SPI-Interface disabled. Port Pins PP3 to PP6 are used as GPIOs 1_B SPI-Interface enabled. Port pins PP3 to PP6 are used for SPI communication
ITInit	1	r	**Interval Timer Initialization active** 0_B No reload 1_B (Re)loads the Interval Timer with content of ITPR/ITPH/ITPL. This bit is automatically cleared after initialization completes
ITEn	0	r	**Interval Timer Enable**[1)] 0_B Interval Timer is deactivated (not possible in NORMAL mode) 1_B Enables Interval Timer countdown

1) Interval Timer is always enabled in NORMAL mode

Configuration Register 2

CFG2	Offset	Wakeup Value	Reset Value
Configuration Register 2	**$D8_H$**	**$000U1000_B$**	**18_H**

7	5	4	3	2	1	0
Res		**PDLMB**	**PDADC**	Res	**WDRES**	**RESET**
		rw	rw		cw	cw

Field	Bits	Type	Description
Res	7:5		**Reserved**
PDLMB	4	rw	**Power Down iRAM lower memory block** 0_B Contents of lower 128 byte of data memory (00_H-$7F_H$) are kept active also in POWER DOWN state 1_B Contents of lower 128 byte of data memory (00_H-$7F_H$) are lost in POWER DOWN state
PDADC	3	rw	**Power Down ADC** 0_B ADC analog circuit is supplied 1_B ADC power down (ADC analog circuit not supplied)
Res	2		**Reserved**
WDRES	1	cw	**Reset Watchdog Timer** 0_B Default 1_B Watchdog Timer is reset and restarts counting from zero Note: WDRES is cleared automatically
RESET	0	cw	**Reset System** 0_B Default 1_B A software-assigned system reset is done. Note: Bit RESET is cleared automatically.

Diagnosis and Status Register

DSR	Offset	Wakeup Value	Reset Value
Diagnosis and Status Register	$D9_H$	$0XUU00XU_B$	$0XXX0000_B$

7	6	5	4	3	2	1	0
SCLK	Res	**OpMODE**		Res		**WUP**	**FlashLCK**
r		r		r		r	w

Field	Bits	Type	Description
SCLK	7	r	**Currently selected system clock** 0_B 12 MHz RC HF oscillator clock selected 1_B Crystal oscillator clock selected
Res	6		**Reserved**
OpMODE	5:4	r	**Operation Mode** Operation Mode applied at chip startup. 00_B TEST mode 01_B PROGRAMMING mode 10_B DEBUG mode 11_B NORMAL mode
Res	3:2	r	**Reserved**
WUP	1	r	**Wake-up Pending** This bit can be used for decision reset / wake-up. 0_B No wake-up pending 1_B Wake-up is pending (read detailed information from WUF/ExtWUF)
FlashLCK	0	w	**FLASH Lock** Is set to 1_B by SW if Lockbyte 3 is set ($D1_H$ is detected at FLASH address $57FF_H$). If Lockbyte 3 is set without setting Lockbyte 2, this byte has no effect and will result a unlocked FLASH. 0_B Full FLASH access (FLASH related SFRs) 1_B Restricted write access

2.4 Fault Protection

The PMA5110 features multiple fault protections that prevent the application from incurring unexpected behavior and deadlocks. This chapter gives a brief overview of the available fault protections.

2.4.1 Watchdog Timer

For operation security, a Watchdog Timer is available to avoid application deadlocks. The Watchdog Timer must be reset periodically by the microcontroller, otherwise the timer generates a reset and forces a restart of PMA5110 program execution. The SFRs which are not supplied in POWER DOWN state are initialized

after a reset generated by the Watchdog Timer.

The Watchdog Timer is automatically reset by a Power On reset, Brown Out reset, xReset, software reset (CFG2.0[RESET]) or when the IDLE state is entered.

The Watchdog Timer duration is fixed to a nominal period of 1 s. The accuracy depends on the accuracy of the 2 kHz RC LP oscillator that is used to clock the Watchdog Timer.

Setting SFR bit CFG2.1 [WDRES] resets the Watchdog Timer (see **Configuration Register 0**). If a Watchdog Timer overflow occurred SFR bit WUF.7 [WDOG] is set to 1_B.

2.4.2 Vmin Detector

This circuit will detect if the supply voltage is below the minimum value required to guarantee correct chip operation. The Library functions that perform measurements will return the Vmin status in a status byte with the measurement result. The Vmin Detector can be used to either monitor the internal regulated supply voltage or the external supply voltage V_{Bat}. The selection of the supply voltage to monitor is done with bit LBD.3 [LBD2V1].

If enabled by LBD.1[LBDEn] and LBD.0[LBDMEn], the power supply voltage is sensed and bit LBD.2 [LBDF] is set to 1_B, if the supply voltage drops below threshold during measurement time.

2.4.2.1 Register Description

Low Battery Detector Control

LBD	Offset	Wakeup Value	Reset Value
Low Battery Detector Control	**EF_H**	**$0B_H$**	**$0B_H$**

7	4	3	2	1	0
Res		**LBD2V1**	**LBDF**	**LBDEn**	**LBDMen**
		rw	rc	rw	rw

Field	Bits	Type	Description
Res	7:4		**Reserved**

Field	Bits	Type	Description
LBD2V1	3	rw	**Low Battery Voltage Switch** 0_B VDDD (internal voltage) 1_B V_{Bat} (external voltage)
LBDF	2	rc	**Low Battery Detector Flag** 0_B Supply voltage is higher then threshold voltage 1_B Supply voltage is lower then threshold voltage
LBDEn	1	rw	**Low Battery Detector enable** 0_B Low Battery Detector disabled 1_B Low Battery Detector enabled
LBDMen	0	rw	**Low Battery Detector measurement enable** *Note: LBDEn must be enabled at least 10us before LBDMEn can be set in order to start the measurement* 0_B Stop measurement 1_B Start measurement

2.4.3 Brownout Detector

The Brownout Detector resets the PMA when the supply voltage drops below VBRD in RUN state and below VPDBR in POWER DOWN state (see **Table 44 “Power On Reset” on Page 193**).

2.4.4 FLASH Memory Checksum

A CRC checksum is stored in the FLASH memory. After Lockbyte 2 is written, the CRC checksum can be recalculated and checked by the application program for verification of program code if needed.

If a single bit error in the FLASH memory occurs, it is corrected by the FLASH internal Error Correction Coder, as an indication the FCSP.7 [ECCErr] bit is set. (see **FLASH Control Register - Sector Protection Control on page 59**)

2.4.5 ADC Measurement Overflow and Underflow

The Library functions that perform measurements will return the over/underflow status in a status byte with the measurement result.

2.5 Clock Controller

The Clock Controller for internal clock management is part of the System Controller.

The PMA51xx always starts up using the 12 MHz RC HF oscillator to provide minimum startup time and minimum current consumption. Changing the system clock from the 12 MHz RC HF oscillator to the crystal (e.g. for RF transmission) is performed automatically by calling a Library function (see **[1]**). If the crystal is selected as system clock, the 12 MHz RC HF oscillator is automatically powered down.

*Note: Since the external crystal needs some startup time, a 3-bit delay timer is integrated to delay the clock switching. Depending on the crystal used, the SFR bits XTCFG.2-0 [XTDLY2-0] can be set to delay from typ. 0 µs up to 1750 µs in 250 µs steps (see **XTAL Configuration Register**).*

The following figure shows which clocks are used for which PMA5110 blocks. Details about the individual blocks can be found in the appropriate chapters of this document

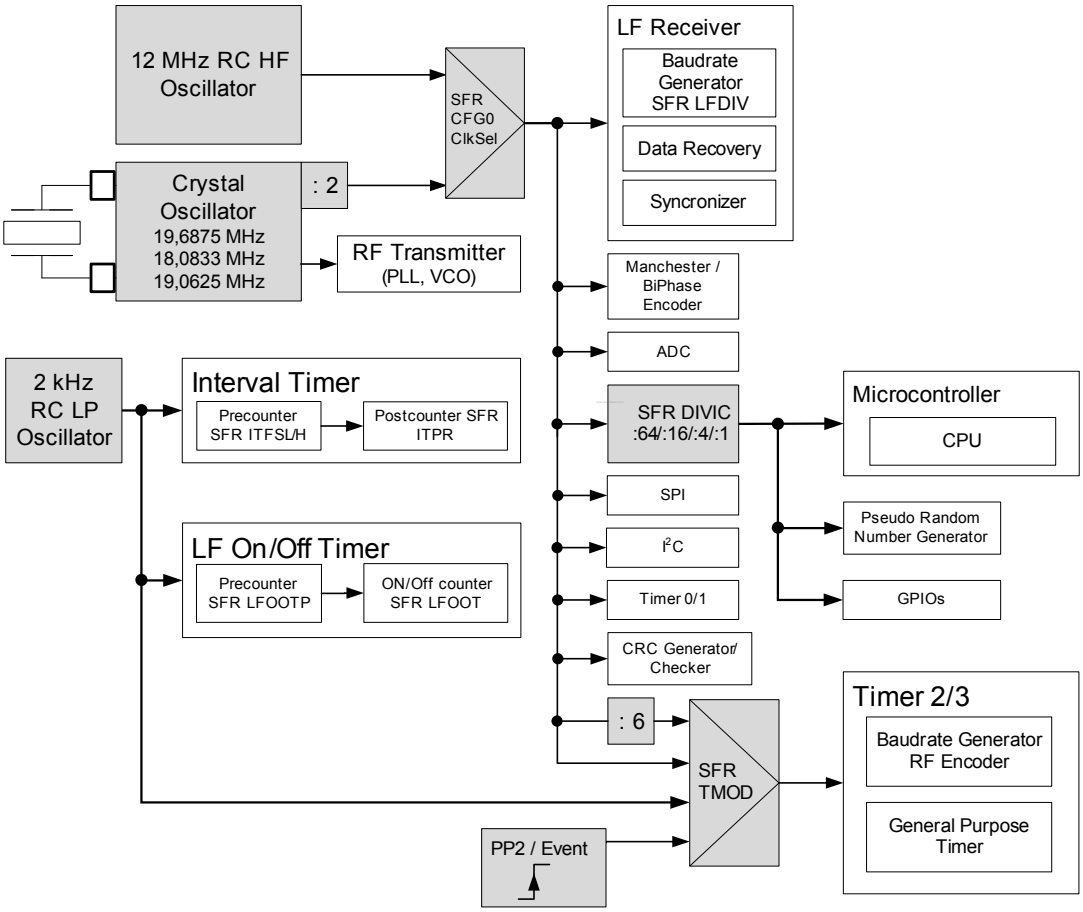


Figure 9 PMA5110 Clock Concept

2.5.1 Internal Clock Divider

To save power, it is possible to enable the internal clock divider to reduce the system clock by a prescaled factor. If SFR DIVIC is set to 00_H (default), the divider is disabled. For a description of the SFR DIVIC see **Internal Clock Divider on page 54**.

2.5.2 2 kHz RC LP Oscillator (Low Power)

The 2 kHz RC LP oscillator stays always active.

2.5.3 12 MHz RC HF Oscillator (High Frequency)

The 12 MHz RC HF oscillator typically runs at 12 MHz. It is used as the default clock source for the PMA51xx in RUN state.

2.5.4 Crystal Oscillator

The nominal crystal operating frequencies are between 18 MHz and 20 MHz depending on the RF band used.

868 MHz / 915 MHz : $f_{XTAL}[Hz] = f_{RF}[Hz] \cdot \frac{1}{48}$

434 MHz : $f_{XTAL}[Hz] = f_{RF}[Hz] \cdot \frac{2}{48}$

315 MHz : $f_{XTAL}[Hz] = f_{RF}[Hz] \cdot \frac{3}{48}$

Figure 10 Formulas for Crystal selection dependent of RF Bands

Frequency pulling from the nominal crystal frequency is achieved by the internal capacitor banks. This is used for fine-tuning the ASK carrier frequency and the lower and upper modulation frequencies for FSK modulation. Thus, frequency differences due to crystals that are not exactly matched or differences in component tolerances can be trimmed device internal.

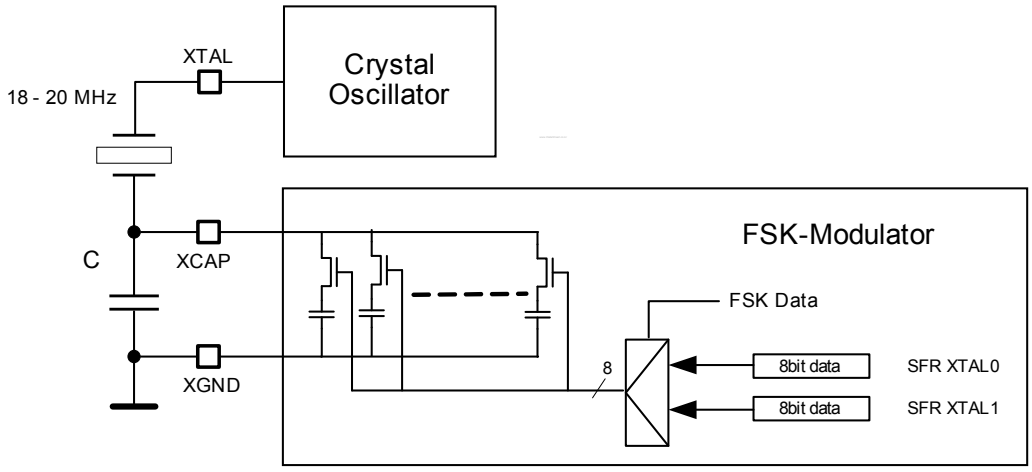


Figure 11 Crystal Oscillator and FSK-Modulator Block Diagram

Trimming of the Crystal Oscillator

The crystal oscillator can be trimmed using the internal capacitor array or externally. To use the internal capacitor array SFR bit RFTX.7 [XCapSH] has to be set to 0_B. The SFRs SFR XTAL0 and SFR XTAL1 allow the trimming of the crystal frequency in a broad range using the internal capacitor array. Setting SFR bit RFTX.7 [XCapSH] to 1_B shorts the internal capacitor array and the crystal oscillator can be trimmed externally.

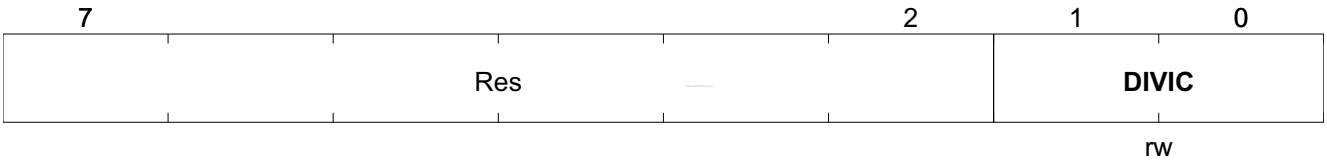
2.5.5 Register Description

Table 10 Registers Overview

Register Short Name	Register Long Name	Offset Address	Wakeup Value	Page Number
DIVIC	Internal Clock Divider	$B9_H$	$000000UU_B$	54
XTCFG	XTAL Configuration Register	$C2_H$	$00000UUU_B$	56
XTAL1	XTAL Frequency Register FSKHIGH/ASK	$C3_H$	$UUUUUUUU_B$	55
XTAL0	XTAL Frequency Register FSKLOW	$C4_H$	$UUUUUUUU_B$	55

Internal Clock Divider

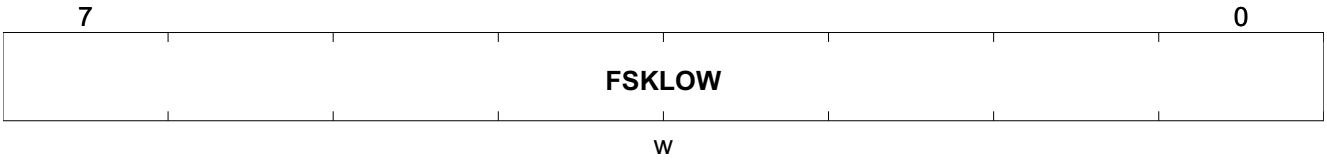
DIVIC	Offset	Wakeup Value	Reset Value
Internal Clock Divider	**$B9_H$**	**$000000UU_B$**	**00_H**



Field	Bits	Type	Description
Res	7:2		**Reserved**
DIVIC	1:0	rw	**System Clock Divider Factor** System clock, selected with CFG0.0[CLKSel0], is divided by 00_B 1 01_B 4 10_B 16 11_B 64

XTAL Frequency Register FSKLOW

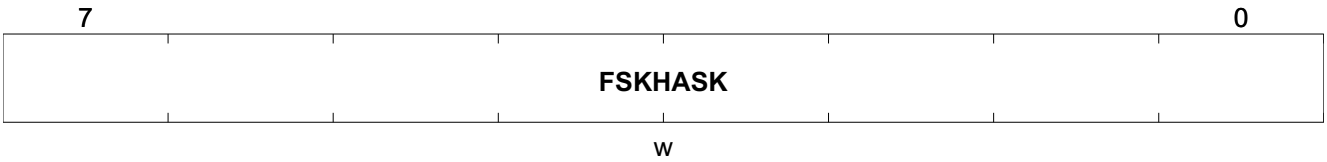
XTAL0	Offset	Wakeup Value	Reset Value
XTAL Frequency Register FSKLOW	$C4_H$	$UUUUUUUU_B$	FF_H



Field	Bits	Type	Description
FSKLOW	7:0	w	**FSK Low Frequency** Capacitor select for lower FSK modulation frequency if RFENC.3[TXDD] = 0_B and RFTX.5[ASKFSK] = 0_B. The capacitor array is binary weighted from FSKLOW.7 = 20pF (MSB) down to FSKLOW.0 = 156fF (LSB)

XTAL Frequency Register FSKHIGH/ASK

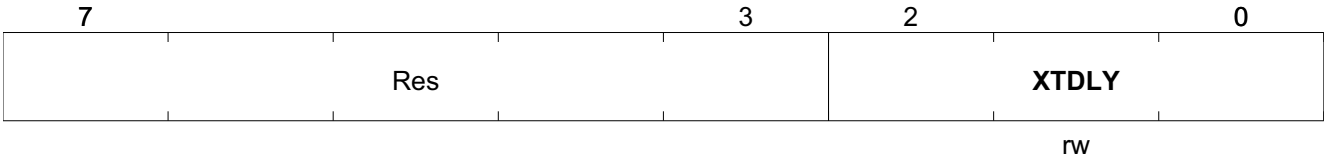
XTAL1	Offset	Wakeup Value	Reset Value
XTAL Frequency Register FSKHIGH/ASK	$C3_H$	$UUUUUUUU_B$	FF_H



Field	Bits	Type	Description
FSKHASK	7:0	w	**FSK High Frequency** Capacitor select for upper FSK modulation frequency if RFENC.3[TXDD] = 1_B and RFTX.5[ASKFSK] = 0_B **ASK Center Frequency** Capacitor select for ASK center frequency fine tuning if RFENC.3[TXDD] = 1_B and RFTX.5[ASKFSK] = 1_B The capacitor array is binary weighted from FSKHASK.7 = 20pF (MSB) down to FSKHASK.0 = 156fF (LSB)

XTAL Configuration Register

XTCFG	Offset	Wakeup Value	Reset Value
XTAL Configuration Register	**$C2_H$**	**$00000UUU_B$**	**03_H**



Field	Bits	Type	Description
Res	7:3		**Reserved**
XTDLY	2:0	rw	**XTAL Startup Delay Time** Delay time in steps of 250µs @ typ. 2 kHz RC LP oscillator clock = 2 kHz 000_B typ. 0µs 001_B typ. 250µs 010_B typ. 500µs 011_B typ. 750µs 100_B typ. 1000µs 101_B typ. 1250µs 110_B typ. 1500µs 111_B typ. 1750µs

2.6 Memory Organization

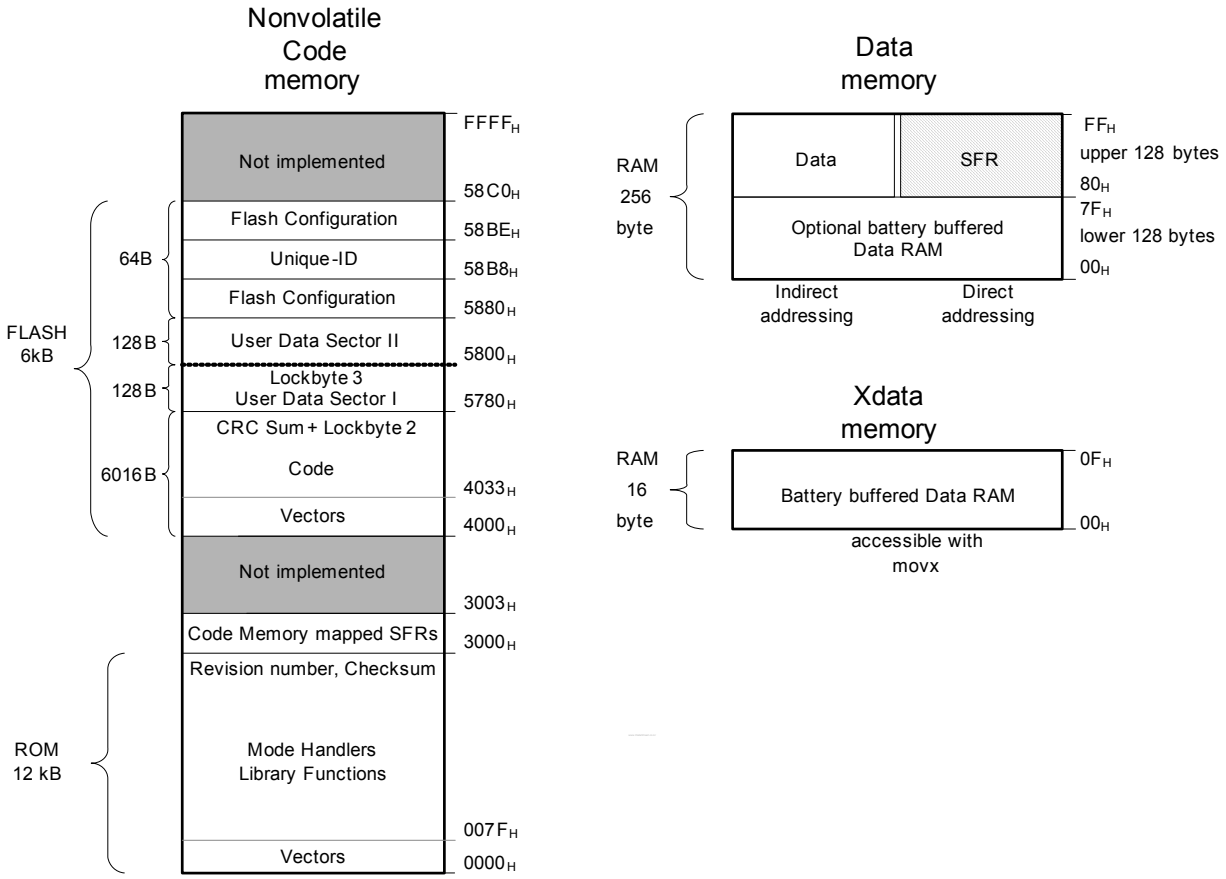


Figure 12 Memory Map

The Following Memory Blocks are implemented

- 12 kbyte ROM
- 6 kbyte FLASH code memory
- 2x128 byte User FLASH code/data memory
- 64 byte read-only FLASH configuration and unique-ID
- 2x128 byte data RAM, of which 128 bytes may be battery buffered
- 16 byte battery-buffered XData RAM

2.6.1 ROM

A 12 kbyte ROM is located in the address range 0000_H to $2FFF_H$.

Function Library and Reset/Wake-up Handlers

The ROM contains the reset handler, the wake-up handler, and the Function Library (see [1]).

A hardware mechanism is implemented to prevent direct jumping into the ROM area. Access to the Library functions is granted via a vector table at the bottom of the ROM address space.

ROM protection

A hardware mechanism protects the ROM code against readout, so a read operation from the ROM in the protected address area returns zero.

2.6.2 FLASH

2.6.2.1 FLASH Organization

The FLASH is divided into four sectors. Each sector can be erased and written individually (byte wise erasing and writing is not possible).

- **4000_H -- $577F_H$ (6016 byte) code sector (sector 0):** This sector contains the code sector for the application program.
- **5780_H -- $587F_H$ (2x128 byte) User Data sector I + User Data sector II (sector 1 + sector 2):** These two sectors contain the user data sector, which can store individual device configuration data. The crystal frequency that is needed for the Library functions could also be saved here.
- **5880_H -- $58BF_H$ (64 byte) configuration sector (sector 3):** This sector contains the FLASH configuration sector for FLASH driver parameters and is write protected.

2.6.2.2 FLASH Protection

Write and erase operations on the FLASH code sector are only allowed in PROGRAMMING mode. To protect the FLASH against unauthorized access, three Lockbytes can be set:

- **Lockbyte 1:** This is written at the end of production test. The FLASH configuration sector is irreversibly switched to read-only.
- **Lockbyte 2:** Address $577F_H$ (Top address of the code sector).
  This byte (as well as a ROM CRC) is optionally written by the programmer together with the code download. When the reset handler detects this byte, it sets the FCSP.1[CodeLCK]. When this bit is set, the DEBUG mode and PROGRAMMING mode are no longer accessible. Their pin settings lead to NORMAL mode wherein the CRC can be checked. This Lockbyte has to be set while programming the code sector to protect application code against undesired read-out.
- **Lockbyte 3:** Address $57FF_H$ (Top of User Data Sector I).
  Lockbyte 3 can be set by the programmer during program download or by the application. After Lockbyte 3 has been set, a reset is necessary to get the User Data Sectors locked. Write accesses to the FLASH registers are blocked after Lockbyte 3 has been set.
  If Lockbyte 3 is set without setting Lockbyte 2, this byte has no effect and will result in an unlocked FLASH.
  How to set Lockbyte 3 is described in **Chapter 2.18.6**.

2.6.2.3 Register Description

FLASH Control Register - Sector Protection Control

FCSP	Offset	Wakeup Value	Reset Value
FLASH Control Register - Sector Protection Control	**$E9_H$**	**$000000UU_B$**	**00_H**

7	6	2	1	0
ECCErr	Res		**CodeLCK**	**ConfLCK**
rc			rw	rw

Field	Bits	Type	Description
ECCErr	7	rc	**ECC Error Detected Bit** 0_B No Error Detected 1_B Error Detected
Res	6:2		**Reserved**
CodeLCK	1	rw	**Code Sector Lock Bit** Is set to 1_B by SW if Lockbyte 2 is set ($D1_H$ is detected at FLASH address $577F_H$). 0_B programmable & erasable 1_B Read only
ConfLCK	0	rw	**Config Sector Lock Bit** Is set to 1_B by SW if FLASH configuration sector has been locked (switched to read only). 0_B programmable & erasable 1_B Read only

2.6.3 RAM

The RAM is available as data storage for the application program. Library functions may use some RAM locations for passing parameters and internal calculations. The RAM area that is used for the Library functions is specified in [1].

The RAM is always powered in RUN state and IDLE state.

The upper 128 bytes of RAM are always switched off in POWER DOWN state and lose their contents in these states. SFR bit CFG2.4[PDLMB] determines if the lower 128 byte of RAM are powered during POWER DOWN state.

If not powered in these states, this RAM loses the content, otherwise it can be used as battery-buffered storage after a POWER DOWN period.

Note: The RAM is not reset during a System Reset. After a Brown Out Reset, this feature can be used to try to recover data from RAM.
After Power On Reset, the RAM is not initialized, and thus contains random data. The application has to initialize the RAM if needed.

2.6.4 Code Memory mapped SFRs

The code memory mapped SFRs can be used to implement an opcode which can be modified in runtime, for example to access SFRs or to implement variable jump addresses.

The registers MMR0, MMR1, and MMR2 - additionally mapped to address 3000_H - 3002_H may contain up to 3-byte opcode. Code address 3003_H contains a hard coded return statement (RET).

2.6.4.1 Register Description

Table 11 Registers Overview

Register Short Name	Register Long Name	Offset Address	Wakeup Value	Reset Value
MMR0	Memory Mapped Register 0	84_H	00_H	00_H
MMR1	Memory Mapped Register 1	85_H	00_H	00_H
MMR2	Memory Mapped Register 2	86_H	00_H	00_H

2.6.5 Battery buffered data RAM

There are 16 bytes of battery buffered data RAM available that can be used by the application to store data during a POWER DOWN state period. This memory consumes relatively little leakage current compared to the whole lower memory block by storing small amount of data.

Note: The battery buffered data RAM is located in the xdata area and therefore not reset by a System Reset. After a Brownout Reset, this feature can be used to possibly recover data from RAM.
After a Power-On Reset, this memory is not initialized, and thus contain random data. The application has to initialize the battery buffered data RAM.

2.6.6 Special Function Registers

Special Function Registers (SFRs) are used to control and monitor the status of the PMA51xx and its peripherals. The following table shows the naming convention for the SFR descriptions that are used throughout this document.

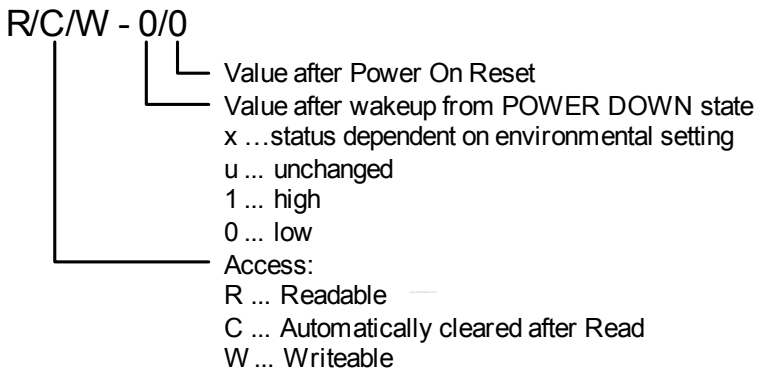


Figure 13 Naming Convention for Register Descriptions

Note: If a single bit or the whole byte value is declared as unchanged, it keeps its state even during POWER DOWN state.

Table 12 “Special Function Registers Overview” on Page 61 shows the power supply of each SFR and gives a reference to the page within this document where a detailed description can be found.

Table 12 Special Function Registers Overview

Register Short Name	Register Long Name	Register Address	Supplied in PDWN	Description
ACC	Accumulator	$E0_H$	No	**Page 65**
ADCC0	ADC Configuration Register 0	DB_H	No	**Page 116**
ADCC1	ADC Configuration Register 1	DC_H	No	**Page 118**
ADCDL	ADC Result Register (low byte)	$D4_H$	No	**Page 119**
ADCDH	ADC Result Register (high byte)	$D5_H$	No	**Page 119**
ADCM	ADC Mode Register	$D2_H$	No	**Page 120**
ADCOFF	ADC Input Offset c-network configuration	DA_H	No	**Page 121**
ADCS	ADC Status Register	$D3_H$	No	**Page 122**
B	Register B	$F0_H$	No	**Page 65**
CFG0	Configuration Register 0	$F8_H$	Yes	**Page 46**

Table 12 Special Function Registers Overview

Register Short Name	Register Long Name	Register Address	Supplied in PDWN	Description
CFG1	Configuration Register 1	$E8_H$	Yes	Page 47
CFG2	Configuration Register 2	$D8_H$	Yes	Page 48
CRCC	CRC Control Register	$A9_H$	No	Page 125
CRCD	CRC Data Register	AA_H	No	Page 126
CRC0	CRC Shift Register (low byte)	AC_H	No	Page 126
CRC1	CRC Shift Register (high byte)	AD_H	No	Page 127
DIVIC	Internal Clock Divider	$B9_H$	Yes	Page 54
DPL	Data Pointer (low byte)	82_H	No	Page 65
DPH	Data Pointer (high byte)	83_H	No	Page 65
DSR	Diagnosis and Status Register	$D9_H$	No	Page 49
ExtWUF	External Wake-up Flag Register	$F1_H$	Yes	Page 37
ExtWUM	External Wake-up Mask Register	$F2_H$	Yes	Page 38
FCSP	FLASH Control Register - Sector Protection Control	$E9_H$	No	Page 59
I2CB	I^2C Baud rate Register	$B1_H$	No	Page 160
I2CC	I^2C Control Register	$A2_H$	No	Page 161
I2CD	I^2C Data Register	$9A_H$	No	Page 162
I2CM	I^2C Mode Register	$A3_H$	No	Page 162
I2CS	I^2C Status Register	$9B_H$	No	Page 163
IE	Interrupt Enable Register	$A8_H$	No	Page 69
IP	Interrupt Priority Register	$B8_H$	No	Page 70
IRQRF	Interrupt Request Flag Register (for extended interrupts)	$8F_H$	No	Page 71
ITPL	Interval Timer Precounter Register (low byte)	BA_H	Yes	Page 44
ITPH	Interval Timer Precounter Register (high byte)	BB_H	Yes	Page 43
ITPR	Interval Timer Period Register	BC_H	Yes	Page 44
LBD	Low Battery Detector Control	EF_H	No	Page 50
LFCDFlt	LF Carrier Detect Filtering	$B2_H$	Yes	Page 94
LFCDM	LF Carrier Detector Mode	$B5_H$	Yes	Page 95
LFDIV0	LF Division Factor (low byte)	$B3_H$	Yes	Page 96
LFDIV1	LF Division Factor (high byte)	$B4_H$	Yes	Page 96
LFOOT	LF On/Off Timer Configuration Register	$C6_H$	Yes	Page 97
LFOOTP	LF On/Off Timer Precounter Register	$C5_H$	Yes	Page 98
LFPCFG	LF Pattern Detection Configuration Register	$C7_H$	Yes	Page 100

Table 12 Special Function Registers Overview

Register Short Name	Register Long Name	Register Address	Supplied in PDWN	Description
LFP0L	LF Pattern 0 Detector Sequence Data LSB	BE_H	Yes	Page 99
LFP0H	LF Pattern 0 Detector Sequence Data MSB	BF_H	Yes	Page 98
LFP1L	LF Pattern 1 Detector Sequence Data LSB	CE_H	Yes	Page 100
LFP1H	LF Pattern 1 Detector Sequence Data MSB	CF_H	Yes	Page 99
LFRX0	LF Receiver Configuration Register 0	$B7_H$	Yes	Page 101
LFRX1	LF Receiver Configuration Register 1	$B6_H$	Yes	Page 102
LFRXC	LF Receiver Control Register	$F9_H$	Yes	Page 103
LFRXD	LF Receiver Data Register	$A5_H$	Yes	Page 104
LFRXS	LF Receiver Status Register	$A4_H$	Yes	Page 105
LFSYNCFG	LF SYNC Matching Configuration Register	AF_H	Yes	Page 107
LFSYN0	LF Sync Pattern (low byte)	$A6_H$	Yes	Page 106
LFSYN1	LF Sync Pattern (high byte)	$A7_H$	Yes	Page 106
MMR0	Memory Mapped Register 0	84_H	No	Page 60
MMR1	Memory Mapped Register 1	85_H	No	Page 60
MMR2	Memory Mapped Register 2	86_H	No	Page 60
P1DIR	IO-Port 1 Direction Register	91_H	Yes	Page 150
P1IN	IO-Port 1 Data IN Register	92_H	Yes	Page 152
P1OUT	IO-Port 1 Data OUT Register	90_H	Yes	Page 153
P1SENS	IO-Port 1 Sensitivity Register	93_H	Yes	Page 154
P3DIR	IO-Port 3 Direction Register	EB_H	Yes	Page 151
P3IN	IO-Port 3 Data IN Register	EC_H	Yes	Page 152
P3OUT	IO-Port 3 Data OUT Register	$B0_H$	Yes	Page 153
P3SENS	IO-Port 3 Sensitivity Register	ED_H	Yes	Page 155
PSW	Program Status Word	$D0_H$	No	Page 66
REF	Resume Event Flag Register	$D1_H$	No	Page 39
RFC	RF Transmitter Control Register	EE_H	No	Page 77
RFD	RF Encoder Tx Data Register	$8E_H$	No	Page 77
RFENC	RF Encoder Tx Control Register	$E7_H$	No	Page 78
RFFSPLL	RF Frequency Synthesizer PLL Configuration	$D7_H$	No	Page 80
RFS	RF Encoder Tx Status Register	$E6_H$	No	Page 81
RFFSLD	RF Frequency Synthesizer Lock Detector Configuration	DF_H	Yes	Page 79

Table 12 Special Function Registers Overview

Register Short Name	Register Long Name	Register Address	Supplied in PDWN	Description
RFTX	RF Transmitter Configuration Register	AE_H	Yes	Page 82
RFVCO	RF Frequency Synthesizer VCO Configuration	DE_H	Yes	Page 83
RNGD	RNG Data Register	AB_H	Yes	Page 128
SP	Stack Pointer	81_H	No	Page 65
SPIB	SPI Baud rate Register (11 bit cascaded register)	$F3_H$	No	Page 171
SPIC	SPI Control Register	$F4_H$	No	Page 172
SPID	SPI Data Register	$F5_H$	No	Page 173
SPIM	SPI Mode Register	$F6_H$	No	Page 173
SPIS	SPI Status Register	$F7_H$	No	Page 175
TCON	Timer Control Register (Timer 0/1)	88_H	No	Page 132
TCON2	Timer Control Register 2 (Timer 2/3)	$C8_H$	No	Page 143
TH0	Timer 0 Register (high byte)	$8C_H$	No	Page 133
TH1	Timer 1 Register (high byte)	$8D_H$	No	Page 133
TH2	Timer 2 Register (high byte)	CD_H	No	Page 144
TH3	Timer 3 Register (high byte)	CB_H	No	Page 144
TL0	Timer 0 Register (low byte)	$8A_H$	No	Page 134
TL1	Timer 1 Register (low byte)	$8B_H$	No	Page 134
TL2	Timer 2 Register (low byte)	CC_H	No	Page 145
TL3	Timer 3 Register (low byte)	CA_H	No	Page 145
TMOD	Timer Mode Register (Timer 0/1)	89_H	No	Page 135
TMOD2	Timer Mode Register 2 (Timer 2/3)	$C9_H$	No	Page 146
WUF	Wake-up Flag Register	$C0_H$	Yes	Page 40
WUM	Wake-up Mask Register	$C1_H$	Yes	Page 41
XTAL0	XTAL Frequency Register (FSKLOW)	$C4_H$	Yes	Page 55
XTAL1	XTAL Frequency Register (FSKHIGH/ASK)	$C3_H$	Yes	Page 55
XTCFG	XTAL Configuration Register	$C2_H$	Yes	Page 56

2.7 Microcontroller

Central part of the PMA51xx is an 8051 instruction set compatible microcontroller. The CPU offers an 8 bit data path, an interrupt controller, several addressing modes (direct, register, register indirect, bit direct), and accesses peripheral components using Special Function Registers (SFR). The architecture of the CPU is well known and not part of this description. However some of the features are not needed or adapted to special product requirements. These features are described herein in detail.

The CPU incorporates basic core internal registers. Accumulator (ACC), Register B (B) and Program Status Word (PSW) are bit addressable registers used to perform arithmetical and logical operations. Stack Pointer (SP) and Data Pointer (DPL/DPH) are included to allow basic programming structures.

2.7.1 Register Description

Table 13 Registers Overview

Register Short Name	Register Long Name	Offset Address	Wakeup Value	Reset Value
SP	Stack Pointer	81_H	07_H	07_H
DPL	Data Pointer (low byte)	82_H	00_H	00_H
DPH	Data Pointer (high byte)	83_H	00_H	00_H
PSW	Program Status Word	$D0_H$	00_H	00_H
ACC	Accumulator	$E0_H$	00_H	00_H
B	Register B	$F0_H$	00_H	00_H

Program Status Word

SFR PSW holds the result of basic arithmetic operations.

PSW	Offset	Wakeup Value	Reset Value
Program Status Word	**$D0_H$**	**00_H**	**00_H**

7	6	5	4	3	2	1	0
CY	**AC**	**F0**	**RS1**	**RS0**	**OV**	**F1**	**P**
rw	rw	rw	rw	rw	rw	rw	r

Field	Bits	Type	Description
CY	7	rw	**Carry Bit** Set to 1_B if ACC changes signed number range through $00_H/FF_H$ (unsigned range overflow).
AC	6	rw	**Auxiliary Carry Bit** Carry-out for BCD operations.
F0	5	rw	**General Purpose Bit 0** May be freely used by software.
RS1	4	rw	**Register Select Bit 1** Register bank select bit 1.
RS0	3	rw	**Register Select Bit 0** Register bank select bit 2.
OV	2	rw	**Overflow Bit** Set to 1_B if ACC changes signed number range through $80_H/7F_H$ with arithmetic operations (signed range overflow).
F1	1	rw	**General Purpose Bit 1** May be freely used by software.
P	0	r	**Parity Bit** Reflects the number of 1s in the ACC (set to 1_B if ACC contains an odd number of 1s)

2.8 Interrupt Sources

As in the integrated CPU, the rest of PMA5110 supports interrupt events from several sources which are listed in **Table 14**.

When an unmasked interrupt occurs, the Program Counter (PC) is automatically set to the vector assigned to the interrupt source. From there, the vector is forwarded via LJMP instruction into the FLASH area and the offset of 4000_H is added.

When an unmasked interrupt occurs while the device is in IDLE state, this state is immediately left and the PC continues operation on the appropriate interrupt vector. After the processing of the Interrupt Service Routine (ISR) (RETI instruction), the device automatically returns to the IDLE state in case no Resume Event has occurred in between. If a Resume Event has been detected during the ISR, the RETI instruction returns the PC to the location after the Idle instruction. It is highly recommended that this instruction to be a NOP.

The priority of the interrupts can be configured using the IP register. Setting a bit in IP to one assigns higher priority to the linked interrupt. A high-priority interrupt can then interrupt a service routine from a low-priority interrupt.

Table 14 Interrupt Vector Locations

Interrupt Vector	Vector Address	Forwarded Address	Interrupt Source
Reset Vector	00_H	4000_H	
Vector 0	03_H	4003_H	External Interrupt 0 (PP9)
Vector 1	$0B_H$	$400B_H$	Timer 0 Interrupt
Vector 2	13_H	4013_H	External Interrupt 1 (PP7)
Vector 3	$1B_H$	$401B_H$	Timer 1 Interrupt
Vector 4	23_H	4023_H	I^2C Interface Interrupt
Vector 5	$2B_H$	$402B_H$	SPI Interface Interrupt
Vector 6	33_H	4033_H	Extended Interrupt: The FLASH software has to detect the interrupt source peripheral from this Vector by reading IRQFR and the appropriate source within the peripheral from the various flag registers. • Timer 2 Interrupt • Timer 3 Interrupt • LF Receiver Interrupt • RF Encoder Interrupt

2.8.1 External Interrupts 0 and 1

The PMA51xx has two external interrupt sources, Ext_Int0 on PP9 and Ext_Int1 on PP7. According to the 8051 standard implementation, the control bits and interrupt flags can be found in the TCON register (please refer to **Timer Control Register Timer 0/1 on page 132**).

When enabled by setting IE.0 [EX0] for External Interrupt 0 (resp. IE.2 [EX1] for External Interrupt 1), interrupts can be generated from PP9 (resp. PP7).

External Interrupts 0 and 1 can be programmed to be level-activated or negative-transition activated by clearing or setting bit TCON.0 [IT0], respectively TCON.2 [IT1]. If bit ITx=0, the corresponding external interrupt is triggered by a detected low-level at the pin. If ITx=1, the corresponding external interrupt is negative edge-triggered. In this mode, if successive samples of the pin show a high in one cycle and a low in the next cycle, interrupt request flag IEx in TCON is set. Flag bit IEx=1 then requests the interrupt.

If the external interrupt is level-activated, the external source has to hold the request active until the requested interrupt is actually generated. Then it has to deactivate the request before the ISR is completed, or else another interrupt will be generated.

Each of the external interrupts has its own interrupt vector.

2.8.2 Timer Interrupts

All four timers on the PMA51xx can be used as interrupt sources.

While Timer 0 and Timer 1 are fully compatible with the original 8051 CPU (for a description please refer to “Timer/Counter interrupts” on Page 76), Timer 2 and Timer 3 interrupts are treated as extended interrupts.

2.8.3 I^2C Interface Interrupts

The data transfer on the I^2C interface can be controlled via interrupts. This module has a separate interrupt vector (vector address 4023_H) where the PC is automatically set whenever one of the I^2C interrupt flags is active and the interrupt source is unmasked.

2.8.4 SPI Interface Interrupts

The data transfer on the SPI interface can be controlled via interrupts. This module has a separate interrupt vector (vector address $402B_H$) where the PC is automatically set whenever one of the SPI interrupt flags is active and the interrupt source is unmasked.

2.8.5 LF Receiver Interrupts

While one feature of the LF Receiver is to wake up the device, it is also possible to receive data via the LF interface in RUN mode by selecting the 12 MHz RC oscillator as the system clock. The wake-up flags are used as interrupt event flags, and wake-up mask bits are used as interrupt mask bits as well.

Interrupt Flags

- WUF.5 [LFCD]: Carrier detected
- WUF.4 [LFSY]: Sync match detected
- WUF.3 [LFPM1]: Pattern match pattern 1
- WUF.2 [LFPM0]: Pattern match pattern 0

Interrupt Mask bits

- WUM.5 [LFCD]: If set to 1 the carrier detector interrupt is masked (disabled)
- WUM.4 [LFSY]: If set to 1 the sync match interrupt is masked (disabled)
- WUM.3 [LFPM1]: If set to 1 the pattern match interrupt for pattern 1 is masked (disabled)
- WUM.2 [LFPM0]: If set to 1 the pattern match interrupt for pattern 0 is masked (disabled)

In addition the extended interrupt sources have to be enabled by setting IE.6 [EID] to 1.

2.8.6 RF Encoder Interrupts

The CPU should be kept in the IDLE state during RF transmission, this leads to a better emission spectrum. Nevertheless, it is possible to coordinate the data transfer interrupt driven. Therefore, two interrupt sources are available for RF transmission:

RF Encoder interrupt source flags:

- RFS.0 [RFBF] RF Encoder Buffer Full
- RFS.1 [RFSE] RF Encoder Shift Register Empty

2.8.7 Register Description

Table 15 Registers Overview

Register Short Name	Register Long Name	Offset Address	Wakeup Value	Page Number
IRQFR	Interrupt Request Flag Register for extended interrupts	$8F_H$	00_H	71
IE	Interrupt Enable Register	$A8_H$	00_H	69
IP	Interrupt Priority Register	$B8_H$	00_H	70

Interrupt Enable Register

IE	Offset	Wakeup Value	Reset Value
Interrupt Enable Register	**$A8_H$**	**00_H**	**00_H**

7	6	5	4	3	2	1	0
EA	**EID**	**ESPI**	**EI2C**	**ET1**	**EX1**	**ET0**	**EX0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
EA	7	rw	**Global interrupt enable** 0_B All interrupts are disabled 1_B Interrupts enabled according to their enable bits
EID	6	rw	**Enable extended interrupts** Timer 2/3, LF Receiver, RF Encoder 0_B Interrupts disabled 1_B Interrupts enabled according to their enable bits
ESPI	5	rw	**Enable interrupts from SPI** 0_B Interrupts disabled 1_B Interrupts enabled
EI2C	4	rw	**Enable interrupts from I2C** 0_B Interrupts disabled 1_B Interrupts enabled according to their enable bits
ET1	3	rw	**Enable interrupts from Timer 1** 0_B Interrupts disabled 1_B Interrupts enabled according to their enable bits
EX1	2	rw	**Enable external interrupts from PP7** 0_B Interrupts disabled 1_B Interrupts enabled

Field	Bits	Type	Description
ET0	1	rw	**Enable interrupts from Timer 0** 0_B Interrupts disabled 1_B Interrupts enabled according to their enable bits
EX0	0	rw	**Enable external interrupts from PP9** 0_B Interrupts disabled 1_B Interrupts enabled

Interrupt Priority Register

IP	Offset	Wakeup Value	Reset Value
Interrupt Priority Register	**$B8_H$**	**00_H**	**00_H**

7	6	5	4	3	2	1	0
Res	**PID**	**PSPI**	**PI2C**	**PT1**	**PX1**	**PT0**	**PX0**
	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
Res	7		**Reserved**
PID	6	rw	**Priority level for extended interrupts** Timer 2/3, LF Receiver, RF Encoder 0_B Low priority 1_B High priority
PSPI	5	rw	**Priority level for SPI interrupts** 0_B Low priority 1_B High priority
PI2C	4	rw	**Priority level for I2C interrupts** 0_B Low priority 1_B High priority
PT1	3	rw	**Priority level for Timer 1 interrupts** 0_B Low priority 1_B High priority
PX1	2	rw	**Priority level for external interrupts from PP7** 0_B Low priority 1_B High priority
PT0	1	rw	**Priority level for Timer 0 interrupts** 0_B Low priority 1_B High priority

Field	Bits	Type	Description
PX0	0	rw	**Priority level for external interrupts from PP9** 0_B Low priority 1_B High priority

Interrupt Request Flag Register for extended interrupts

IRQFR	Offset	Wakeup Value	Reset Value
Interrupt Request Flag Register for extended interrupts	**$8F_H$**	**00_H**	**00_H**

7	6	5	4	3	2	1	0
Res				**IRQRFE**	**IRQFLF**	**IRQFT3**	**IRQFT2**
				rc	rc	rc	rc

Field	Bits	Type	Description
Res	7:4		**Reserved**
IRQRFE	3	rc	**Interrupt Request Flag RF Encoder** 0_B No interrupt occurred or flag cleared by readout 1_B RF Encoder interrupt occurred
IRQFLF	2	rc	**Interrupt Request Flag LF Receiver** 0_B No interrupt occurred or flag cleared by readout 1_B LF Receiver interrupt occurred
IRQFT3	1	rc	**Interrupt Request Flag Timer 3** 0_B No interrupt occurred or flag cleared by readout 1_B Timer 3 interrupt occurred
IRQFT2	0	rc	**Interrupt Request Flag Timer 2** 0_B No interrupt occurred or flag cleared by readout 1_B Timer 2 interrupt occurred

2.9 RF Transmitter

The RF Transmitter consists of a PLL Frequency Synthesizer that is contained fully on chip, a Lock Detector, and a Power Amplifier.

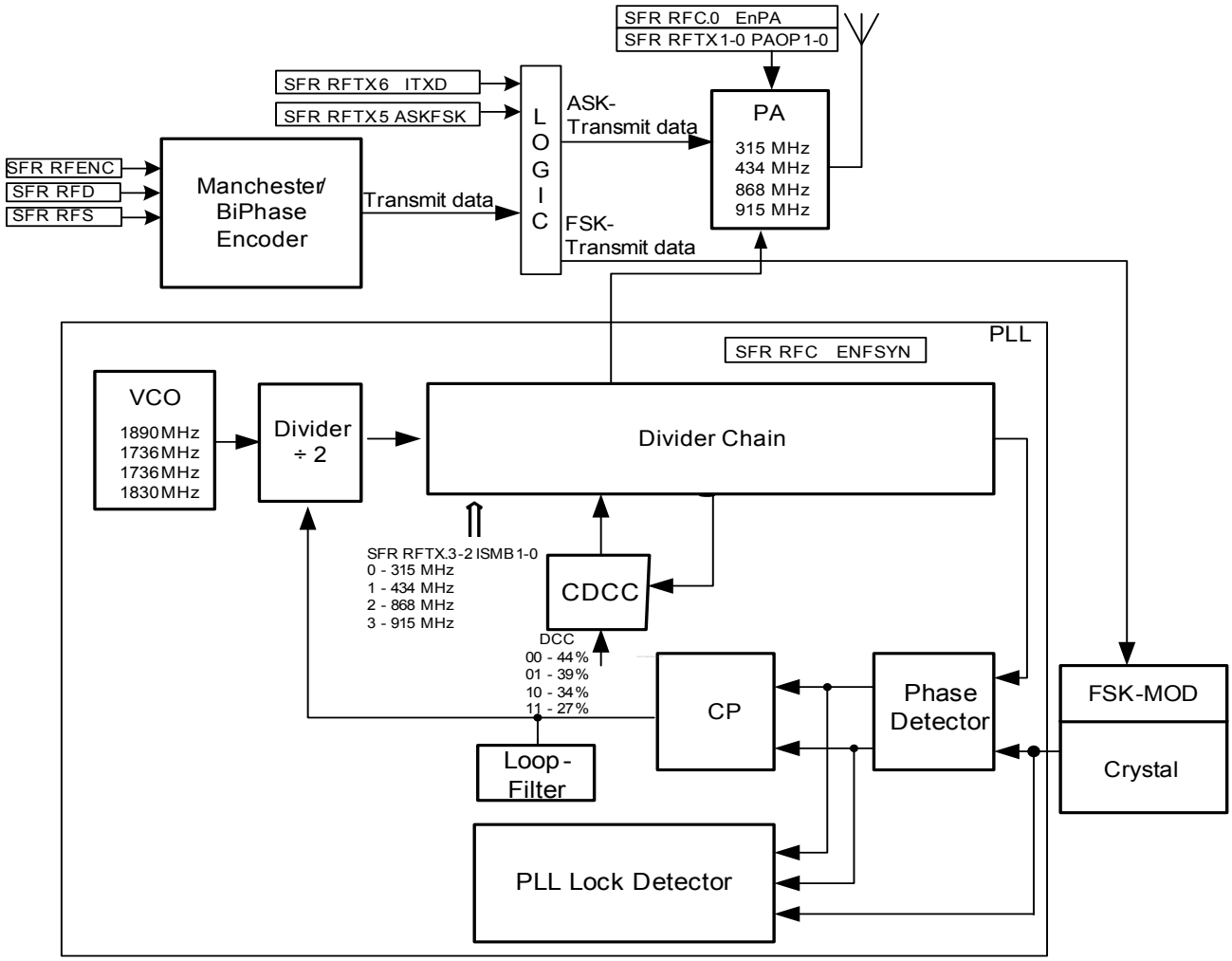


Figure 14 RF Transmitter Block Diagram

The RF Transmitter can be configured for the 315/434/868/915 MHz ISM-Band frequencies by setting SFR bits RFTX.3-2 [ISMB1-0] and choosing the proper crystal. Manchester/BiPhase/NRZ coded data with a bit rate up to 32 kbit/s (64 kchips/s) for the temperature range -40°C to +85°C and 20 kbit/s (40 kchips/s) for temperatures above +85°C can be transmitted using ASK or FSK modulation.

The PLL Synthesizer and the Power Amplifier can be enabled separately by using the SFR RFC control register. The Power Amplifier should be switched on with a delay of at least 100 µs after enabling the Frequency Synthesizer. This delay is needed for PLL locking.

2.9.1 Phase-Locked Loop (PLL)

The PLL consists of an on-chip VCO, an asynchronous divider chain with selectable overall division ratio, a phase detector with charge pump, and an internal loop filter. (see **RF Frequency Synthesizer PLL Configuration on page 80**)

The PLL can be enabled manually by setting SFR bit RFC.1 [ENFSYN]. The PLL lock frequency is determined by the crystal used (see **Figure 10 “Formulas for Crystal selection dependent of RF Bands” on Page 53**) and the appropriate configuration in the SFR bits RFTX.3-2 [ISMB1-0].

2.9.2 Voltage-Controlled Oscillator (VCO)

16 frequency tuning curves are available to tune the VCO. The Library Function *VCOTuning()* can be used to select the appropriate tuning curve for the VCO depending on environmental conditions (temperature, V_{Bat}) and to enable the PLL (please refer to **[1]**).

Selection of the tuning curve can also be done using RFVCO.3-0 [VCOF3-0]. This is done automatically by the Reset Handler after power up or a system reset by using the PLL Lock Detector and the PLL lock-detection routine.

Additionally, the PLL Lock Detector for VCO tuning curve selection may be used by the user program code before RF data transmission.

Note: Recalibration of the tuning curve is typically necessary when the supply voltage changes by more than 800 mV or the temperature changes by more than 70 degrees.

2.9.3 Power Amplifier (PA)

The highly efficient Power Amplifier is enabled automatically if a byte is transmitted (RFS.1 [RFSE] is set to 0_B). Alternatively, the Power Amplifier is enabled immediately by using RFC.0 [ENPA]. RFENC.3 [TXDD] is used to define the quiescent state (symbol that is sent when no data is available in RFD). The nominal transmit power levels are +5/8/10 dBm into a 50 Ω load at a supply voltage of 3.0 V. The Power Amplifier operating point must be optimized to the output power +5/8/10 dBm regarding current consumption by properly setting the RFTX.1-0 [PAOP1-0], RFFSPLL.3-2 [DCC1-0] and using an optimal-sized matching circuit. The Power Amplifier should be enabled at least 100 µs after enabling the RF Frequency Synthesizer because of the PLL lock-in time.

2.9.4 ASK Modulator

ASK modulation is done by turning on and off the Power Amplifier, depending on the baseband data to be transmitted (On/Off-Keying) by using RFENC.3 [TXDD] or the Manchester/Biphase Encoder (see also **Manchester/BiPhase Encoder with Bit Rate Generator**). For information about FSK modulation, please see **Crystal Oscillator**.

2.9.5 Manchester/BiPhase Encoder with Bit Rate Generator

A Manchester/BiPhase encoder controlled by the CPU is available as source for the RF Transmitter. The encoding bit rate can be set with Timer 3 (see **Chapter 2.14.2.3**). The application software needs to configure the timer and can subsequently send the raw uncoded data to the Manchester/BiPhase Encoder which takes care about encoding and the RF transmission itself (controlling the Power Amplifier). Using the hardware encoder allows the CPU to be operated at a reduced clock rate thereby reducing the peak current consumption during RF transmission. The reduced CPU clock rate also reduces the possibility of clock noise artifacts in the RF signal (see **Chapter 2.5.1**). Furthermore, the encoder creates a resume event after sending each byte therefore the application can enter IDLE state while sending each databyte (see **Chapter 2.1.2.3**). It is recommended to use both reduced clock rate and IDLE mode for best performance during RF transmission. A library function is available for comfortable configuration of the Manchester/BiPhase Encoder.

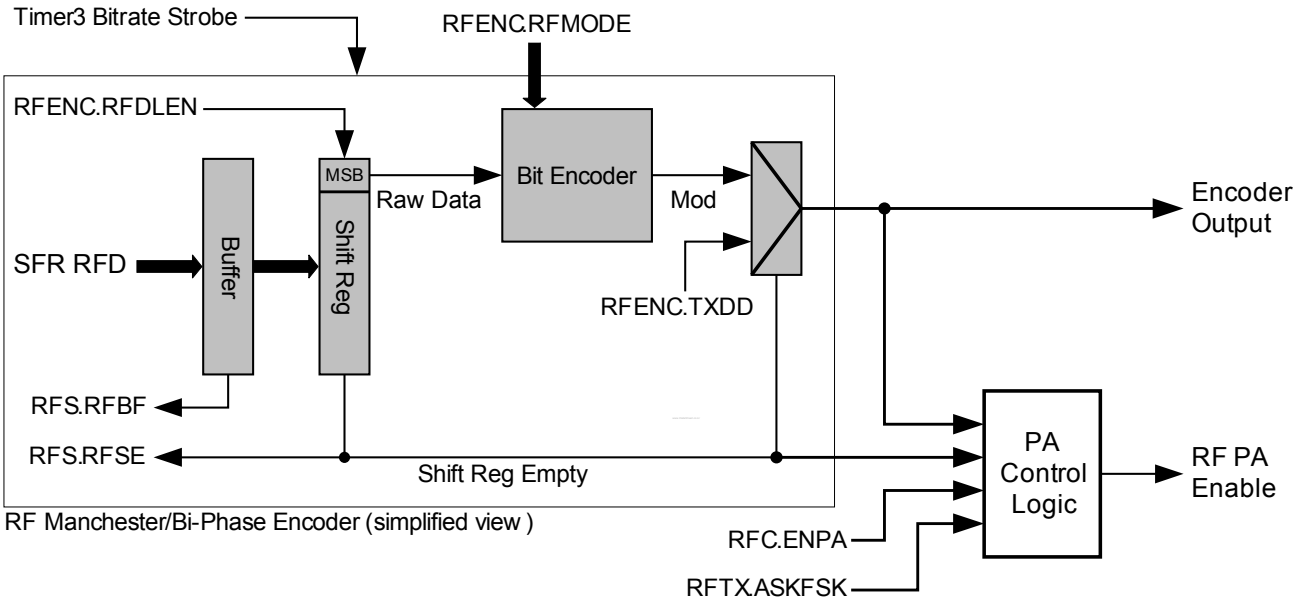


Figure 15 Manchester/BiPhase Encoder

For a transmission using Manchester, BiPhase or Chip coding data is written to SFR RFD. The Manchester/BiPhase Encoder automatically enables the Power Amplifier when a new data byte is written to SFR RFD and disables the Power Amplifier after transmitting the last data bit automatically as well.

The encoding selection can be changed every time before a data byte is written to the SFR RFD by adjusting SFR bits RFENC.2-0 [RFMode2-0].

The Chip coding mode (SFR bits RFENC.2-0 [RFMode2-0] = 101b) can be used to send data with a user-defined encoding scheme, e.g. for sending a preamble. The Chip mode sends each bit without encoding, but at twice the data rate.

For full flexibility in terms of timing and protocol the RF PA can be controlled without using the Bit Encoder. If the shift register is empty, the data value defined by SFR bit RFENC.3 [TXDD] is assigned to the Encoder Output after the RF PA has been enabled by setting SFR bit RFC.1 [ENFSYN] and SFR bit RFC.0 [EnPA]. If any byte is written into SFR RFD the Bit Encoder takes over control of the RF PA until the last bit has been transmitted and the shift register is empty again.

The RF Encoder Output can be connected to PP2, if enabled via CFG1.4[RfTXPEn]. When this alternate port functionality is enabled, the SFR bit RFC.1 [ENFSYN] and SFR bit RFC.0 [EnPA] must be set in order to allow the RF Encoder output to properly modulate the RF PA.

Note: The Power Amplifier should be switched on using SFR bit RFC.0 [EnPA] *with a delay of at least 100 µs after enabling the Frequency Synthesizer using* SFR bit RFC.1 [ENFSYN] *. This delay is needed for PLL locking.*

The following figure shows the different timing diagrams for the various encoding schemes:

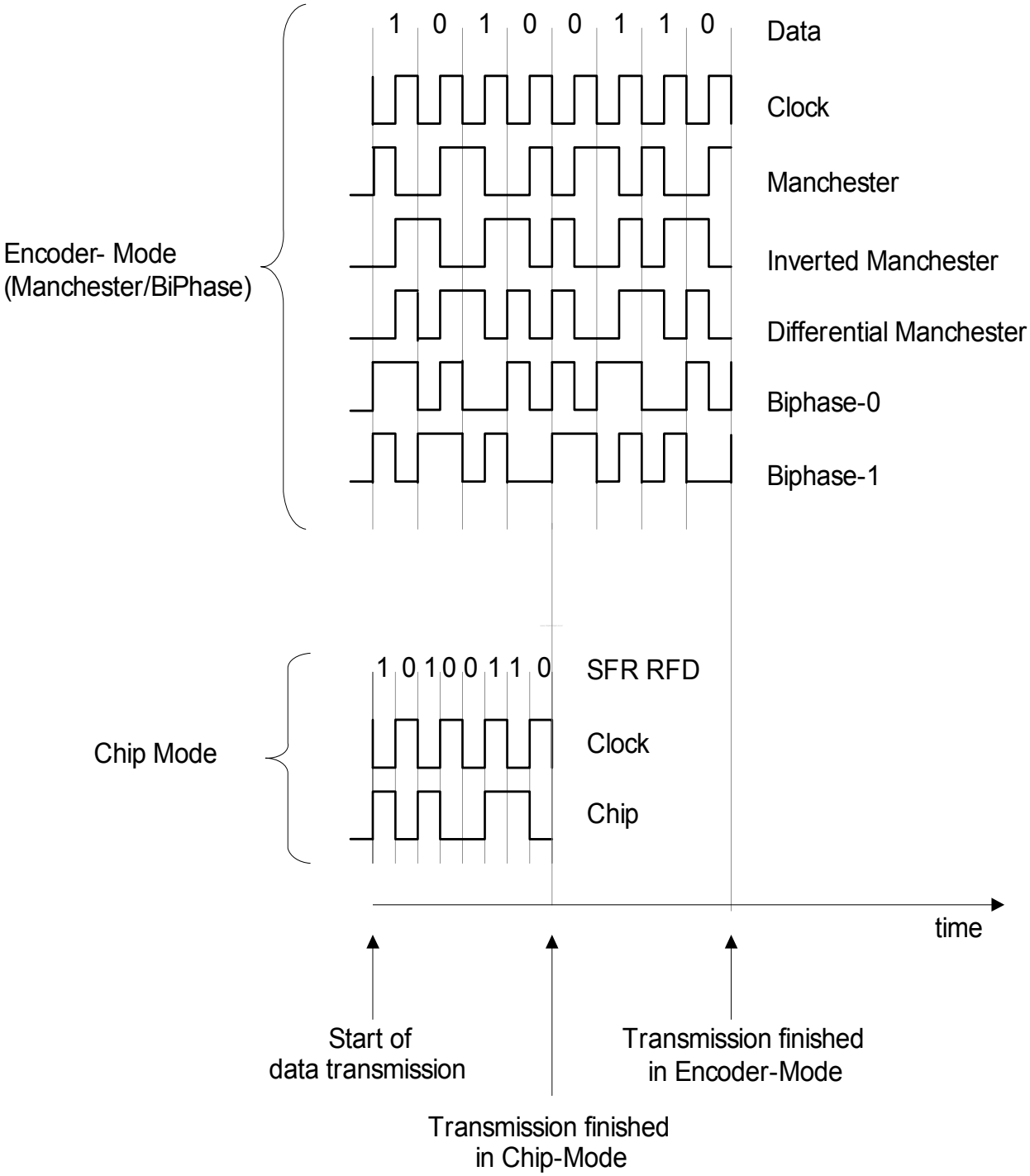


Figure 16 Diagram of the Different RF Encoder Modes

Timer 3 (see **Chapter 2.14.2.3**) provides the bit rate clock and has to be set according to the desired bit rate. The bit rate timer value can be calculated with the following formula:

$$Timer\ value = \frac{f_{Timer\ clock\ source}[Hz]}{8 \cdot Bitrate\left[\frac{1}{s}\right]} - 1$$

Figure 17 Calculation of RF bit rate timer value

Timer 3 has to be configured properly using timer registers (see Registers **TL2**, **TH2**, **TL3**, **TH3**, **TMOD2**, **TCON2**).

The SFR RFS represents the status of the RF Encoder.

After writing a data byte to SFR RFD, the SFR bit RFS.0 [RFBF] is set. It is cleared automatically when the data byte in SFR RFD is transferred to the shift register.

The application should poll SFR bit RFS.0 [RFBF] to determine when the data is transferred to the shift register and SFR RFD can take the next data byte for processing.
It is necessary to provide the transmitter with a continuous data stream. If no data is available, the transmitter falls back to quiescent state (see SFR bit RFENC.3 [TXDD]), if the Power Amplifier has been enabled by SFR bit RFC.1 [ENFSYN] and SFR bit RFC.0 [EnPA], otherwise the Power Amplifier is turned off automatically.

SFR bit RFS.1 [RFSE] is set when the last data bit has been transmitted. If this bit is set, the Power Amplifier and the PLL can be disabled. If there are any data in the shift register this bit is cleared.

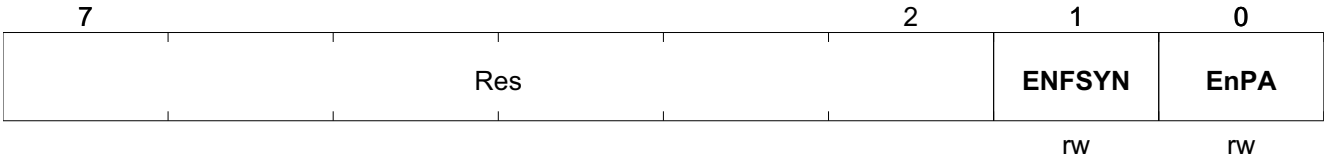
2.9.6 Register Description

Table 16 Registers Overview

Register Short Name	Register Long Name	Offset Address	Wakeup Value	Page Number
RFD	RF Encoder TX Data Register	$8E_H$	00_H	**77**
RFTX	RF Transmitter Configuration Register	AE_H	$UUUUUUUU_B$	**82**
RFFSPLL	RF Frequency Synthesizer PLL Configuration	$D7_H$	82_H	**80**
RFVCO	RF Frequency Synthesizer VCO Configuration	DE_H	$UUUUUUUU_B$	**83**
RFFSLD	RF Frequency Synthesizer Lock Detector Configuration	DF_H	$000UUUUU_B$	**79**
RFS	RF Encoder Tx Status Register	$E6_H$	02_H	**81**
RFENC	RF Encoder Tx Control Register	$E7_H$	$E0_H$	**78**
RFC	RF Transmitter Control Register	EE_H	00_H	**77**

RF Transmitter Control Register

RFC	Offset	Wakeup Value	Reset Value
RF Transmitter Control Register	**EE_H**	**00_H**	**00_H**

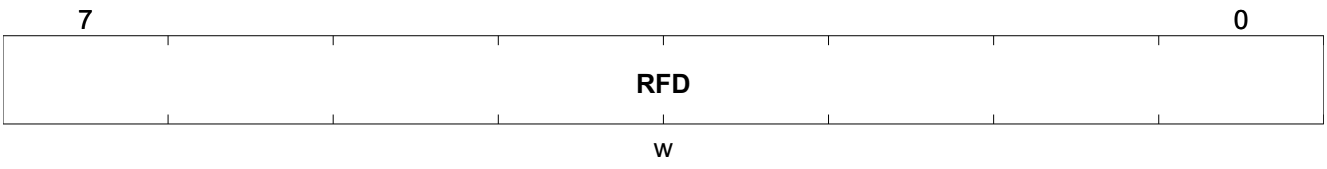


Field	Bits	Type	Description
Res	7:2		**Reserved**
ENFSYN	1	rw	**Enable RF Frequency Synthesizer** 0_B RF Frequency Synthesizer disabled 1_B RF Frequency Synthesizer enabled
EnPA	0	rw	**Enable RF Power Amplifier** 0_B RF Power Amplifier disabled 1_B RF Power Amplifier enabled

RF Encoder TX Data Register

By writing a data byte to the SFR RFD, the data transmission is invoked automatically. By default, the transmission takes place byte-aligned. If fewer than 8 bits are to be transmitted, SFR bits RFENC.7-5 [RFDLen2-0] can be set to determine the number of bits that should be transmitted with MSB first. In this case the unused LSBs are disregarded.

RFD	Offset	Wakeup Value	Reset Value
RF Encoder TX Data Register	**$8E_H$**	**00_H**	**00_H**



Field	Bits	Type	Description
RFD	7:0	w	**RF Encoder TX Data Register**

RF Encoder Tx Control Register

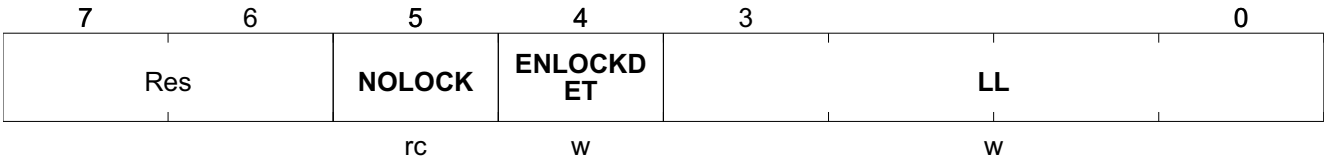
RFENC	Offset	Wakeup Value	Reset Value
RF Encoder Tx Control Register	$E7_H$	$E0_H$	$E0_H$

7	5	4	3	2	0
RFDLen		RFMASK	TXDD	RFDMode	
rw		rw	rw	rw	

Field	Bits	Type	Description
RFDLen	7:5	rw	**RF Data Length** Number of bits to be transmitted from SFR RFD with MSB first. If fewer than 8 bits are transmitted, the unused LSBs are disregarded. 000_B 1 bit 001_B 2 bits 010_B 3 bits 011_B 4 bits 100_B 5 bits 101_B 6 bits 110_B 7 bits 111_B 8 bits
RFMASK	4	rw	**RF Interrupt Mask Flag** 0_B Interrupt enabled 1_B Interrupt disabled (masked)
TXDD	3	rw	**Transmit data** If SFR bit RFC.1-0 [ENFSYN-EnPA] is set. Defines quiescent state on RF TX. Symbol that is sent when no data is available in RFD. 0_B RF TX transmits symbol for 0_B 1_B RF TX transmits symbol for 1_B
RFDMode	2:0	rw	**RF Encoder Mode** A diagram of the different RF Encoder Modes can be found in **Figure 16**. 000_B Manchester 001_B Inverted Manchester 010_B Differential Manchester 011_B BiPhase-0 100_B BiPhase-1 101_B Chips: Data bits are interpreted as chips 110_B Reserved 111_B Reserved

RF Frequency Synthesizer Lock Detector Configuration

RFFSLD	Offset	Wakeup Value	Reset Value
RF Frequency Synthesizer Lock Detector Configuration	DF_H	$000UUUUU_B$	08_H



Field	Bits	Type	Description
Res	7:6		**Reserved**
NOLOCK	5	rc	**PLL Lock Indicator** 0_B PLL has locked or bit cleared by read out 1_B PLL has not locked while ENLOCKDET=1_B
ENLOCKDET	4	w	**Enable Lock Detector** 0_B Lock Detector disabled 1_B Lock Detector enabled
LL	3:0	w	**Lock Limit Selection** Sets the number of phase synchronization violation. LL3-0 count value is reset to zero when the ENLOCKDET bit is reset. 0000_B First violation will trigger NOLOCK 0001_B Second violation will trigger NOLOCK **...** 1110_B 15^{th} violation will trigger NOLOCK 1111_B 16^{th} violation will trigger NOLOCK

RF Frequency Synthesizer PLL Configuration

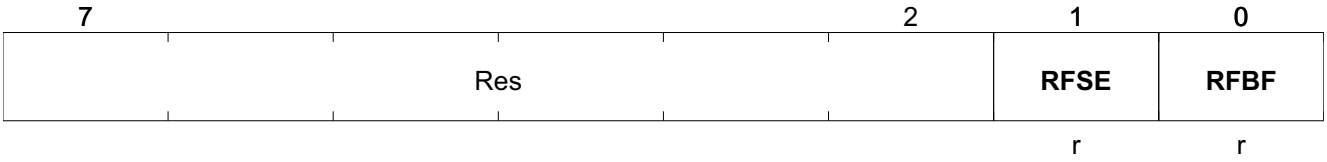
RFFSPLL	Offset	Wakeup Value	Reset Value
RF Frequency Synthesizer PLL Configuration	$D7_H$	82_H	82_H

7	6	5	4	3	2	1	0
FPDPOL	DDCC	ABLP		DCC		CPCU	
w	w	w		w		w	

Field	Bits	Type	Description
FPDPOL	7	w	**Frequency-Phase-Detector polarity** Must be 1_B
DDCC	6	w	**Disable RF divider duty cycle control** 0_B RF divider duty cycle control enabled 1_B RF divider duty cycle control disabled
ABLP	5:4	w	**Antibacklash pulse width selection** 00_D 1.2ns (default value, do not change)
DCC	3:2	w	**RF divider duty cycle control (high/low ratio)** The RF divider duty cycle control can be used to increase the Power Amplifier output power at low supply voltages. 00_B 44% 01_B 39% 10_B 34% 11_B 27%
CPCU	1:0	w	**Charge pump current selection** 10_B 20µA (default value, do not change)

RF Encoder Tx Status Register

RFS	Offset	Wakeup Value	Reset Value
RF Encoder Tx Status Register	$E6_H$	02_H	02_H



Field	Bits	Type	Description
Res	7:2		**Reserved**
RFSE	1	r	**RF Encoder Shift Register Empty** This bit is automatically set by hardware if no further bits are available in the shift register. 0_B RF Encoder shift register is not empty 1_B RF Encoder shift register is empty
RFBF	0	r	**RF Encoder Buffer Full** This bit is automatically set by hardware on write access to register RFD or cleared if data in register RFD is transferred to shift register respectively. 0_B RF Encoder buffer empty 1_B RF Encoder buffer full

RF Transmitter Configuration Register

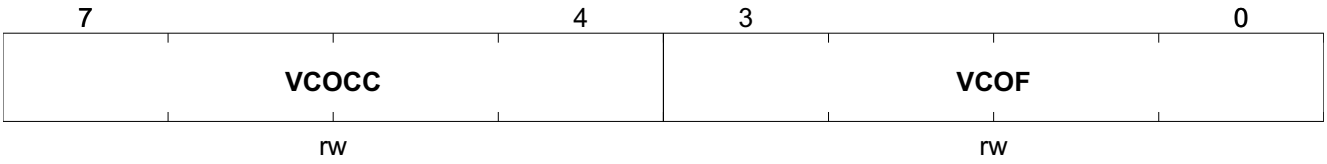
RFTX	Offset	Wakeup Value	Reset Value
RF Transmitter Configuration Register	AE_H	$UUUUUUUU_B$	07_H

7	6	5	4	3	2	1	0
XCapSH	**INVTXDAT**	**ASKFSK**	Res	**ISMB**		**PAOP**	
w	w	w		w		w	

Field	Bits	Type	Description
XCapSH	7	w	**Enable XCAP short** More information about this bit can be found in **Chapter 2.5.4**. 0_B XCAP short disabled 1_B XCAP short enabled
INVTXDAT	6	w	**Invert TX Data** 0_B TX data not inverted 1_B TX data inverted
ASKFSK	5	w	**TX Mode** 0_B FSK 1_B ASK
Res	4		**Reserved**
ISMB	3:2	w	**RF Frequency Select ISMB** 00_B 315MHz frequency range 01_B 434MHz frequency range 10_B 868MHz frequency range 11_B 915MHz frequency range
PAOP	1:0	w	**RF Power Amplifier Output Power Selection** 00_B 5dBm 01_B 8dBm 10_B 8dBm 11_B 10dBm

RF Frequency Synthesizer VCO Configuration

RFVCO	Offset	Wakeup Value	Reset Value
RF Frequency Synthesizer VCO Configuration	DE_H	$UUUUUUUU_B$	90_H



Field	Bits	Type	Description
VCOCC	7:4	rw	**VCO Core Current Selection** 0000_B 0µA 0001_B 200µA 0010_B 400µA 0011_B 600µA 0100_B 800µA 0101_B 1000µA 0110_B 1200µA 0111_B 1400µA 1000_B 1600µA 1001_B 1800µA 1010_B 2000µA 1011_B 2200µA 1100_B 2400µA 1101_B 2600µA 1110_B 2800µA 1111_B 3000µA
VCOF	3:0	rw	**VCO Tuning Curve Selection** 0000_B Tuning Curve 0 0001_B Tuning Curve 0 **...** 1110_B Tuning Curve 14 1111_B Tuning Curve 15

2.10 LF Receiver

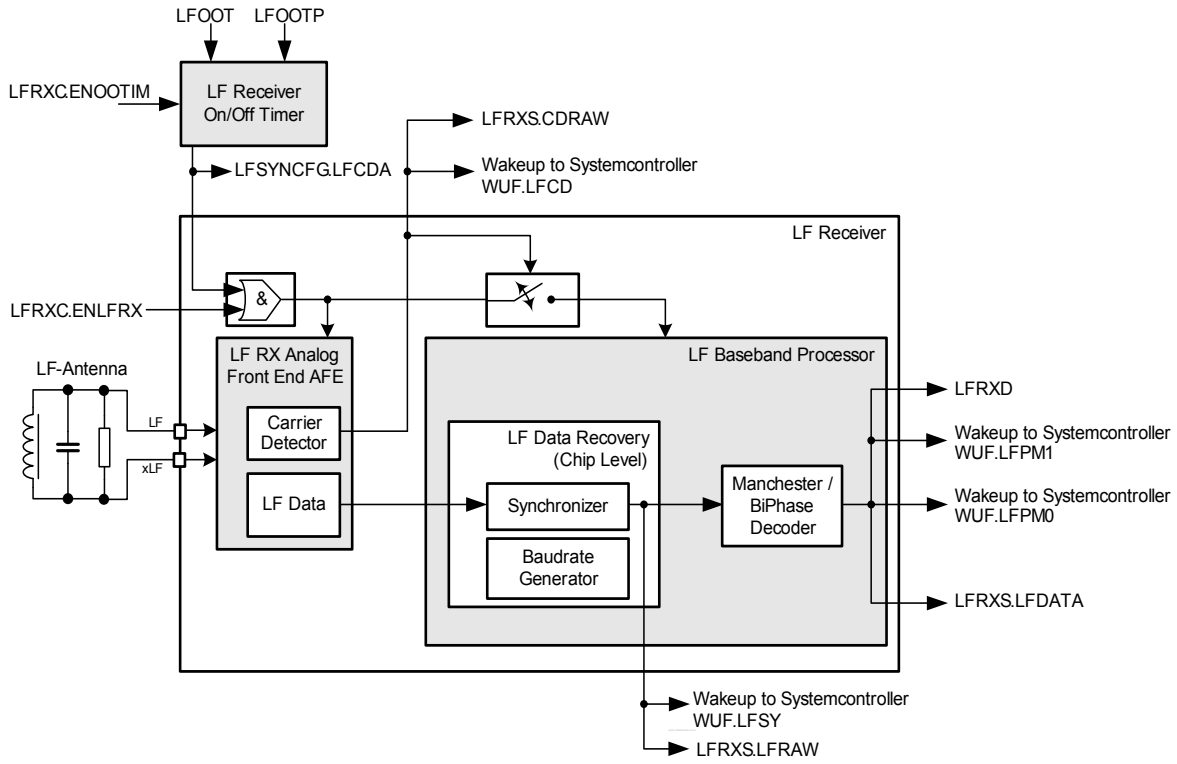


Figure 18 LF Receiver

The LF Receiver is used for wireless data transmission towards the PMA5110 and for waking up the device from POWER DOWN state.

It can generate a wake-up directly by the Carrier Detector if the carrier amplitude is above a preset threshold, or it can decode the received data and not wake up the microcontroller until a predefined sync match pattern or wake-up pattern is detected in the data stream.

Data recovery using a synchronizer and a decoder is available for Manchester and BiPhase coded data. The synchronizer can also handle Manchester/BiPhase code violations. Any other coding scheme can be handled directly by the microcontroller on the chip level without using the decoder.

An LF On/Off Timer is implemented to generate periodic on/off switching of the LF Receiver in the POWER DOWN state. This can be done to reduce the current consumption.

2.10.1 LF Receiver Analog Front End Configuration

The LF Receiver Analog Front End (AFE) consists of an input attenuator with an Automatic Gain Control (AGC), an amplifier with selectable gain, an ASK demodulator, a Data Filter and Data Slicer with adjustable filter bandwidth for different data rate. Additionally, a Carrier Detector with adjustable threshold is implemented. A LF Carrier Detector Filter can be enabled to avoid wake-up by interferers.

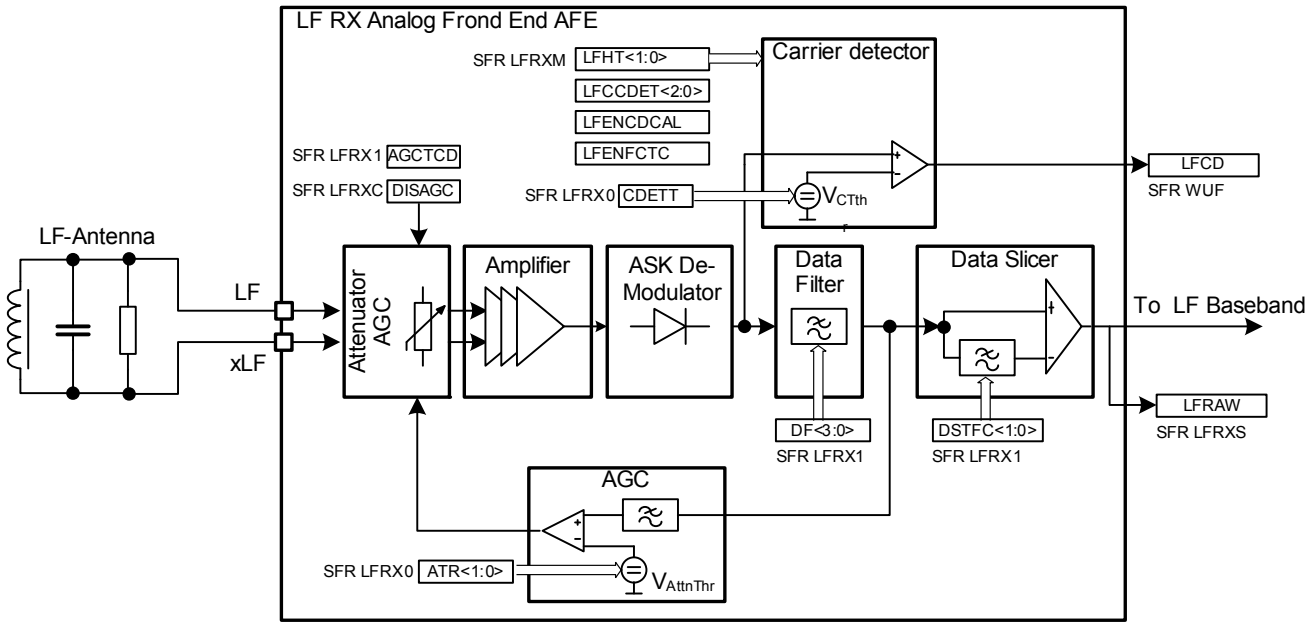


Figure 19 LF Receiver AFE Block Diagram

2.10.1.1 Attenuator (AGC) and Data Filter / Data Slicer

An input attenuator is provided to limit strong signals and interferers across the differential input. The attenuator detects the receiver input level and acts as an automatic gain control block (fast attack, slow decay). The attenuator decay slew rate can be adjusted by changing the decay slew rate using SFR bits LFRX1.7-6 [AGCTCD1-0].

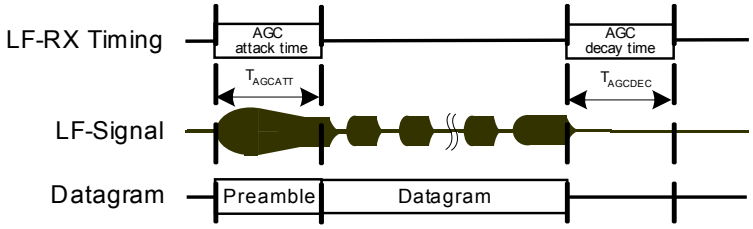


Figure 20 LF Receiver AFE Block Diagram

SFR LFRX1 is as well used to configure the data slicer and data filter according to the desired bit rate.

2.10.1.2 LF Carrier Detector

A level-detection circuit is implemented to determine if the carrier amplitude is above a predetermined level. This can be used to wake up the PMA5110 from the POWER DOWN state by an externally applied LF signal. In the POWER DOWN state, the LF Carrier Detector can either:

- Generate a wake-up and enter the RUN state as soon as an LF carrier is detected (SFR bit WUF.5 [LFCD] = 1_B)
- Enable the LF baseband and the 12 MHz RC HF oscillator in the POWER DOWN state to process the incoming LF signal by looking for a sync match or pattern match (SFR bits WUF.2,3 or 4 = 1_B). If a sync match or pattern match is received, the system controller generates a wake-up and enters the RUN state for further data processing.

Note: In both cases the overall LF sensitivity is determined by the LF Carrier Detector, since it determines if the LF baseband is enabled or disabled.

Since the LF-Signal is ASK modulated a carrier detect hold time is specified to prolong the carrier detect signal. A minimum hold time must be set depending on the data rate using LFCDM.1-0 [LFHT1-0] (

The hold time functionality is illustrated in the following figure.

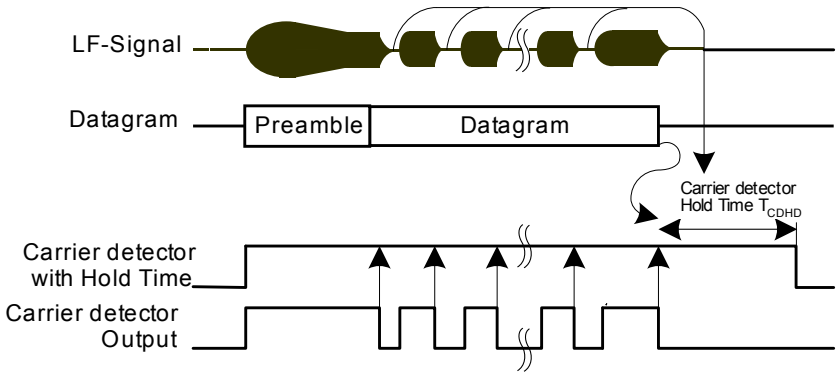


Figure 21 LF Receiver Carrier Detector Hold Time Behavior

2.10.1.2.1 Carrier Detector Threshold Calibration

To achieve high sensitivity, the Carrier Detector has to be calibrated to compensate for possible system noise and production spread. This calibration is enabled by setting SFR bit LFCDM.3 [LFENCDCAL] and is executed every time the LF Receiver is switched on (either manually by SFR bit LFRXC.2 [ENLFRX] or automatically by the LF On/Off Timer). Since this is done during the settling time of the LF Receiver, no extra delay is required for this calibration.

The Carrier Detector Threshold Level which is used for this calibration can be set by SFR bits LFRX0.7-4[CDETT].

Attention: To stabilize the specified sensitivity S_{LF1} (please refer to Table 38), the Library function LFSensitivityCalibration() has to be used (please refer to [1]).

If set, SFR bit LFCDM.2 [LFENFCTC] “freezes” the calibrated threshold level. If this bit is not set, the threshold will follow the mean value of the input signal, resulting in a threshold signal that is dependent on the LF signal strength and length.

If SFR bit LFCDM.2 [LFENFCTC] is set, a periodic recalibration is required, especially at higher temperatures since the “frozen” threshold level might drift after the Carrier Detector Freeze Hold Time (T_{CDCFH}). The recalibration is achieved automatically by the next off/on transition of the LF On/Off Timer or by disabling/enabling the LF Receiver manually by SFR bit LFRXC.2 [ENLFRX].

Note: If the LF Receiver is disabled/enabled manually at least one 2 kHz RC LP oscillator period has to be wait between off and on transition to achieve the automatic recalibration.

The following figure shows the timing behavior of the calibration.

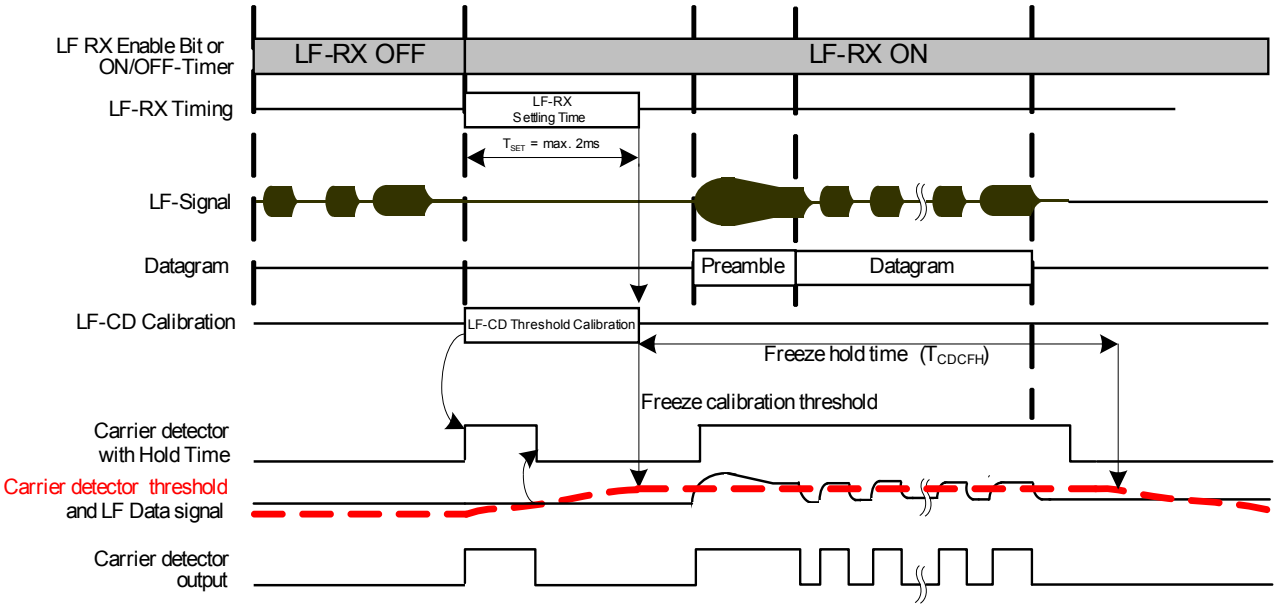


Figure 22 Carrier Detector Threshold Calibration Timing (with “freeze”)

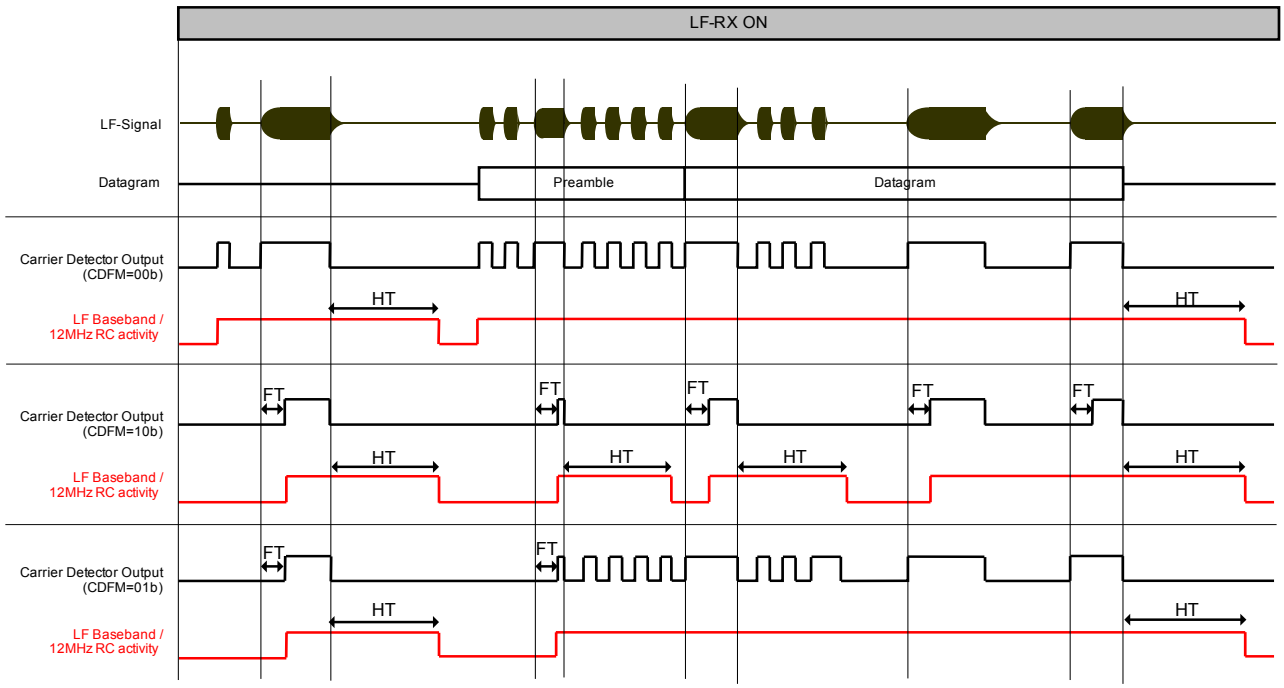
2.10.1.2.2 Carrier Detector Filtering

To prevent the device from undesired carrier-detect wake-ups and to prevent the LF baseband and 12 MHz RC HF oscillator from being enabled due to interference, an LF Carrier Detector Filter is implemented. SFR LFCDFlt is used to determine the filtering mode and the filtering time.

Three LF Carrier Detector filtering operation modes are available:

- LFCDFlt.1-0 [CDFM] = 00_B
  The LF Carrier Detector Filter is switched off so the wake-up functionality will remain without any filtering
- LFCDFlt.1-0 [CDFM] = 10_B
  The LF Carrier Detector Filter is always active - This mode is suitable for applications that use a carrier wake-up without any data transmission
- LFCDFlt.1-0 [CDFM] = 01_B
  The LF Carrier Detector Filter is deactivated when an ON pulse is received. The Preamble must contain an ON pulse (LF carrier active) longer than the selected filter time to enable the LF baseband and the 12 MHz RC HF oscillator. After the ON-pulse is received, the filter is disabled for data receiving until no more data is received. Depending on the selected hold time (SFR bits LFCDM.1-0 [LFHT1-0]), the filter will be re-enabled after the last received bit.

The following figure shows the behavior of the various modes.



FT: Filtering Time (determined by SFR Bit LFCDFLT.1-0[CDFT1-0])
HT: Hold Time (determined by SFR Bit LFCDM.1-0[LFHT1-0])

Figure 23 LF Receiver Carrier Detector Filtering

2.10.2 LF Receiver On/Off Timer

An On/Off Timer is implemented to reduce the LF Receiver current consumption in POWER DOWN state. It can be enabled by SFR bit LFRXC.3 [ENOOTIM].

The LF Receiver Analog Frontend will be periodically switched on or off corresponding to the timer settings. The current state of the LF Receiver (on or off) is available in SFR bit LFSYNCFG.7[LFCDA].

The LF Receiver On/Off Timer incorporates a precounter (SFR LFOOTP) as time base and a post counter for independently setting the On time and the Off time (SFR LFOOT).

2.10.2.1 LF Receiver On/Off Timer Calibration

The calibration process is done automatically by a Library function (see **[1]**). The time base is automatically calibrated to 50 ms by this function. If another (uncalibrated) time base is needed, SFR LFOOTP can be configured manually by using the equation shown in **Figure 24**.

$$timebase[s] = \frac{LFOOTP + 1}{f_{2\,kHz\,RC\,LP\,Oscillator}[Hz]}$$

Figure 24 Calculation of time base for LF Receiver On/Off Timer

The On time and the Off time can be configured individually using SFR LFOOT. They can be calculated using the equations shown in **Figure 25** and **Figure 26**.

$$ontime[s] = \frac{(ONTIM+1)\cdot\left(Integer\left(\frac{LFOOTP}{4}\right)+1\right)}{f_{2kHz\,RC\,LP\,Oscillator}[Hz]} = \frac{(ONTIM+1)\cdot\left(Integer\left(\frac{LFOOTP}{4}\right)+1\right)\cdot timebase[s]}{LFOOTP+1}$$

Figure 25 Calculation of On time for LF Receiver On/Off Timer

$$offtime[s] = \frac{(OFFTIM+1)\cdot(LFOOTP+1)\cdot 4}{f_{2kHz\,RC\,LP\,Oscillator}[Hz]} = (OFFTIM+1)\cdot timebase[s]\cdot 4$$

Figure 26 Calculation of Off time for LF Receiver On/Off Timer

2.10.3 LF Receiver Baseband Processor

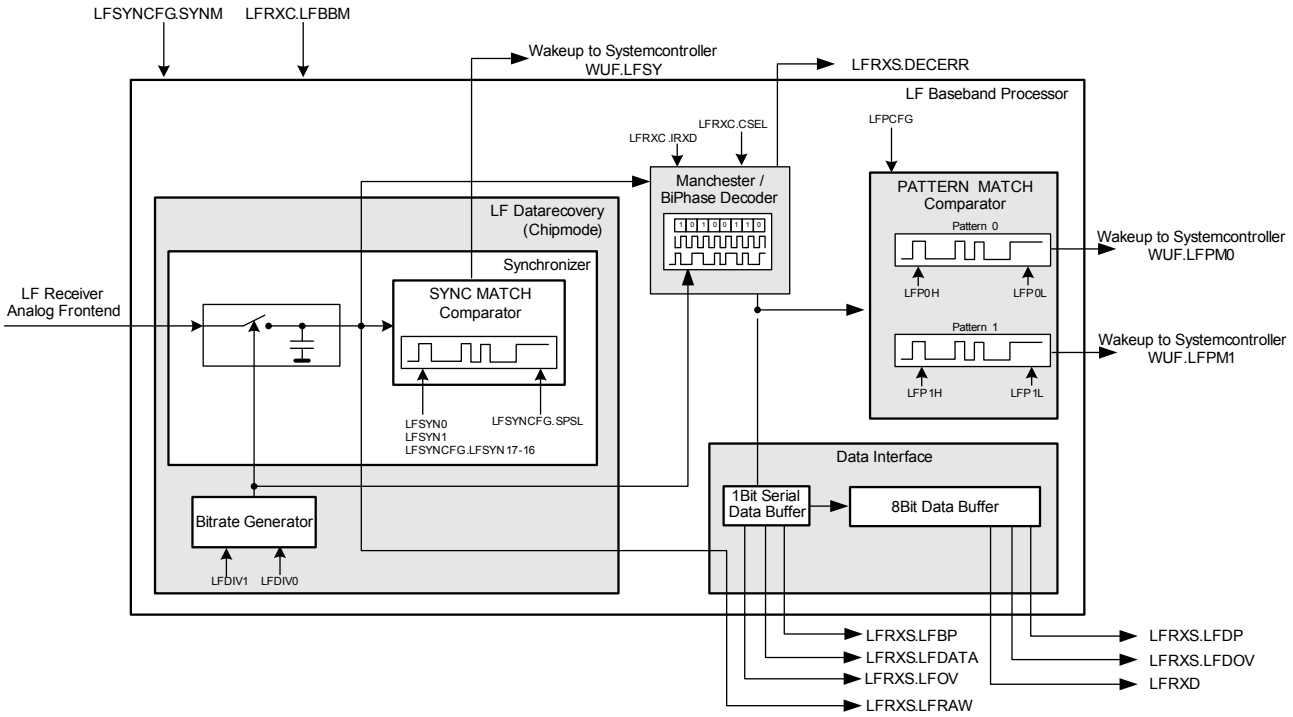


Figure 27 LF Receiver Baseband

The LF Receiver Baseband Processor ca n be configured to receive the following datagram formats by using the SFR bits LFSYNCFG.1-0 [SYNM1-0].

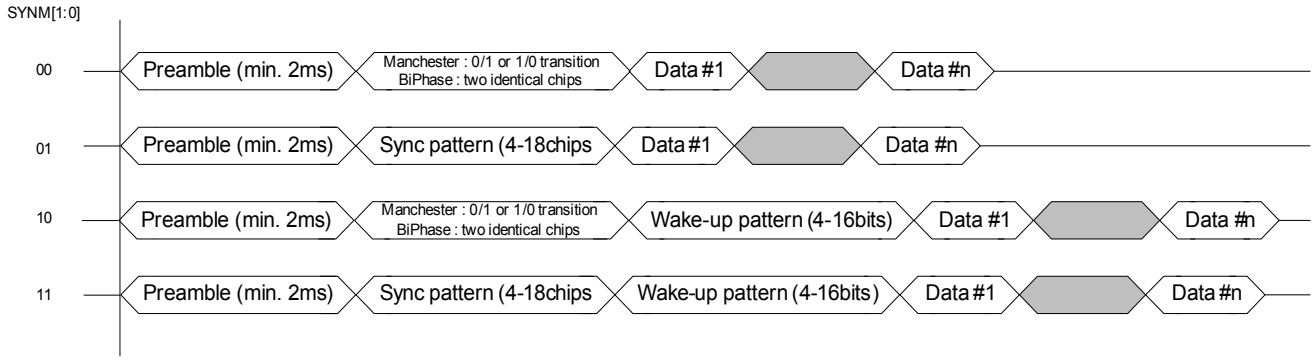


Figure 28 LF Receiver Baseband Configurations

2.10.3.1 Synchronizer

A sync pattern of up to 18 chips can be specified (SFR LFSYN1, SFR LFSYN0 and SFR bits LFSYNCFG.5-4 [LFSYN17-16]) and compared to the synchronized received bit stream. The comparison takes place before decoding, so sync patterns with code violations can also be detected. Code violations are defined to have at least three consecutive chips without level transitions.

Note: The sync pattern should maintain a 50/50 ratio of LOW / HIGH chips to preserve a DC Level of 50% and must not contain more than 3 consecutive chips at the same level.

2.10.3.2 Bit rate Generator

The SFR LFDIV1 and SFR LFDIV0 define the LF Receiver bit rate. Depending on the selected system clock, either the left or the right formula has to be used.

$$\left(LFDIV1/0 = \frac{f_{12MHz\,RC\,HF\,Oscillator}[Hz]}{16 \cdot baudrate\left[\frac{1}{s}\right]} \right) or \left(LFDIV1/0 = \frac{f_{Crystal}[Hz]}{32 \cdot baudrate\left[\frac{1}{s}\right]} \right)$$

Figure 29 Calculation of LF Receiver bit rate

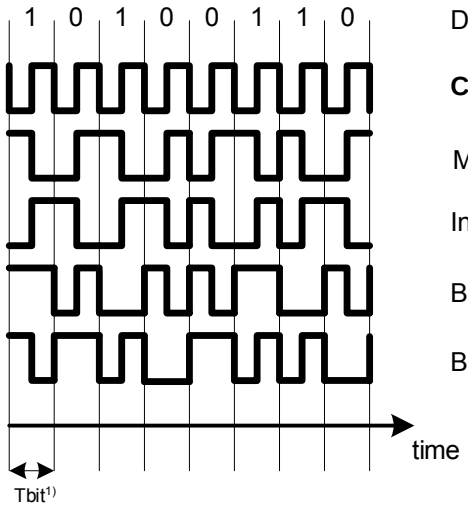
For sync match and pattern match, the bit rate generator is needed in POWER DOWN state. The only available system clock in POWER DOWN state is the 12 MHz RC HF oscillator.

To avoid switching bit rates, the system clock should never be changed during LF reception is running.

Due to the drift of the 12 MHz RC HF oscillator, a calibration mechanism is provided as a Library function and is described in [1]. This Library function automatically configures SFR LFDIV0 and SFR LFDIV1.

2.10.3.3 LF Data Decoder

The decoder can be used for Manchester or BiPhase encoded data. If a code violation is detected SFR bit LFRXS.6 [DECERR] is set to 1_B. Figure 30 shows a summary of the available coding schemes and the appropriate register settings.



Register Configuration	
LFRXC.CSEL	LFRXC.IRXD
0	0
0	1
1	0
1	1

1) Duration of a Manchester / BiPhase coded bit

Figure 30 LF Receiver Data Decoder schemes

2.10.3.4 Wake-up Pattern Detector

Two different wake-up patterns with a length of 4, 8 or 18 bits can be stored by using SFRs LFP0H, LFP0L, LFP1H and LFP1L.

SFR WUM determines on which pattern (pattern 0, pattern 1, or both) a wake-up occurs.

2.10.3.5 LF Receiver Data Interface

The received data can be read by the microcontroller using the following different interfaces:

- 8 bit data byte (synchronized, Manchester/BiPhase decoded)
- Serial bit stream data (synchronized, Manchester/BiPhase decoded)

- RAW data (synchronized, chip level)
- RAW Carrier Detect (not synchronized)

2.10.3.5.1 8 bit data byte

Synchronized and decoded data bytes are received using SFR LFRXD. Decoded bits are shifted into an 8 bit receive buffer, until a byte boundary is reached. The received byte is then shifted into the SFR LFRXD, and a flag SFR bit LFRXS.3 [LFDP] is set, while the following byte starts shifting into the receive buffer. If the SFR LFRXD is not read before the following byte is received, it will be overwritten and an overflow flag SFR bit LFRXS.4 [LFDOV] is set.

2.10.3.5.2 Serial bit stream data

Synchronized and decoded serial data is received in the SFR bit LFRXS.0 [LFDATA]. A flag SFR bit LFRXS.1 [LFBP] is set if data is pending, while the following bit is buffered. If the SFR bit LFRXS.0 [LFDATA] is not read before the following bit is received, it will be overwritten, and an overflow flag SFR bit LFRXS.2 [LFOV] is set.

2.10.3.5.3 RAW data

Synchronized and not decoded serial data (on the chip level) can be read by the microcontroller using SFR bit LFRXS.5 [LFRAW]. This can be used for any coding scheme.

2.10.3.5.4 RAW Carrier Detect

Not synchronized and not decoded serial data can be read by the microcontroller using SFR bit LFRXS.7 [CDRAW]. This indicates if a carrier signal is currently present (SFR bit LFRXS.7[CDRAW] = 1_B) or not (SFR bit LFRXS.7 [CDRAW] = 0_B).

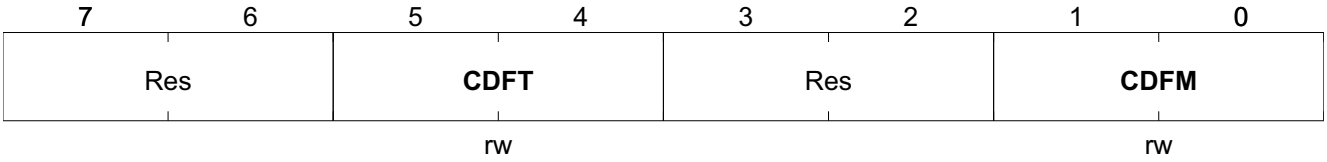
2.10.4 Register Description

Table 17 Registers Overview

Register Short Name	Register Long Name	Offset Address	Wakeup Value	Page Number
LFRXS	LF Receiver Status Register	$A4_H$	00_H	105
LFRXD	LF Receiver Data Register	$A5_H$	00_H	104
LFSYN0	LF Sync Pattern 0	$A6_H$	$UUUUUUUU_B$	106
LFSYN1	LF Sync Pattern 1	$A7_H$	$UUUUUUUU_B$	106
LFSYNCFG	LF SYNC Matching Configuration Register	AF_H	X0UUUUUUB	107
LFCDFlt	LF Carrier Detect Filtering	$B2_H$	$00UU00UU_B$	94
LFDIV0	LF Division Factor low byte	$B3_H$	$UUUUUUUU_B$	96
LFDIV1	LF Division Factor high byte	$B4_H$	$00000UUU_B$	96
LFCDM	LF Carrier Detector Mode	$B5_H$	$UUUUUUUU_B$	95
LFRX1	LF Receiver Configuration Register 1	$B6_H$	$UUUUU0UU_B$	102
LFRX0	LF Receiver Configuration Register 0	$B7_H$	$UUUUUUUU_B$	101
LFP0L	LF Pattern 0 Detector Sequence Data LSB	BE_H	$UUUUUUUU_B$	99
LFP0H	LF Pattern 0 Detector Sequence Data MSB	BF_H	$UUUUUUUU_B$	98
LFOOTP	LF On/Off Timer Precounter	$C5_H$	$UUUUUUUU_B$	98
LFOOT	LF On/Off Timer Configuration Register	$C6_H$	$UUUUUUUU_B$	97
LFPCFG	LF Pattern Detection Configuration Register	$C7_H$	$00000UUU_B$	100
LFP1L	LF Pattern 1 Detector Sequence Data LSB	CE_H	$UUUUUUUU_B$	100
LFP1H	LF Pattern 1 Detector Sequence Data MSB	CF_H	$UUUUUUUU_B$	99
LFRXC	LF Receiver Control Register	$F9_H$	$UUUUUUUU_B$	103

LF Carrier Detect Filtering

LFCDFlt	Offset	Wakeup Value	Reset Value
LF Carrier Detect Filtering	$B2_H$	$00UU00UU_B$	00_H



Field	Bits	Type	Description
Res	7:6		**Reserved**
CDFT	5:4	rw	**Carrier Detector Filtering Timer** 00_B Shortest filtering time 10_B Short filtering time 11_B Long filtering time 11_B Longest filtering time
Res	3:2		**Reserved**
CDFM	1:0	rw	**Carrier Detector Filtering Mode** Detailed information can be found in **Chapter 2.10.1.2.2**. 00_B Filter disabled 01_B Filter disabled after ON pulse received (re-enabled again 1-8ms after last bit is received, dependent on hold time determined by SFR bit LFCDM.1-0 [LFHT1-0] 10_B Filter always active 11_B Reserved

LF Carrier Detector Mode

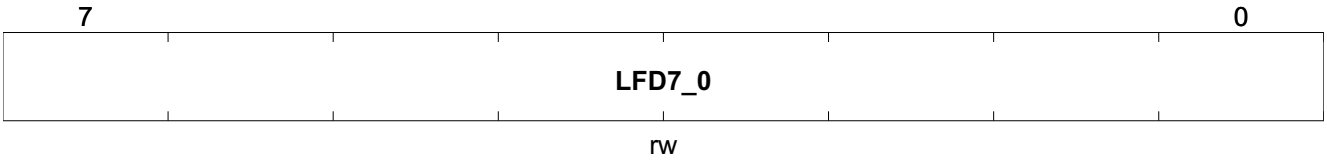
LFCDM	Offset	Wakeup Value	Reset Value
LF Carrier Detector Mode	$B5_H$	$UUUUUUUU_B$	00_H

7	6	5	4	3	2	1	0
LFOOEXT	LFCCDET			LFENCDCAL	LFENFCTC	LFHT	
rw	rw			rw	rw	rw	

Field	Bits	Type	Description
LFOOEXT	7	rw	**LF ON-time Extension on Carrier Detect** 0_B LF On/Off time is acting as configured in **LFOOT on page 198**LFOOT on page 97 and **LFOOTP on page 98** 1_B LF On time is extended as long as a LF carrier, that exceeds the threshold, is present.
LFCCDET	6:4	rw	**LF Calibrate Carrier Detect Threshold Selection** *Note: Must be set to 000_B*
LFENCDCAL	3	rw	**LF Enable Carrier Detect Calibration** 0_B LF carrier detect calibration disabled 1_B LF carrier detect calibration enabled
LFENFCTC	2	rw	**LF Enable Calibration Threshold Freeze** 0_B LF calibration threshold freeze disabled 1_B LF calibration threshold freeze enabled
LFHT	1:0	rw	**LF Carrier Detector Hold Time Selection** 00_B 2x 2 kHz RC LP oscillator period (typ. 1 ms) 01_B 4x 2 kHz RC LP oscillator period (typ. 2 ms) 10_B 8x 2 kHz RC LP oscillator period (typ. 4 ms) 11_B 16x 2 kHz RC LP oscillator period (typ. 8 ms)

LF Division Factor low byte

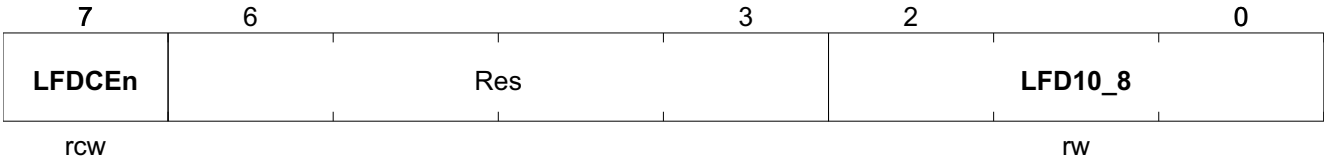
LFDIV0	Offset	Wakeup Value	Reset Value
LF Division Factor low byte	$B3_H$	$UUUUUUUU_B$	00_H



Field	Bits	Type	Description
LFD7_0	7:0	rw	**LF bit rate generator division factor bit 7 down to bit 0**

LF Division Factor high byte

LFDIV1	Offset	Wakeup Value	Reset Value
LF Division Factor high byte	$B4_H$	$00000UUU_B$	00_H

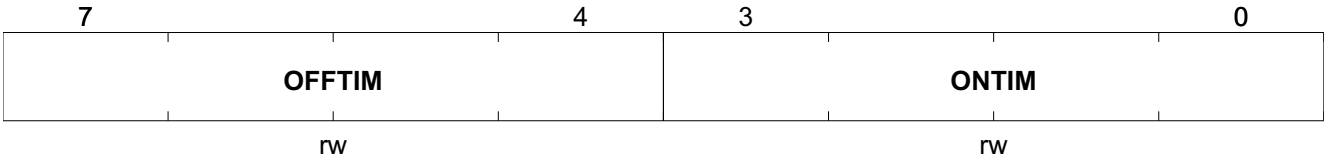


Field	Bits	Type	Description
LFDCEn	7	rcw	**LF Division Calibration Enable** *Note: Under control of Library functions*
Res	6:3		**Reserved**
LFD10_8	2:0	rw	**LF bit rate generator division factor bit 10 down to bit 8**

Note: These SFRs can be modified manually as well for using other (uncalibrated) bit rates.

LF On/Off Timer Configuration Register

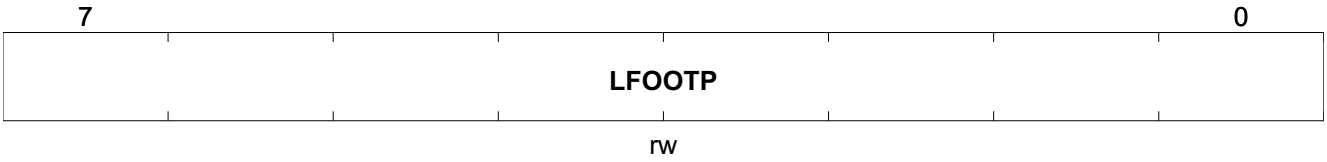
LFOOT	Offset	Wakeup Value	Reset Value
LF On/Off Timer Configuration Register	**$C6_H$**	**$UUUUUUUU_B$**	**00_H**



Field	Bits	Type	Description
OFFTIM	7:4	rw	**Off time (MSB-LSB)** Binary weighted Off time. Example: If time base is set to 50ms in LFOOTP the following value range is available (please refer to **Figure 26 “Calculation of Off time for LF Receiver On/Off Timer” on Page 89**): 0000_B 200ms **...** 1111_B 3.2s
ONTIM	3:0	rw	**On time (MSB-LSB)** Binary weighted On time. Example: If time base is set to 50ms in LFOOTP the following value range is available (please refer to **Figure 25 “Calculation of On time for LF Receiver On/Off Timer” on Page 89**): 0000_B 12.5ms **...** 1111_B 200ms

LF On/Off Timer Precounter

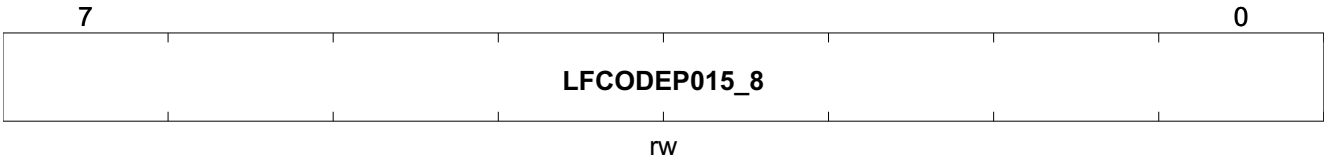
LFOOTP	Offset	Wakeup Value	Reset Value
LF On/Off Timer Precounter	$C5_H$	$UUUUUUUU_B$	64_H



Field	Bits	Type	Description
LFOOTP	7:0	rw	**LF Receiver On/Off Timer Precounter setting**

LF Pattern 0 Detector Sequence Data MSB

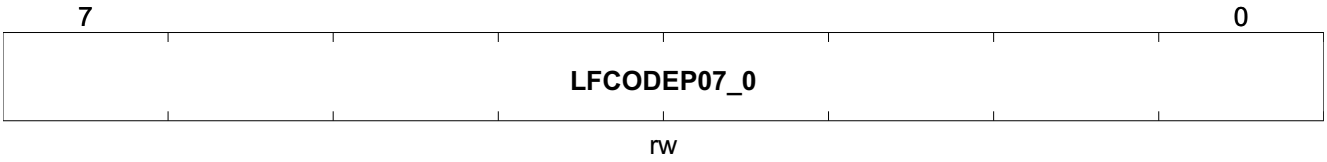
LFP0H	Offset	Wakeup Value	Reset Value
LF Pattern 0 Detector Sequence Data MSB	BF_H	$UUUUUUUU_B$	FF_H



Field	Bits	Type	Description
LFCODEP015_8	7:0	rw	**Code pattern 0 sequence bit 15 down to bit 8**

LF Pattern 0 Detector Sequence Data LSB

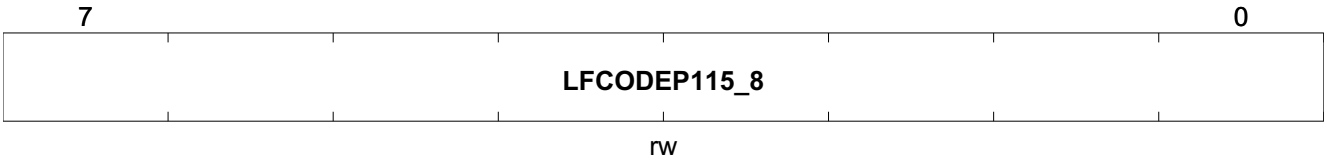
LFP0L	Offset	Wakeup Value	Reset Value
LF Pattern 0 Detector Sequence Data LSB	BE_H	$UUUUUUUU_B$	FF_H



Field	Bits	Type	Description
LFCODEP07_0	7:0	rw	**Code pattern 0 sequence bit 7 down to bit 0**

LF Pattern 1 Detector Sequence Data MSB

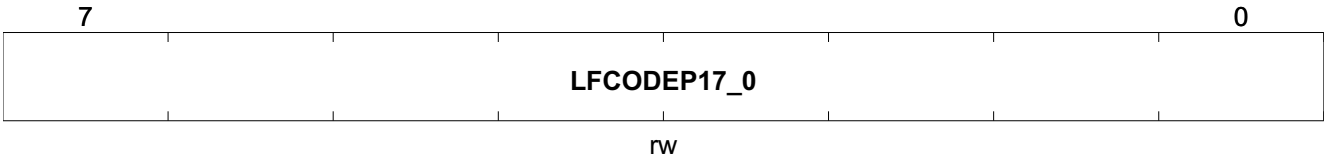
LFP1H	Offset	Wakeup Value	Reset Value
LF Pattern 1 Detector Sequence Data MSB	CF_H	$UUUUUUUU_B$	FF_H



Field	Bits	Type	Description
LFCODEP115_8	7:0	rw	**Code pattern 1 sequence bit 15 down to bit 8**

LF Pattern 1 Detector Sequence Data LSB

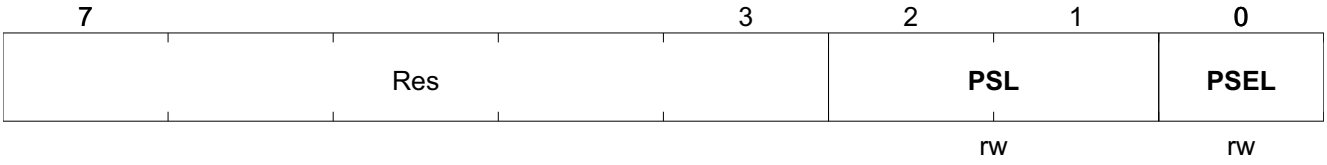
LFP1L	Offset	Wakeup Value	Reset Value
LF Pattern 1 Detector Sequence Data LSB	CE_H	$UUUUUUUU_B$	FF_H



Field	Bits	Type	Description
LFCODEP17_0	7:0	rw	**Code pattern 1 sequence bit 7 down to bit 0**

LF Pattern Detection Configuration Register

LFPCFG	Offset	Wakeup Value	Reset Value
LF Pattern Detection Configuration Register	$C7_H$	$00000UUU_B$	00_H

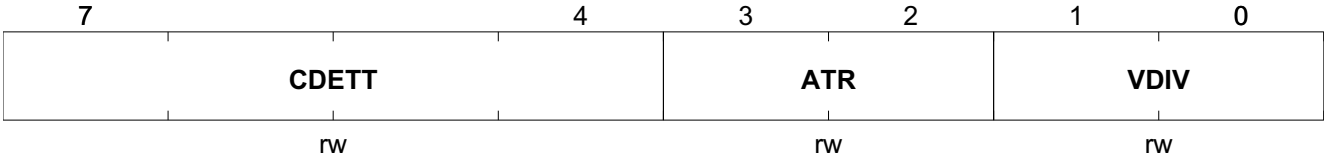


Field	Bits	Type	Description
Res	7:3		**Reserved**
PSL	2:1	rw	**Pattern sequence length (MSB-LSB)** 00_B 4 bit pattern length (LFP0L.[3:0] or LFP1L.[3:0] 01_B 8 bit pattern length (LFP0L.[7:0] or LFP1L.[7:0]) 10_B 16 bit pattern length (LFP1H.[15:8] / LFP1L.[7:0] or LFP0H.[15:8] / LFP0L.[7:0]) 11_B Reserved
PSEL	0	rw	**Pattern select** 0_B Only wake-up pattern 0 (LFP0L and LFP0H) can generate a pattern match wake-up. 1_B Both, wake-up pattern 0 (LFP0L and LFP0H) and wake-up pattern 1 (LFP1L and LFP1H) can generate a pattern match wake-up.

LF Receiver Configuration Register 0

The SFR LFRX0 determines the attenuation of the LF input signal (SFR bit LFRX0.0 [VDIV1-0]) and the threshold for the Carrier Detector (SFR bits LFRX0.7-4 [CDETT3-0]). Please refer to **Product Characteristics** for proper setting of these bits.

LFRX0	Offset	Wakeup Value	Reset Value
LF Receiver Configuration Register 0	**$B7_H$**	**$UUUUUUUU_B$**	**39_H**



Field	Bits	Type	Description
CDETT	7:4	rw	**Carrier Detector Threshold Level Selection** Use PMA Library function **LFSensitivityCalibration()** to automatically configure these bits. Please refer to **[1]**.
ATR	3:2	rw	**Attenuator Threshold Selection** *Note: Must be set to 10_B*
VDIV	1:0	rw	**Antenna Voltage Divider Factor Selection** 00_B Divided by 9 01_B Divided by 1 10_B Divided by 29 11_B Reserved

LF Receiver Configuration Register 1

LFRX1	Offset	Wakeup Value	Reset Value
LF Receiver Configuration Register 1	**$B6_H$**	**$UUUUU0UU_B$**	**31_H**

7	6	5	4	3	2	1	0
AGCTCD		**DSTFC**		**LFGAIN**	Res	**DF**	
rw		rw		rw		rw	

Field	Bits	Type	Description
AGCTCD	7:6	rw	**AGC Time Constant Decay Slew Rate Selection** *Note: Must be set to 00_B*
DSTFC	5:4	rw	**Data Slicer Threshold Filter Corner Frequency Selection** *Note: Must be set to 00_B*
LFGAIN	3	rw	**LF Receiver Front End Gain Select** *Note: Must be set to 1_B*
Res	2		**Reserved**
DF	1:0	rw	**Data Filter Corner Frequency Selection** 00_B Reserved 01_B Recommended for a data rate of 2000/3900/4000 bit/s 10_B Reserved 11_B Reserved

LF Receiver Control Register

LFRXC	Offset	Wakeup Value	Reset Value
LF Receiver Control Register	$F9_H$	$UUUUUUUU_B$	00_H

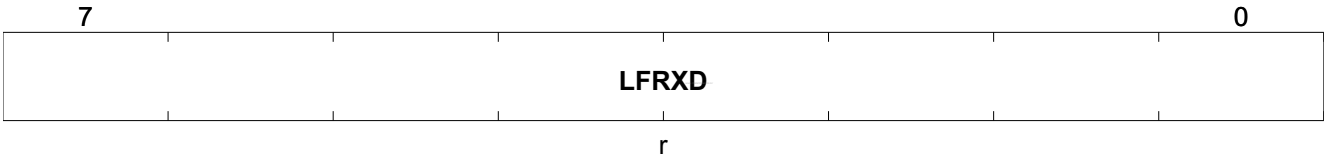
7	6	5	4	3	2	1	0
CDRECAL	DISAGC	LFBBM		ENOOTIM	ENLFRX	IRXD	CSEL
rw	rw	rw		rw	rw	rw	rw

Field	Bits	Type	Description
CDRECAL	7	rw	**Carrier Detector Threshold re-calibration** *Note: This bit must be set to 0_B*
DISAGC	6	rw	**Disable Automatic Gain Control (AGC)** 0_B AGC is enabled 1_B AGC is disabled
LFBBM	5:4	rw	**LF Baseband Processor Mode Selection** 00_B Disabled: The entire digital part of the receiver is disabled. The LF Analog Frontend including Carrier Detector is still active (if enabled by ENLFRX) 01_B Raw data recovery: The digital frontend and the synchronizer are active. Data is recovered at chip level and can be handled by the microcontroller. This mode can be used for the implementation of custom coding and synchronization schemes. 10_B Raw/decoded data recovery: The full LF baseband functionality including the decoding of Manchester/BiPhase coded data is available. 11_B Reserved
ENOOTIM	3	rw	**Enable On/Off Timer** 0_B LF Receiver is always on (if also enabled by ENLFRX) 1_B LF Receiver is controlled by On/Off Timer (if also enabled by ENLFRX)
ENLFRX	2	rw	**Enable LF Receiver** 0_B LF Receiver disabled 1_B LF Receiver enabled (Controlled by ENOOTIM)
IRXD	1	rw	**Invert LF Receiver data** 0_B Data not inverted 1_B Data inverted

Field	Bits	Type	Description
CSEL	0	rw	**Decoder Code Select** IRXD=0_B 0_B Manchester coded data 1_B BiPhase 0 coded data IRXD=1_B 0_B Inverted Manchester coded data 1_B BiPhase 1 coded data

LF Receiver Data Register

LFRXD	Offset	Wakeup Value	Reset Value
LF Receiver Data Register	**$A5_H$**	**00_H**	**00_H**



Field	Bits	Type	Description
LFRXD	7:0	r	**LF Receiver data register**

LF Receiver Status Register

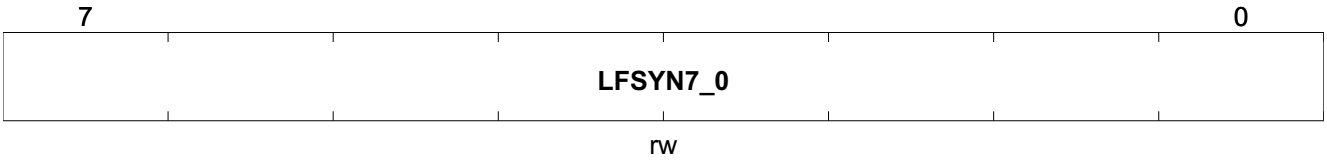
LFRXS	Offset	Wakeup Value	Reset Value
LF Receiver Status Register	$A4_H$	00_H	00_H

7	6	5	4	3	2	1	0
CDRAW	DECERR	LFRAW	LFDOV	LFDP	LFOV	LFBP	LFDATA
r	rc	r	rc	rc	rc	rc	r

Field	Bits	Type	Description
CDRAW	7	r	**LF Carrier detect raw data**
DECERR	6	rc	**Manchester/Biphase decode error** 0_B No error detected 1_B Decode error detected
LFRAW	5	r	**LF Receiver raw data**
LFDOV	4	rc	**LF data byte overwritten** 0_B No error detected 1_B LF data byte overwritten
LFDP	3	rc	**LF data byte pending** If this bit is set LF data can be read from LFRXD
LFOV	2	rc	**LF serial decoded data overwritten** 0_B No error detected 1_B LF serial decoded data overwritten
LFBP	1	rc	**LF serial decoded data pending** If this bit is set new LF serial decoded data is available at LFDATA since the last read access to LFRXS
LFDATA	0	r	**LF serial decoded data**

LF Sync Pattern 0

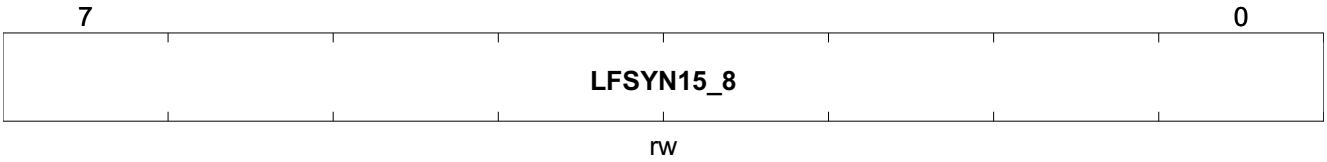
LFSYN0	Offset	Wakeup Value	Reset Value
LF Sync Pattern 0	$A6_H$	$UUUUUUUU_B$	FF_H



Field	Bits	Type	Description
LFSYN7_0	7:0	rw	**LF Sync Pattern Chip 7 - Chip 0**

LF Sync Pattern 1

LFSYN1	Offset	Wakeup Value	Reset Value
LF Sync Pattern 1	$A7_H$	$UUUUUUUU_B$	FF_H



Field	Bits	Type	Description
LFSYN15_8	7:0	rw	**LF Sync Pattern Chip 15 - Chip 8**

LF SYNC Matching Configuration Register

LFSYNCFG	Offset	Wakeup Value	Reset Value
LF SYNC Matching Configuration Register	AF_H	$X0UUUUUU_B$	38_H

7	6	5	4	3	2	1	0
LFCDA	Res	**LFSYN17**	**LFSYN16**	**SPSL**		**SYNM**	
r		rw	rw	rw		rw	

Field	Bits	Type	Description
LFCDA	7	r	**LF Receiver On/Off indicator** 0_B LF Receiver is currently off 1_B LF Receiver is currently on
Res	6		**Reserved**
LFSYN17	5	rw	**Sync pattern sequence chip 17**
LFSYN16	4	rw	**Sync pattern sequence chip 16**
SPSL	3:2	rw	**Sync pattern sequence length (MSB-LSB)** 00_B 4 chips sync pattern length (LFSYN0.[3:0]) 01_B 8 chips sync pattern length (LFSYN0.[7:0]) 10_B 16 chips sync pattern length (LFSYN1.[7:0] and LFSYN0.[7:0]) 11_B 18 chips sync pattern length (LFSYNCFG.[5:4], LFSYN1.[7:0] and LFSYN0.[7:0])
SYNM	1:0	rw	**LF synchronizer mode** Detailed information can be found in **Chapter 2.10.3.1**. 00_B Synchronization with 0/1 or 1/0 transition (Manchester) or 2 consecutive chips with same level (BiPhase). Set wake-up mask SFR WUM for Carrier Detect wake-up. 01_B Synchronization with sync pattern. Set wake-up mask SFR WUM for sync match wake-up. 10_B Synchronization with 0/1 or 1/0 transition (Manchester) or 2 consecutive chips with same level (BiPhase) and a subsequent wake-up pattern. Set wake-up mask SFR WUM for pattern match wake-up. 11_B Synchronization with sync pattern and wake-up pattern. Set wake-up mask SFR WUM for sync match and/or pattern match wake-up.

2.11 Sensor Interfaces and Data Acquisition

The PMA5110 has two internal sensors to acquire environmental data, two highly sensitive differential analog interfaces with 4 programmable gain factors (from 76 +-20 %, 60 +-20 %, 50 +-20 % and 38 +-20 %), and one standard differential analog interface (gain factor 1):

- Temperature sensor
- Battery voltage monitoring
- External data through analog interface

The analog data is acquired and digitalized by the internal 10-bit ADC. Measurement routines for acquiring temperature and battery voltage data are available within the Function Library that is described in [1].

2.11.1 Sensor Interface

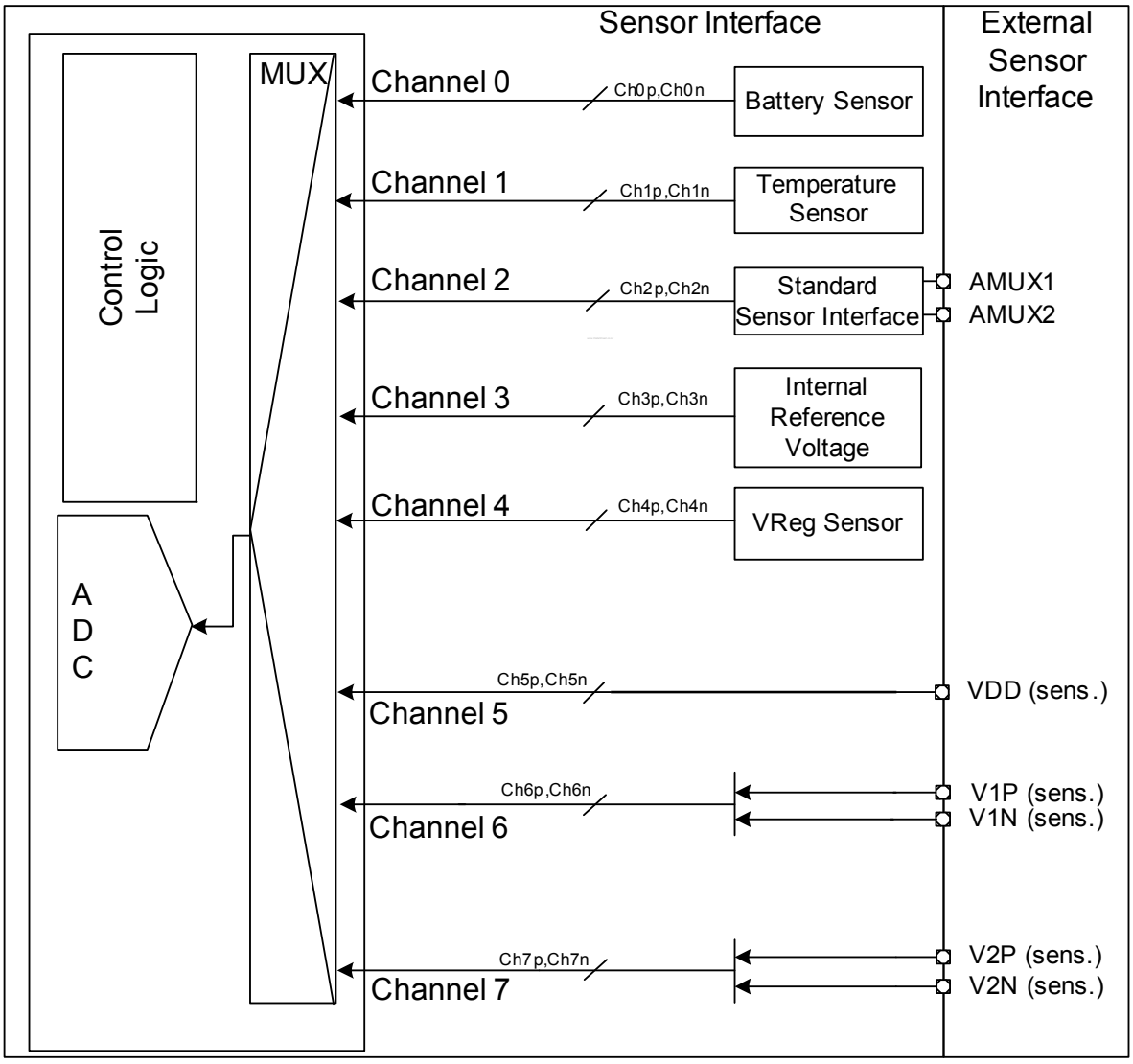


Figure 31 Block Diagram of the Sensor Interface

The sensor interface connects to the external sensors and to the internal (on-chip) temperature and battery-voltage sensors.

All signal channels can be configured for differential or single-ended operation. Differential operation is only recommended for signals in which the common-mode voltage is stable, while the positive and negative signal voltages vary symmetrically around the common-mode voltage.

The input multiplexer selects one channel for the input signal and one channel for the reference voltage to the ADC. Any channel can be selected as the reference except channels 6 and 7, which are specially adapted to the low-level signals from external sensors.

2.11.1.1 Two Differential Highly Sensitive Interfaces to External Sensors

Differential highly sensitive sensor interface 1 (Channel 6)

V1P/V1N are the positive/negative differential voltage inputs.

Differential highly sensitive sensor interface 2 (Channel 7)

V2P/V2N are the positive/negative differential voltage inputs.

Channel gain selection

The SFR bit ADCC1.5-4 [GAIN1-0] gain factor selection allows the selection of the sensitivity of the analog input channels 6 and 7. The gain factor is one for all other input channels (see **Table 18 “Selection of the Gain Factor” on Page 109**).

Table 18 Selection of the Gain Factor

Gain factor (gain)	Channel ADCM.CS2-0	GAIN1	GAIN0
76 +/- 20%	11X	0	0
60 +/- 20%	11X	0	1
50 +/- 20%	11X	1	0
38 +/- 20%	11X	1	1
1	Others	0	0
1	Others	0	1
1	Others	1	0
1	Others	1	1

Sensor Excitation

Sensors connected to channel 6 or 7 can have their supply voltages provided by the PMA5110. For channel 6, connect the supply terminals of the sensor between VDD(sens) and VM1 (pin 3). For channel 7, use VDD(sens) and VM2. The supply is switched on only when a measurement of the corresponding channel is done. A settling time delay between sensor power-on and measurement can be programmed, refer to **Chapter 2.11.4.1.2**.

Wheatstone Bridge Sensor Connection

Wheatstone bridges can be used to set the operating point of external sensors, if needed. **Figure 32 “Wheatstone Bridge Sensor Connection” on Page 110** shows the connection of two wheatstone bridges to the differential high sensitivity sensor interfaces 1 and 2 (channel 6 and channel 7).

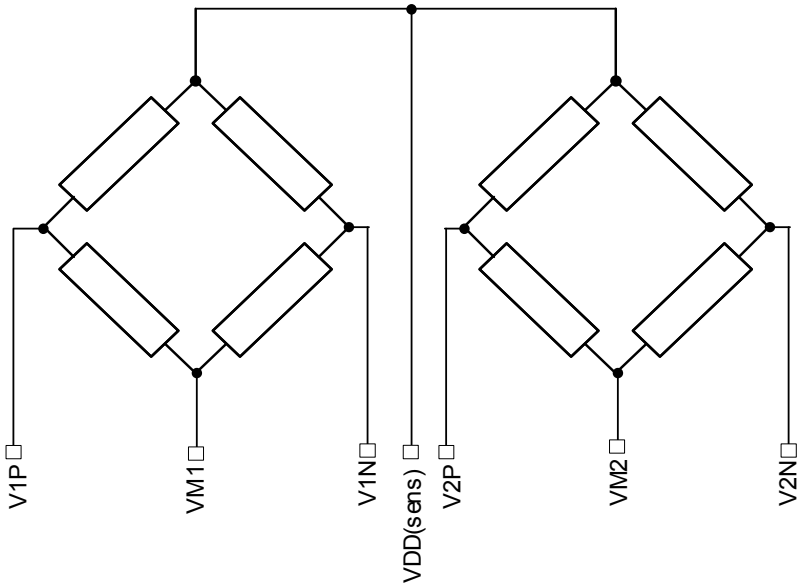


Figure 32 Wheatstone Bridge Sensor Connection

2.11.1.2 Interface to Other Signals

Battery-voltage Interface (Channel 0)

The positive input to the battery-voltage signal is derived by dividing voltage V_{Bat} by 3.5. The negative input is connected to GND. The battery voltage is converted with a resolution of approximately 4.1 mV, using an internal reference voltage of 1210 mV (channel 3) as a reference.

Temperature-sensor Interface (Channel 1)

The temperature signal to the ADC is a single-ended signal, with a temperature-sensitive voltage between 500 and 1100 mV. The temperature-sensor signal is digitized with a resolution of approximately 0.5°C, using an internal reference voltage of 1210 mV (channel 3) as a reference.

Standard-sensor Interface (Channel 2)

The positive input signal must be applied at AMUX1, and the negative input at AMUX2.

2.11.1.3 Reference Voltages

When channel 6 or 7 is selected as input to the ADC, the reference voltage should be identical to the supply voltage of the sensor bridge, in order to get correct ratiometric operation. If the sensor bridge is connected between the VDD(sens) and VM1 (or VM2) pins of the PMA5110, channel 5 will provide the correct reference voltage.

If the sensor is supplied by external power, the positive and negative supply voltages of the sensor bridge should be connected to channel 2, and this channel should be used as a reference (see **Figure 33**). The supply voltage of the sensor must always be within the range GND to V_{REG}.

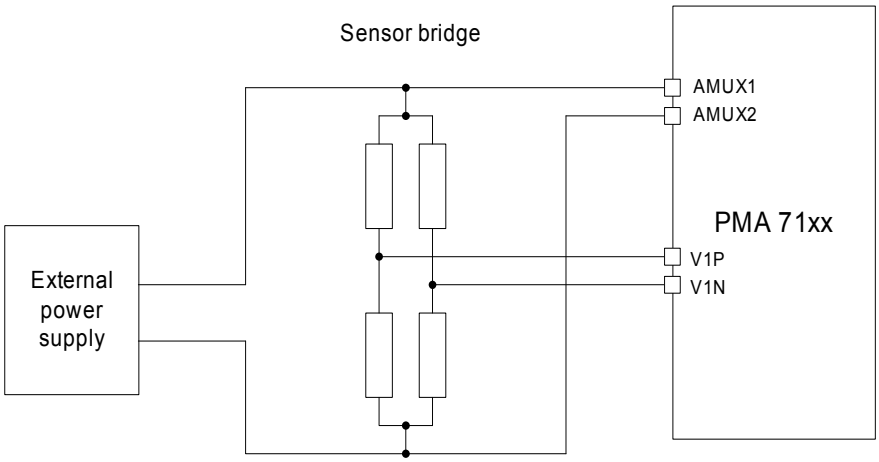


Figure 33 External Sensor Use Channel 2 as Reference Voltage

3 channels on the ADC input multiplexer carry voltages that are intended as reference voltages for the converter:

Internal Reference Voltage (Channel 3)

This reference is a nominal voltage of 1210 mV. It is intended as a reference for the temperature and V_{Bat} measurements.

VREG Reference (Channel 4)

This reference is the V_{REG} voltage. This is the highest allowable input voltage to the ADC, and is meant as a reference for the test signal, to allow as large a test signal as possible.

BRIDGE SUPPLY Reference (Channel 5)

When channel 6 or 7 is selected as the input to the ADC, the reference voltage is the bridge supply voltage. A multiplexer selects the appropriate negative bridge supply. This reference must be used with the ratiometric sensors in order to achieve an accuracy that is independent of the battery voltage.

2.11.2 Temperature Sensor

Temperature measurement is performed by a dedicated Library function.

See **Temperature Sensor Characteristics** for the sensor specification.

2.11.3 Battery Voltage Monitor

Battery voltage measurement is performed by a dedicated Library function.

See **Battery Sensor Characteristics** for the sensor specification.

2.11.4 Analog to Digital Converter (ADC)

The ADC is a fully differential charge-balancing 10-bit converter. It uses a technique known as redundant successive approximation, which requires 12 decisions to arrive at a 10-bit result. The redundancy means that the ranges of the successive approximation partially overlap, making the conversion more robust to noise.

The ADC can perform sub conversions with any number of bits. This means that the charge redistribution is done with the result of the previous conversion as a starting point, and doing the comparator decisions only for the selected number of less significant bit positions.

A digitally controlled attenuator allows the gain setting of the highly sensitive ADC inputs. At ADC inputs, inverters are used to perform two identical conversions with inverted comparator input signals to compensate comparator offset digitally. They are controlled by the SFR bit ADCC1.6 [CSI] (see **ADC Configuration Register 1**). If the average of the 2 measurements is taken, the offset of the comparator is canceled.

2.11.4.1 ADC Timing

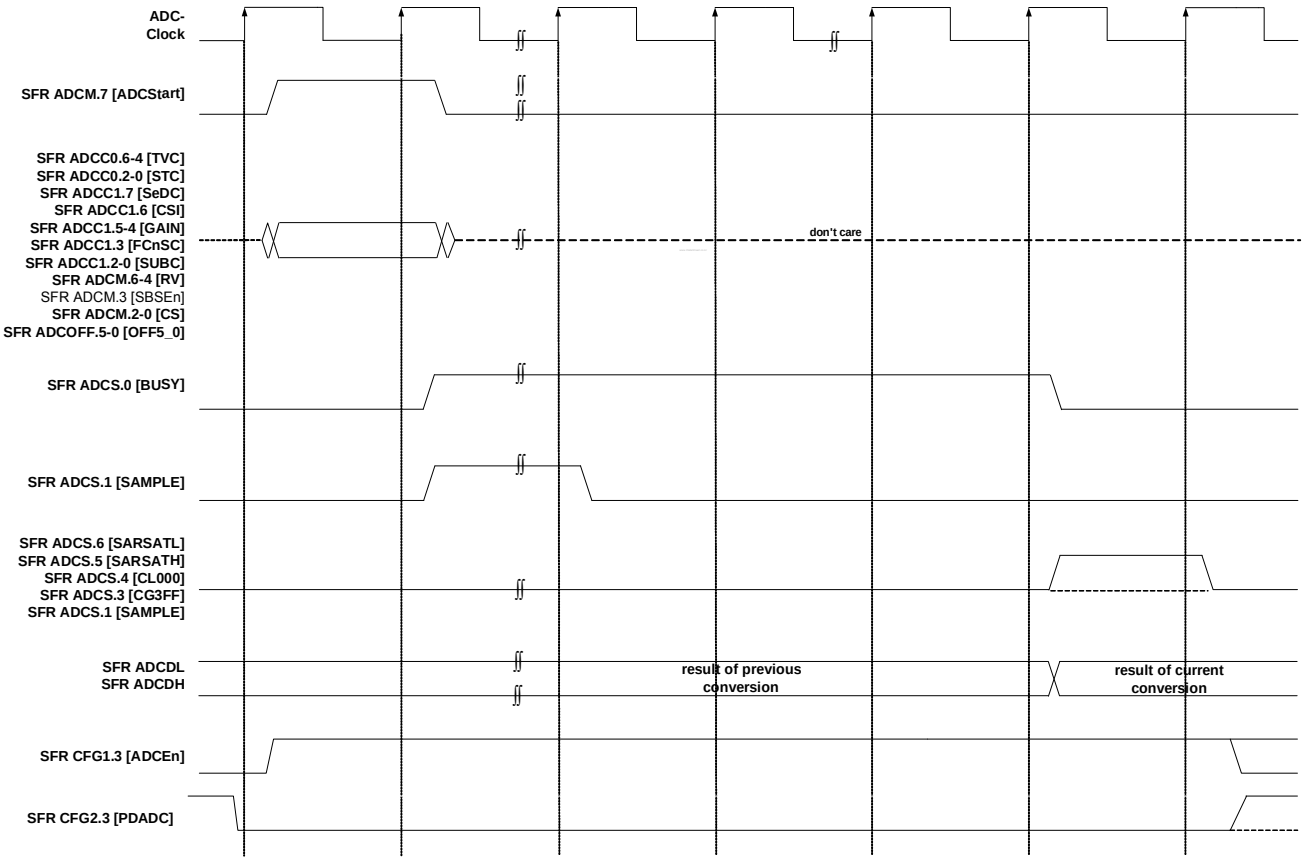


Figure 34 ADC Timing diagram (standard conversion)

ADC power (VADC) must be turned on (using CFG2.3 [PDADC]) before the ADC is enabled (using CFG1.3 [ADCEn]). AD conversions can then be started by setting ADCM.7 [ADCStart] to 1_B. ADCM.3 [SBSEn] can be used to enable the Wheatstone Bridge supply if needed. The timing diagram of a conversion is shown above. ADC-Start and all other control signals are latched with the following rising edge of the ADC-Clock. This generates the status bits ADCS.0 [BUSY] as well as ADCS.1 [SAMPLE] which indicates the sample and hold activity of the channel input signals. The result registers ADCDH and ADCDL are written at the same time. With the next rising edge of the ADC-Clock the result bits are stable. ADC power (VADC) can then be turned off again

by setting CFG2.3 [PDADC]. Only the analog part of the ADC is powered off, thus the result register will not be affected thereby.

2.11.4.1.1 Clock Divider

An ADC clock divider allows the adaption of the ADC speed to the CPU8051 and peripheral units clock f_{CPU}. The clock divider factor settings are selected by ADCC0.6-4 [TVC]. The ADC clock frequency is calculated with equation shown in **Figure 35**.

$$f_{ADC}[Hz] = \frac{f_{CPU}[Hz]}{TVC}$$

TVC .. ADCC0.6-4 [TVC]

Figure 35 ADC frequency calculation

2.11.4.1.2 Sample Time Delay

The sample time delay (Sample time adjustment factor STC) of the analog input channel is selected by the bits ADCC0.2-0 [STC2-0]. The sample time t_{sample} of the analog input channels can be calculated using the formula shown in **Figure 36 “ADC sample time delay” on Page 113**.

$$t_{sample}[s] = \frac{1}{f_{CPU}[Hz]} \cdot TVC \cdot STC$$

TVC .. ADCC0.6-4 [TVC]
STC .. ADCC0.2-0 [STC]

Figure 36 ADC sample time delay

The scheme of sample time generation is drawn in **Figure 37 “Generation of ADC clock and the sample time signal” on Page 113**.

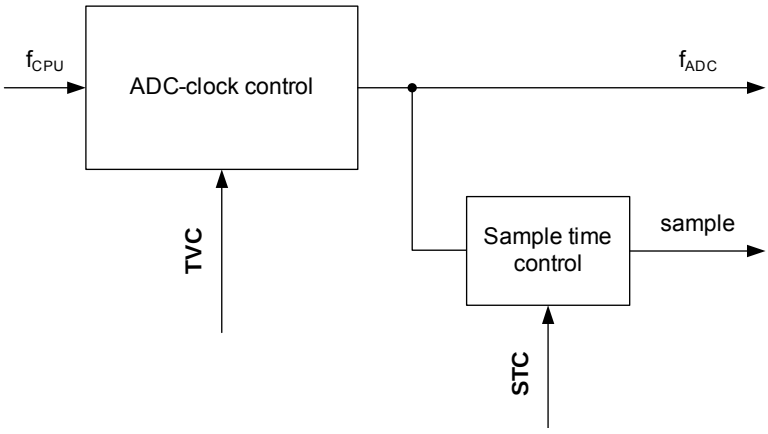


Figure 37 Generation of ADC clock and the sample time signal

2.11.4.1.3 Conversion Time

The ADC conversion time has three contributors. First, the sample time where the input signal voltage level is stored in the sampling capacitors. Second, the successive approximation to determine the output code. A full conversion needs 12 ADC clock cycles to produce a 10 bit conversion result. Third, 2 CPU clock cycles f_{CPU} to synchronize all input and output signals to the interface. The conversion time is calculated with the formula shown in **Figure 38 “Calculation of the ADC conversion time using full conversion” on Page 114**.

$$t_{conv}[s] = \frac{1}{f_{CPU}[Hz]} \cdot (TVC \cdot (STC + 12) + 2)$$

TVC .. ADCC0.6-4 [TVC]
STC .. ADCC0.2-0 [STC]

Figure 38 Calculation of the ADC conversion time using full conversion

Sub conversions with reduced length need less ADC clock cycles. The conversion time for sub conversions is calculated with the formula shown in **Figure 39 "Calculation of the ADC conversion time using sub conversion" on Page 114**.

$$t_{conv}[s] = \frac{1}{f_{CPU}[Hz]} \cdot (TVC \cdot (STC + SUBC) + 2)$$

TVC .. ADCC0.6-4 [TVC]
STC .. ADCC0.2-0 [STC]
SUBC .. ADCC1.2-0 [SUBC]

Figure 39 Calculation of the ADC conversion time using sub conversion

2.11.4.2 ADC Configuration

2.11.4.2.1 Reference- and Signal Voltage Selection

The input multiplexer of the ADC is used for selection of both reference voltage (see SFR bit ADCM.6-4 [RV2-0]) and signal voltage (see SFR bit ADCM.2-0 [CS2-0]).

2.11.4.2.2 Single ended / Differential Conversion

In order to obtain the highest accuracy, single-ended conversion must be used for channels 0 - 2. In single-ended conversion, only the positive input of the selected channel is used, the negative input is connected to GND internally. The high sensitivity inputs (channel 6 and 7) must be used in the differential mode.

2.11.4.2.3 Comparator Signal Inversion

The ADCC1.6 [CSI] inverts the polarity of the comparator with respect to the signal. By averaging two conversions with opposite polarity, the comparator offset is eliminated.

2.11.4.2.4 Channel Gain Selection

The ADCC1.5-4 [GAIN1-0] gain factor selection allows the selection of the sensitivity of the analog input channels 6 and 7. The gain is one for all other input channels

2.11.4.2.5 Full Conversion or Sub Conversion

The ADCC1.3 [FCnSC] allows the selection of a conversion of all bits of the code range (10 bits, full conversion) or of a reduced number of bits (sub conversion). The number of bits is chosen by the bits ADCC1.2-0 [SUBC]. All higher bits are taken from the result of the previous conversion. The ADC state machine automatically subtracts half of the sub conversion range from the result of the previous conversion. Therefore the signal values can vary between the value of the previous conversion minus half of the weight of the sub conversion range to the value of the previous conversion plus half of the weight of the sub conversion range.

2.11.4.2.6 Analog Offset Correction of the Wheatstone Bridge Signals

In order to use the full ADC input range to convert the sensor signals, it is desirable to perform a correction of the output voltage from the connected wheatstone bridge. The correction can be viewed as a constant voltage which is added to the wheatstone bridge output. The implementation takes advantage of the differential charge

redistribution structure of the ADC, by adding additional capacitor arrays for the offset correction. The analog offset correction performs two functions

1. Cancel the major part of the sensor's offset voltage.
2. Position the sensor signal so that it utilizes the full input range of the ADC.

It is also possible to operate the ADC with zero offset correction.

The bits ADCOFF.5-0 [OFF5-0] allow the selection of an analog offset correction to the analog input voltage. The offset is a function of the reference voltage, the bits ADCOFF.5-0 [OFF5-0] parameter and a fixed gain factor of 1/50. The number format is 2's complement.

The offset value can be calculated with the formula shown in **Figure 40 "ADC offset voltage calculation" on Page 115**.

$$U_{offset} = \frac{U_{ref}}{32} \cdot \frac{goff}{50} \cdot \left(\sum_{i=0}^{4} 2^i \cdot OFF(i) - (2^5 \cdot OFF(5)) \right)$$

OFF .. ADCOFF.5-0

Figure 40 ADC offset voltage calculation

The offset gain factor (goff) is determined by the selection of input channel (ADCM.2-0[CS]) and input gain (ADCC1.5-4[GAIN]) as described in **Table 18 "Selection of the Gain Factor" on Page 109**. The reference voltage U_{ref} is the input voltage of the selected reference voltage source (ADCM.6-4[RV2-0]).

2.11.4.3 ADC Conversion Result

The ADC conversion result ($result_{code}$) data format is binary unsigned and stored in ADCH and ADCL.

The type of single ended/differential conversion is selected with bit ADCC1.7[SeDC]. The result of a single ended/differential conversion can be calculated with the formulas shown in **Figure 41 "Calculation of single ended conversion" on Page 115** and **Figure 42 "Calculation of differential conversion" on Page 115**. The truncation function takes the integer value of the calculation. The gain factor is obtained from **Table 18 "Selection of the Gain Factor" on Page 109**. $U_{Channel}$ is the voltage at the selected input channel. For U_{offset} voltage calculation see **Figure 40 "ADC offset voltage calculation" on Page 115**.

$$result_{code} = trunc\left(2^{10} \cdot gain \cdot \frac{U_{channel} + U_{offset}}{U_{ref}} \right)$$

Figure 41 Calculation of single ended conversion

$$result_{code} = 2^9 + trunc\left(2^9 \cdot gain \cdot \frac{U_{channel} + U_{offset}}{U_{ref}} \right)$$

Figure 42 Calculation of differential conversion

Output Status Bits

The ADC provides separate status bits for underflow and overflow after the conversion. The output value remains at the maximum value in case of an overflow, and at the minimum value in case of an underflow. All status bits are defined in ADCS and are active high.

2.11.5 Register Description

Table 19 Registers Overview

Register Short Name	Register Long Name	Offset Address	Wakeup Value	Page Number
ADCM	ADC Mode Register	$D2_H$	77_H	120
ADCS	ADC Status Register	$D3_H$	00_H	122
ADCDL	ADC Result Register low byte	$D4_H$	00_H	119
ADCDH	ADC Result Register high byte	$D5_H$	00_H	119
ADCOFF	ADC Input Offset c-network configuration	DA_H	00_H	121
ADCC0	ADC Configuration Register 0	DB_H	00_H	116
ADCC1	ADC Configuration Register 1	DC_H	00_H	118

ADC Configuration Register 0

ADCC0	Offset	Wakeup Value	Reset Value
ADC Configuration Register 0	DB_H	00_H	00_H

7	6	4	3	2	0
Res	TVC		Res	STC	
	rw			rw	

Field	Bits	Type	Description
Res	7		**Reserved**
TVC	6:4	rw	**Internal Clock Divider** 000_B Divider factor 8 001_B Divider factor 10 010_B Divider factor 12 011_B Divider factor 14 100_B Divider factor 16 101_B Divider factor 18 110_B Divider factor 20 111_B Divider factor 1
Res	3		**Reserved**

Field	Bits	Type	Description
STC	2:0	rw	**Sample Time Adjustment** 000_B 2 periods of ADC clock 001_B 4 periods of ADC clock 010_B 5 periods of ADC clock 011_B 6 periods of ADC clock 100_B 7 periods of ADC clock 101_B 8 periods of ADC clock 110_B 12 periods of ADC clock 111_B 16 periods of ADC clock

ADC Configuration Register 1

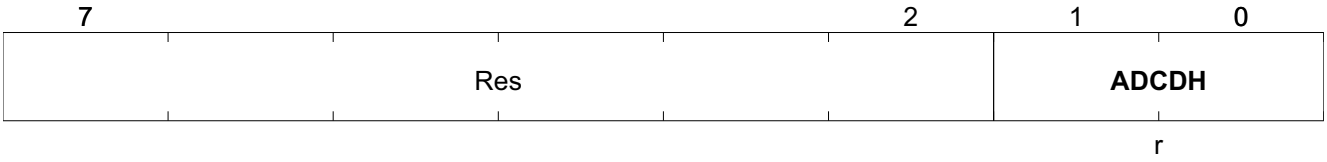
ADCC1	Offset	Wakeup Value	Reset Value
ADC Configuration Register 1	DC_H	00_H	00_H

7	6	5	4	3	2	0
SeDC	CSI	GAIN		FCnSC	SUBC	
rw	rw	rw		rw	rw	

Field	Bits	Type	Description
SeDC	7	rw	**Single ended or differential conversion** 0_B Single ended conversion 1_B Differential conversion
CSI	6	rw	**Comparator signal inversion** 0_B Signal inversion off 1_B Signal inversion on
GAIN	5:4	rw	**Gain setting of channel 7-6 (see Table 18)** All other channels have gain one. 00_B Gain factor 76 +/-20% 01_B Gain factor 60 +/-20% 10_B Gain factor 50 +/-20% 11_B Gain factor 38 +/-20%
FCnSC	3	rw	**Full conversion or sub conversion** 0_B Sub conversion (reduced number of bits converted (see SUBC)) 1_B Full conversion (all bits are determined)
SUBC	2:0	rw	**Sub conversion** Number of converted bits. The result of the previous conversion acts as offset for the current conversion. 000_B 2 bits converted 001_B 3 bits converted 010_B 4 bits converted 011_B 5 bits converted 100_B 6 bits converted 101_B 7 bits converted 110_B 8 bits converted 111_B 9 bits converted

ADC Result Register High Byte

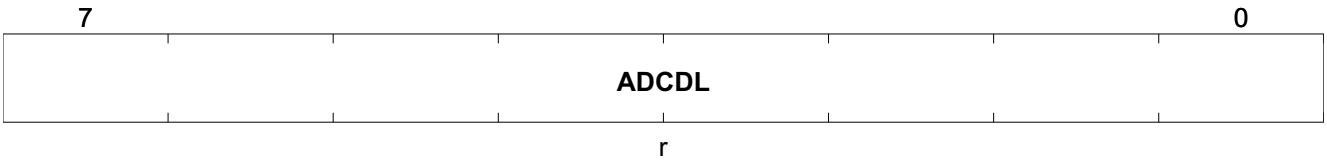
ADCDH	Offset	Wakeup Value	Reset Value
ADC Result Register high byte	$D5_H$	00_H	00_H



Field	Bits	Type	Description
Res	7:2		**Reserved**
ADCDH	1:0	r	**ADC conversion data bit 9 - bit 8**

ADC Result Register Low Byte

ADCDL	Offset	Wakeup Value	Reset Value
ADC Result Register low byte	$D4_H$	00_H	00_H



Field	Bits	Type	Description
ADCDL	7:0	r	**ADC conversion data bit 7 - bit 0**

ADC Mode Register

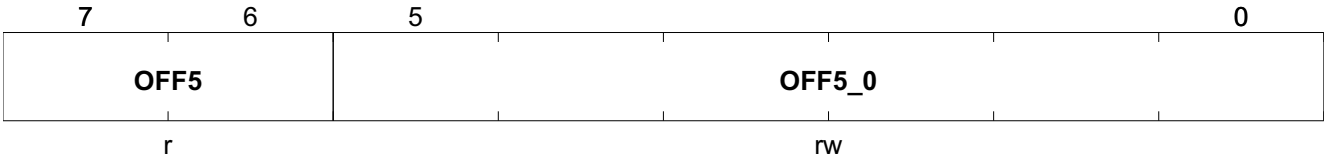
ADCM	Offset	Wakeup Value	Reset Value
ADC Mode Register	$D2_H$	77_H	77_H

7	6	4	3	2	0
ADCStart	RV		SBSEn	CS	
rcw	rw		rcw	rw	

Field	Bits	Type	Description
ADCStart	7	rcw	**ADC conversion start** 0_B Idle 1_B ADC starts conversion. Bit is cleared automatically
RV	6:4	rw	**Reference voltage selection** 000_B Battery sensor signal (channel 0) 001_B Temperature sensor signal (channel 1) 010_B Standard differential analog interface AMUX1, AMUX2 (channel 2) 011_B Internal reference voltage (channel 3) 100_B V_{reg} Sensor signal (channel 4) 101_B Wheatstone bridge supply - $VDD_{sens\ (channel\ 5)}$ 110_B Reserved 111_B Reserved
SBSEn	3	rcw	**Sensor bridge supply enable** 0_B Sensor bridge supply disabled 1_B Sensor bridge supply enabled. Bit is cleared automatically
CS	2:0	rw	**Analog channel selection** 000_B Battery sensor signal (channel 0) 001_B Temperature sensor signal (channel 1) 010_B Standard differential analog interface AMUX1, AMUX2 (channel 2) 011_B Internal reference voltage (channel 3) 100_B V_{reg} Sensor signal (channel 4) 101_B Wheatstone bridge supply - VDD_{sens} (channel 5) 110_B Differential high sensitivity input 1 (channel 6) 111_B Differential high sensitivity input 2 (channel 7)

ADC Input Offset c-Network Configuration

ADCOFF	Offset	Wakeup Value	Reset Value
ADC Input Offset c-network configuration	DA_H	00_H	00_H



Field	Bits	Type	Description
OFF5	7:6	r	**ADC Input offset compensation copy of bit 5** These two bits are set automatically by hardware and always have the same value as OFF.5. This is needed for correct representation of 2's complement for all 8 bits of this register.
OFF5_0	5:0	rw	**ADC Input offset compensation network selection** The offset voltage can be calculated with the offset value (OFF) using formula **Figure 40 "ADC offset voltage calculation" on Page 115**. The number format of the offset value (OFF) is 2's complement. 000000_B 00_H 000001_B 01_H 000010_B 02_H **...** 011110_B $1E_H$ 011111_B $1F_H$ 100000_B -20_H 100001_B $-1F_H$ 100010_B $-1E_H$ **...** 111110_B -02_H 111110_B -01_H

ADC Status Register

ADCS	Offset	Wakeup Value	Reset Value
ADC Status Register	$D3_H$	00_H	00_H

7	6	5	4	3	2	1	0
Res	**SARSATL**	**SARSATH**	**CL000**	**CG3FF**	Res	**SAMPLE**	**BUSY**
	r	r	r	r		r	r

Field	Bits	Type	Description
Res	7		**Reserved**
SARSATL	6	r	**Negative saturation of SAR**
SARSATH	5	r	**Positive saturation of SAR**
CL000	4	r	**Saturation of c-net control word** 000_H saturation of c-net control word
CG3FF	3	r	**Saturation of c-net control word** $3FF_H$ saturation of c-net control word
Res	2		**Reserved**
SAMPLE	1	r	**Sample/Hold** 0_B hold 1_B sample
BUSY	0	r	**Busy** 0_B Conversion finished 1_B Conversion running

2.12 16 bit CRC (Cyclic Redundancy Check) Generator/Checker

CRC is a powerful method to detect errors in data packets that have been transmitted over a distorted connection. The CRC Generator/Checker divides each byte of a transmitted/received data packet by a polynomial, leaving the remainder, which represents the checksum. The CRC Generator/Checker uses the 16-bit CCITT polynomial 1021_H ($x^{16}+x^{12}+x^5+1$). The 16-bit start value is determined by SFR CRC0 and SFR CRC1.

The CRC Generator/Checker can process 8-bit parallel and/or serial data. **Figure 43** gives an overview over the CRC Generator/Checker. A CRC generation and CRC checking example can be found in **Figure 44**.

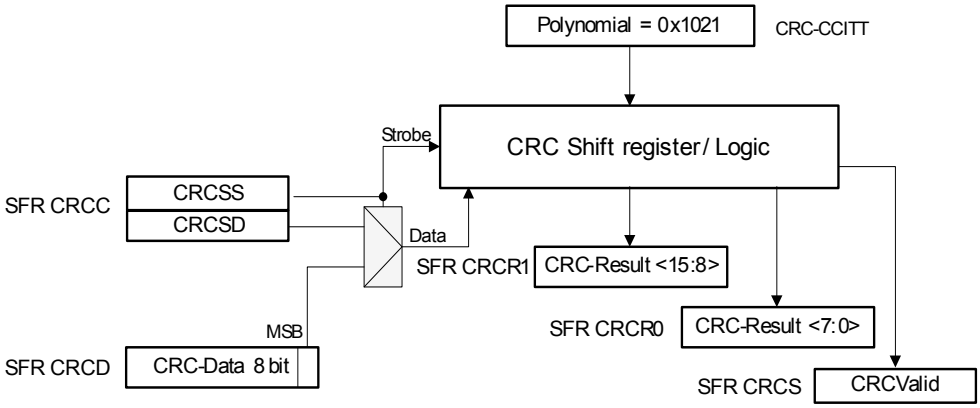


Figure 43 CRC (Cyclic Redundancy Check) Generator/Checker

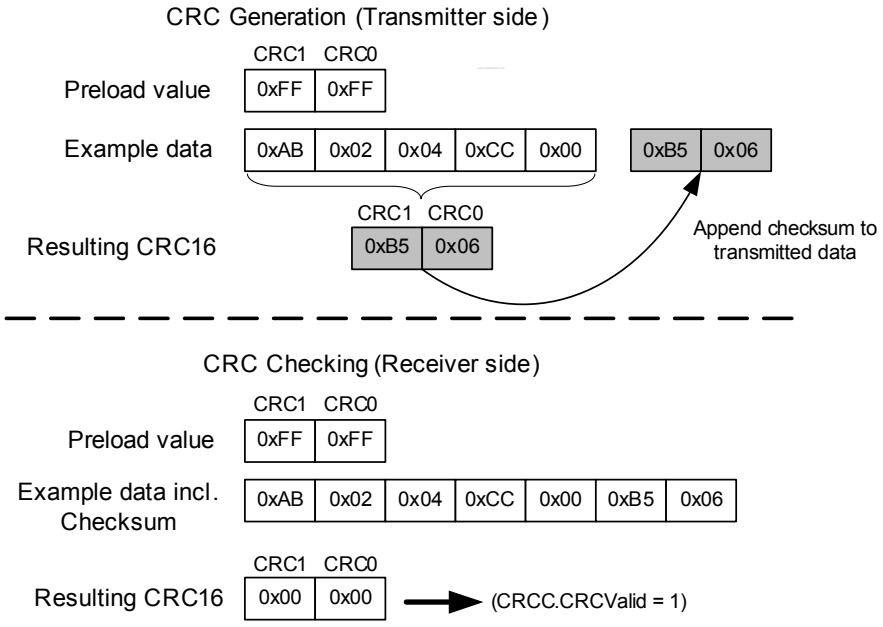


Figure 44 CRC (Cyclic Redundancy Check) Generator/Checker example

2.12.1 Byte-aligned CRC Generation

CRC generation is done by executing the following steps:

- The CRC shift register has to be initialized by writing a start value to both SFR CRC0 and SFR CRC1. If the CRC shift register is not initialized, the default value is 00_H.
- The data bytes which are used for the CRC generation have to be shifted one after the other into the SFR CRCD. The process of CRC generation is automatically invoked when data bytes are written to the SFR CRCD.

- The resulting checksum is available in the CRC result register SFR CRC0 and SFR CRC1 after the last data byte has been processed.

2.12.2 Byte-aligned CRC Checking

CRC checking is done by executing the following steps:

- The CRC shift register has to be initialized by writing the initialization value of the CRC generation process to both SFR CRC0 and SFR CRC1.
- The data bytes which should be checked have to be shifted one after the other into the SFR CRCD. It is important that the order (MSB-LSB) is the same as it was during CRC generation. The process of CRC checking is automatically invoked when data bytes are written to the SFR CRCD.
- The 16-bit CRC value is written to the SFR CRCD beginning with the high byte after processing all user data.
- The SFR Bit CRCC.1[CRCValid] indicates the correctness of the CRC calculation after the last data byte has been processed and both SFR CRC0 and SFR CRC1 are 0.

2.12.3 Serial bit stream CRC Generation/Checking

The CRC Generator/Checker features an additional serial mechanism to perform CRC generation and checking of non-byte-aligned data streams. In this case SFR Bit CRCC.5[CRCSS] and SFR Bit CRCC.6[CRCSD] are used instead of SFR CRCD.

The data stream is written bit-by-bit into SFR Bit CRCC.6[CRCSD]. Each bit is processed by forcing the flag SFR Bit CRCC.5[CRCSS] to 1_B.

The following figure shows an example of the usage of SFR Bit CRCC.5[CRCSS] and SFR Bit CRCC.6[CRCSD].

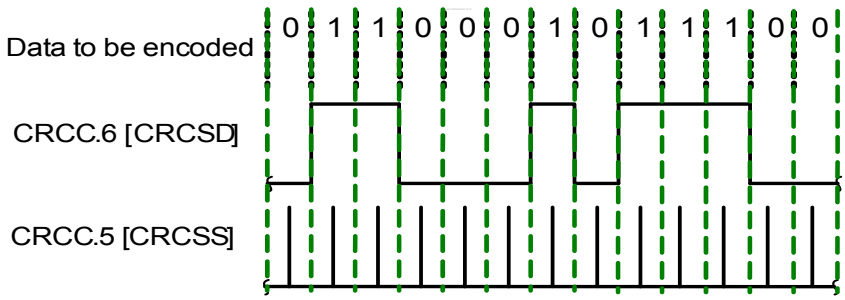


Figure 45 Example of Serial CRC Generation/checking

Note: The serial and byte-aligned generation/checking mechanism is interchangeable within the same generation/checking process. For example, if a data packet consists of 18 bits, then 16 bits can be processed byte-aligned via SFR CRCD and the two remaining bits can be processed bit-aligned by using SFR Bit CRCC.5[CRCSS] and SFR Bit CRCC.6[CRCSD].

2.12.4 Register Description

Table 20 Registers Overview

Register Short Name	Register Long Name	Offset Address	Wakeup Value	Page Number
CRCC	CRC Control Register	$A9_H$	02_H	125
CRCD	CRC Data Register	AA_H	00_H	126
CRC0	CRC Shift Register low byte	AC_H	00_H	126
CRC1	CRC Shift Register high byte	AD_H	00_H	127

CRC Control Register

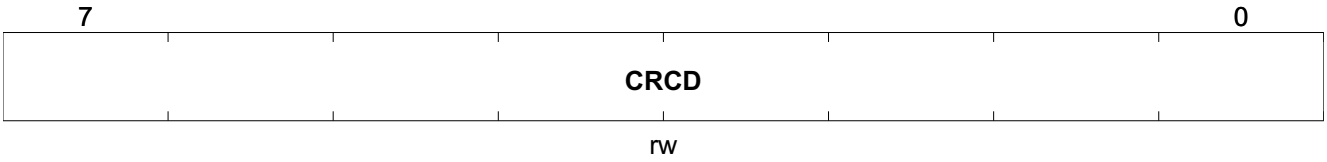
CRCC	Offset	Wakeup Value	Reset Value
CRC Control Register	$A9_H$	02_H	02_H

7	6	5	4	2	1	0
Res	CRCSD	CRCSS	Res		CRCValid	Res
	rw	rw			r	

Field	Bits	Type	Description
Res	7		**Reserved**
CRCSD	6	rw	**CRC Serial Data**
CRCSS	5	rw	**CRC Serial Data Strobe** Use CRCSS to serial strobe data bit CRCSD into CRC encoding/decoding procedure. 0_B No calculation cycle is done 1_B One calculation cycle is done with every write access to CRCSD or CRCSS
Res	4:2		**Reserved**
CRCValid	1	r	**CRC Valid** Is set by hardware on valid CRC results, that means all CRC-bits are 0 0_B CRC result invalid (at least one bit in CRC0 or CRC1 is 1_B) 1_B CRC result valid (all bits in CRC0 and CRC1 are 0_B)
Res	0		**Reserved**

CRC Data Register

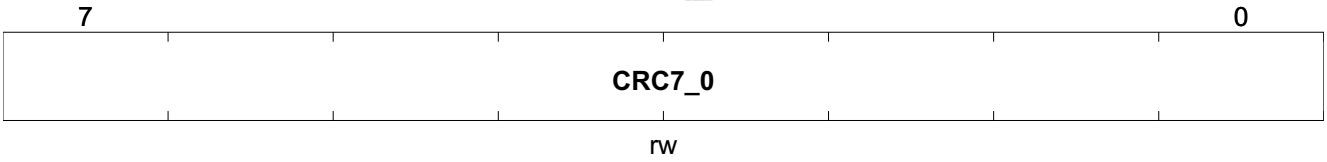
CRCD	Offset	Wakeup Value	Reset Value
CRC Data Register	AA_H	00_H	00_H



Field	Bits	Type	Description
CRCD	7:0	rw	**CRC Data Register**

CRC Shift Register low byte

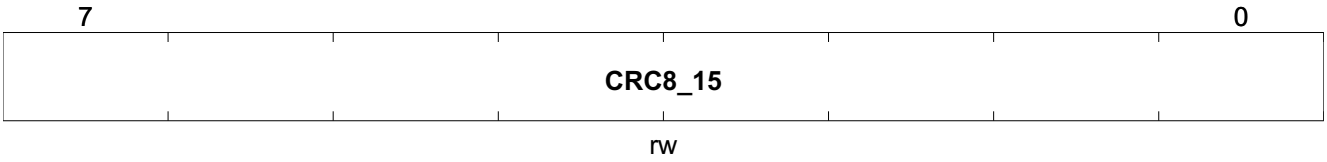
CRC0	Offset	Wakeup Value	Reset Value
CRC Shift Register low byte	AC_H	00_H	00_H



Field	Bits	Type	Description
CRC7_0	7:0	rw	**CRC Shift Register bit 7 down to bit 0**

CRC Shift Register high byte

CRC1	Offset	Wakeup Value	Reset Value
CRC Shift Register high byte	AD_H	00_H	00_H



Field	Bits	Type	Description
CRC8_15	7:0	rw	**CRC Shift Register bit 15 down to bit 8**

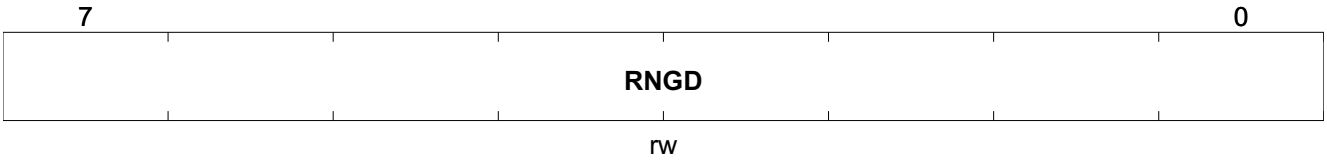
2.13 8 bit Pseudo Random Number Generator

For many applications, a pseudo-random number generator is needed, e.g. to vary the interval period between transmissions. For this purpose, a Maximum Length linear Feedback Shift Register (MLFSR) is available as a hardware unit. A user-defined start value (except 00_H) can be written to SFR RNGD. The default value after startup is 55_H. With every read access to SFR RNGD a new pseudo-random number is generated.

2.13.1 Register Description

Random Number Generator Data Register

RNGD	Offset	Wakeup Value	Reset Value
Random Number Generator Data Register	**AB_H**	**$UUUUUUUU_B$**	**55_H**



Field	Bits	Type	Description
RNGD	7:0	rw	**Random Number Generator Data Register**

2.14 Timers

The PMA51xx comprises four independent 16-bit timers. Timers 0/1 operate as up-counters, and Timers 2/3 operate as down-counters.

2.14.1 Timer 0 and Timer 1

Timer/Counter 0 and 1 are fully compatible with Timer/Counter 0 and 1 of the Standard 8051 microcontroller. Timer 0/1 operate as up-counters and use the selected system clock divided by 6.

2.14.1.1 Basic Timer Operations

The external inputs PP1 and PP9 can be programmed to function as a gate for Timer/Counters 0 and 1 to facilitate pulse-width measurements. Each timer consists of two 8-bit registers (TH0 and TL0 for Timer/Counter 0, TH1 and TL1 for Timer/Counter 1) that may be combined to one timer configuration depending on the mode that is established. The functions of the timers are controlled by two SFRs, TCON and TMOD. The operating modes are described and shown for Timer 0. If not explicitly noted, this applies also to Timer 1.

Setting the SFR bit TCON.4[TR0] (respectively SFR bit TCON.6[TR1]) starts Timer 0 (resp. Timer 1). It counts using the selected clock (see SFR TMOD) until the timer has an overflow. SFR bit TCON.5[TF0] (resp. SFR bit TCON.7[TF1] is set.
If the selected timer mode uses timer reload, then the timer is automatically reloaded and restarted.

If the selected timer mode does not use timer reload, the timer is stopped and SFR bit TCON.4[TR0] (resp. SFR bit TCON.6[TR1]) is cleared.

2.14.1.2 Timer Modes

Timer/Counter 0 and 1 can be used in the following four operating modes:

- Mode 0: 8 bit timer/counter with a divide-by-32 prescaler (13 bit timer register: 8 bit + 5 bit prescaler)
- Mode 1: 16 bit timer/counter
- Mode 2: 8 bit timer/counter with 8 bit auto-reload
- Mode 3: Timer/Counter 0 is configured as one 8 bit timer/counter and one 8 bit counter counting machine cycles.Timer/counter 1 in this mode holds its count. The effect is the same as setting TR1 = 0.

2.14.1.2.1 Timer/Counter 0/1 - Mode 0

Figure 46 “Timer/Counter 0, Mode 0, 13-Bit Timer/Counter” on Page 129 shows the Mode 0 operation.

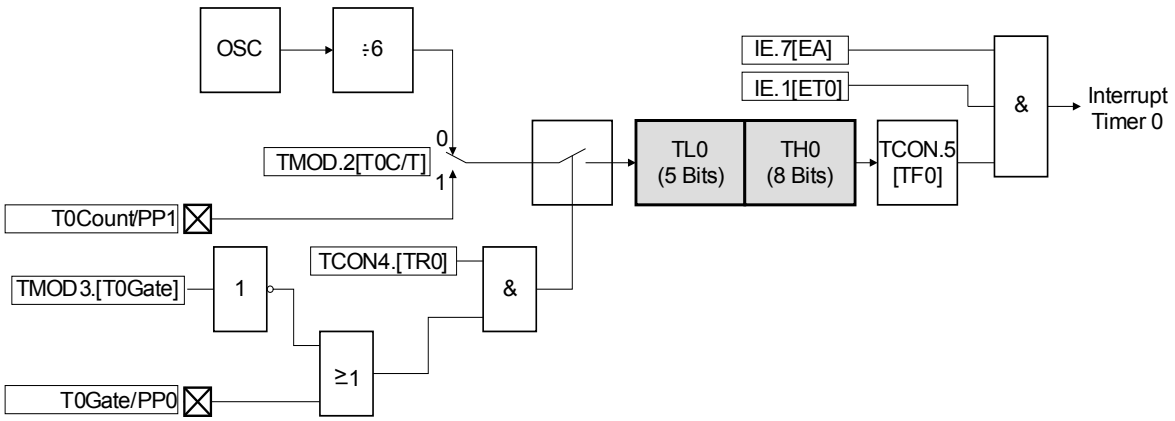


Figure 46 Timer/Counter 0, Mode 0, 13-Bit Timer/Counter

2.14.1.2.2 Timer/Counter 0/1 - Mode 1

Mode 1 is equal to Mode 0 but in Mode 1, the timer register is running with all 16 bits.

2.14.1.2.3 Timer/Counter 0/1 - Mode 2

Mode 2 configures the Timer register as an 8-bit counter in TL0 (resp. TL1) with automatic reload, as shown in **Figure 47 “Timer/Counter 0, Mode 2: 8-bit Timer/Counter with auto-reload” on Page 130**. Overflow from TL0 (resp. TL1) not only sets TCON.5 [TF0] (resp. TCON.7 [TF1]), but also reloads TL0 (resp. TL1) with the contents of TH0 (resp. TH1), which is preset by software. The reload leaves TH0 (resp. TH1) unchanged.

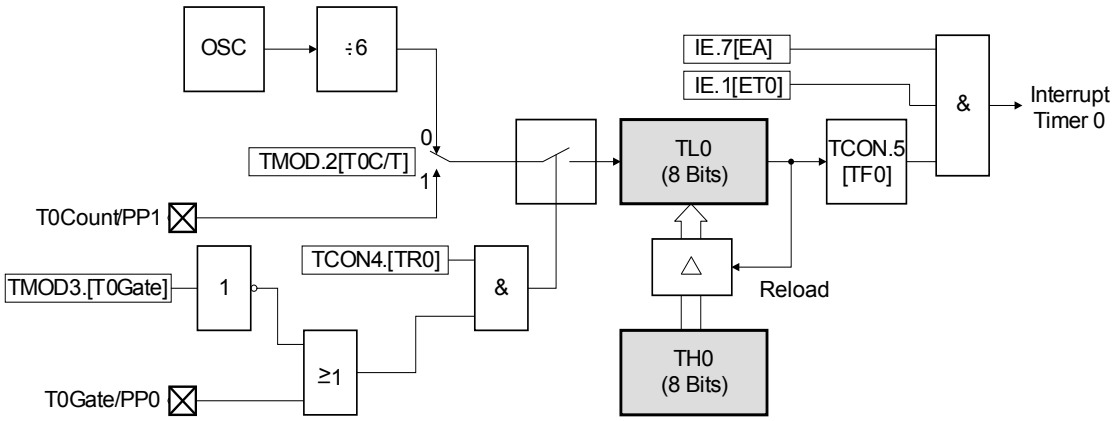


Figure 47 Timer/Counter 0, Mode 2: 8-bit Timer/Counter with auto-reload

2.14.1.2.4 Timer/Counter 0/1 - Mode 3

Mode 3 has different effects on Timer 0 and Timer 1. Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TCON.6 [TR1]=0. Timer 0 establishes TL0 and TH0 as two separate counters (**Figure 48 “Timer/Counter 0, Mode 3: Two 8-bit Timers/Counters” on Page 131**). TL0 uses the Timer 0 control bits: TMOD.2 [T0C/T], TMOD.3 [T0Gate], TCON.4 [TR0], TCON.5 [TF0] and the pin status of PP0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TCON.6 [TR1] and TCON.7 [TF1] from Timer 1. Thus, TH0 now controls the Timer 1 interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer or counter. When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3, or in fact, in any application not requiring an interrupt from Timer 1 itself.

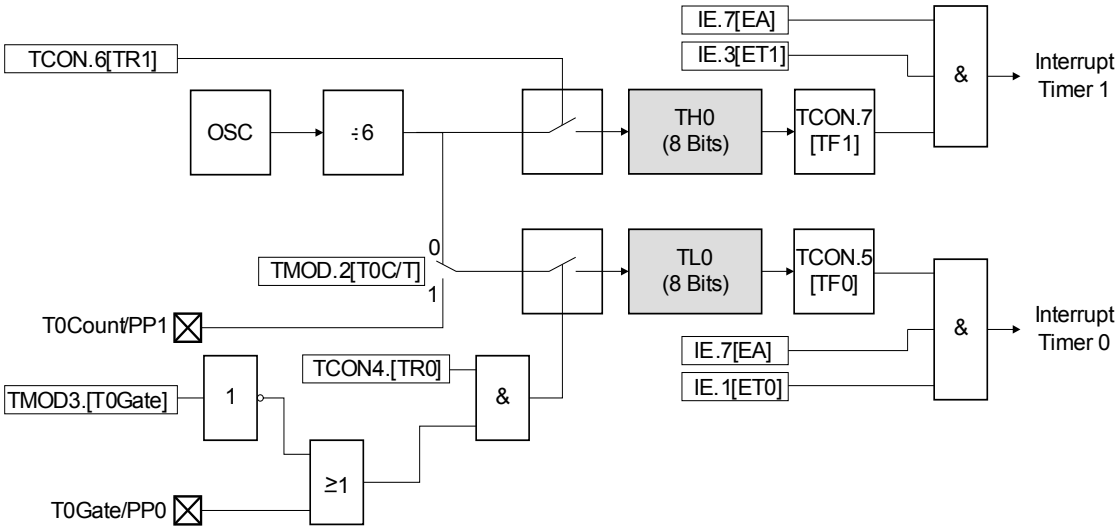


Figure 48 Timer/Counter 0, Mode 3: Two 8-bit Timers/Counters

2.14.1.3 Timer/Counter 0/1 Interrupt support

This module supports interrupt generation on overflow of Timer/Counter 0 as well as Timer/Counter 1. In addition to these timer/counter interrupts, two external interrupts are handled by this unit (ref. to standard 8051).

On overflow of the up counting timer/counter from all 1_B to all 0_B, the flag TCON.5 [TF0] or TCON.7 [TF1] is set by hardware. These flags acts as interrupt request flags. A 1_B indicates a pending interrupt request. These flags are cleared by hardware as on standard 8051 when the corresponding interrupt vector has been fetched by the CPU.

2.14.1.4 Register Description

Table 21 Registers Overview

Register Short Name	Register Long Name	Offset Address	Wakeup Value	Page Number
TCON	Timer Control Register Timer 0/1	88_H	00_H	132
TMOD	Timer Mode Register Timer 0/1	89_H	00_H	135
TL0	Timer 0 Register low byte	$8A_H$	00_H	134
TL1	Timer 1 Register low byte	$8B_H$	00_H	134
TH0	Timer 0 Register high byte	$8C_H$	00_H	133
TH1	Timer 1 Register high byte	$8D_H$	00_H	133

Timer Control Register Timer 0/1

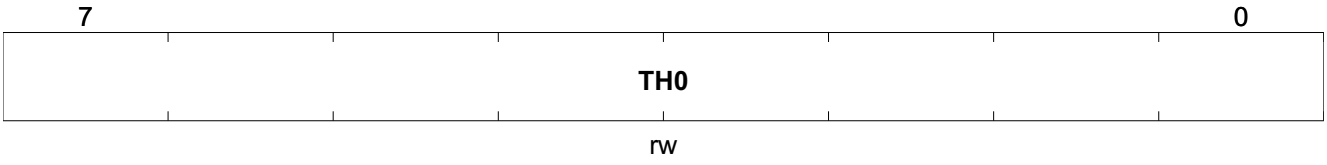
TCON	Offset	Wakeup Value	Reset Value
Timer Control Register Timer 0/1	88_H	00_H	00_H

7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
TF1	7	rw	**Timer 1 Overflow Flag** This flag is set on timer overflow and automatically cleared by hardware if the interrupt service routine is entered. In polling mode this bit has to be cleared by software.
TR1	6	rw	**Timer 1 Run Control Bit** 0_B Stop Timer 1 / Timer 1 does not run 1_B Start Timer 1 / Timer 1 runs
TF0	5	rw	**Timer 0 Overflow Flag** This flag is set on timer overflow and automatically cleared by hardware if the interrupt service routine is entered. In polling mode this bit has to be cleared by software.
TR0	4	rw	**Timer 0 Run Control Bit** 0_B Stop Timer 0 / Timer 0 does not run 1_B Start Timer 0 / Timer 0 runs
IE1	3	rw	**Interrupt 1 Request Flag** This is the interrupt request flag for external interrupt 1 (PP7) 0_B Interrupt 1 has not been triggered 1_B Interrupt 1 has been triggered
IT1	2	rw	**Interrupt 1 Type Control bit** 0_B Interrupt 1 is triggered by a low level on PP7 1_B Interrupt 1 is triggered by a falling edge on PP7
IE0	1	rw	**Interrupt 0 Request Flag** This is the interrupt request flag for external interrupt 0 (PP9) 0_B Interrupt 0 has not been triggered 1_B Interrupt 0 has been triggered
IT0	0	rw	**Interrupt 0 Type Control bit** 0_B Interrupt 0 is triggered by a low level on PP9 1_B Interrupt 0 is triggered by a falling edge on PP9

Timer 0 Register high byte

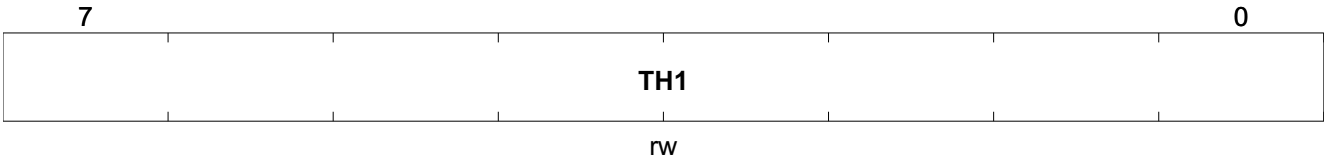
TH0	Offset	Wakeup Value	Reset Value
Timer 0 Register high byte	$8C_H$	00_H	00_H



Field	Bits	Type	Description
TH0	7:0	rw	**Timer 0 Register high byte**

Timer 1 Register high byte

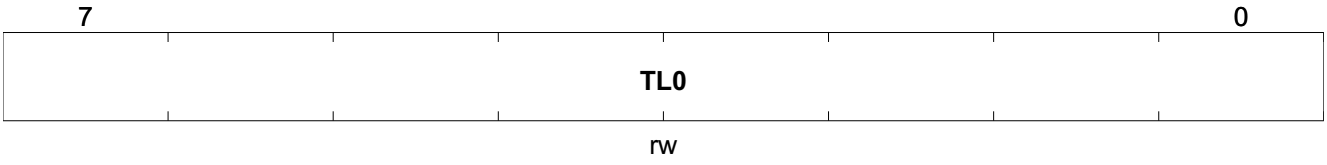
TH1	Offset	Wakeup Value	Reset Value
Timer 1 Register high byte	$8D_H$	00_H	00_H



Field	Bits	Type	Description
TH1	7:0	rw	**Timer 1 Register high byte**

Timer 0 Register low byte

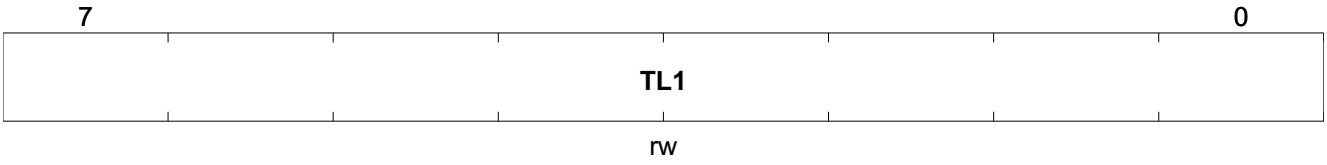
TL0	Offset	Wakeup Value	Reset Value
Timer 0 Register low byte	$8A_H$	00_H	00_H



Field	Bits	Type	Description
TL0	7:0	rw	**Timer 0 Register low byte**

Timer 1 Register low byte

TL1	Offset	Wakeup Value	Reset Value
Timer 1 Register low byte	$8B_H$	00_H	00_H



Field	Bits	Type	Description
TL1	7:0	rw	**Timer 1 Register low byte**

Timer Mode Register Timer 0/1

TMOD	Offset	Wakeup Value	Reset Value
Timer Mode Register Timer 0/1	89_H	00_H	00_H

7	6	5	4	3	2	1	0
T1Gate	T1C/T	T1M		T0Gate	T0C/T	T0M	
rw	rw	rw		rw	rw	rw	

Field	Bits	Type	Description
T1Gate	7	rw	**Timer 1 Gate Control bit** 0_B Internal Enable: Use TR1 to enable the Timer/Counter 1_B External Enable: Use PP8 and TR1 to enable the Timer/Counter
T1C/T	6	rw	**Timer 1 Counter / Timer select** 0_B Timer 1_B Counter: Count input is PP9
T1M	5:4	rw	**Timer 1 Mode select** 00_B Mode 0: 8 bit timer with a divided-by-32 prescaler 01_B Mode 1: 16 bit timer 10_B Mode 2: 8 bit timer with 8 bit auto-reload 11_B Mode 3: Timer 1 hold its count. The effect is the same like setting TR1=0
T0Gate	3	rw	**Timer 0 Gate Control bit** 0_B Internal Enable: Use TR0 to enable the Timer/Counter 1_B External Enable: Use PP0 and TR0 to enable the Timer/Counter
T0C/T	2	rw	**Timer 0 Counter / Timer select** 0_B Timer 1_B Counter: Count input is PP1
T0M	1:0	rw	**Timer 0 Mode select** 00_B Mode 0: 8 bit timer with a divided-by-32 prescaler 01_B Mode 1: 16 bit timer 10_B Mode 2: 8 bit timer with 8 bit auto-reload 11_B Mode 3: Two 8 bit timers

2.14.2 Timer 2 and Timer 3

Timer 2 and Timer 3 operate as down-counters. The clock source and the timer mode can be selected using SFR TMOD2.

2.14.2.1 Basic Timer Operations

Setting the SFR Bit TCON2.0[T2Run] (respectively SFR Bit TCON2.4[T3Run]) starts Timer 2 (resp. Timer 3). It counts using the selected clock (see SFR TMOD2) until the timer is elapsed. SFR Bit TCON2.1[T2Full] (resp. SFR Bit TCON2.5[T3Full] is set.

If the selected timer mode used timer reload, then the timer is automatically reloaded and restarted on underrun.

If the selected timer mode didn't use timer reload, the timer is stopped on underrun and SFR Bit TCON2.0[T2Run] (resp. SFR Bit TCON2.4[T3Run]) is cleared.

2.14.2.2 Timer Modes

Depending on the setting of the 3 bits of SFR Bit TMOD2.2 0[TM2-0], there are 8 timer modes selectable with Timer 2 and Timer 3.

2.14.2.2.1 Timer 2/3 - Mode 0

Comprises:

- 16-bit timer with reload

The timer unit is configured as a 16-bit reloadable timer. SFR TL2 and SFR TH2 hold the start value. If SFR Bit TCON2.0[T2Run] is set, the timer starts counting down. SFR Bit TCON2.1[T2Full] is set when the timer is elapsed (underflow from 00_H to FF_H). The timer value is reloaded from SFR TL3 and SFR TH3, and the timer is restarted automatically. SFR Bit TCON2.1[T2Full] has to be reset by software. It is not cleared on read access.

Note: In this mode, both SFR Bit TCON2.4[T3Run] and SFR Bit TCON2.5[T3Full] are not used.

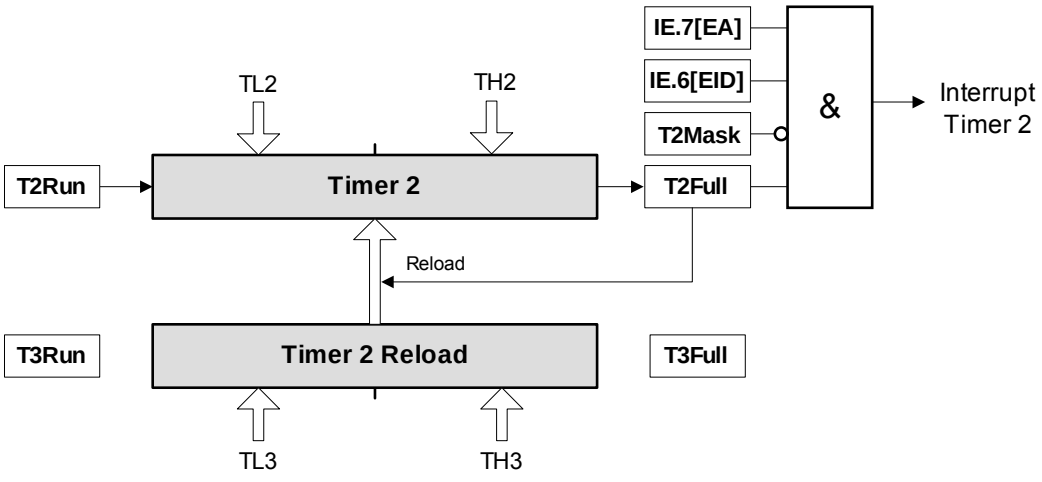


Figure 49 Timer 2/3 - Mode 0

2.14.2.2.2 Timer 2/3 - Mode 1

Comprises:

- 16-bit timer without reload
- 8-bit timer with reload and bit rate strobe signal for RF Transmitter

Timer 2 operates as a 16-bit timer with start value in SFR TL2 and SFR TH2, timer run bit SFR Bit TCON2.0[T2Run] and timer elapsed indicator SFR Bit TCON2.1[T2Full]. If the timer elapses, it stops, sets SFR Bit TCON2.1[T2Full], and resets the timer run bit SFR Bit TCON2.0[T2Run].

Timer 3 sets up a reloadable 8-bit timer holding the startup value in SFR TL3, timer reload value in SFR TH3, timer run bit in SFR Bit TCON2.4[T3Run], and timer elapsed indicator in SFR Bit TCON2.5[T3Full].

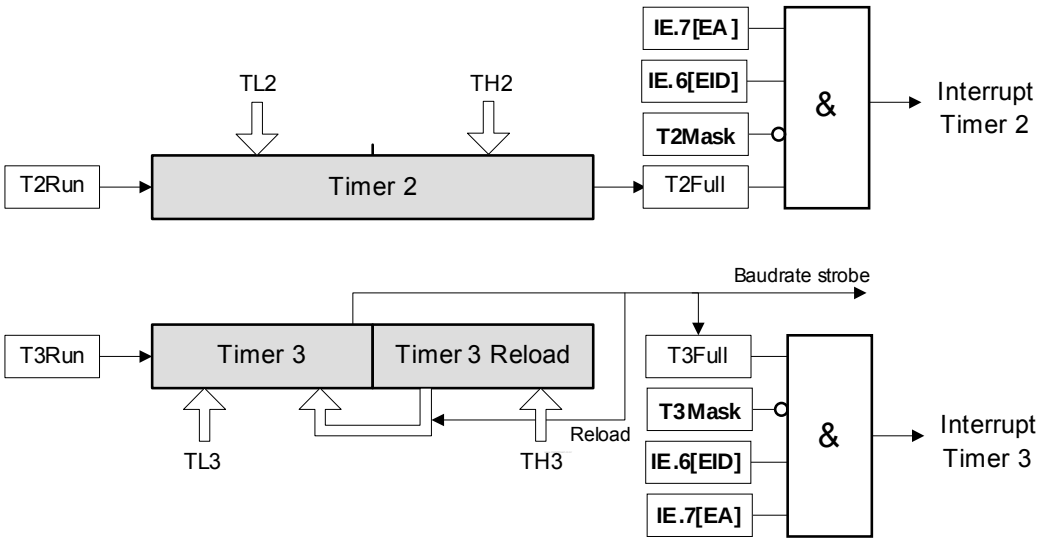


Figure 50 Timer 2/3 - Mode 1

2.14.2.2.3 Timer 2/3 - Mode 2

Comprises:

- 8-bit timer with reload
- 8-bit timer with reload and bit rate strobe signal for RF Transmitter

Timer 2 sets up a reloadable 8-bit timer holding the start value SFR TL2, timer reload value SFR TH2, timer run bit SFR Bit TCON2.0[T2Run], and timer elapsed indicator SFR Bit TCON2.1[T2Full].

Timer 3 sets up a reloadable 8-bit timer holding the start value SFR TL3, timer reload value SFR TH3, timer run bit SFR Bit TCON2.4[T3Run], and timer elapsed indicator SFR Bit TCON2.5[T3Full].

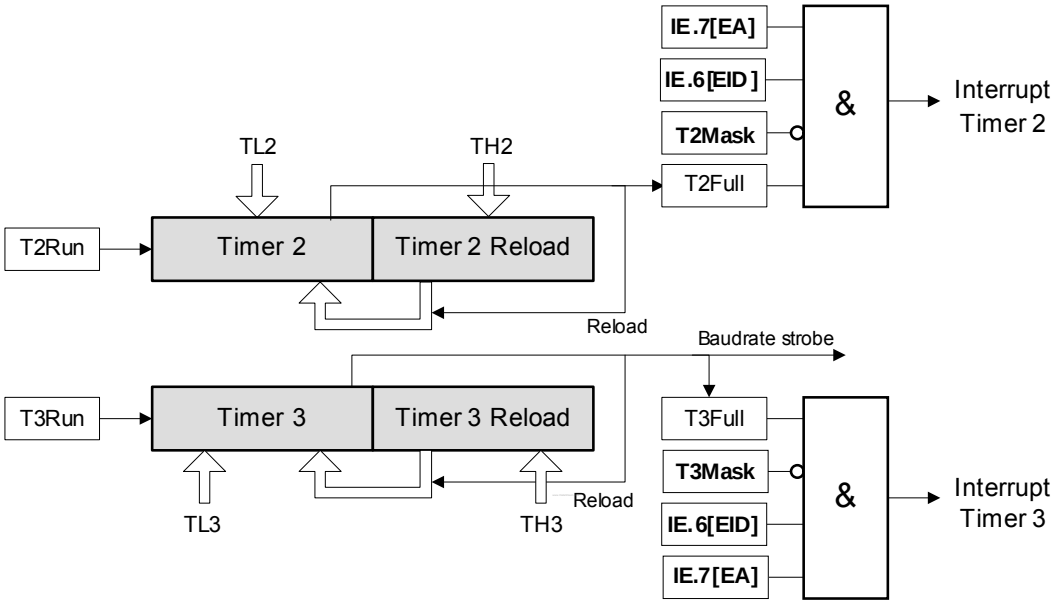


Figure 51 Timer 2/3 - Mode 2

2.14.2.2.4 Timer 2/3 - Mode 3

Comprises:

- 8-bit timer without reload (1)
- 8-bit timer without reload (2)
- 8-bit timer with reload and bit rate strobe signal for RF Transmitter

Timer 2 (1) utilizes SFR TL2 as starting value and T2Full as timer elapsed flag. Setting SFR Bit TCON2.0[T2Run] starts the timer, and SFR Bit TCON2.1[T2Full] is set when the timer is elapsed. SFR Bit TCON2.0[T2Run] is reset automatically if the timer elapses.

Timer 2 (2) utilizes SFR TH2 as starting value and SFR Bit TCON2.5[T3Full] as timer elapsed flag. Setting SFR Bit TCON2.4[T3Run] starts the timer, and SFR Bit TCON2.5[T3Full] is set when the timer is elapsed. SFR Bit TCON2.4[T3Run] is reset automatically if the timer elapses.

Timer 3 operates exclusively as an 8-bit bit rate timer for Manchester coding. Therefore the timer needs neither a run nor an elapsed bit. It is started automatically when the timer mode is set.

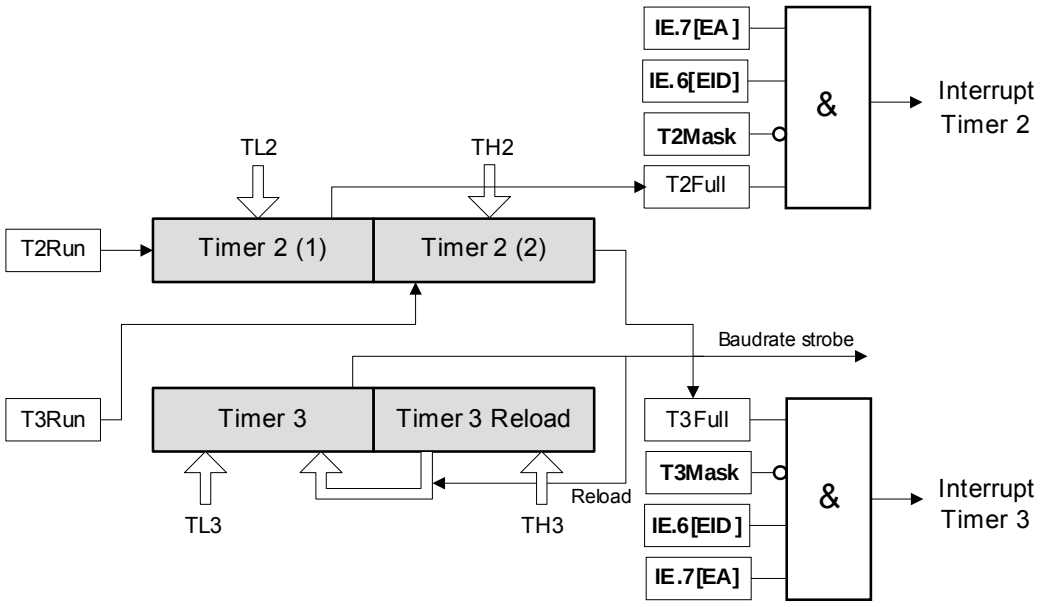


Figure 52 Timer 2/3 - Mode 3

2.14.2.2.5 Timer 2/3 - Mode 4

Comprises:

- 16-bit timer with reload and bit rate strobe signal for RF Transmitter

The timer unit is configured as a 16-bit reloadable timer. SFR TL3 and SFR TH3 hold the start value. As soon as SFR Bit TCON2.4[T3Run] is set, the timer starts counting. SFR Bit TCON2.5[T3Full] is set when the timer is elapsed. The timer value is reloaded from SFR TL2 and SFR TH2 and the timer is restarted automatically. SFR Bit TCON2.5[T3Full] has to be reset by software. It is not cleared on read-access.

Note: In this mode, both SFR Bit TCON2.0[T2Run] and SFR Bit TCON2.1[T2Full] are not used.

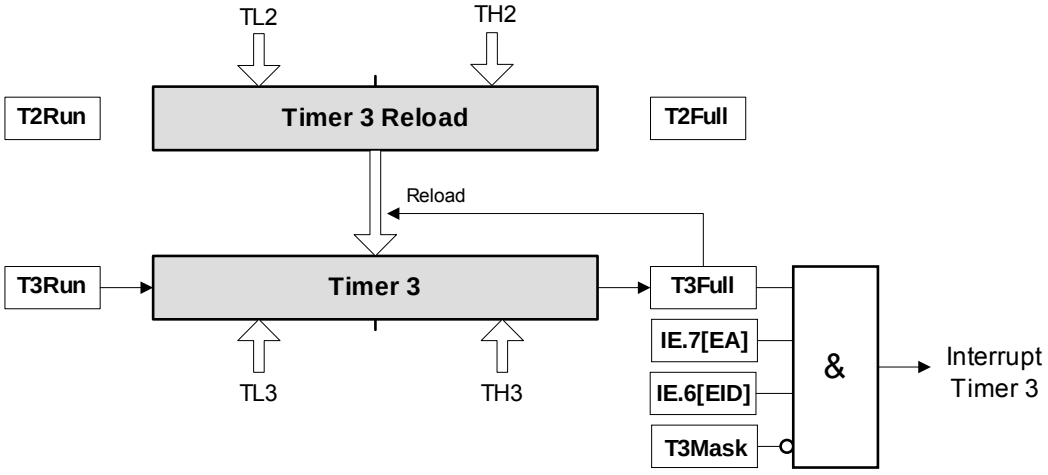


Figure 53 Timer 2/3 - Mode 4

2.14.2.2.6 Timer 2/3 - Mode 5

Comprises:

- 8-bit timer with reload
- 16-bit timer without reload and bit rate strobe signal for RF Transmitter

Timer 2 sets up a reloadable 8-bit timer holding the start value in SFR TL2, timer reload value in SFR TH2, timer run bit SFR Bit TCON2.0[T2Run], and timer elapsed indicator in SFR Bit TCON2.1[T2Full].

Timer 3 operates as a 16-bit timer with the start value in SFR TL3 and SFR TH3, timer run bit SFR Bit TCON2.4[T3Run], and timer elapsed indicator SFR Bit TCON2.5[T3Full]. If the timer elapses, the timer stops SFR Bit TCON2.5[T3Full] is set, and the timer run bit SFR Bit TCON2.4[T3Run] is reset.

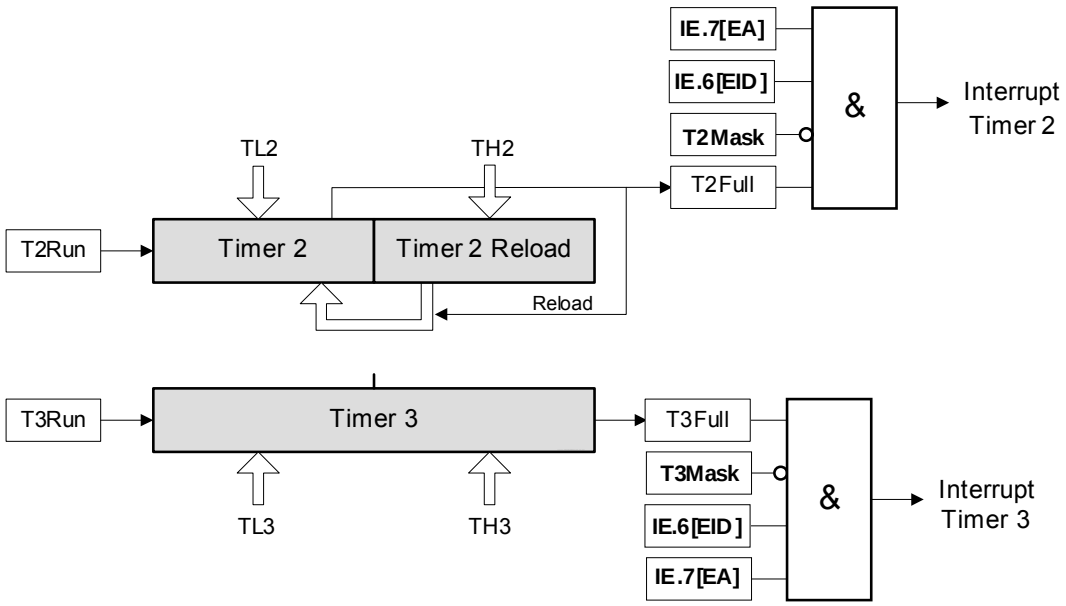


Figure 54 Timer 2/3 - Mode 5

2.14.2.2.7 Timer 2/3 - Mode 6

Comprises:

- 16-bit timer without reload
- 16-bit timer without reload and bit rate strobe signal for RF Transmitter

Timer 2 operates as a 16-bit timer with the start value in SFR TL2 and SFR TH2, timer run bit SFR Bit TCON2.0[T2Run], and timer elapsed indicator SFR Bit TCON2.1[T2Full]. If the timer is elapsed the timer is stopped, SFR Bit TCON2.1[T2Full] is set, and the timer run bit SFR Bit TCON2.0[T2Run] is reset.

Timer 3 operates as a 16-bit timer with the start value in SFR TL3 and SFR TH3, timer run bit SFR Bit TCON2.4[T3Run], and timer elapsed indicator SFR Bit TCON2.5[T3Full]. If the timer elapses, the timer stops, SFR Bit TCON2.5[T3Full] is set, and the timer run bit SFR Bit TCON2.4[T3Run] is reset.

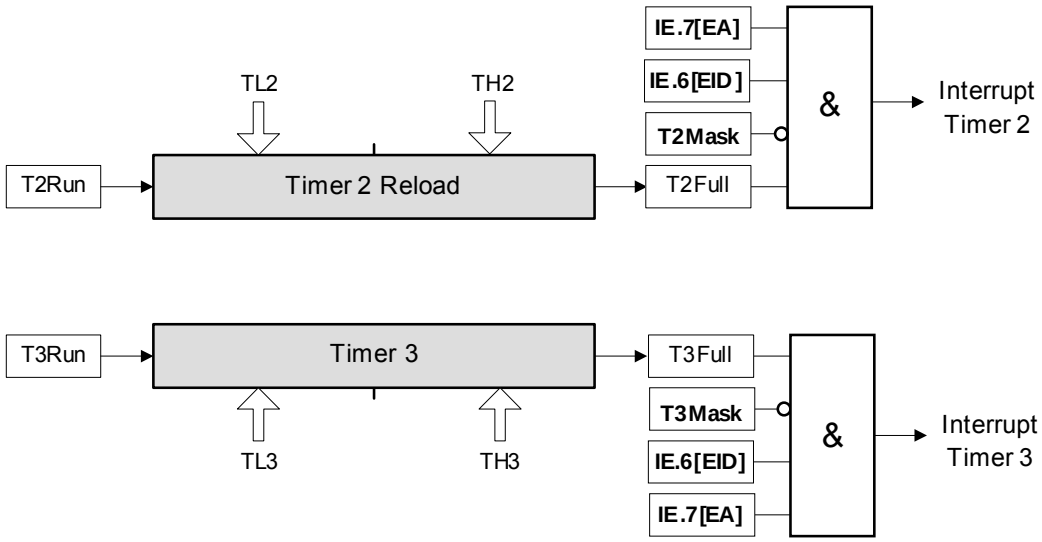


Figure 55 Timer 2/3 - Mode 6

2.14.2.2.8 Timer 2/3 - Mode 7

Comprises:

- 16-bit timer for Interval Timer calibration
- 8-bit timer with reload and bit rate strobe signal for RF Transmitter

Timer 2 operates as a 16-bit clock counter during one 2 kHz RC LP oscillator period with the counting value provided in SFR TL2 and SFR TH2, a timer run bit SFR Bit TCON2.0[T2Run], and timer overflow indicator SFR Bit TCON2.1[T2Full]. When SFR Bit TCON2.0[T2Run] is set, the counter starts counting on the next rising edge of the 2 kHz RC LP oscillator, and is stopped at the subsequent rising edge. This timer mode is used for Interval Timer Calibration by the Library functions, for example (see [1]).

Timer 3 sets up a reloadable 8-bit timer holding the startup value in SFR TL3, timer reload value in SFR TH3, timer run bit in SFR bit TCON2.4[T3Run], and timer elapsed indicator in SFR Bit TCON2.5[T3Full].

Note: This timer mode is not recommended for application usage. It is used by the Library functions for calibration.

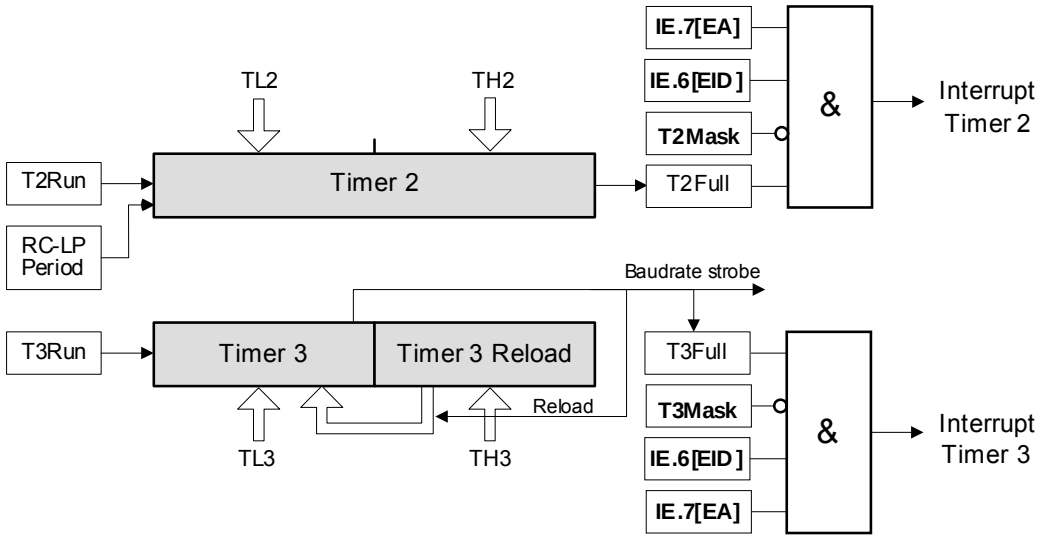


Figure 56 Timer 2/3 - Mode 7

2.14.2.3 Register Description

Table 22 Registers Overview

Register Short Name	Register Long Name	Offset Address	Wakeup Value	Page Number
TCON2	Timer Control Register Timer 2/3	$C8_H$	00_H	143
TMOD2	Timer Mode Register 2 Timer 2/3	$C9_H$	00_H	146
TL3	Timer 3 Register low byte	CA_H	00_H	145
TH3	Timer 3 Register high byte	CB_H	00_H	144
TL2	Timer 2 Register low byte	CC_H	00_H	145
TH2	Timer 2 Register high byte	CD_H	00_H	144

Timer Control Register Timer 2/3

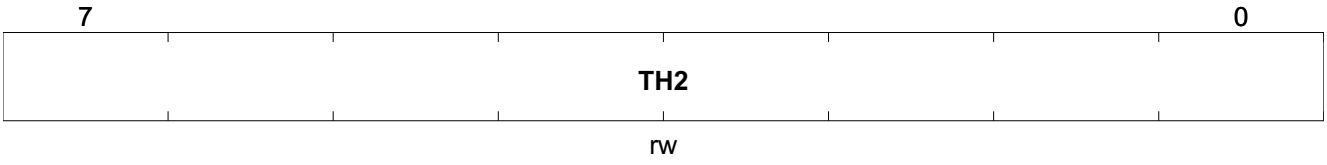
TCON2	Offset	Wakeup Value	Reset Value
Timer Control Register Timer 2/3	**$C8_H$**	**00_H**	**00_H**

7	6	5	4	3	2	1	0
T3Mask	Res	**T3Full**	**T3Run**	**T2Mask**	Res	**T2Full**	**T2Run**
rw		rw	rw	rw		rw	rw

Field	Bits	Type	Description
T3Mask	7	rw	**Timer 3 Interrupt Mask** 0_B Timer 3 interrupt is not blocked 1_B Timer 3 interrupt is blocked (masked)
Res	6		**Reserved**
T3Full	5	rw	**Timer 3 Full Bit** 0_B No Timer 3 underrun occurred 1_B Timer 3 underrun occurred
T3Run	4	rw	**Timer 3 Run Bit** 0_B Stop Timer 3 / Timer 3 does not run 1_B Start Timer 3 / Timer 3 runs
T2Mask	3	rw	**Timer 2 Interrupt Mask** 0_B Timer 2 interrupt is not blocked 1_B Timer 2 interrupt is blocked (masked)
Res	2		**Reserved**
T2Full	1	rw	**Timer 2 Full Bit** 0_B No Timer 2 underrun occurred 1_B Timer 2 underrun occurred
T2Run	0	rw	**Timer 2 Run Bit** 0_B Stop Timer 2 / Timer 2 does not run 1_B Start Timer 2 / Timer 2 runs

Timer 2 Register high byte

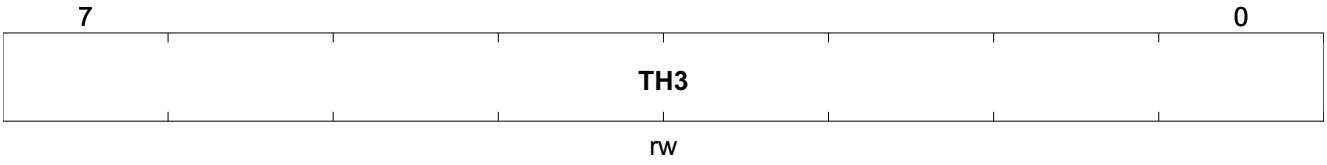
TH2	Offset	Wakeup Value	Reset Value
Timer 2 Register high byte	CD_H	00_H	00_H



Field	Bits	Type	Description
TH2	7:0	rw	**Timer 2 Register high byte**

Timer 3 Register high byte

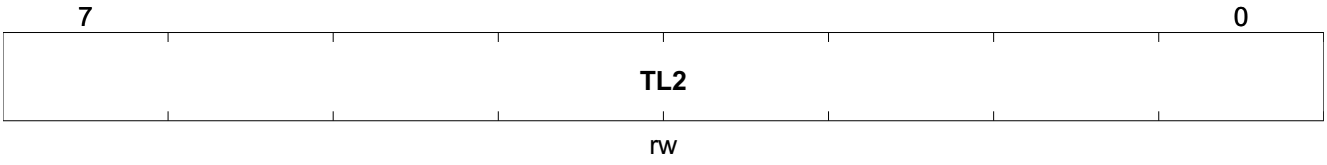
TH3	Offset	Wakeup Value	Reset Value
Timer 3 Register high byte	CB_H	00_H	00_H



Field	Bits	Type	Description
TH3	7:0	rw	**Timer 3 Register high byte**

Timer 2 Register low byte

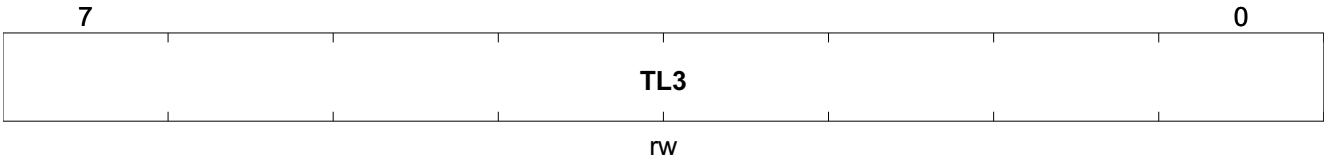
TL2	Offset	Wakeup Value	Reset Value
Timer 2 Register low byte	CC_H	00_H	00_H



Field	Bits	Type	Description
TL2	7:0	rw	**Timer 2 Register low byte**

Timer 3 Register low byte

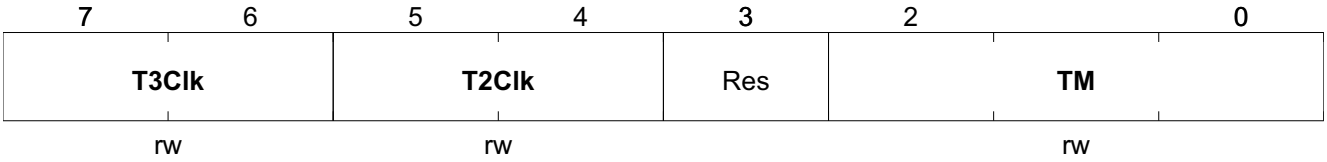
TL3	Offset	Wakeup Value	Reset Value
Timer 3 Register low byte	CA_H	00_H	00_H



Field	Bits	Type	Description
TL3	7:0	rw	**Timer 3 Register low byte**

Timer Mode Register 2 Timer 2/3

TMOD2	Offset	Wakeup Value	Reset Value
Timer Mode Register 2 Timer 2/3	$C9_H$	00_H	00_H



Field	Bits	Type	Description
T3Clk	7:6	rw	**Timer 3 Clock Source Select** (see **Figure 9 "PMA5110 Clock Concept" on Page 52**) 00_B undivided system clock 01_B system clock divided by 6 10_B 2 kHz LP RC oscillator clock 11_B PP2 event count (rising edge)
T2Clk	5:4	rw	**Timer 2 Clock Source Select** (see **Figure 9 "PMA5110 Clock Concept" on Page 52**) 00_B undivided system clock 01_B system clock divided by 6 10_B 2 kHz LP RC oscillator clock 11_B Timer 3 overflow event count
Res	3		**Reserved**
TM	2:0	rw	**Timer Mode** 000_B Mode 0 001_B Mode 1 010_B Mode 2 011_B Mode 3 100_B Mode 4 101_B Mode 5 110_B Mode 6 111_B Mode 7

2.15 General Purpose Input/Output (GPIO)

Ten GPIO pins are available and can either be used by the application for general purposes, or are assigned to a peripheral (**Alternative Port Functionality**). When used as GPIO pins, they can be accessed directly by the processor. Pull-up and pull-down resistors are configurable on demand to allow wired-AND and wired-OR functions. All peripheral port pins are configured as input with the pull-up resistor, which is enabled after a Power On Reset. Pin status will be kept during POWER DOWN state.

2.15.1 GPIO Port Configuration

The following table shows the different possible configurations for the GPIO Port.

Table 23 GPIO Port Configuration

PPDx	PPOx	PPSx	I/O	Pull-up/ Pull-down	Comment
0	0	-	Output	No	LOW (sink)
0	1	-	Output	No	HIGH (source)
1	0	-	Input	No	High-Z (Tri-State Bidirectional)
1	1	0	Input	Pull-up	Weak-High (Quasi Bidirectional)
1	1	1	Input	Pull-down	Weak-Low (Quasi Bidirectional)

*Note: In addition, SFR Bit PPSx defines the wake-up sensitivity for the external wake-up source (see **External Wake-up on PP1-PP4 and PP6-PP9**).*

The x in the table above has to be replaced by 0 to 9 (PP0 - PP9).

2.15.2 Spike Suppression on Input Pins

To avoid metastability when reading the GPIO pins, a synchronization stage is included and a two-stage spike filter suppresses spikes; thus data is available to be read after a delay no greater than 2 system clock periods.

Due to the synchronization stage, the following might occur:

- Signal duration (T_{SIGNAL}) < 1 system clock period (1 T_{CLK}): Signal is suppressed
- 1 T_{CLK} < T_{SIGNAL} < 2 T_{CLK}: Undefined if suppressed or passed
- T_{SIGNAL} > 2 T_{CLK}: Signal is available in P1In or P3In register

2.15.3 External Wake-up on PP1-PP4 and PP6-PP9

PP1-PP4 and PP6-PP9 can additionally be used as external wake-up sources. To enable the external wake-ups the appropriate bit in the SFR ExtWUM must be set to 0_B and the pin must be configured as input by setting the appropriate bits in P1DIR respectively P3DIR to 1_B.
The internal pull-up/pull-down resistor is enabled if the appropriate bits in SFR P1OUT respectively in SFR P3OUT are set. SFR P1SENS respectively SFR P3SENS selects the sensitivity (active high/active low). For the settings where the internal pull-up resistor is enabled, a LOW on the appropriate PPx causes a wake-up. When the pull-down resistor is enabled with the appropriate setting a HIGH on PPx causes a wake-up. A logical description of the external wake-ups and the internal pull-up/pull-down resistors is show in **Figure 57 “Logical description of external wake-ups and internal pull-up/pull-down resistors” on Page 148**.

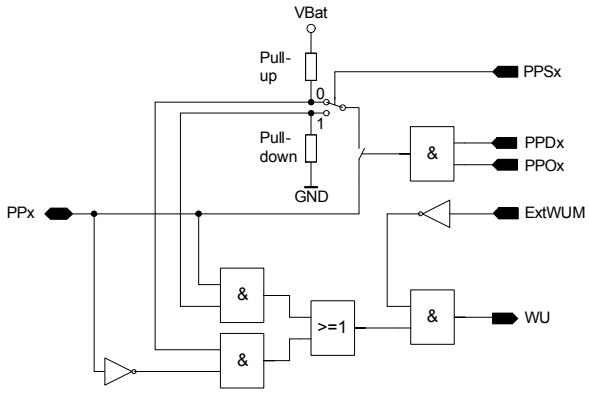


Figure 57 Logical description of external wake-ups and internal pull-up/pull-down resistors

2.15.4 Alternative Port Functionality

In the following table, the alternative port functionality is shown - which has higher priority than standard I/O port functionality.

Table 24 I/O Port 1 - Alternative Functionality

Pin	Function	I/O	Description
PP0	I2C-SCL	I	I2C Serial Clock Line Configured to I2C clock pin if SFR Bit CFG1.6 [I2CEn] is set. Weak-High has to be provided either by the internal pull-up resistor, by an external pull-up resistor or by the I2C master device.
	Port Pin I/O	I/O	Standard I/O port functionality controlled by P1Dir.0, P1Out.0, P1In.0.
	T0Gate	I/O	Can be used (alternative to the TMOD.3 [T0Gate]) as enable function for Timer 0
	OPMode1	I/O	Select operation mode (NORMAL-, DEBUG-, PROGRAMMING MODE)
PP1	I2C-SDA	I/O	I2C Serial Data Configured to I2C data pin if bit CFG1.6 [I2CEn] is set. Weak-High has to be provided either by the internal pull-up resistor, by an external pull-up resistor, or by the I2C master device.
	Port Pin I/O	I/O	Standard I/O port functionality controlled by P1Dir.1, P1Out.1, P1In.1, P1Sens.1.
	WU0	I/O	Wake-up by external wake-up source. Wake-up functionality in POWER DOWN state when enabled by setting ExtWUM.0 to zero. Wake-up level sensitivity dependent on P1Sens.1 (if set to 0, sensitive on low-level).
	T0Count	I/O	Can be used (alternative to CPU clock, TMOD.2[T0C/T]) as source for Timer 0 in counter mode.
	OPMode2	I/O	Select operation mode (NORMAL-, DEBUG-, PROGRAMMING MODE)
PP2	TxDataOut	I/O	RF Encoder data output: If bit CFG1.4[RFTXPEN] is set to one, the Manchester/BiPhase encoded data is delivered serially to PP2.
	Port Pin I/O	I/O	Standard I/O port functionality controlled by P1Dir.2, P1Out.2, P1In.2, P1Sens.2.
	WU1	I/O	Wake-up by external wake up source. Wake-up functionality in POWER DOWN state when enabled by setting ExtWUM.1 to zero. Wake-up level sensitivity dependent on P1Sens.2 (if set to 0, sensitive on low-level).
	T3Count	I/O	Can be used as clock source for Timer 3 when selected via TMOD2.7 - 6 [T3Clk.x].

Table 24 I/O Port 1 - Alternative Functionality (cont'd)

Pin	Function	I/O	Description
PP3	SPI_CS	I/O	SPI bus interface chip select
	Port Pin I/O	I/O	Standard I/O port functionality controlled by P1Dir.3, P1Out.3, P1In.3, P1Sens.3
	WU2	I/O	Wake-up by external wake-up source. Wake-up functionality in POWER DOWN state when enabled by setting ExtWUM.2 to zero. Wake-up level sensitivity dependent on P1Sens.3 (if set to 0, sensitive on low-level).
PP4	SPI_MISO	I/O	SPI bus interface master in slave out
	Port Pin I/O	I/O	Standard I/O port functionality controlled by P1Dir.4, P1Out.4, P1In.4, P1Sens.4
	WU3	I/O	Wake-up by external wake-up source. Wake-up functionality in POWER DOWN state when enabled by setting ExtWUM.3 to zero. Wake-up level sensitivity dependent on P1Sens.4 (if set to 0 sensitive on low-level).
PP5	SPI_MOSI	I/O	SPI bus interface master out slave in
	Port Pin I/O	I/O	Standard I/O port functionality controlled by P1Dir.5, P1Out.5, P1In.5, P1Sens.5
PP6	SPI_Clk	I/O	SPI bus interface clock
	Port Pin I/O	I/O	Standard I/O port functionality controlled by P1Dir.6, P1Out.6, P1In.6, P1Sens.6
	WU4	I/O	Wake-up by external wake-up source. Wake-up functionality in POWER DOWN state when enabled by setting ExtWUM.4 to zero. Wake-up level sensitivity dependent on P1Sens.6 (if set to 0, sensitive on low-level).
PP7	Port Pin I/O	I/O	Standard I/O port functionality controlled by P1Dir.7, P1Out.7, P1In.7, P1Sens.7
	ExtInt1	I/O	When enabled by setting IE.2 [EX1], this pin can generate an interrupt event that is sensitive to pin level or falling edge. The separation by level or edge is done via TCON.2 [IT1]. The interrupt flag is TCON3.[IE1].
	WU5	I/O	Wake-up by external wake-up source. Wake-up functionality in POWER DOWN state when enabled by setting ExtWUM.5 to zero. Wake-up level sensitivity dependent on P1Sens.7 (if set to 0, sensitive on low-level).
PP8	Port Pin I/O	I/O	Standard I/O port functionality controlled by P3Dir.0, P3Out.0, P3In.0, P3Sens.0
	WU6	I/O	Wake-up by external wake-up source. Wake-up functionality in POWER DOWN state when enabled by setting ExtWUM.6 to zero. Wake-up level sensitivity dependent on P3Sens.0 (if set to 0, sensitive on low-level).
	T1Gate	I/O	Can be used (alternative to the TMOD.7 [T1Gate]) as enable function for Timer 1
PP9	Port Pin I/O	I/O	Standard I/O port functionality controlled by P3Dir.1, P3Out.1, P3In.1, P3Sens.1
	Ext_Int0	I/O	When enabled by setting IE.0 [EX0] this pin can generate an interrupt event sensitive on pin level or falling edge. The separation by level or edge is done via TCON.0 [IT0]. The interrupt flag is TCON1.[IE0].
	WU7	I/O	Wake-up by external wake up source. Wake-up functionality in POWER DOWN state when enabled by setting ExtWUM.7 to zero. Wake-up level sensitivity dependent on P3Sens.1 (if set to 0, sensitive on low-level).
	T1Count	I/O	Can be used (alternative to CPU clock, TMOD.6[T1C/T]) as source for Timer 1 in counter mode.

2.15.5 Register Description

Table 25 Registers Overview

Register Short Name	Register Long Name	Offset Address	Wakeup Value	Page Number
P1Out	IO-Port 1 Data OUT Register	90_H	$UUUUUUUU_B$	153
P1Dir	IO-Port 1 Direction Register	91_H	$UUUUUUUU_B$	150
P1In	IO-Port 1 Data IN Register	92_H	$XXXXXXXX_B$	152
P1SENS	IO-Port 1 Sensitivity Register	93_H	$UUUUUUUU_B$	154
P3Out	IO-Port 3 Data OUT Register	$B0_H$	$000000UU_B$	153
P3Dir	IO-Port 3 Direction Register	EB_H	$000000UU_B$	151
P3In	IO-Port 3 Data IN Register	EC_H	$000000XX_B$	152
P3SENS	IO-Port 3 Sensitivity Register	ED_H	$000000UU_B$	155

IO-Port 1 Direction Register

P1Dir	Offset	Wakeup Value	Reset Value
IO-Port 1 Direction Register	91_H	$UUUUUUUU_B$	FF_H

7	6	5	4	3	2	1	0
PD1_7	PD1_6	PD1_5	PD1_4	PD1_3	PD1_2	PD1_1	PD1_0
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PD1_7	7	rw	**PP7 direction** 0_B output 1_B input
PD1_6	6	rw	**PP6 direction** 0_B output 1_B input
PD1_5	5	rw	**PP5 direction** 0_B output 1_B input
PD1_4	4	rw	**PP4 direction** 0_B output 1_B input
PD1_3	3	rw	**PP3 direction** 0_B output 1_B input

Field	Bits	Type	Description
PD1_2	2	rw	**PP2 direction** 0_B output 1_B input
PD1_1	1	rw	**PP1 direction** 0_B output 1_B input
PD1_0	0	rw	**PP0 direction** 0_B output 1_B input

IO-Port 3 Direction Register

P3Dir	Offset	Wakeup Value	Reset Value
IO-Port 3 Direction Register	**EB_H**	**$000000UU_B$**	**03_H**

7	...	2	1	0
Res			**PP9D**	**PP8D**
			rw	rw

Field	Bits	Type	Description
Res	7:2		**Reserved**
PP9D	1	rw	**PP9 direction** 0_B output 1_B input
PP8D	0	rw	**PP8 direction** 0_B output 1_B input

IO-Port 1 Data In Register

P1In	Offset	Wakeup Value	Reset Value
IO-Port 1 Data IN Register	92_H	$XXXXXXXX_B$	$XXXXXXXX_B$

7	6	5	4	3	2	1	0
PI1_7	PI1_6	PI1_5	PI1_4	PI1_3	PI1_2	PI1_1	PI1_0
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
PI1_7	7	r	**PP7 Data In**
PI1_6	6	r	**PP6 Data In**
PI1_5	5	r	**PP5 Data In**
PI1_4	4	r	**PP4 Data In**
PI1_3	3	r	**PP3 Data In**
PI1_2	2	r	**PP2 Data In**
PI1_1	1	r	**PP1 Data In**
PI1_0	0	r	**PP0 Data In**

IO-Port 3 Data In Register

P3In	Offset	Wakeup Value	Reset Value
IO-Port 3 Data IN Register	EC_H	$000000XX_B$	$000000XX_B$

7	2	1	0
Res		PI3_1	PI3_0
		r	r

Field	Bits	Type	Description
Res	7:2		**Reserved**
PI3_1	1	r	**PP9 Data In**
PI3_0	0	r	**PP8 Data In**

IO-Port 1 Data Out Register

P1Out	Offset	Wakeup Value	Reset Value
IO-Port 1 Data OUT Register	90_H	$UUUUUUUU_B$	FF_H

7	6	5	4	3	2	1	0
P1_7	P1_6	P1_5	P1_4	P1_3	P1_2	P1_1	P1_0
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
P1_7	7	rw	**PP7 Data Out**
P1_6	6	rw	**PP6 Data Out**
P1_5	5	rw	**PP5 Data Out**
P1_4	4	rw	**PP4 Data Out**
P1_3	3	rw	**PP3 Data Out**
P1_2	2	rw	**PP2 Data Out**
P1_1	1	rw	**PP1 Data Out**
P1_0	0	rw	**PP0 Data Out**

IO-Port 3 Data Out Register

P3Out	Offset	Wakeup Value	Reset Value
IO-Port 3 Data OUT Register	$B0_H$	$000000UU_B$	03_H

7	2	1	0
Res		P3_1	P3_0
		rw	rw

Field	Bits	Type	Description
Res	7:2		**Reserved**
P3_1	1	rw	**PP9 Data Out**
P3_0	0	rw	**PP8 Data Out**

IO-Port 1 Sensitivity Register

This register is used select the pull-up / pull-down functionality of the GPIOs. For proper usage of the pull-up / pull-down functionality check the settings of registers P1DIR and P1OUT and see **Table 23 “GPIO Port Configuration” on Page 147**.

P1SENS	Offset	Wakeup Value	Reset Value
IO-Port 1 Sensitivity Register	**93_H**	**$UUUUUUUU_B$**	**00_H**

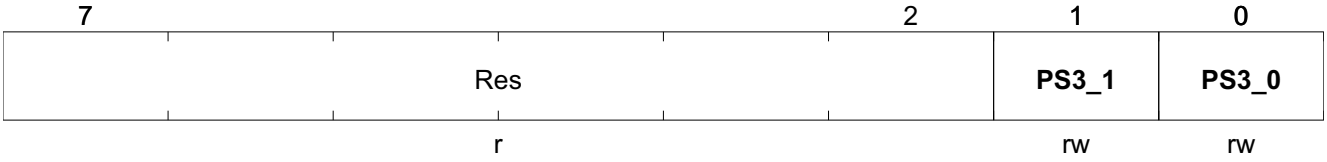
7	6	5	4	3	2	1	0
PS1_7	**PS1_6**	**PS1_5**	**PS1_4**	**PS1_3**	**PS1_2**	**PS1_1**	**PS1_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PS1_7	7	rw	**PP7 sensitivity** 0_B Pull-up 1_B Pull-down
PS1_6	6	rw	**PP6 sensitivity** 0_B Pull-up 1_B Pull-down
PS1_5	5	rw	**PP5 sensitivity** 0_B Pull-up 1_B Pull-down
PS1_4	4	rw	**PP4 sensitivity** 0_B Pull-up 1_B Pull-down
PS1_3	3	rw	**PP3 sensitivity** 0_B Pull-up 1_B Pull-down
PS1_2	2	rw	**PP2 sensitivity** 0_B Pull-up 1_B Pull-down
PS1_1	1	rw	**PP1 sensitivity** 0_B Pull-up 1_B Pull-down
PS1_0	0	rw	**PP0 sensitivity** 0_B Pull-up 1_B Pull-down

IO-Port 3 Sensitivity Register

This register is used select the pull-up / pull-down functionality of the GPIOs. For proper usage of the pull-up / pull-down functionality check the settings of registers P3DIR and P3OUT and see **Table 23 “GPIO Port Configuration” on Page 147**.

P3SENS	Offset	Wakeup Value	Reset Value
IO-Port 3 Sensitivity Register	**ED_H**	**$000000UU_B$**	**00_H**



Field	Bits	Type	Description
Res	7:2	r	**For future use**
PS3_1	1	rw	**PP9 sensitivity** 0_B Pull-up 1_B Pull-down
PS3_0	0	rw	**PP8 sensitivity** 0_B Pull-up 1_B Pull-down

2.16 I²C Interface

For communication between external hardware (like EEPROMs, remote I/O ports, LCD drivers, RAMs...) and the PMA51xx, an I²C master/slave interface is implemented. This interface is compatible to the I²C specification.

- PP1 is used as a Serial Data line (SDA)
- PP0 is used as a Serial Clock Line (SCL)
- In Idle Mode the I²C lines are weak high
- PMA51xx responds to the I²C- Address defined in SFR I2CM (reset value is $6C_H$) or to a general call if enabled by addressing slave address 00_H. General call is enabled by setting SFR bit I2CC.6[GCEn].
- The following data transfer rates according to I²C specification can be achieved
  - Slave Mode: Normal Mode (up to 100kbit/s) and Fast Mode (up to 400 kbit/s)
  - Master Mode: Normal Mode (up to 100 kbit/s)

Note: The I²C interface is used in DEBUG Mode, therefore it must not be reconfigured in DEBUG Mode. Furthermore debugging of the I²C interface itself is not possible and will lead to debugging errors.

2.16.1 Module Structure

Figure 58 points out the internal structure of the I²C-module. All activities are controlled by the Control Logic internal Control Finite State Machine (FSM). Control over the I²C bus pins is implemented in block Pin Control, responsible for start and stop bit detection and pin timing.

Besides the Control FSM the block Control Logic in addition comprises the communications timing (Timing & Delay) using the Baud rate Counter, the Bit Counter for counting incoming data bits and the Arbitration Logic for multi master operation.

The control logic internal FSM is controlled by the control register I2CC. Configuration information is given by the mode register I2CM (device address) and the baud rate register I2CB (determining the working speed of the I²C-bus). To provide information about appearing events and status information the status register I2CS is used.

The virtual register I2CD is used to store incoming and outgoing data bytes. Outgoing data bytes are moved from the internal register TX-Buffer to the Shift Register, incoming data bits are collected in the Shift Register and moved to RX-Buffer if a full byte has been received. If an address is received, this byte is compared to the device address in mode register I2CM.

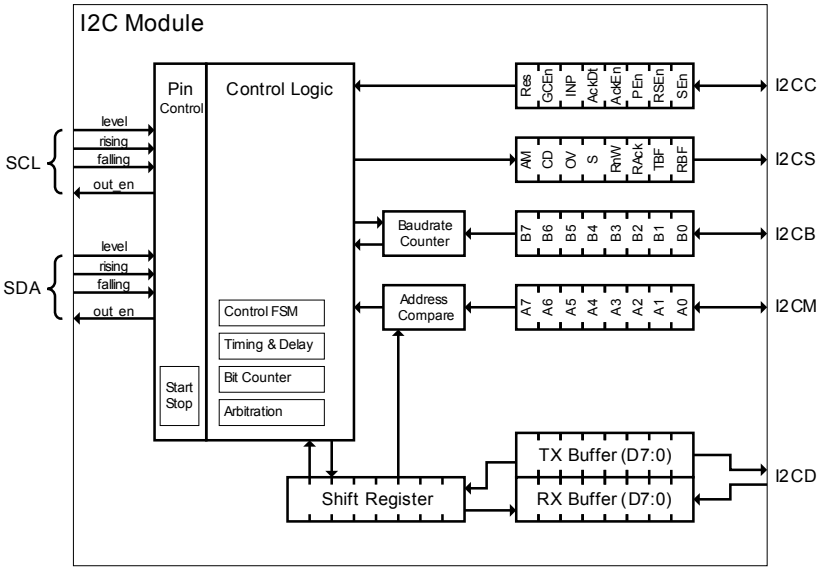


Figure 58 I²C module structure

2.16.2 I²C Programming Instructions

To enable the I²C-bus interface SFR bit CFG1.6 [I2CEn] has to be set. Further settings has to be done to prepare the I²C-module for master or slave operation.

- Configure the device by setting register I2CC. General calls can be enabled by setting bit I2CC.6[GCEn], the service request mechanism (polling/interrupt mode) has to be decided via bit I2CC.5[INP].
- Enter the device address in mode register I2CM. If no changes are done the I²C-bus matches to the predefined address $6C_H$.
- The baud rate register I2CB has to be set according to the used mode and to the demands of transmission speed. In master mode the register has to be set to a maximum transfer rate proportional value.

According to the settings and according to the sequence handling mode (polling or interrupt mode) differing programming instructions have to be executed.

2.16.2.1 Slave Mode Sequence (Polling Mode)

Once the I²C-bus module has been enabled and configured to polling mode by setting bit I2CC.5[INP] to 0_B, the I²C interface waits for a start condition to occur. Subsequently the following 8 bits (7 bits address, 1 bit RnW) are shifted into an internal shift register and compared to the internal device address. When the address matches the hardware automatically generates an acknowledge and bit I2CS.7[AM] is set. Together with the address the direction bit RnW is transferred. According to its value (stored in bit I2CS.3[RnW]) different actions has to be set:

Receive I²C-data

- If bit I2CS.0[RBF] is set a data byte has been shifted in and transferred to the internal RX-Data register. The received byte is ready to be read out. An acknowledge is automatically set by hardware as long as no receive buffer overflow (bit I2CS.5[OV] in status register) has occurred.
- If bit I2CS.4[S] is set a stop condition has occurred and the transmission is closed.
- If bit I2CS.7[AM] is set a restart condition has been set on I²C-bus and a matching address has been transmitted. In case of a write access a branch to the transmit data subroutine has to be performed.

Transmit I²C-data

- In the transmit data subroutine the data to be transmitted first has to be written to register I2CD. I2CS.1[TBF] is set until the byte is transferred to the shift register and transmission is started physically - I2CS.1[TBF] is cleared again and new data can be written to I2CD. If no data byte is provided, the I²C clock line SCL is held low by the slave (the bus is blocked).
- If bit I2CS.4[S] is set, the transmission process has been terminated by the master and the transmission subroutine may be left.

2.16.2.2 Slave Mode Sequence (Interrupt Mode)

Interrupt handling is enabled by setting bit I2CC.5[INP] to 1_B. With every interrupt event the software routine restarts at the entry point of the I²C interrupt service routine, so the actual state and the cause for this interrupt has to be identified before continuing with the next step. Compared to the polling mode differing status information are needed for this non sequential handling and should be handled the following way:

- If I2CS.4[S] is set to 1_B the transfer is still active, otherwise it has been terminated.
- If I2CS.7[AM] is set, the I²C interface has been addressed as slave device (slave interrupt), otherwise a master interrupt request is pending.
- If I2CS.6[CD] is set an unexpected start or stop condition has been detected if the device has been addressed as slave device - or if acting as master device a collision has been detected on I²C bus (arbitration).
- If I2CS.3[RnW] is set, a read sequence is executed and the I²C slave device has to provide data by writing to register I2CD, otherwise a write sequence is executed and data are provided within register I2CD.

- If a write sequence is executed and I2CS.0[RBF] is set, then the received data can be read from I2CD - otherwise the address byte can be read from I2CD to decide whether to handle a general call (if enabled with I2CC.6[GCEn]) or a slave transfer.

I^2C slave interrupts are generated on following events:

- If a general call has been received
- If data are received and ready to be read out from I2CD.
- If data have to be transmitted and are required in I2CD.
- If the transfer has been stopped by a stop condition or by an unexpected start or stop condition.

2.16.2.3 General Call Sequence

If a general call address is sent and bit I2CM.6[GCEn] is set the I^2C bus behaves like a slave receiver, i.e. a slave mode sequence procedures may be taken. The general call protocol handling has to be done by software.

2.16.2.4 Master Mode Sequence (Polling Mode)

After enabling the I^2C-bus module the I^2C device behaves like a slave. If I^2C bus is free of communication a master transfer can be initiated by writing an address byte (including the access direction bit RnW) to I2CD and setting a start condition with bit I2CC.0[SEn]. The start condition and the following address byte is transmitted immediately on SCL and SDA. An existing I^2C device with fitting device address will then respond with an acknowledge. If the polling mode was enabled by setting bit I2CC.5[INP] to 0_B bit I2CS.3[RAck] will then be set accordingly. Consecutively the master may transmit (write data to I2CD) or receive data (read data from I2CD after reception) according to the transmitted RnW bit.

Receive I^2C-data

After data reception (I2CS.0[RBF] is set) the master has to set an acknowledge. This is done by setting bit I2CC.4[AckEn] and bit I2CC.5[AckDt].

Transmit I^2C-data

After writing data to register I2CD they are transmitted. If finished the master will be informed with I2CS.3[RAck] if the data have been acknowledged.

If no more data are needed to be transmitted/received the master can stop the transfer by setting a stop condition with bit I2CC.3[PEn] - or continue with a new transfer by setting a restart condition with bit I2CC.2[RSEn]. If a stop condition is issued bit I2CS.4[S] is set again. In multi master mode also pay attention to collision detection indicated by bit I2CS.6[CD].

2.16.2.5 Master Mode Sequence (Interrupt Mode)

Contrary to the master mode sequence in polling mode the I^2C bus handling in interrupt mode has to be included in the slave mode interrupt sequence due to the non sequential interrupt handling. Nevertheless the master mode sequence has to be started by providing address information in I2CD and a start condition enable by setting bit I2CC.0[SEn]. Handling of the I^2C transfer is then done in the interrupt service routine doing the following checks:

- If I2CS.4[S] is set to 1_B the transfer is still active, otherwise the stop condition has terminated the transfer.
- If I2CS.7[AM] is set, the I^2C interface has been addressed as slave device (slave interrupt), otherwise a master interrupt request is pending.
- If I2CS.6[CD] is set a collision has been detected on I^2C bus (arbitration) and an other master device took over the control.
- If I2CS.3[RnW] is set, a read sequence has been started and the I^2C master device has to read the received data from register I2CD and provide acknowledge information writing I2CC.4[AckDt] and I2CC.3[AckEn].

- If I2CS.3[RnW] is not set, a write sequence has been started. According to the received acknowledge information provided by I2CS.2[RAck] data have to be provided by writing register I2CD or transfer has to be terminated generating a stop condition with I2CC.2[PEn] or a restart condition with I2CC.1[RSEn].

I^2C master interrupts are generated on following events:

- If the I^2C device has been addressed a slave interrupt is received (master acting as slave).
- If a bus collision has occurred.
- If data (or slave address) has been transmitted. Received acknowledge information can be read and further steps can be decided writing to I2CC. New data to transmit can be provided by writing to I2CD.
- If data have been received. Acknowledge information should be provided by the master interface and further steps can be decided by writing to I2CC. Data can be read from register I2CD.

2.16.3 Register Description

Table 26 Registers Overview

Register Short Name	Register Long Name	Offset Address	Wakeup Value	Page Number
I2CD	I2C Data Register	$9A_H$	00_H	162
I2CS	I2C Status Register	$9B_H$	00_H	163
I2CC	I2C Control Register	$A2_H$	00_H	161
I2CM	I2C Mode Register	$A3_H$	$6C_H$	162
I2CB	I2C Baud rate Register	$B1_H$	00_H	160

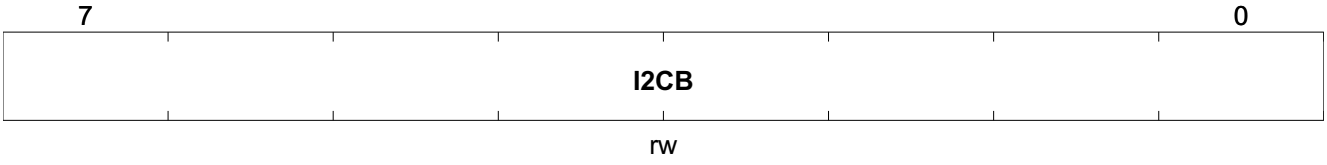
I²C Baud rate Register

This register is used to control the I²C-bus transmission speed in master mode. In slave mode this register is used to determine the data setup time after SCL hold (delay by slave). The value can be calculated by the equation shown in Figure 59.

$$I2CB = SCL_{high}[s] \cdot (\frac{f_{SYS}[Hz]}{2}) - 1$$

Figure 59 Calculation of I²C baud rate

I2CB	Offset	Wakeup Value	Reset Value
I2C Baud rate Register	$B1_H$	00_H	00_H



Field	Bits	Type	Description
I2CB	7:0	rw	**I2C Baud rate Register** Data transfer rate compliant value for SCL hold time (master behavior) or data setup time after SCL hold (slave behavior).

I²C Control Register

I2CC	Offset	Wakeup Value	Reset Value
I2C Control Register	$A2_H$	00_H	00_H

7	6	5	4	3	2	1	0
Res	**GCEn**	**INP**	**AckDt**	**AckEn**	**PEn**	**RSEn**	**SEn**
	rw	rw	rw	rw	rw	rw	rw

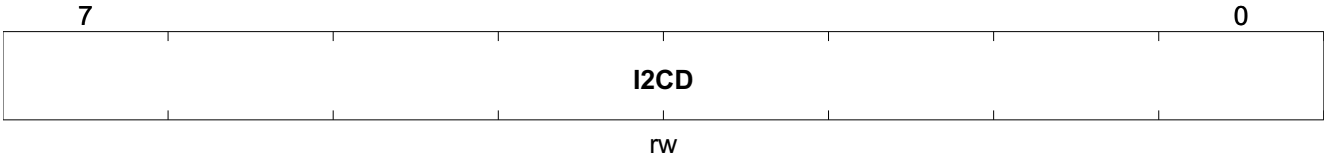
Field	Bits	Type	Description
Res	7		**Reserved**
GCEn	6	rw	**General Call Enable** 0_B General Call disabled 1_B General Call enabled, if bit CFG1.6[I2CEn] is set
INP	5	rw	**Mode selection (interrupt / not polling)** Selection of the I²C mode. The behavior of the I²C Status Register (SPIS) changes accordingly. 0_B Polling mode 1_B Interrupt mode
AckDt	4	rw	**Acknowledge data** Provides acknowledge information if acknowledge is set by I2CC.3[AckEn] in master mode. 0_B Give a not Acknowledge on incoming data 1_B Acknowledge incoming data
AckEn	3	rw	**Acknowledge sequence enable** Sets acknowledge information defined in I2CC.4[AckDt] on I2C bus in master mode. This bit is automatically reset by hardware afterwards. 0_B Idle 1_B Acknowledge data defined in AckDt is sent
PEn	2	rw	**Stop condition enable** Initiates a stop condition on the correct position in the transmission frame in master mode. This bit is automatically reset by hardware afterwards. 0_B Idle 1_B Set stop condition
RSEn	1	rw	**Restart condition enable** Initiates a restart condition on the correct position in the transmission frame in master mode. If commonly set with stop condition the stop condition is executed. This bit is automatically reset by hardware afterwards. 0_B Idle 1_B Set restart condition

Field	Bits	Type	Description
SEn	0	rw	**Start condition enable** Initiates a start condition on the correct position in the transmission frame in master mode. This bit is automatically reset by hardware afterwards. 0_B Idle 1_B Set start condition

I²C Data Register

RX-Buffer and TX-Buffer are two data transmission registers that are accessible by the virtual register I2CD. If read, the content of the RX-Buffer is provided, if written the TX-Buffer is filled.

I2CD	Offset	Wakeup Value	Reset Value
I2C Data Register	**$9A_H$**	**00_H**	**00_H**

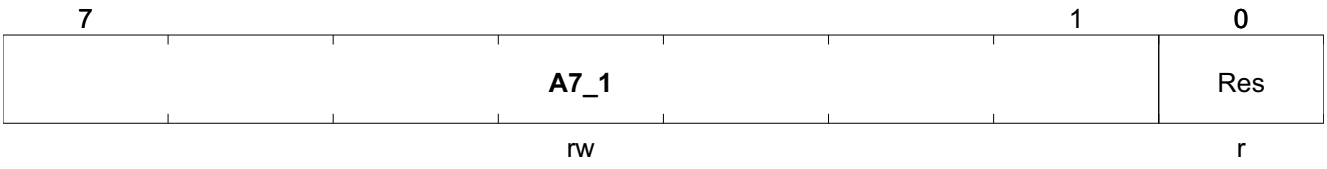


Field	Bits	Type	Description
I2CD	7:0	rw	**I2C Data Register** Provide access to TX-Buffer if written and RX-Buffer if read.

I²C Mode Register

This register is used to set the I²C address of the PMA51xx.

I2CM	Offset	Wakeup Value	Reset Value
I2C Mode Register	**$A3_H$**	**$6C_H$**	**$6C_H$**



Field	Bits	Type	Description
A7_1	7:1	rw	**I2C Address bit 7 down to bit_1**
Res	0	r	**I2C Address Bit 0** This bit is fixed to 0_B

I²C Status Register

I2CS	Offset	Wakeup Value	Reset Value
I2C Status Register	$9B_H$	00_H	00_H

7	6	5	4	3	2	1	0
AM	**CD**	**OV**	**S**	**RnW**	**RAck**	**TBF**	**RBF**
rc	rc	rc	rc	r	r	r	r

Field	Bits	Type	Description
AM	7	rc	**Address matched / Slave transfer** Polling mode (I2CC.5[INP] is set to 0_B): Set if received device address matches with received address byte (corresponding to 7-bit or 10-bit addressing mode). Interrupt mode (I2CC.5[INP] is set to 1_B): Set while PMA51xx has been addressed as slave device. This bit is automatically reset by hardware when the transfer is stopped. 0_B Idle 1_B Address matched (polling) / Slave transfer (interrupt)
CD	6	rc	**Collision detected** If master transfer is executed, this bit is set if a collision was detected. If a slave transfer is executed, this bit is set if an unexpected start/stop condition occurs during address/data transfer. 0_B Idle 1_B Collision detected
OV	5	rc	**Overflow** Set if new data have been received and old data in the RX-Buffer (I2CD register) were not read. Set if data are still pending in the TX-Buffer when new data are written into I2CD. 0_B Idle 1_B Buffer overflow detected
S	4	rc	**Stop bit detected / Transfer active** Polling mode (I2CC.5[INP] is set to 0_B): Set if stop condition has been detected. Interrupt mode (I2CC.5[INP] is set to 1_B): Set as long as an ongoing transfer is detected. 0_B Idle 1_B Stop bit detected (polling) / ongoing transfer (interrupt)
RnW	3	r	**Read / not write bit information** Contains the type of transfer. If master transfer is executed this bit is automatically captured on sending the address. If a slave transfer is executed this bit is captured on receiving the address. 0_B Write transfer (slave-receiver / master-transmitter) 1_B Read transfer (slave-transmitter / master-receiver)

Field	Bits	Type	Description
RAck	2	r	**Received acknowledge level** Contains the level of the received acknowledge. 0_B Received NOT acknowledge (nACK) 1_B Received acknowledge (ACK)
TBF	1	r	**Transmit buffer full** Set if register I2CD is written. Cleared by hardware if the TX-Buffer is moved to the shift register, thus the data byte is transmitted. 0_B Transmit buffer empty 1_B Transmit buffer full
RBF	0	r	**Receive buffer full** Set if the content from the shift register is moved to the RX-Buffer, thus data byte is received. Cleared by hardware if register I2CD is read. 0_B Receive buffer empty 1_B Receive buffer full

2.17 SPI Interface

The Serial Peripheral Interface (SPI) is a very simple synchronous interface to transfer data on a serial bus, connecting an intelligent master controller with general-purpose slave circuits such as slave controller, RAMs, memories, and so on. A simple 2-wire (half-duplex mode) or 3-wire (full-duplex mode) bus is used for communication.

- High-speed synchronous data transfer
- Four programmable bit rates through prescaler
- 2-wire bus for half-duplex transmission; a serial clock line (SPI_Clk) and concatenated data line (SPI_MISO,SPI_MOSI)
- 3-wire bus for full-duplex transmission; a serial clock line (SPI_Clk) and two serial data lines (SPI_MISO,SPI_MOSI)
- A 4-wire bus for full-duplex transmission plus handshaking can be implemented by also utilizing the Chip Select (SPI_CS). This pin can be used for indicating the beginning of a new byte sequence.
- Master or Slave Operation
- Clock Control - Polarity (idle low/high) and phase (sample data with rising/falling clock edge) are programmable
- Bit Width (1 to 8 bits) and Bit Order (MSB or LSB first) are configurable
- Compatible with SSC (High-Speed Synchronous Serial Interface) and standard SPI interfaces
- Protocol is defined by software

2.17.1 SPI Functionality

The basic interaction principle between master and slave SPI devices is shown in **Figure 60**. Writing to the SPI shift register of the master SPI device starts the SPI clock generation (line SCK). The two 8 bit shift registers in master and slave device can be considered as one distributed circular shift register (including line MISO and MOSI). When data is shifted from the master to the slave with the generated clock, data is also shifted in the opposite direction simultaneously. During one shift cycle, data in the master and the slave is interchanged resulting a full duplex transmission.

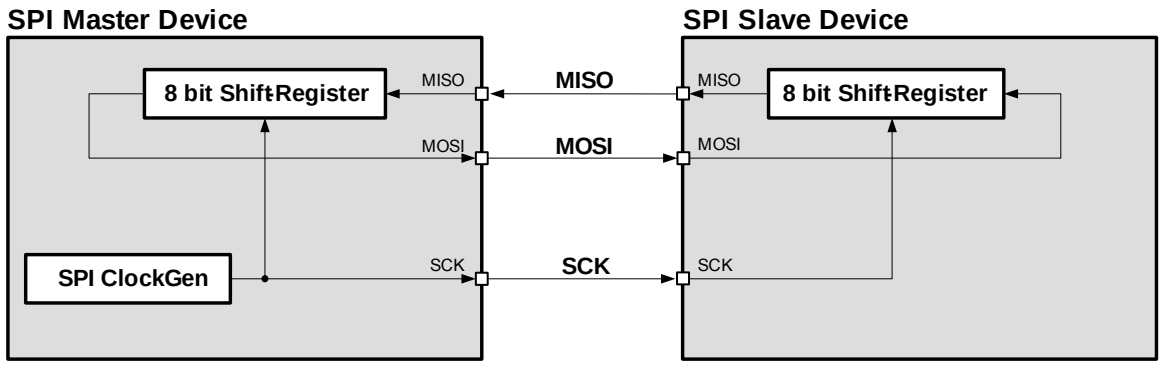


Figure 60 SPI principle

Different SPI devices are connected through three lines. The definition of these lines is always determined by the master. The line connected to the master's data output is the transmit line MOSI[1)], the receive line is connected to its data input line MISO[2)]. The serial clock is distributed over line SCK[3)]. Only the device selected for master operation generates and outputs the serial clock. All slaves receive and react to this clock.

1) MOSI = Master Out Slave In
2) MISO = Master In Slave Out
3) SCK = Serial clock

The output of the master's shift register is connected to the external transmit line, which in turn is connected to the slaves' shift register input (MOSI). The output of the slaves' shift register is connected to the external receive line in order to enable the master to receive the data shifted out of one slave (MISO). The external connections are hard-wired, the function and direction of the pins are determined by configuration as master- or slave device.

When initializing the devices select only one device for master operation, all others must be programmed for slave operation. Initialization includes the operating mode (clock phase, clock polarity, data byte order, bit width and transfer rate). To deselect the actual master (slave-select functionality) and re-establish connection with another master, a corresponding protocol has to be fulfilled by software using an additional free port pin.

To avoid collisions on line MISO due to several slave devices, only one slave is allowed to pull the line to low (wired AND connection), i.e. enables the driver of its pin. Only this slave can put its data onto the master's receive line and only receiving of data from the master is possible. The master selects the slave device from which it expects data either by separate select lines (free port lines), or by using a suitable protocol to tell all the other slave devices to only output state high on line MISO.

According to the hard-wired connection, two different operation modes are possible - Full-Duplex and Half-Duplex operation.

2.17.1.1 Full-Duplex Operation

The master device line MOSI (master out) is connected to line MOSI of all slave devices (slave in). Accordingly line MISO is connected between master and slave devices. Additionally to this two data lines the clock line SCK has to be wired respectively. This way data are transmitted across a 3-wire bus in full duplex mode (refer to **Figure 61**). Data bytes are transmitted from master to slave and simultaneously from slave to master.

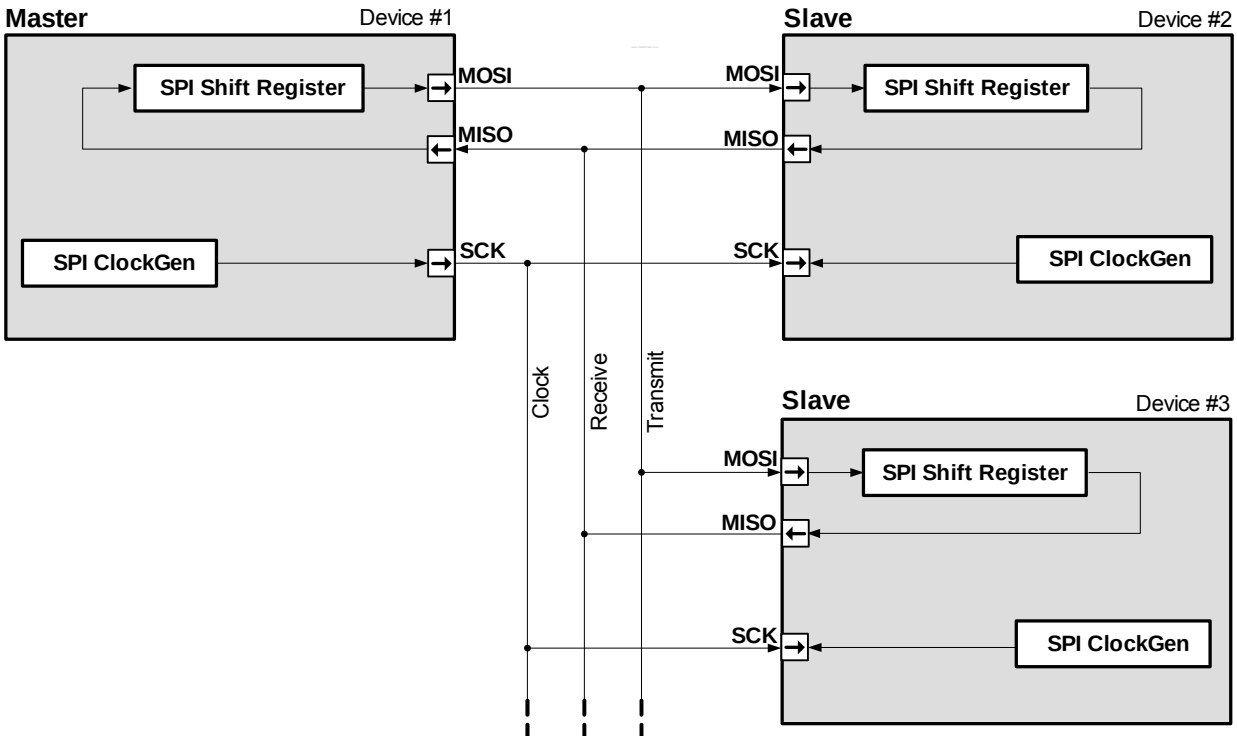


Figure 61 Full-Duplex configuration

2.17.1.2 Half-Duplex Operation

In a Half-Duplex configuration only one data line is necessary for both receiving and transmitting data. **Figure 62** shows, that line MISO and MOSI of each master and slave device is shortened to one data line. The clock line SCK is connected exclusively. The master device controls the data transfer by generating the shift clock, while the slave device receives it.

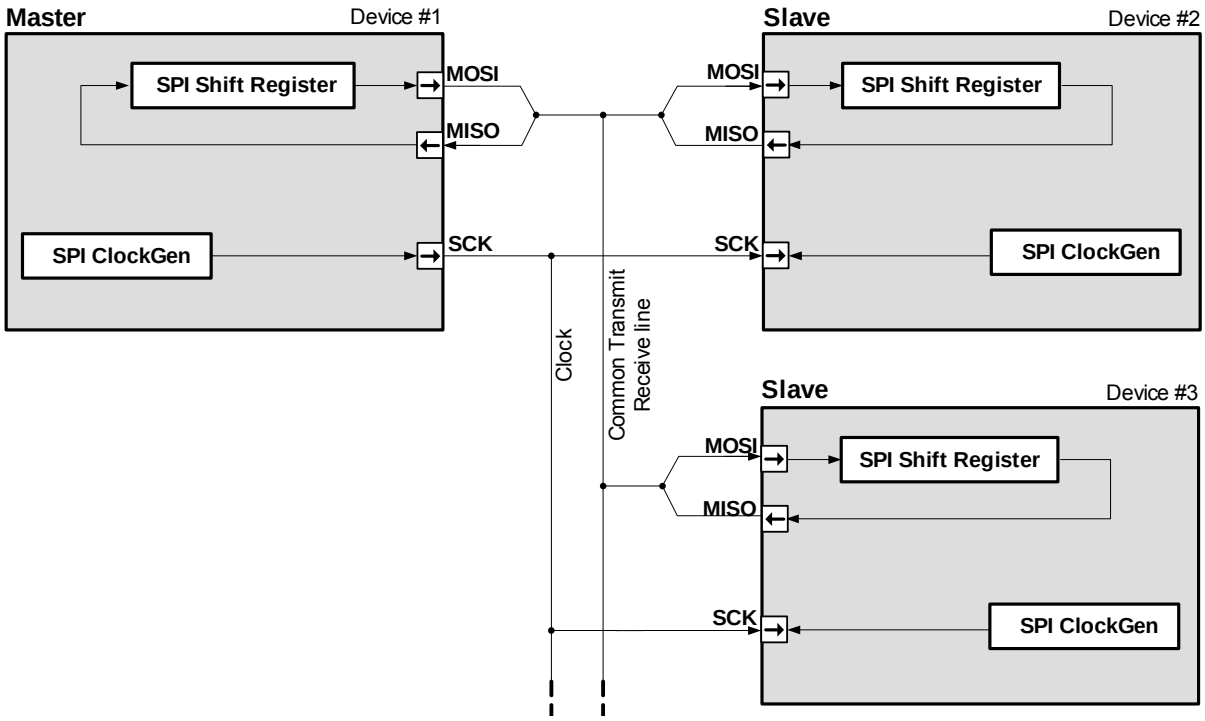


Figure 62 Half-Duplex Configuration

Due to the fact that all transmit and receive pins are connected to one data line, an appropriate protocol has to be used to avoid collisions, i.e. only one device (master or slave) may transmit data unidirectional, all other (arbitrary) devices are only allowed to receive these data (therefore the shift register has to contain FF_H). Because line MISO and MOSI of each device is shortened, the transmitting device will clock its own data at the input pin. By these means any corruptions on the common data exchange line are detected.

2.17.1.3 Data Modes

There are four combinations of SCK phase and polarity with respect to serial data, which is determined by control bits SPIC.2[CPHA] and SPIC.3[CPOL] (refer to **Figure 63**). Additionally the data order (bit SPIC.5[DORD]) (MSB-first or LSB-first) and the data width (bit SPIM.2:0[DWS]) (variable from 1 to 8 bits) may be changed.

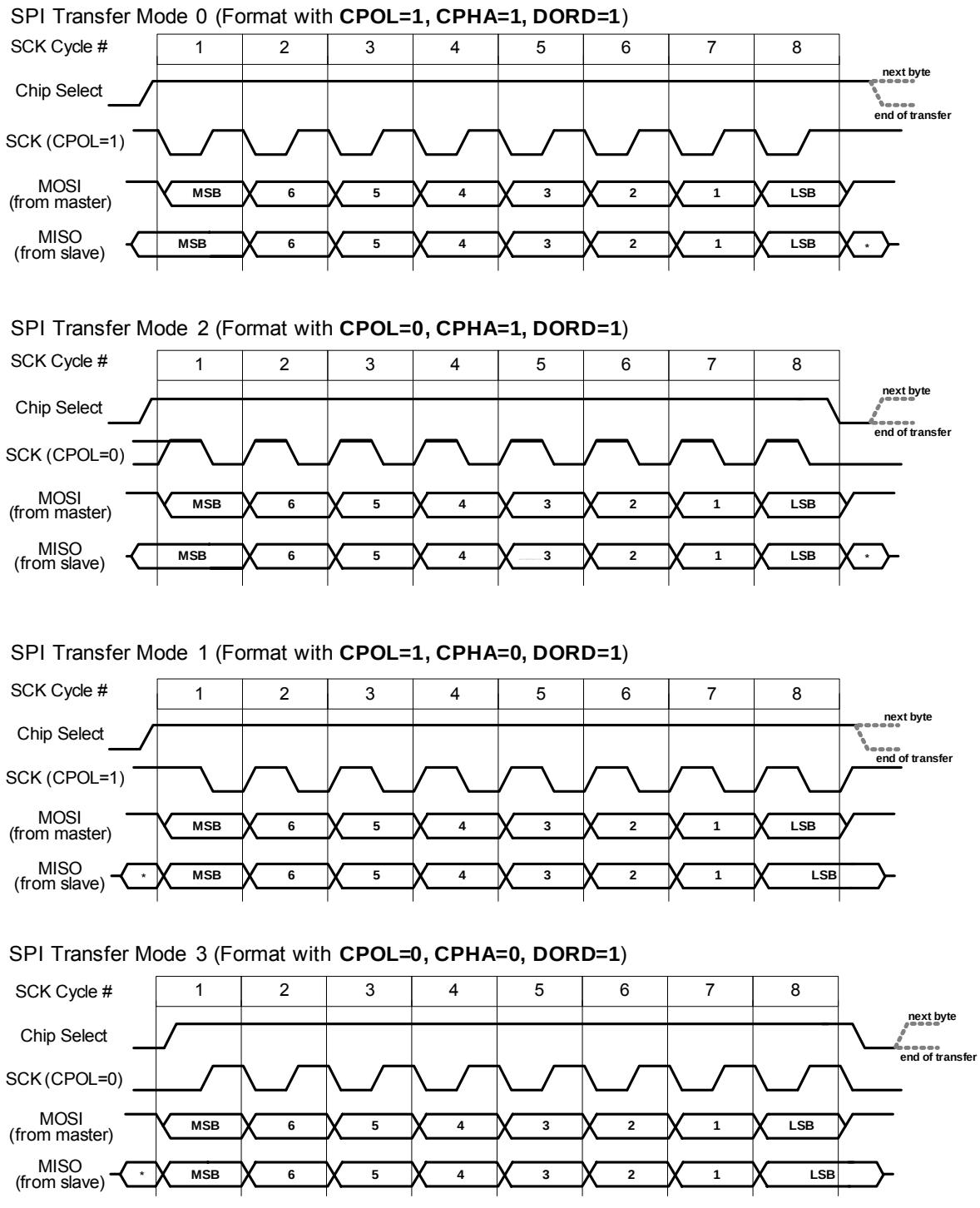


Figure 63 SPI data modes

2.17.2 Module Structure

Figure 64 points out the main blocks inside the SPI module. The Pin Control block separates and assigns incoming and outgoing SPI signals. According to this signals and the configurations done in SPI control register (SPIC) and SPI mode register (SPIM) the SPI Control block coordinates Shift Register shift-in and shift-out.

The Clock Control block is only relevant in SPI master mode: the SPI clock is generated by the internal baud rate timer. The baud rate timer is a 8 bit down counter, its overrun toggles the SPI clock.

Transmit Buffer and Receive Buffer are used to store incoming and outgoing data bytes. Outgoing data bytes are first transferred from Transmit Buffer to the Shift Register that dispenses bit by bit in compliance to the data order (MSB or LSB first) set by bit SPIC.5[DORD]. At start of a frame 2 bytes can be written into the TX buffer. First is moved through TX buffer into Shift register. Second byte is hold in TX buffer until first byte was sent.

Incoming data bits are collected in the Shift Register. If all bits are received - the exact amount is defined by SPIM.2-0[DWS2-0] - the whole byte is moved to Receive Buffer.

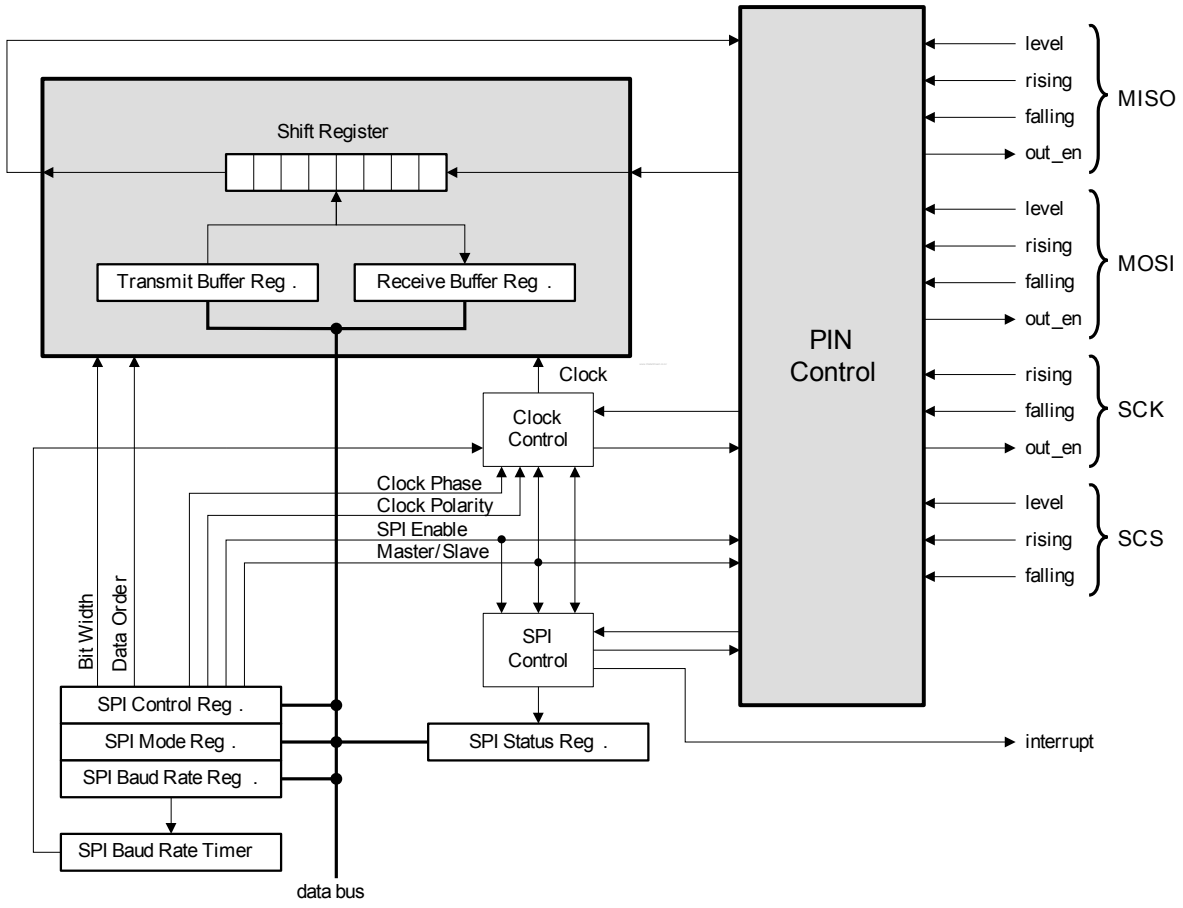


Figure 64 SPI module structure

2.17.3 Interrupt Support

Six events generates an interrupt. First three sources are normal operating interrupts, last three are failures:

- Receive Buffer Full (SPIS.1[SRBF]) and Reload TX buffer as one single event because of SPI behavioral.
- Chip select (SPI_CS) detected (SPIS.3[SCSD]) (Slave Mode only).
- Chip select (SPI_CS) lost and the last word was transferred completely (Slave Mode only).
- Receive Buffer Overrun (SPIS.7[SRE]) (data lost) detected.
- Phase Error detected (SPIS.5[SPE]).

- Slave Communication Corrupt detected (SPIS.4[SSCC]). In this case the Slave Select was lost within a word (Slave Mode only).

All these interrupt source bits are located in the status register (SPIS) and will be cleared on read access. A read access to status register acknowledges the interrupt.

It is not possible to mask one or more of these interrupt sources individually, only all SPI interrupts can be masked by setting SFR bit IE.5 [ESPI] to 0_B.

2.17.4 SPI Programming Instructions

To enable the SPI-bus interface bit CFG1.2[SPIEn] has to be set. Resume with setting correct configuration in control and mode register (SPIC and SPIM).

2.17.4.1 Slave Mode Sequence

Once the SPI interface has been enabled, configured as slave, and selected via chip select (SPI_CS/PP3), it waits for incoming data, which are shifted-in synchronously to the delivered SPI clock. There are two possibilities to select the slave:

1. The SPI slave is selected by the master via an hard-wired signal connected to SPI_CS/PP3.
2. The SPI slave sets the chip select to 0_B by setting PP3 direction to output and PP3 to 0_B.

After all bits has been transmitted, bit SPIS.1[SRBF] is set and the data can be read out from register SPID. If data should be (according to the realized protocol) transmitted simultaneously to the next incoming data byte, simply write the desired byte to the SPI data register SPID.

2.17.4.2 Master Mode Sequence

After enabling the SPI interface and configuration as master device it waits for further actions. Data are transmitted/received as soon as the SPI data register SPID is written. If more than one data byte has to be transmitted keep in mind to check bit SPIS.0[STBF] to not overwrite the old data byte. In full duplex mode data bytes are simultaneously received from slave devices. If a byte has to be read according to the implemented protocol simply check bit SPIS.1 [SRBF] in status register and read out the received value from register SPID.

2.17.5 Register Description

Table 27 Registers Overview

Register Short Name	Register Long Name	Offset Address	Wakeup Value	Page Number
SPIB	SPI Baud rate Register	$F3_H$	00_H	171
SPIC	SPI Control Register	$F4_H$	00_H	172
SPID	SPI Data Register	$F5_H$	00_H	173
SPIM	SPI Mode Register	$F6_H$	00_H	173
SPIS	SPI Status Register	$F7_H$	41_H	175

SPI Baud rate Register

The internal baud rate timer is needed only in master mode. It is implemented as 8-bit down counter. The Register SPIB holds counter's reload value. A underrun from 00_H to FF_H initiates both timer reload and a SPI clock event. This SPI clock event generates either a rising or falling edge on the SPI clock line. For a full SPI clock cycle two SPI clock events are necessary.

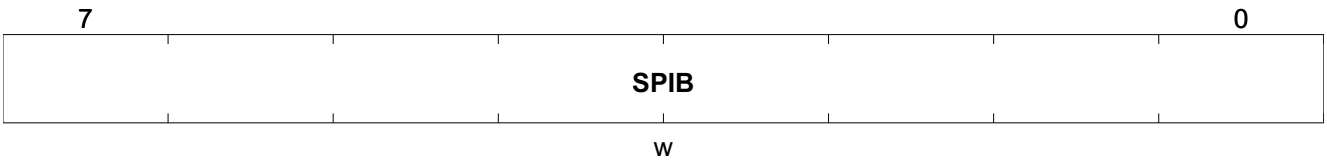
The baud rate can be calculated by the formula shown in **Figure 65**.

$$f_{SPI}[Hz] = \left(\frac{f_{SYS}[Hz]}{(SPIB + 1) \cdot 2} \right)$$

Figure 65 Calculation of SPI baud rate

All reload values for SPIB from 00_H to FF_H are valid.

SPIB	Offset	Wakeup Value	Reset Value
SPI Baud rate Register	**$F3_H$**	**00_H**	**00_H**



Field	Bits	Type	Description
SPIB	7:0	w	**SPI Baud rate Register** Reload value for baud rate timer

SPI Control Register

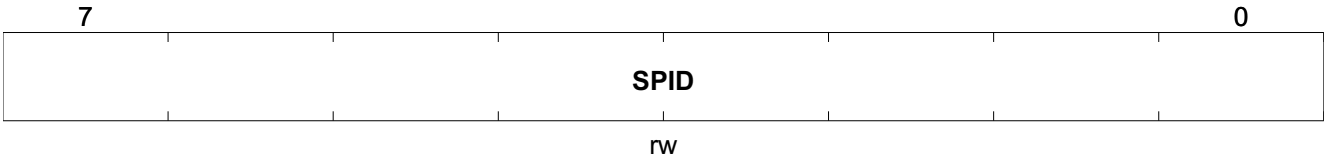
SPIC	Offset	Wakeup Value	Reset Value
SPI Control Register	$F4_H$	00_H	00_H

7	6	5	4	3	2	1	0
Res	CSEn	DORD	MSTR	CPOL	CPHA	Res	
	rw	rw	rw	rw	rw		

Field	Bits	Type	Description
Res	7		**Reserved**
CSEn	6	rw	**Chip select enable (slave mode only)** Resets the internal FSM if CS is lost during transmission in slave mode. 0_B Disable SPI chip select 1_B Enable SPI chip select
DORD	5	rw	**Data order** Defines the bit order for transmission. 0_B LSB is transmitted first 1_B MSB is transmitted first
MSTR	4	rw	**Master/Slave select** Defines if the module operates as master or slave device. 0_B Slave (controls SPI_MISO) 1_B Master (controls SPI_MOSI, SPI_Clk)
CPOL	3	rw	**Clock polarity selection** Defines the initial state of SPI clock line. 0_B Idle clock line is low and leading clock edge is a low to high transition. 1_B Idle clock line is high and leading clock edge is a high to low transition.
CPHA	2	rw	**Clock phase selection** Determines whether data are active with rising or falling edge of SPI clock line. 0_B Transmission starts without a rising or falling edge on SPI clock. With first edge detected the first data bit is latched, with the following edge data are shifted. 1_B A rising or falling edge is generated on SPI clock line before data are set. With the following clock edge data are latched before shifted on with consecutive one.
Res	1:0		**Reserved**

SPI Data Register

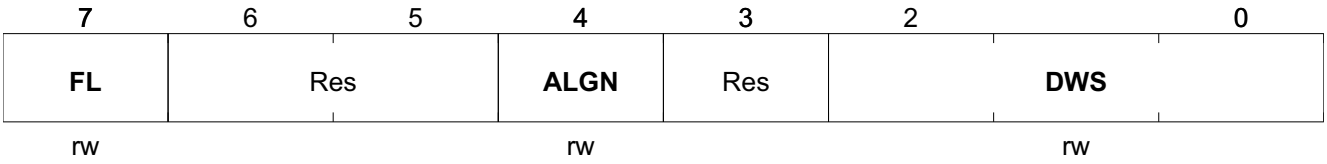
SPID	Offset	Wakeup Value	Reset Value
SPI Data Register	$F5_H$	00_H	00_H



Field	Bits	Type	Description
SPID	7:0	rw	**SPI Data Register** Read from RX buffer and write to TX buffer

SPI Mode Register

SPIM	Offset	Wakeup Value	Reset Value
SPI Mode Register	$F6_H$	00_H	00_H



Field	Bits	Type	Description
FL	7	rw	**SPI force level** Select output mode for SPI lines SPI_MISO, SPI_MOSI and SPI_Clk. 0_B SPI lines are pull-up driven weak high level 1_B SPI lines are active driven high level
Res	6:5		**Reserved**
ALGN	4	rw	**Data alignment** Defines the bit alignment for SPI transmission. This is only relevant in case, data width selection is not 8 bits (see DWS). 0_B Right align 1_B Left align
Res	3		**Reserved**

Field	Bits	Type	Description
DWS	2:0	rw	**Data width selection** Defines the number of transmitted bits per byte. 000_B 8 bits 001_B 1 bit 010_B 2 bits 011_B 3 bits 100_B 4 bits 101_B 5 bits 110_B 6 bits 111_B 7 bits

SPI Status Register

SPIS	Offset	Wakeup Value	Reset Value
SPI Status Register	$F7_H$	41_H	41_H

7	6	5	4	3	2	1	0
SRE	STE	SPE	SSCC	SCSD	SCSL	SRBF	STBE
rc	r	rc	rc	rc	rc	rc	r

Field	Bits	Type	Description
SRE	7	rc	**SPI receive error** Is set by hardware if a new data frame is completely received but the previous data was not read out from the receive data buffer SPID (data will be overwritten). This bit acts as interrupt request flag. It is cleared by hardware on read access. 0_B Normal state 1_B Error occurred
STE	6	r	**SPI transmission completed** This bit is set if the SPI transmission has been completed. 0_B Transmission running 1_B Transmission completed
SPE	5	rc	**SPI phase error** Is set by hardware if the incoming data at pin MISO (master mode) respectively MOSI (slave mode) sampled with CPU clock, changes between 1 sample before and 2 samples after latching edge of the clock signal. This bit acts as interrupt request flag. It is cleared by hardware on read access. 0_B Normal state 1_B Phase error detected
SSCC	4	rc	**SPI Slave communication corrupted** Set by hardware if the chip select is lost during transmission (in slave mode only). This bit acts as interrupt request flag. It is cleared by hardware on read access. 0_B Normal state 1_B Transmission corrupted
SCSD	3	rc	**SPI chip select detected** Set by hardware in slave mode only if an falling edge is detected on SPI-CS pin (SPI transmission start). This bit acts as interrupt request flag. It is cleared by hardware on read access. 0_B Inactive 1_B Chip select detected (falling edge on chip select detected)

Field	Bits	Type	Description
SCSL	2	rc	**SPI chip select lost** Set by hardware in slave mode if a rising edge is detected on SPI-CS. This bit acts as interrupt request flag. It is cleared by hardware on read access. 0_B Inactive 1_B Chip select lost (rising edge on chip select detected)
SRBF	1	rc	**SPI receive buffer full** Is set by hardware if a data byte is received completely. The receive buffer (SPID) is ready to be read. This bit acts as interrupt request flag. It is cleared by hardware on read access. 0_B No new data in receive buffer 1_B New data in receive buffer
STBE	0	r	**SPI transmit buffer empty** Is reset by hardware if register SPID is written and automatically set if data byte is transferred to SPI internal shift register. 0_B There are still data in transmit buffer 1_B Transmit buffer is empty

2.18 PROGRAMMING Mode Operation

In PROGRAMMING mode, the PMA51xx is accessible as a slave using the I²C Interface.

The device uses the internal 12 MHz RC HF oscillator as its clock source.

To avoid programming failures, all PROGRAMMING mode commands are protected by a 16-bit CRC at the end of each command (**Chapter 2.12** shows details about the CRC polynomial used).
The checksum has to be calculated over all bytes in the command excluding the PMA51xx I²C device address. **Figure 66 "Legend for I²C-Commands in PROGRAMMING mode" on Page 177** shows the legend used for the description of the I²C commands.

PROGRAMMING mode Commands

- FLASH Write Line
- FLASH Erase
- FLASH Check Erase Status
- FLASH Read Line
- FLASH Set Lockbyte 3
- FLASH Read Status

	from programmer to PMA	**S**	start condition
	from PMA to programmer	**P**	stop condition
CRCH	MSB of CRC checksum	**SR**	restart condition or stop / start condition
CRCL	LSB of CRC checksum	**A**	acknowledge
Data0-31	data which is written into / read from FLASH	**nA**	not acknowledge
Pause	Time where no communication is allowed	**Sector**	selection of the sector
Status	Status byte		

Figure 66 Legend for I²C-Commands in PROGRAMMING mode

2.18.1 FLASH Write Line

The FLASH Write Line command writes 32 bytes to the FLASH. The FLASH Code Sector and FLASH User Data Sectors can be written using this command. The start address has to be a multiple of 20_H. As shown in **Figure 12** FLASH address range 4000_H to $587F_H$ is accessible.

This command should only be used if the FLASH line is fully erased. If an already programmed FLASH line gets overwritten (without being erased first) the resulting data is undefined. After the stop condition (P) is received the data is programmed into the FLASH. During the programming time incoming I²C commands are not acknowledged. Programming time is specified in **Table 46**. **Figure 67** shows the structure of the FLASH Write Line command. It is important to note that no type of *verification* is performed after a write. In order to see if this write command was successful, a **Read Status** command must be issued, or a **FLASH Read Line** command may be used to read back the stored values.

Note:

1. *If transferring the start address, the lower 5 bits are cleared automatically.*
2. *If less than 36 data bytes are received, nothing is written into the FLASH. The Read Status command can be used to check an invalid command length error.*
3. *If an already written section in the FLASH gets re-written (without being erased before), the resulting data is undefined.*

4. *After the stop condition (P) is received the data is programmed into the FLASH. During the programming time incoming I²C commands are not acknowledged.*

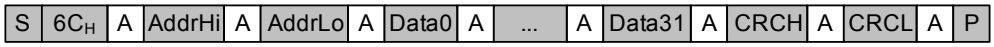


Figure 67 FLASH Write Line command

2.18.2 FLASH Read Line

The contents of the FLASH memory (4000_H to $587F_H$) can be read out via the I²C interface. **Figure 68** shows the structure of the FLASH read line command.

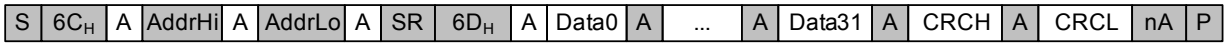


Figure 68 FLASH Read Line command

2.18.3 FLASH Erase

The FLASH Erase command is show in **Figure 69** and can be used to erase the Code Sector and the User Data Sectors. The FLASH Erase time is specified in **Table 46**. **Figure 70** and **Table 28** describe the bits of the Sector byte.

Note: After the stop condition (P) is received the selected FLASH sectors are being erased. During the erase time incoming I²C commands are not acknowledged.

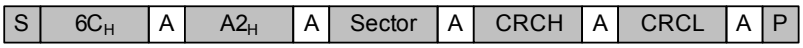


Figure 69 FLASH Erase command

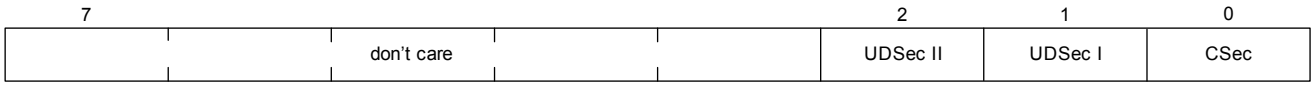


Figure 70 FLASH Erase: Sector byte

Table 28 FLASH Erase: Sector byte

Bits	Field	Description
2	UDSec II	0_B: don't erase User Data Sector II 1_B: erase whether User Data Sector II is erased
1	UDSec I	0_B: don't erase User Data Sector I 1_B: erase whether User Data Sector I is erased
0	CSec	0_B: don't erase Code Sector 1_B: erase whether Code Sector is erased

2.18.4 FLASH Check Erase Status

This function returns the status of the selected FLASH sector(s). The time required for checking the sectors depends on the selected sectors. The structure of the I^2C command *FLASH Check Erase Status* is shown in **Figure 71**. **Figure 72** and **Table 29** describe the bits of the Sector byte. The Status byte is illustrated in **Figure 73** and **Table 30**.

Note: After the first stop condition (P) is received the selected FLASH sectors are checked. During this time incoming I^2C commands are not acknowledged.

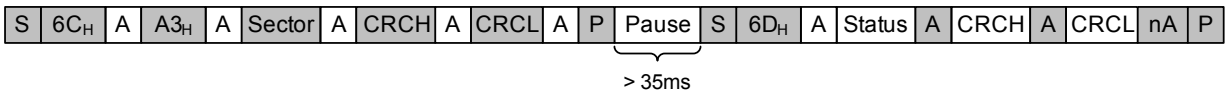


Figure 71 FLASH Check Erase Status command

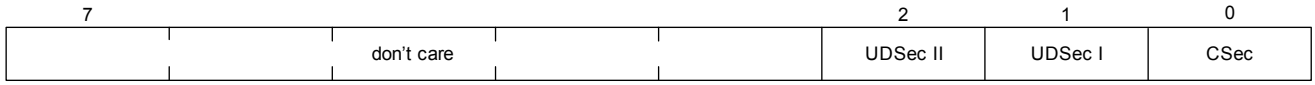


Figure 72 FLASH Check Erase Status: Sector byte

Table 29 FLASH Check Erase Status: Sector byte

Bits	Field	Description
2	UDSec II	0_B: don't check User Data Sector II 1_B: check whether User Data Sector II is erased
1	UDSec I	0_B: don't check User Data Sector I 1_B: check whether User Data Sector I is erased
0	CSec	0_B: don't check Code Sector 1_B: check whether Code Sector is erased

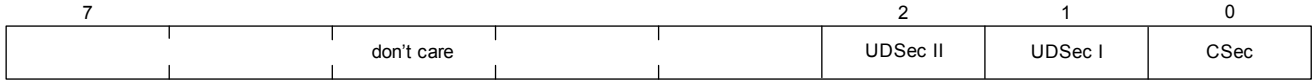


Figure 73 FLASH Check Erase Status: Status byte

Table 30 FLASH Check Erase Status: Status byte

Bits	Field	Description
2	UDSec II	0_B: User Data Sector II is erased or untested 1_B: at least one bit is set in User Data Sector II
1	UDSec I	0_B: User Data Sector I is erased or untested 1_B: at least one bit is set in User Data Sector I
0	CSec	0_B: Code Sector is erased or untested 1_B: at least one bit is set in Code Sector

2.18.5 FLASH Set Code Lock (Lockbyte 2)

To set Lockbyte 2 $D1_H$ has to be written to FLASH address $577F_H$ (top address of Code Sector). After the Lockbyte 2 is set, a startup in DEBUG or PROGRAMMING mode is not possible any more.

Note: To activate the Code Sector Lock the PMA51xx has to be reset after Lockbyte $D1_H$ has been set.

2.18.6 FLASH Set User Data Sector Lock (Lockbyte 3)

This command sets the Lockbyte for FLASH User Data Sectors I + II.

Note: It is required to set Code Sector Lock (Lockbyte 2) to enable User Data Sector Lock (Lockbyte 3) to become effective.

Note: To activate the User Data Sector Lock (Lockbyte 3) the PMA51xx has to be reset after setting the Lockbytes for User Data Sector and Code Sector.

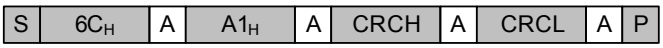


Figure 74 FLASH Set Lockbyte 3 command

2.18.7 Read Status

This function is intended to read out the status of the previous executed functions (pass/fail). It can be called whenever desired to verify if there were errors since the last *Read status* call. **Figure 76** and **Table 31** describe the bits of the Status byte.

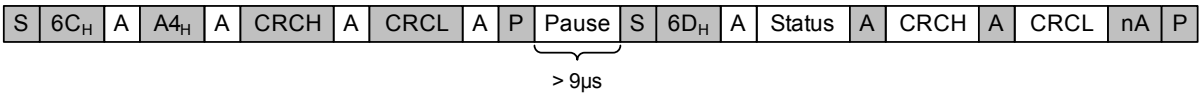


Figure 75 Read Status command

Figure 76 Read Status: Status byte

Table 31 Read Status: Status byte

Bits	Field	Description
7:4	CmdCnt	Number of executed commands since the first detected error. 1111_B: 15 commands or more 1110_B: 14 commands ... 0001_B: 1 command 0000_B: error occurred in last command
3:2	ErrCnt	Erroneous events since the last Read status call. 11_B: three or more errors 10_B: two errors 01_B: one error 00_B: no error
1	InvCmdL	1_B: Invalid command length or execution fail since the last Read status call 0_B: Command length and execution correct since the last Read status call
0	CRCFail	1_B: CRC Failure detected since the last Read status call 0_B: no CRC Error occurred since the last Read status call

2.19 DEBUG Mode Operation

Debugging of the PMA is done via the I²C interface, therefore the I²C interface must not be reconfigured in DEBUG Mode. Furthermore debugging of the I²C interface itself is not possible and will lead to debugging errors.

Note: The FLASH is protected against write access in DEBUG mode. RAM area EB_H - FF_H is used by the Debugger and must not contain any application code when PMA is used in DEBUG mode.

2.19.1 ROM Debug Function

The debug function mainly consists of a debug handler and a single stepper. The debug handler processes the I²C communication and debug command interpretation. The debug commands **SetSFR, ReadSFR, SetData, ReadData** and **SetPC, ReadPC** are executed directly by the debug handler.

The debug commands **Single Step, Run Interruptible** and **Run until Breakpoint** are executed by the single stepper. The single stepper fetches the current opcode and enables opcode execution depending on the debug command.

2.19.2 DEBUG Mode Commands

In DEBUG mode the PMA51xx is accessible as a slave using the I²C interface.

Figure 77 shows the legend used for the description of the I²C commands.

■	from debugger to PMA	**S**	start condition
□	from PMA to debugger	**P**	stop condition
PCL	Program counter low byte	**SR**	restart condition or stop / start condition
PCH	Program counter high byte	**A**	acknowledge
BPL	Break point low byte	**nA**	not acknowledge
BPH	Break point high byte	**Addr**	SFR / idata / xdata address
Pause	Time where no comunication is allowed	**Data**	Data byte read from / written to SFR / idata / xdata

Figure 77 Legend for I²C communication in DEBUG

2.19.2.1 Set SFR

Set an SFR to a user-defined value.

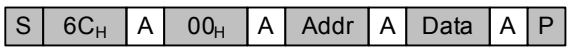


Figure 78 Set SFR command

Addr: Address of SFR to be set.

Data: Byte value that is written into the SFR address specified by *Addr*.

2.19.2.2 Read SFR

Read the value of one SFR.

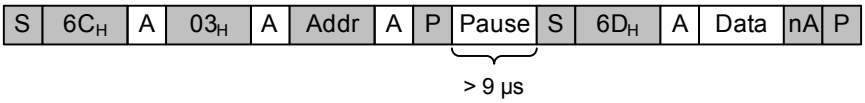


Figure 79 Read SFR command

Addr: Address of SFR to be read.

Data: Byte value that is read from the SFR at address specified by *Addr*.

2.19.2.3 Set IData

Set one byte in the internal data memory (RAM) to a user-defined value.

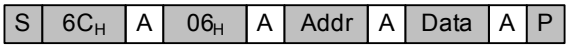


Figure 80 Set IData command

Addr: Address of the internal data memory to be set (Range: 00_H - FF_H).

Data: Byte value that is written into the internal data memory at address specified by *Addr*.

2.19.2.4 Read IData

Read one byte of the internal data memory (RAM).

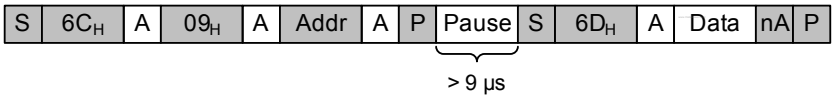


Figure 81 Read IData command

Addr: Address of the internal data memory to be read (Range: 00_H - FF_H).

Data: Byte value that is read from the internal data memory at address specified by *Addr*.

2.19.2.5 Set XData

Set one byte in the external data memory (battery buffered data RAM) to a user-defined value.

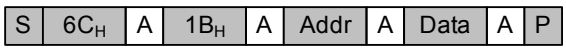


Figure 82 Set XData command

Addr: Address of the external data memory to be set (Range: 00_H - $0F_H$).

Data: Byte value that is written into the external data memory at address specified by *Addr*.

2.19.2.6 Read XData

Read one byte of the external data memory (battery buffered data RAM).

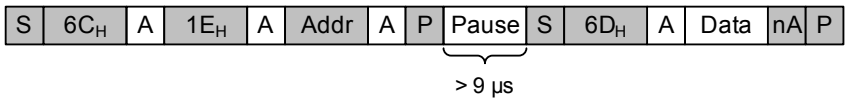


Figure 83 Read XData command

Addr: Address of the external data memory to be read (Range: 00_H - $0F_H$).

Data: Byte value that is read from the external data memory at address specified by *Addr*.

2.19.2.7 Set PC

Set the Program Counter to a user-defined value.

Figure 84 Set PC command

PCL: MSB of the new Program Counter.

PCH: LSB of the new Program Counter.

2.19.2.8 Read PC

Reads the Program Counter.

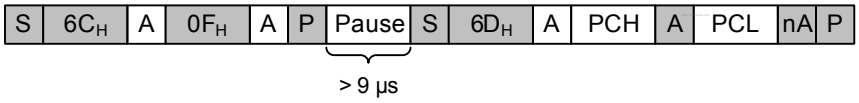


Figure 85 Read PC command

PCL: MSB of the actual Program Counter.

PCH: LSB of the actual Program Counter.

2.19.2.9 Single Step

Execute one opcode instruction and return to the debug handler.

Note: A Library function can not be single stepped and is stepped through automatically until the FLASH is re-entered.

Figure 86 Single Step

2.19.2.10 Run Interruptible

The function consists of device internal consecutive single steps until any I^2C command is received on the bus. Compared to running the program in real time this function has a slower execution speed by a factor of about 1/50, dependent on the executed program.

Figure 87 Run Interruptible

2.19.2.11 Run until Breakpoint

The debugged program is executed without single steps in real time. This enables debugging of runtime critical functions like RF-Transmission or LF data receiving. The execution is stopped when the PC matches the defined breakpoint.

Note: If the breakpoint is not hit the communication to the debugger is lost.

Figure 88 Run until Breakpoint

3 Reference

3.1 Electrical Data

3.1.1 Absolute Maximum Ratings

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design/characterization.

Table 32 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Supply Voltage	V_{Bat}	-0.3		+4.0	V		■	1.1
Operating Temperature	T_j	-40		+125	°C			1.2
ESD HBM integrity	V_{HBM}			2	kV	All pins According to ESD Standard JEDEC EIA / JESD22-A114-B	■	1.3
Latch up	I_{LU}	-100		+100	mA	EIA JESD78A	■	1.4
Input voltage at digital input pins	$V_{InDigital}$	-0.3		V_{Bat}+0.3	V			1.5
LF Receiver input voltage	V_{InLF}	-0.3		+0.3	V			1.6
Input and output current for digital I/O pins	I_{IOmax}			4	mA	Less than 10 mA on all digital pins	■	1.7
LF Receiver input current	I_{LFIN}			4	mA		■	1.8
XTAL input voltage	V_{InXT}	-0.3		V_{REG}+0.3	V		■	1.9
Storage Temperature	T_s	-40		+150[1)]	°C	1) Max 1000 hours accumulated over lifetime	■	1.10

3.1.2 Operating Range

Within the operational range the IC operates as explained in the circuit description.

Table 33 Operating Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Supply voltage	V_{Bat1}	2.1		3.6	V	Temperature sensor, LF Receiver and FLASH programming		2.1
	V_{Bat2}	1.9		3.6	V	Every module which is not mentioned at 2.1 (V_{Bat1})		2.2
Ambient temperature range	T_{amb}	-40		125	°C	Normal operation		2.4
	T_{FLC}	0		85	°C	FLASH code sector programming		2.5
	T_{FLD}	-40		85	°C	FLASH data sector programming		2.6

3.1.3 Product Characteristics

Product characteristics involve the spread of values guaranteed within the specified voltage and ambient temperature range.

Typical characteristics are the median of the production.

Supply voltage: V_{bat} = 1.9V ... 3.6V, unless otherwise specified

Ambient temperature: T_{amb} = -40°C ... +125°C, unless otherwise specified

3.1.3.1 Temperature Sensor

Table 34 Temperature Sensor Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Measurement error	T_{Error}	-3		+3	°C	T = -20 ... 70°C	■	3.1
Measurement error		-5		+5	°C	T = T_j	■	3.2

3.1.3.2 Battery Sensor

Table 35 Battery Sensor Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Measurement error	V_{Error}	-100		100	mV		■	4.1

3.1.3.3 Supply Currents

Table 36 Supply Currents

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Supply Current RF Transmission FSK modulation	I_{5dBm}		9,7		mA	f = 315 MHz, V_{Bat} = 3 V, T = 25°C SFR DIVIC = 03_H	■	5.1
	I_{8dBm}		12,2		mA		■	5.2
	I_{10dBm}		12,8		mA		■	5.3
Supply Current RF Transmission FSK modulation	I_{5dBm}		9,9		mA	f = 434 MHz, V_{Bat} = 3 V, T = 25°C SFR DIVIC = 03_H	■	5.4
	I_{8dBm}		12,3		mA		■	5.5
	I_{10dBm}		13,8		mA		■	5.6
Supply Current RF Transmission FSK modulation	I_{5dBm}		11,8		mA	f = 868 MHz, V_{Bat} = 3 V, T = 25°C SFR DIVIC = 03_H	■	5.7
	I_{8dBm}		12,9		mA		■	5.8
	I_{10dBm}		16,9		mA		■	5.9
Supply Current RF Transmission FSK modulation	I_{5dBm}		12,6		mA	f = 915 MHz, V_{Bat} = 3 V, T = 25°C SFR DIVIC = 03_H	■	5.10
	I_{8dBm}		15,3		mA		■	5.11
	I_{10dBm}		17,1		mA		■	5.12
Supply Current RF Transmission FSK modulation	I_{5dBm}		8,9		mA	f = 315 MHz, V_{Bat} = 3 V, T = -40°C SFR DIVIC = 03_H	■	5.13
	I_{8dBm}		11		mA		■	5.14
	I_{10dBm}		12		mA		■	5.15
Supply Current RF Transmission FSK modulation	I_{5dBm}		9,2		mA	f = 434 MHz, V_{Bat} = 3 V, T = -40°C SFR DIVIC = 03_H	■	5.16
	I_{8dBm}		11,5		mA		■	5.17
	I_{10dBm}		12,9		mA		■	5.18
Supply Current RF Transmission FSK modulation	I_{5dBm}		11,3		mA	f = 868 MHz, V_{Bat} = 3 V, T = -40°C SFR DIVIC = 03_H	■	5.19
	I_{8dBm}		12,8		mA		■	5.20
	I_{10dBm}		16,8		mA		■	5.21
Supply Current RF Transmission FSK modulation	I_{5dBm}		11,3		mA	f = 915 MHz, V_{Bat} = 3 V, T = -40°C SFR DIVIC = 03_H	■	5.22
	I_{8dBm}		13,4		mA		■	5.23
	I_{10dBm}		16,7		mA		■	5.24
Supply Current RF Transmission FSK modulation	I_{5dBm}		10,9		mA	f = 315 MHz, V_{Bat} = 3 V, T = 125°C SFR DIVIC = 03_H	■	5.25
	I_{8dBm}		13,1		mA		■	5.26
	I_{10dBm}		13,9		mA		■	5.27
Supply Current RF Transmission FSK modulation	I_{5dBm}		11,1		mA	f = 434 MHz, V_{Bat} = 3 V, T = 125°C SFR DIVIC = 03_H	■	5.28
	I_{8dBm}		13,4		mA		■	5.29
	I_{10dBm}		15		mA		■	5.30
Supply Current RF Transmission FSK modulation	I_{5dBm}		12,3		mA	f = 868 MHz, V_{Bat} = 3 V, T = 125°C SFR DIVIC = 03_H	■	5.31
	I_{8dBm}		11,6		mA		■	5.32
	I_{10dBm}		16,3		mA		■	5.33

Table 36 Supply Currents (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Supply Current RF Transmission FSK modulation	I_{5dBm}		13,3		mA	f = 915 MHz, V_{Bat} = 3 V, T = 125°C SFR DIVIC = 03_H	■	5.34
	I_{8dBm}		14,8		mA		■	5.35
	I_{10dBm}		16,7		mA		■	5.36
Supply Current POWER DOWN	I_{PD}		590		nA	V_{Bat} = 3.0V, T = 25°C		5.37
			10,8		µA	V_{Bat} = 3.0V, T = 125°C	■	5.38
Supply Current IDLE	I_{IDLE}		0,80		mA	V_{Bat} = 3.0V, T = 25°C (SFR DIVIC = 00_H, system clock = 12 MHz RC Osc.)		5.39
			0,93		mA	V_{Bat} = 3.0V, T = 125°C (SFR DIVIC = 00_H, system clock = 12 MHz RC Osc.)	■	5.40
Supply Current RUN	I_{RUN}		1,87		mA	V_{Bat} = 3.0V, T = 25°C (SFR DIVIC = 00_H, system clock = 12 MHz RC Osc.)		5.41
			2,0		mA	V_{Bat} = 3.0V, T = 125°C (SFR DIVIC = 00_H, system clock = 12 MHz RC Osc.)	■	5.42

3.1.3.4 RF-Transmitter

The RF Transmitter is characterized on the evaluation board with 50 Ohm matching network for specified frequency. The schematic and the element values of the matching network can be found in **Figure 89 "Matching network for the power amplifier" on Page 196** and **Table 50 "Values of the matching network for the power amplifier" on Page 196**. Tolerances of the passive elements not taken into account.

Table 37 RF Transmitter

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Transmit frequency	f_{TX}	300		320	MHz		■	6.1
		433		450	MHz			6.2
		865		870	MHz		■	6.3
		902		928	MHz		■	6.4
Data rate	DR_{RF}			32	kBps	T=-40°C - 85°C (64 kChips/s)	■	6.5
				20	kBps	T=-40°C - 125°C (40 kChips/s)	■	6.6
Output Power	OP_{RF}		5		dBm	T=25°C, V_{BAT}=3V		6.7
			8		dBm	T=25°C, V_{BAT}=3V		6.8
			10		dBm	T=25°C, V_{BAT}=3V		6.9
Carrier to spurious ratio (incl. harmonics) @D1=315/915MHz				-28	dBc	FCC 15.231a/b/e 2^{nd} to 10^{th} harmonic RBW = 100kHz	■	6.10

Table 37 RF Transmitter (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Carrier to noise ratio @D1=315/915MHz				-20	dBc	FCC 15.231a/b/e RBW = 100kHz measured at frequency edge: 0,25%*f_C for 315MHz 0,5%*f_C for 915MHz f_C:carrier frequency	■	6.11
SSB Phase Noise @D1=315MHz			-95	-89	dBc/Hz	RBW = 100kHz, +25°C @ 10kHz offset,	■	6.12
			-93	-87	dBc/Hz	@ 100kHz offset,	■	6.13
			-120	-114	dBc/Hz	@ 1MHz offset,	■	6.14
			-136	-130	dBc/Hz	@ 10MHz offset	■	6.15
SSB Phase Noise @D1=434MHz			-93	-87	dBc/Hz	RBW = 100kHz, +25°C @ 10kHz offset,	■	6.16
			-90	-84	dBc/Hz	@ 100kHz offset,	■	6.17
			-113	-107	dBc/Hz	@ 1MHz offset,	■	6.18
			-132	-126	dBc/Hz	@ 10MHz offset	■	6.19
SSB Phase Noise @D1=868MHz			-87	-81	dBc/Hz	RBW = 100kHz, +25°C @ 10kHz offset,	■	6.20
			-85	-79	dBc/Hz	@ 100kHz offset,	■	6.21
			-110	-104	dBc/Hz	@ 1MHz offset,	■	6.22
			-134	-128	dBc/Hz	@ 10MHz offset	■	6.23
SSB Phase Noise @D1=915MHz			-86	-80	dBc/Hz	RBW = 100kHz, +25°C @ 10kHz offset,	■	6.24
			-85	-79	dBc/Hz	@ 100kHz offset,	■	6.25
			-109	-103	dBc/Hz	@ 1MHz offset,	■	6.26
			-135	-129	dBc/Hz	@ 10MHz offset	■	6.27

3.1.3.5 LF Receiver

The LF Receiver is only available on PMA5110.

Table 38 LF Receiver, V_{Bat} = 2.1-3.6V

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
LF Baseband Sensitivity	S_{LF1}		2.5		mV_{pp}	After calling a Library function for calibration. T=25°C, V_{Bat}=3V	■	7.1
Data rate	DR_{LF}	2		4	kbit/s		■	7.2
Data rate error	DR_{error}	-2		2	%		■	7.3
Carrier frequency	f_{CLF}	120	125	130	kHz		■	7.4

Table 38 LF Receiver, V_{Bat} = 2.1-3.6V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
LF Current consumption	I_{LF_AFE}		1		µA	25°C; 3 V Analog frontend only		7.5
	I_{LF_BB}		440		µA	25°C; 3 V Including baseband	■	7.6
Input dynamic range	DR_{LF}	70			dB	**LF Baseband Sensitivity**, AGC enabled	■	7.7
Differential input capacitance	C_{inLF}		15		pF	@125 kHz	■	7.8
Differential input resistance	R_{inLF}		500		kOhm	AGC disabled	■	7.9
Preamble length	$T_{preamble}$	2			ms	Included in reference datagram	■	7.10
Carrier Detector Freeze Hold Time	T_{CDCH}	2			s	Worst case @ 125°C	■	7.11

3.1.3.6 Crystal oscillator

Table 39 Crystal oscillator

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Crystal startup time	t_{XTAL}		1.2		ms	IFX Testboard with these Crystals[1) 2) 3) 4)]		8.1
Crystal oscillator startup delay time	$t_{XTALADJ}$	0		1750	µs	Progammable in 250µs steps SFR XTCFG	■	8.2
Crystal frequency	f_{XTAL}	18		20	MHz			8.3
Parasitic capacitance	C_{PCBmax}			4	pF	Determined by PCB Layout	■	8.4
Serial resistance of the crystal	R_{Rmax}			60	Ohm			8.5
Input inductance XTALOUT	L_{OSC}		2.2		uH		■	8.6
Crystal fine tuning capacitance	C_{tune}		40		pF	Selectable with 156 fF resolution (8 bits)	■	8.7

1) NX5032SA EXS00A-CS00269 C_L = 12pF, $f_{Crystal}$ = 19,6875 MHz
2) NX5032SA EXS00A-CS00270 C_L = 12pF, $f_{Crystal}$ = 19,0625 MHz
3) NX5032SA EXS00A-CS00271 C_L = 12pF, $f_{Crystal}$ = 18,089583 MHz
4) NX5032SA EXS00A-CS00272 C_L = 12pF, $f_{Crystal}$ = 18,080 MHz

3.1.3.6.1 Crystal oscillator recommendation

As crystal oscillator for PMA51xx NX5032SD

Table 40 NDK crystal oscillator recommendation for PMA51xx

Nominal Frequency (MHz)	NDK specification number	Shunt capacitance (C_0)	Motional capacitance (C_1)
19.6875	EXS00A-02825	1.58pF±15%	6.73fF±15%
19.0625	EXS00A-03550	1.64pF±15%	6.97fF±15%
18.089583	EXS00A-03551	1.55pF±15%	6.50fF±15%
18.080	EXS00A-03552	1.60pF±15%	6.70fF±15%

3.1.3.7 12 MHz RC HF oscillator

Table 41 12 MHz RC HF oscillator

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Operating frequency	f_{RCHF}	-3%	12.00	+3%	MHz	V_{Bat} = 3.0V, T = 25°C		9.1
Overall drift	df_{RCHF}	-5		+5	%			9.2

3.1.3.8 2 kHz RC LP oscillator

Table 42 2 kHz RC LP oscillator

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Operating frequency	f_{RCLP}	1.3	2	2.8	kHz	V_{Bat} = 3.0V, T = 25°C		10.1
Overall drift	df_{RCLP}	-7		+7	%	Referring to nominal condition		10.2

3.1.3.9 Interval Timer

Table 43 Interval Timer

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Wake-up interval timer range	T_{WU}	0.05		255	s	Adjustable with resolution of 8 bit. Calibrated with Library Function.	■	11.1
Wake-up interval timer step	T_{WUST}	0.05		1	s		■	11.2
Frequency calibration error	f_{ITCE}	-5		+5	%	T_{WUST} = 0.5s, systemclock = XTAL	■	11.3

3.1.3.10 Power On Reset

Table 44 Power On Reset

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Power On Reset level	V_{POR}	0.2	0.4	1.7	V	Minimum supply voltage level measured at Pin V_{REG} for a valid logic LOW at Power On Reset circuit		12.1
Power On release level	V_{THR}	1.7		1.8	V	Measured at Pin V_{REG}		12.2
Power On reset time	t_{POR}	0.25	1	10	ms			12.3
Brown Out detect level in RUN state	V_{BRD}	1.7		1.8	V	Measured at Pin V_{REG}		12.4
Brown Out detect level in POWER DOWN	V_{PDBR}	0.7		1.7	V	Measured at Pin V_{REG}		12.5
Mode selection time	t_{MODE}			2.5	ms		■	12.6
Minimum detectable Brown Out glitch in RUN state	t_{brd}			1	µs		■	12.7
Minimum detectable Brown Out glitch in POWER DOWN	t_{brdpd}			100	µs		■	12.8

3.1.3.11 VMIN Detector

Table 45 VMIN Detector

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Low battery threshold warning level	TH_{LBat}	2.0	2.1	2.2	V			14.1

3.1.3.12 6k FLASH Code memory data

Table 46 6k FLASH Code memory data

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Temperature range Erase/program	TR_{FL}	0		85	°C			15.1
Erase/Program Supply voltage range regulated	V_{FLBat}	2.1			V			15.2
Endurance	En_{FLCode}	1000			cycles	One cycle: Programming of all wordlines and erasing each sector once.	■	15.3
Data Retention	$t_{RCode@125\ °C}$	2			yrs		■	15.4
	$t_{RCode@85\ °C}$	40			yrs		■	15.5
Erase time			102		ms	RC HF oscillator @12 MHz		15.6
Write time/line			2.2		ms	RC HF oscillator @12 MHz Line = 32 byte		15.7

3.1.3.13 2 times 128 byte FLASH Data memory

Table 47 2 times 128 byte FLASH Data memory

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Temperature range Erase/program	TR_{FL}	-40		85	°C			16.1
Erase/Program Supply voltage range regulated	V_{FLBat}	2.1			V			16.2

Table 47 2 times 128 byte FLASH Data memory (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Endurance	ER_{Data}	100	1000		kcycles	Over lifetime Retention is a function of endurance.	■	16.3
Data Retention	$t_{RData@85\ °C}$	40			yrs		■	16.4
	$t_{RData@125\ °C}$	2			yrs		■	16.5
Erase time			102		ms	RC HF oscillator @12 MHz		16.6
Write time/line			2.2		ms	RC HF oscillator @12 MHz Line = 32byte		16.7

3.1.3.14 ADC Interface

The ADC Interface is only available on PMA5110.

Table 48 ADC Interface

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
ADC input voltage range	VR_{ADC}	GND		V_{Reg}				17.1
ADC resolution	R_{ADC}	10			bit		■	17.2
Offset correction range	R_{OFFC}			6	bit		■	17.3
Differential non-linearity	DNL	-1.0		1.0	lsb			17.4
Integral non-linearity	INL	-1.5		1.5	lsb			17.5

3.1.3.15 Digital I/O Pin

Table 49 Digital I/O Pin

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Input low voltage	V_{IL}			0.5	V		■	18.1
Input high voltage	V_{IH}	V_{Bat} -0.5			V		■	18.2
Output low voltage	V_{OL}			0.5	V	I_{OL} = 1.6mA		18.3
Output high voltage	V_{OH}	V_{Bat} -0.5			V	I_{OH} = -1.6mA		18.4
Output transition time	t_{THL}, t_{TLH}			30	ns	20pF load, 10% ... 90%	■	18.5
Input capacitance	C_{pad}			2	pF		■	18.6
Internal pull-up or pull-down resistor	R_{uPPx}, $R_{downPPx}$ [1]		50		kOhm			18.7
Internal pull-up or pull-down resistor	R_{upPPy}, $R_{downPPy}$ [2]		250		kOhm			18.8

1) PPx are: PP0, PP1

2) PPy are: PP2, PP3, PP4, PP5, PP6, PP7, PP8, PP9

3.1.4 Matching Network for the Power Amplifier

Figure 89 and Table 50 show the schematic and the element values of the matching network used for the characterization of the RF Transmitter.

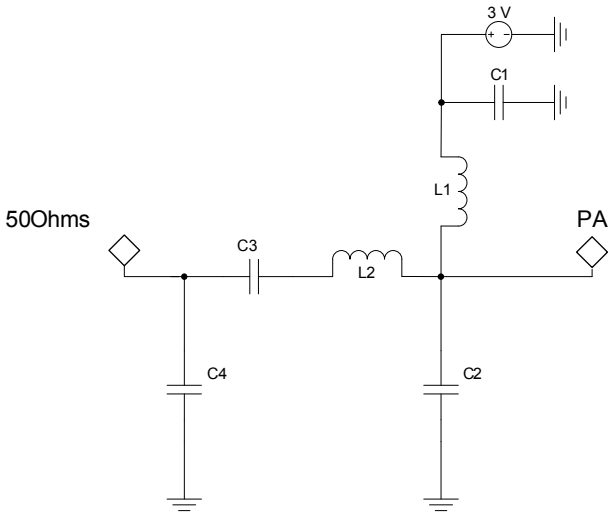


Figure 89 Matching network for the power amplifier

Table 50 Values of the matching network for the power amplifier

Frequency [MHz]	Output Power [dBm]	C1 [pF]	C2 [pF]	C3 [pF]	C4 [pF]	L1 [nH]	L2 [nH]
315	5	100	5,6	12	22	72	72
	8	100	5,6	12	15	72	72
	10	100	4,7	22	8,2	82	72
434	5	100	4,7	56	18	36	33
	8	100	4,7	39	12	36	36
	10	100	5,6	27	12	36	33
868	5	100	1,8	27	8,2	10	10
	8	100	1,8	33	6,8	10	10
	10	100	2,2	56	5,6	9,5	9,5
915	5	100	1,8	33	8,2	9,5	9,5
	8	100	2,2	27	6,8	9,5	9,5
	10	100	1,8	18	5,6	9,5	9,5

4 Register Overview

Table 51 Register Overview

Register Short Name	Register Long Name	Offset Address	Page Number
ACC	Accumulator	$E0_H$	65
ADCC0	ADC Configuration Register 0	DB_H	116
ADCC1	ADC Configuration Register 1	DC_H	118
ADCDH	ADC Result Register high byte	$D5_H$	119
ADCDL	ADC Result Register low byte	$D4_H$	119
ADCM	ADC Mode Register	$D2_H$	120
ADCOFF	ADC Input Offset c-network configuration	DA_H	121
ADCS	ADC Status Register	$D3_H$	122
B	Register B	$F0_H$	65
CFG0	Configuration Register 0	$F8_H$	46
CFG1	Configuration Register 1	$E8_H$	47
CFG2	Configuration Register 2	$D8_H$	48
CRC0	CRC Shift Register low byte	AC_H	126
CRC1	CRC Shift Register high byte	AD_H	127
CRCC	CRC Control Register	$A9_H$	125
CRCD	CRC Data Register	AA_H	126
DIVIC	Internal Clock Divider	$B9_H$	54
DPH	Data Pointer (high byte)	83_H	65
DPL	Data Pointer (low byte)	82_H	65
DSR	Diagnosis and Status Register	$D9_H$	49
ExtWUF	External Wake-up Flag Register	$F1_H$	37
ExtWUM	External Wake-up Mask Register	$F2_H$	38
FCSP	FLASH Control Register - Sector Protection Control	$E9_H$	59
I2CB	I2C Baud rate Register	$B1_H$	160
I2CC	I2C Control Register	$A2_H$	161
I2CD	I2C Data Register	$9A_H$	162
I2CM	I2C Mode Register	$A3_H$	162
I2CS	I2C Status Register	$9B_H$	163
IE	Interrupt Enable Register	$A8_H$	69
IP	Interrupt Priority Register	$B8_H$	70
IRQFR	Interrupt Request Flag Register for extended interrupts	$8F_H$	71
ITPH	Interval Timer Precounter Register High Byte	BB_H	43
ITPL	Interval Timer Precounter Register Low Byte	BA_H	44
ITPR	Interval Timer Period Register	BC_H	44

Table 51 Register Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
LBD	Low Battery Detector Control	EF_H	50
LFCDFlt	LF Carrier Detect Filtering	$B2_H$	94
LFCDM	LF Carrier Detector Mode	$B5_H$	95
LFDIV0	LF Division Factor low byte	$B3_H$	96
LFDIV1	LF Division Factor high byte	$B4_H$	96
LFOOT	LF On/Off Timer Configuration Register	$C6_H$	97
LFOOTP	LF On/Off Timer Precounter	$C5_H$	98
LFP0H	LF Pattern 0 Detector Sequence Data MSB	BF_H	98
LFP0L	LF Pattern 0 Detector Sequence Data LSB	BE_H	99
LFP1H	LF Pattern 1 Detector Sequence Data MSB	CF_H	99
LFP1L	LF Pattern 1 Detector Sequence Data LSB	CE_H	100
LFPCFG	LF Pattern Detection Configuration Register	$C7_H$	100
LFRX0	LF Receiver Configuration Register 0	$B7_H$	101
LFRX1	LF Receiver Configuration Register 1	$B6_H$	102
LFRXC	LF Receiver Control Register	$F9_H$	103
LFRXD	LF Receiver Data Register	$A5_H$	104
LFRXS	LF Receiver Status Register	$A4_H$	105
LFSYN0	LF Sync Pattern 0	$A6_H$	106
LFSYN1	LF Sync Pattern 1	$A7_H$	106
LFSYNCFG	LF SYNC Matching Configuration Register	AF_H	107
MMR0	Memory Mapped Register 0	84_H	60
MMR1	Memory Mapped Register 1	85_H	60
MMR2	Memory Mapped Register 2	86_H	60
P1Dir	IO-Port 1 Direction Register	91_H	150
P1In	IO-Port 1 Data IN Register	92_H	152
P1Out	IO-Port 1 Data OUT Register	90_H	153
P1SENS	IO-Port 1 Sensitivity Register	93_H	154
P3Dir	IO-Port 3 Direction Register	EB_H	151
P3In	IO-Port 3 Data IN Register	EC_H	152
P3Out	IO-Port 3 Data OUT Register	$B0_H$	153
P3SENS	IO-Port 3 Sensitivity Register	ED_H	155
PSW	Program Status Word	$D0_H$	66
REF	Resume Event Flag Register	$D1_H$	39
RFC	RF Transmitter Control Register	EE_H	77
RFD	RF Encoder TX Data Register	$8E_H$	77
RFENC	RF Encoder Tx Control Register	$E7_H$	78
RFFSLD	RF Frequency Synthesizer Lock Detector Configuration	DF_H	79
RFFSPLL	RF Frequency Synthesizer PLL Configuration	$D7_H$	80

Table 51 Register Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
RFS	RF Encoder Tx Status Register	$E6_H$	81
RFTX	RF Transmitter Configuration Register	AE_H	82
RFVCO	RF Frequency Synthesizer VCO Configuration	DE_H	83
RNGD	Random Number Generator Data Register	AB_H	128
SP	Stack Pointer	81_H	65
SPIB	SPI Baud rate Register	$F3_H$	171
SPIC	SPI Control Register	$F4_H$	172
SPID	SPI Data Register	$F5_H$	173
SPIM	SPI Mode Register	$F6_H$	173
SPIS	SPI Status Register	$F7_H$	175
TCON	Timer Control Register Timer 0/1	88_H	132
TCON2	Timer Control Register Timer 2/3	$C8_H$	143
TH0	Timer 0 Register high byte	$8C_H$	133
TH1	Timer 1 Register high byte	$8D_H$	133
TH2	Timer 2 Register high byte	CD_H	144
TH3	Timer 3 Register high byte	CB_H	144
TL0	Timer 0 Register low byte	$8A_H$	134
TL1	Timer 1 Register low byte	$8B_H$	134
TL2	Timer 2 Register low byte	CC_H	145
TL3	Timer 3 Register low byte	CA_H	145
TMOD	Timer Mode Register	89_H	135
TMOD2	Timer Mode Register 2 Timer 2/3	$C9_H$	146
WUF	Wake-up Flag Register	$C0_H$	40
WUM	Wake-up Mask Register	$C1_H$	41
XTCFG	XTAL Configuration Register	$C2_H$	56
XTAL1	XTAL Frequency Register FSKHIGH/ASK	$C3_H$	55
XTAL0	XTAL Frequency Register FSKLOW	$C4_H$	55

References

This section contains documents used for cross- reference throughout this document.

[1] PMA Function Library Guide

5 Package Outlines

Dimensions are defined in millimeter.

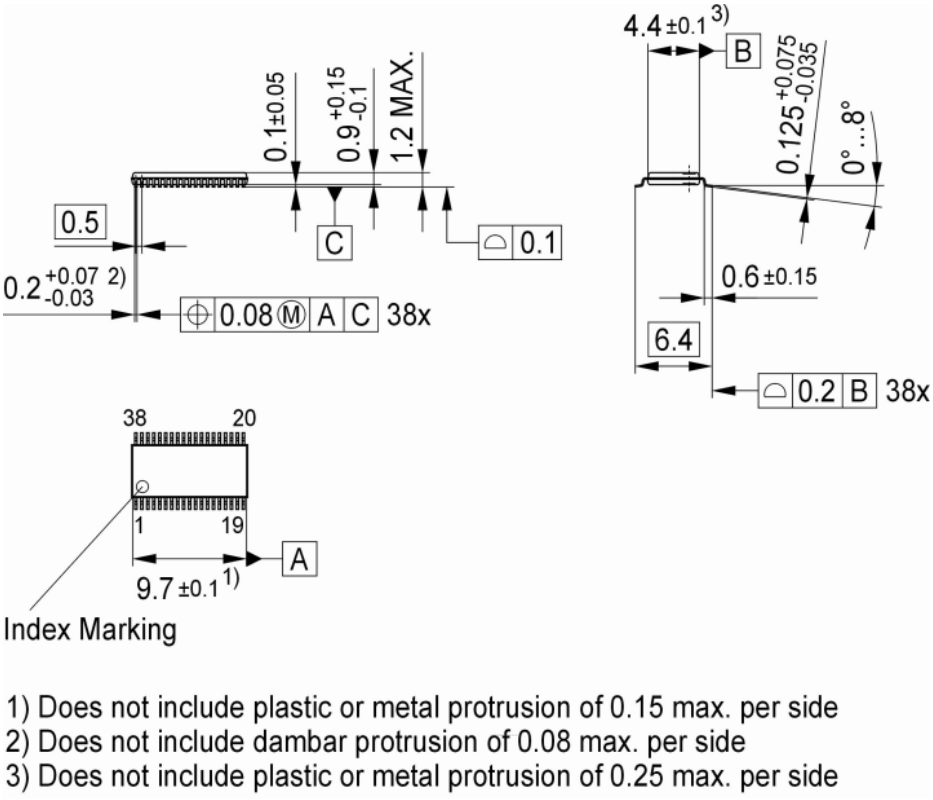


Figure 90 Package Outline PG-TSSOP-38

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