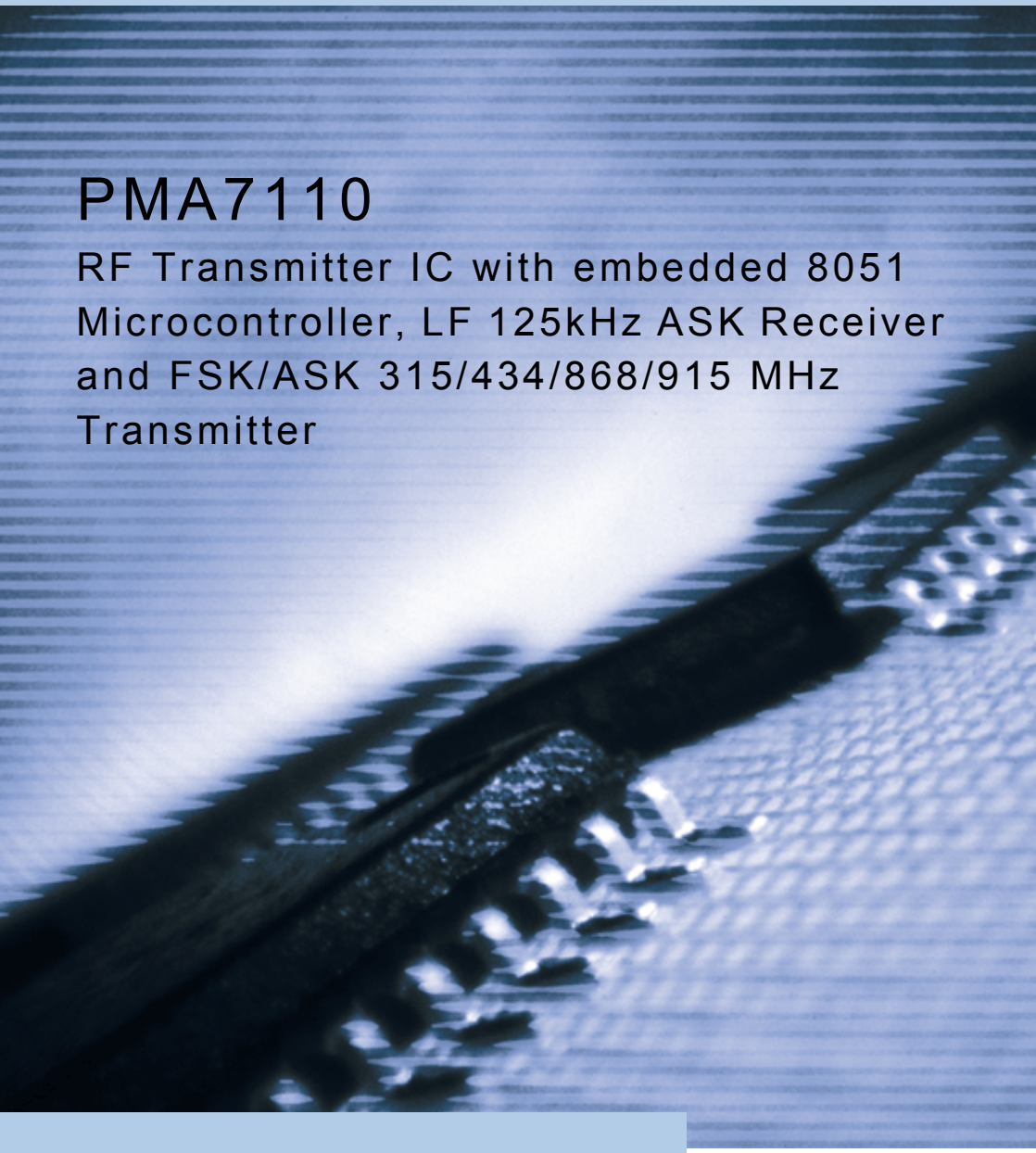
PMA7110

RF Transmitter IC with embedded 8051 Microcontroller, LF 125kHz ASK Receiver and FSK/ASK 315/434/868/915 MHz Transmitter



Sense & Control

Never stop thinking

Edition 2008-04-28

Published by Infineon Technologies AG,
Am Campeon 1-12
85579 Neubiberg, Germany

Attention please!

The information herein is given to describe certain components and shall not be considered as a guarantee of characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or the Infineon Technologies Companies and our Infineon Technologies Representatives worldwide (**www.infineon.com**).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

PMA7110

RF Transmitter IC with embedded 8051 Microcontroller, LF 125kHz ASK Receiver and FSK/ASK 315/434/868/915 MHz Transmitter

Sense & Control

Never stop thinking

PMA7110

Revision History:2008-04-28 V0.9

Page 129	update typical value of transmit current consumption
Page 132	Update RF characterization for D9 ~ D17
Page 128, Page 141	Update flash code/data memory program temeprature and erase cycle: B4, O1, O2, O6 ~ O8.

We Listen to Your Comments
Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:
sensors@infineon.com

1 Product Description . . . 9
1.1 Overview . . . 9
1.2 Features . . . 10
1.3 Applications . . . 10

2 Functional Description . . . 11
2.1 Pin Description . . . 11
2.2 Functional Block Diagram . . . 28
2.3 Operating Modes and States . . . 29
2.3.1 Operating mode selection . . . 29
2.3.2 State Description . . . 32
2.3.2.1 INIT State . . . 32
2.3.2.2 RUN State . . . 33
2.3.2.3 IDLE State . . . 33
2.3.2.4 POWER DOWN State . . . 34
2.3.2.5 THERMAL SHUTDOWN state . . . 34
2.3.2.6 State Transitions . . . 35
2.3.2.7 Status of PMA7110 Blocks in Different States . . . 37
2.4 Fault protection . . . 40
2.4.1 Watchdog Timer . . . 40
2.4.2 VMIN Detector . . . 40
2.4.3 FLASH Memory Checksum . . . 40
2.4.4 ADC Measurement Overflow & Underflow . . . 40
2.4.5 TMAX Detector . . . 40
2.5 Functional Block Description . . . 41
2.5.1 Sensor Interfaces and Data Acquisition . . . 41
2.5.1.1 Sensor Interface . . . 41
2.5.1.2 Two differential high sensitive interfaces to external Sensors . . . 43
2.5.1.3 Interface to other signals . . . 44
2.5.1.4 Reference voltages . . . 44
2.5.1.5 Temperature Sensor . . . 46
2.5.1.6 Battery Voltage Monitor . . . 46
2.5.2 Memory Organization and Special Function Registers (SFR) . . . 47
2.5.2.1 ROM . . . 48
2.5.2.2 FLASH . . . 49
2.5.2.3 RAM . . . 51
2.5.2.4 Special Function Registers . . . 51
2.5.3 Microcontroller . . . 57
2.5.4 System Configuration Registers . . . 58
2.5.5 General Purpose Registers (GPR) . . . 61
2.5.6 System Controller . . . 62
2.5.6.1 Wakeup Logic . . . 62
2.5.6.2 Interval Timer . . . 68

2.5.6.3 Interval Timer Calibration . . . 69
2.5.7 Clock Controller . . . 70
2.5.7.1 2 kHz RC LP Oscillator (Low Power) . . . 71
2.5.7.2 12 MHz RC HF Oscillator (High Frequency) . . . 71
2.5.7.3 Crystal Oscillator . . . 71
2.5.8 Interrupt Sources on the <Dev_NameShort1> . . . 74
2.5.9 RF 315/434/868/915 MHz FSK/ASK Transmitter . . . 78
2.5.9.1 Phase Locked Loop PLL . . . 79
2.5.9.2 Power Amplifier PA . . . 80
2.5.9.3 ASK Modulator . . . 80
2.5.9.4 Voltage Controlled Oscillator (VCO) . . . 80
2.5.9.5 Manchester/BiPhase Encoder with bit Rate Generator . . . 81
2.5.10 LF Receiver . . . 85
2.5.11 16Bit CRC (Cyclic Redundancy Check) Generator/Checker . . . 86
2.5.12 Pseudo Random Number Generator . . . 89
2.5.13 Timer Unit (Timer 0, Timer 1, Timer 2, Timer 3) . . . 90
2.5.13.1 Basic Timer Configuration . . . 90
2.5.13.2 General Operation Description Timer 0 and Timer 1 . . . 93
2.5.13.3 Timer Modes for Timer 2 and Timer 3 . . . 97
2.5.14 General Purpose Input/Output (GPIO) . . . 105
2.5.14.1 Peripheral Port Basic Configuration . . . 105
2.5.14.2 Spike Suppression on Input Pins . . . 108
2.5.14.3 External Wakeup on PP1-PP4 and PP6-PP9 . . . 109
2.5.14.4 Alternative Port Functionality . . . 109
2.5.15 I2C- Interface . . . 111
2.5.15.1 Slave mode sequence . . . 113
2.5.15.2 General call sequence . . . 114
2.5.15.3 Master mode sequence . . . 114
2.5.16 Serial Peripheral Interface SPI . . . 114
2.5.17 PROGRAMMING mode Operation . . . 117
2.5.17.1 FLASH Write Line . . . 117
2.5.17.2 FLASH Erase . . . 118
2.5.17.3 FLASH Check Erase Status . . . 120
2.5.17.4 FLASH Read Line . . . 121
2.5.17.5 FLASH Set Lockbyte 2 . . . 121
2.5.17.6 FLASH Set Lockbyte 3 . . . 121
2.5.17.7 Read Status . . . 122
2.5.18 DEBUG mode Operation . . . 123
2.5.18.1 Debug Special Function Registers . . . 123
2.5.18.2 Debugging Facility . . . 123
2.5.18.3 Debugger Commands . . . 124

3 Reference . . . 126

3.1 Electrical Data 126
3.1.1 Absolute Maximum Ratings 126
3.1.2 Operating Range 127
3.1.3 Product Characteristics 128
3.2 Reference SFR Registers 144
3.3 Reference Documents 157

4 Package Outlines 158

1 Product Description

1.1 Overview

The PMA7110 is a low power wireless FSK/ASK Transmitter with embedded microcontroller, which offers a single chip solution for various industrial, consumer and automotive applications in frequency bands 315/434/868/915 MHz. With its highly integrated mixed signal peripherals, PMA7110 requires only few external components. The operating voltage range is 1.9 - 3.6 V.

The PMA7110 contains

- 8051 based microcontroller
- Advanced power control system to minimize power consumption
- RF transmitter
- LF receiver
- Multifunctional interface for external Sensors and embedded temperature and battery voltage sensor

Measurement via embedded temperature and voltage sensor, reading signal from analog inputs (e.g. from external analog sensor) are performed under software control, so that the microcontroller can format and prepare this data for the RF transmission.

An intelligent power control system enables the build of ultra low power applications by using powersaving modes.

The integrated microcontroller is instruction set compatible to the standard 8051 processor. It is equipped with various peripherals (e.g. a hardware Manchester/BiPhase Encoder/Decoder and CRC Generator/Checker) enabling an easy implementation of customer-specific applications.

The low power consumption FSK/ASK Transmitter for 315/434/868/915 MHz frequency bands contains a fully integrated VCO, a PLL synthesizer, an ASK/ FSK modulator and an efficient power amplifier. Fine tuning of the center frequency can be done by an on-chip capacitor bank.

To store the microcontroller application program code and its unique ID-Number, an on-chip FLASH memory is integrated. Additional ROM storage is provided for the ROM library functions covering standard tasks required by various applications.

1.2 Features

- Supply voltage range from 1.9 V up to 3.6 V
- Operating temperature range -40 to +85 °C
- Low supply current
- Temperature sensor
- Battery voltage measurement
- Integrated RF- transmitter for ISM band 315/434/868/915 MHz
- Selectable transmit power 5/8/10 dBm into 50 Ohm load
- Transmit data rates up to 32kbit/s or 64kchips/s in manchester code
- FSK/ASK modulation capability
- Frequency deviation up to 100 kHz in FSK mode
- Fully integrated VCO and PLL synthesizer
- Crystal oscillator tuning on chip
- LF receiver with input signal amplitude of min. 0.25 mVpp
- LF receiver data rate from 2000 bit up to 4000 bit (Manchester/BiPhase coded)
- 8051 instruction set compatible microcontroller (cycle-optimized)
- 6 kbyte Flash Code and 2x128 bytes flash data memory (for user-application like EEPROM emulation)
- 12 kbyte ROM (for ROM library functions)
- 256 bytes RAM (128 bytes configurable to keep content in Power Down mode), 16 bytes XData memory (supplied in PowerDown)
- I^2C bus interface
- SPI bus interface
- 10 free programmable bidirectional GPIO pins with on chip pull-up/down resistors
- 4 independent 16 bit timers
- 10bit ADC with 3 pair differential channels (e.g. as IO for external sensors)
- Wakeup from POWER DOWN state using the Interval Timer, the LF receiver or external wakeup sources connected via a GPIO
- Manchester/BiPhase encoder and decoder
- Hardware CRC generator
- Pseudo Random Number Generator
- Watchdog timer
- on chip debugging via I^2C interface

Note:In PMA7110 the Thermal Shout down function is not used.

1.3 Applications

- Remote control systems for industrial and consumer applications
- Security- and Alarm-systems
- Home automation systems
- Automatic meter reading
- Active Tagging

2 Functional Description

2.1 Pin Description

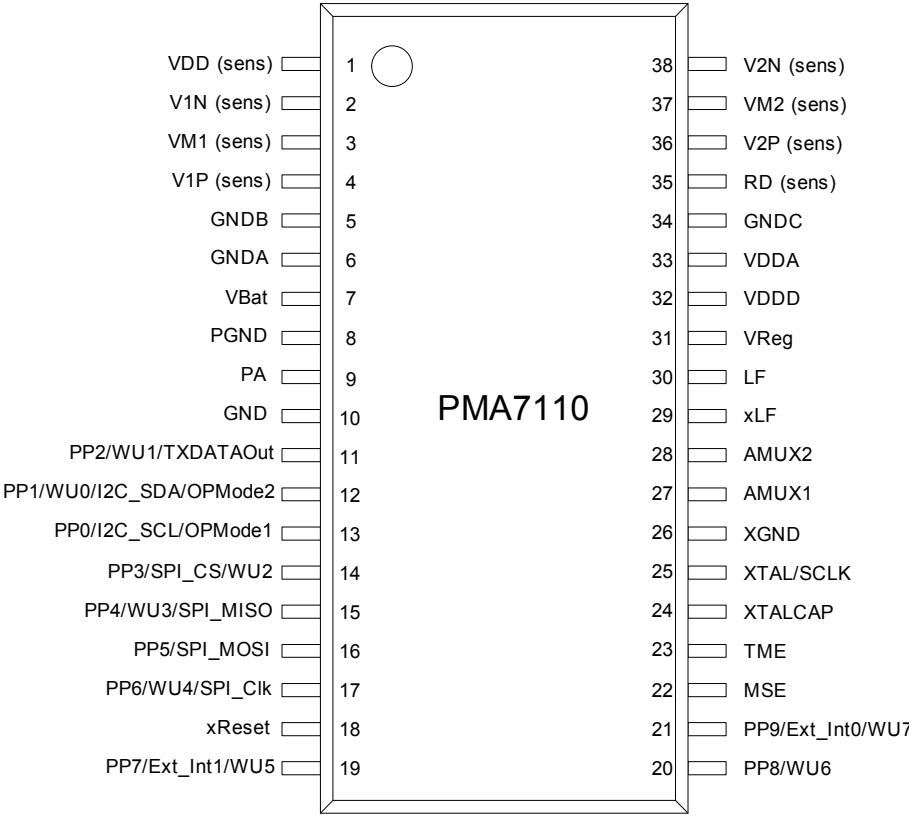


Figure 1 Pin-out of PMA7110 in TSSOP38 package

Table 1 Pin Description

Pin	Name	Type	Description	Comments
1	VDD(sens.)	Supply	Sensor positive supply	same voltage as chip analog supply
2	V1N(sens.)	Analog	Channel1, negative sensor input	output of wheatstone bridge sensor
3	VM1(sens.)	Supply	Sensor negative supply	same voltage as chip GND
4	V1P(sens.)	Analog	Channel1, positive sensor input	output of wheatstone bridge sensor
5	GNDB	Supply	Ground	
6	GNDA	Supply	Ground	
7	VBat	Supply	Battery supply voltage	
8	PGND	Supply	RF transmitter ground	
9	PA	Analog	RF transmitter output	
10	GND	Analog	Ground	
11	PP2/WU1/ TXDATAOut	Digital	GPIO, External wakeup source, Serial output of Manchester/Biphase encoded data	internal pullup/pulldown switchable
12	PP1/WU0/ I2C_SDA/ OPMode2	Digital	GPIO, External wakeup source, I2C bus interface data, Select operation mode	internal pullup/pulldown switchable
13	PP0/ I2C_SCL/ OPMode1	Digital	GPIO, I2C bus interface clock, Select operation mode	internal pullup/pulldown switchable
14	PP3/SPI_CS/ WU2	Digital	GPIO, SPI bus interface chip select, External wakeup source	internal pullup/pulldown switchable
15	PP4/WU3 /SPI_MISO	Digital	GPIO, SPI bus interface master in slave out, External wakeup source	internal pullup/pulldown switchable
16	PP5/ SPI_MOSI	Digital	GPIO, SPI bus interface master out slave in	internal pullup/pulldown switchable
17	PP6/WU4 /SPI_Clk	Digital	GPIO, SPI bus interface clock, External wakeup source	internal pullup/pulldown switchable

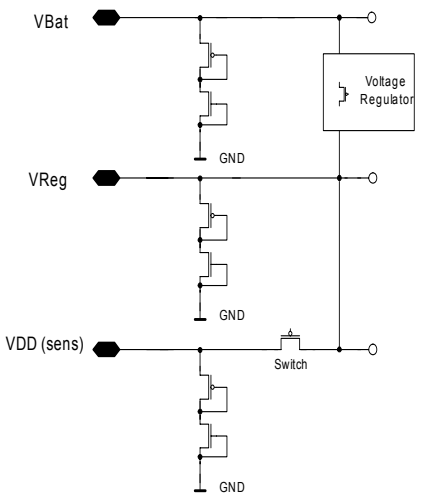
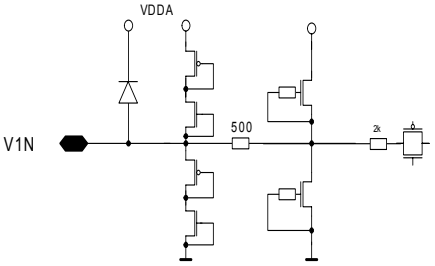
Table 1 Pin Description

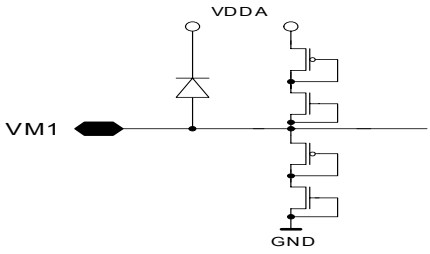
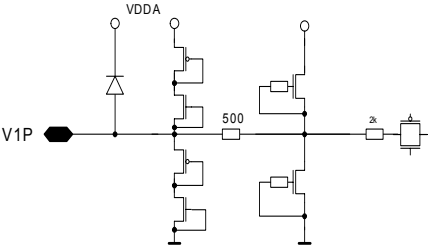
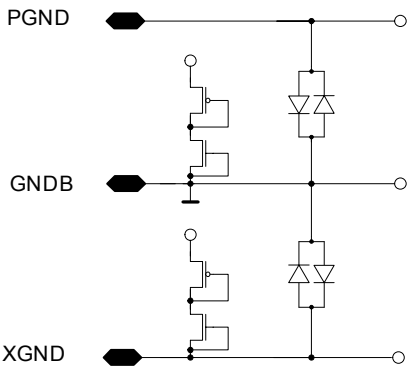
Pin	Name	Type	Description	Comments
18	xReset	Digital	External reset	low active
19	PP7/WU5 /Ext_Int1	Digital	GPIO, External wakeup source	internal pullup/pulldown switchable
20	PP8/WU6	Digital	GPIO, External wakeup source	internal pullup/pulldown switchable
21	PP9/WU7 /Ext_Int1	Digital	GPIO, External wakeup source, External Interrupt source	internal pullup/pulldown switchable
22	MSE	Digital	Mode select enable	high active, set to GND in normal mode
23	TME	Digital	Test mode enable	high active, set to GND in normal mode
24	XTALCAP	Analog	Crystal oscillator load capacitance	
25	XTAL/SCLK	Analog	Crystal oscillator input, External reference clock	
26	XGND	Supply	Crystal oscillator ground	
27	AMUX1	Analog	additional differential ADC standard input1 for external sensor	connect to GND if not use
28	AMUX2	Analog	additional differential ADC standard input2 for external sensor	connect to GND if not use
29	XLF	Analog	Differential LF receiver Input2	
30	LF	Analog	Differential LF receiver Input1	
31	VReg	Supply	Internal voltage regulator output	connect to decoupling capacitor (C_{BCAP}=100nF)
32	VDDD	Supply	Digital supply	
33	VDDA	Supply	Analog supply	
34	GNDC	Supply	Ground	
35	RD(sens.)	Analog		use only by having diagnostic resistor on sensor bridge, otherwise none connection

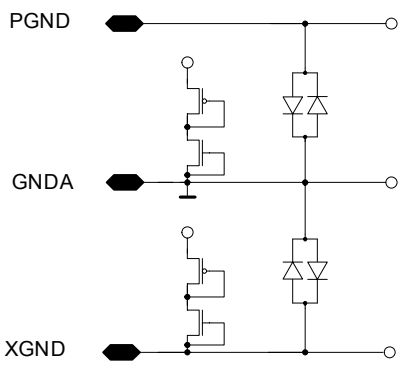
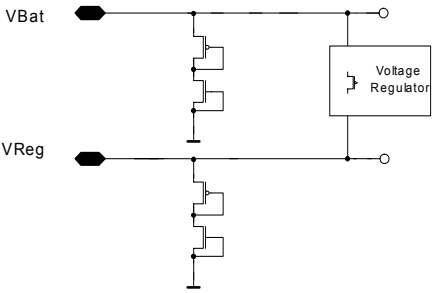
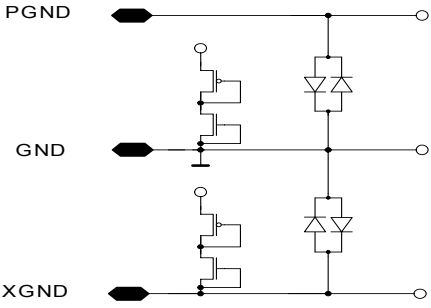
Table 1 Pin Description

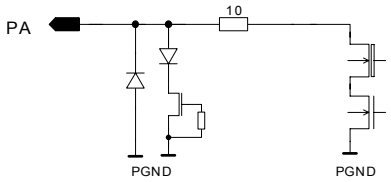
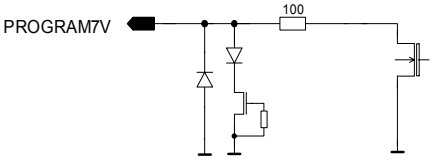
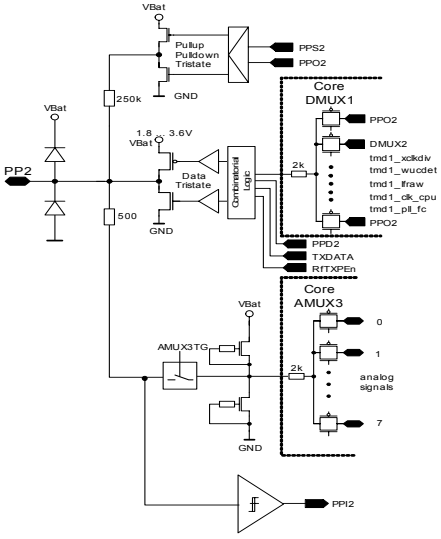
Pin	Name	Type	Description	Comments
36	V2P(sens.)	Analog	Channel2, positive sensor input	output of wheatstone bridge sensor
37	VM2(sens.)	Supply	Sensor negative supply	same voltage as chip GND
38	V2N(sens.)	Analog	Channel2, negative sensor input	output of wheatstone bridge sensor

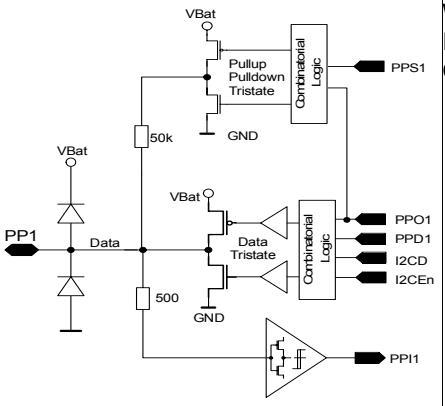
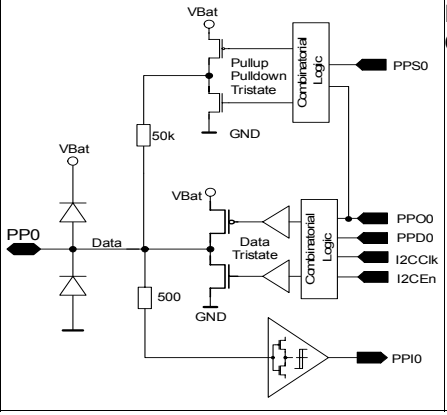
Table 2 Pin I/O equivalent schematics

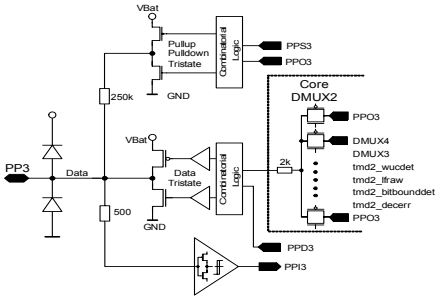
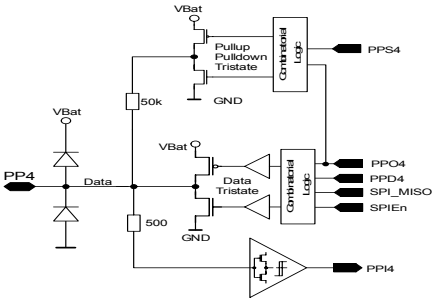
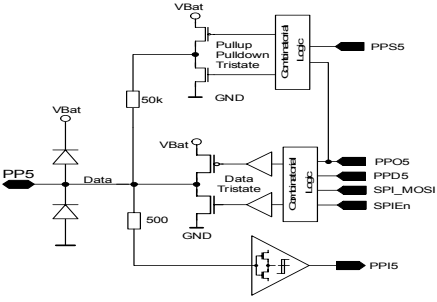
Pin No.	PAD name	Equivalent I/O Schematic	Function
1	VDD (Sens.)		Sensor Positive Supply
2	V1N (Sens.)		Channel 1 Negative Signal

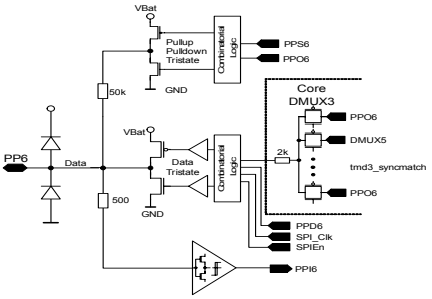
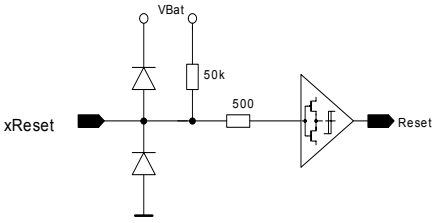
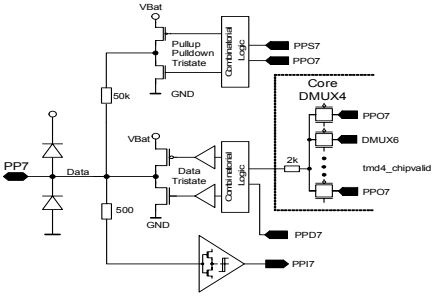
Pin No.	PAD name	Equivalent I/O Schematic	Function
3	VM1 (Sens.)		Channel 1 Negative Supply
4	V1P (Sens.)		Channel 1 Positive Signal
5	GNDB		Ground

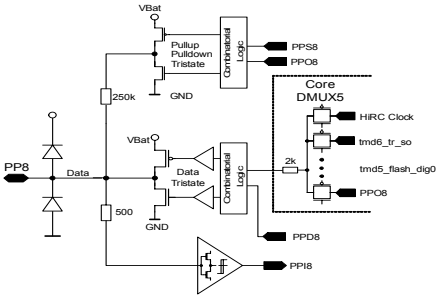
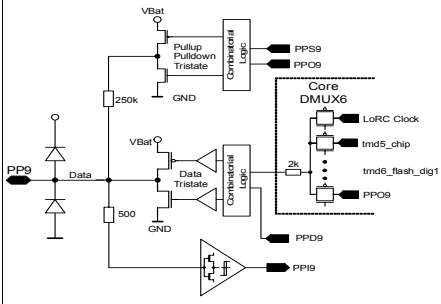
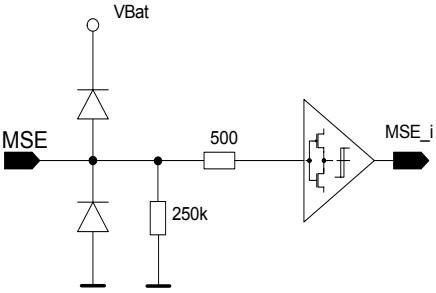
Pin No.	PAD name	Equivalent I/O Schematic	Function
6	GNDA		
7	VBat		Power supply voltage regulators
8	PGND double bond		Power amplifier ground

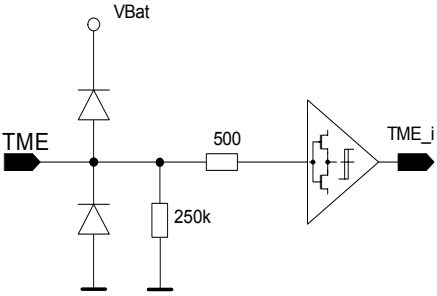
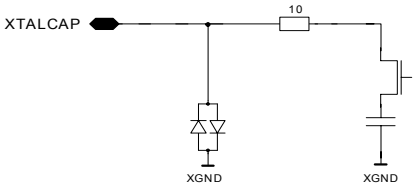
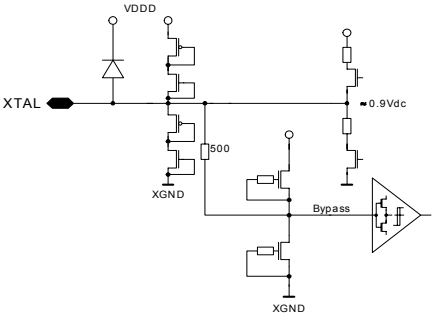
Pin No.	PAD name	Equivalent I/O Schematic	Function
9	PA		Power amplifier output stage
10	GND		
11	PP2/WU1 /TXDATAOut		GPIO port WU1 Serial output of Manchester/Biphase encoded data

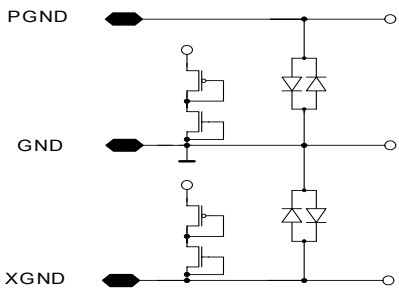
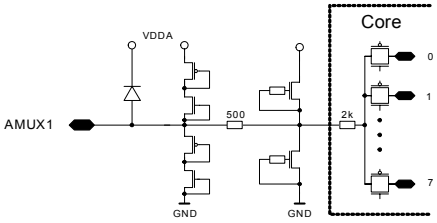
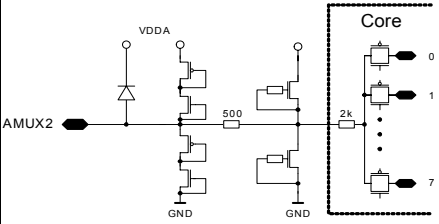
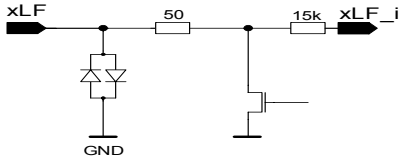
Pin No.	PAD name	Equivalent I/O Schematic	Function
12	PP1/ WU0/I2C_SDA /OPMode2		GPIO port WU0 I2C_SDA OPMode2
13	PP0/I2C_SCL /OPMode1		GPIO port I2C_SCL OPMode1

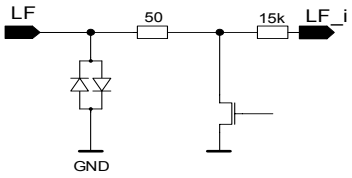
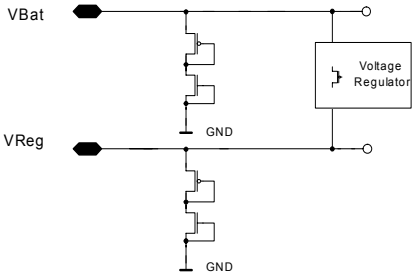
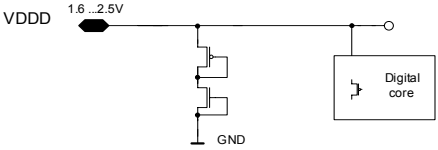
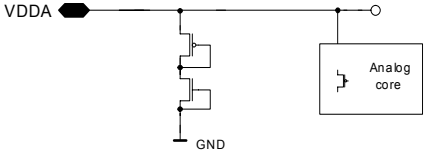
Pin No.	PAD name	Equivalent I/O Schematic	Function
14	PP3/SPI_CS /WU2		GPIO port WU2 SPI_CS
15	PP4/WU3 /SPI_MISO		GPIO port WU3 SPI_MISO
16	PP5/SPI_MOSI		GPIO port SPI_MOSI

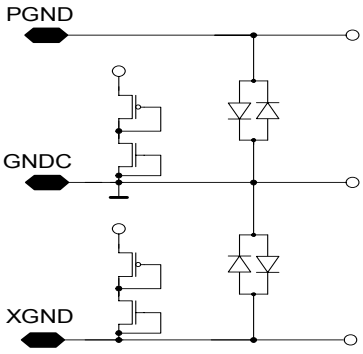
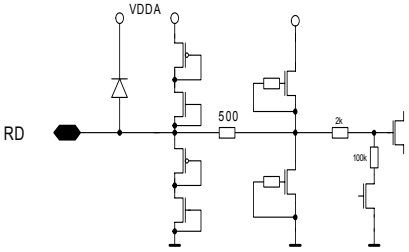
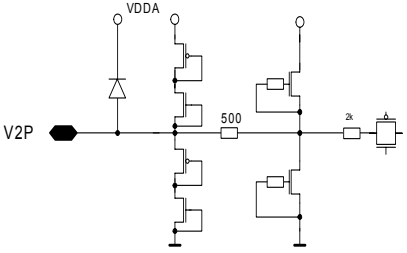
Pin No.	PAD name	Equivalent I/O Schematic	Function
17	PP6/WU4 /SPI_Clk		GPIO port WU4 SPI_Clk
18	xReset		Reset input
19	PP7/WU5 /Ext_Int1		GPIO port WU5 Ext_Int1

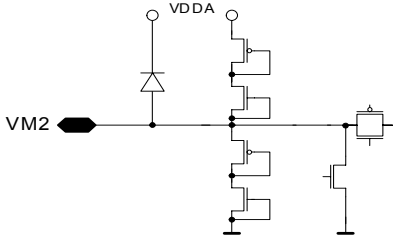
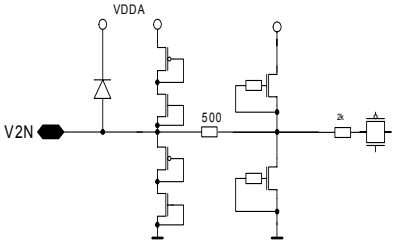
Pin No.	PAD name	Equivalent I/O Schematic	Function
20	PP8/WU6		GPIO port WU6
21	PP9/WU7 /Ext_Int0		GPIO port WU7 Ext_Int0
22	MSE		Mode Select Enable

Pin No.	PAD name	Equivalent I/O Schematic	Function
23	TME		Test Mode Enable
24	XTALCAP		Crystal oscillator output
25	XTAL/SCLK		Crystal oscillator input SCLK

Pin No.	PAD name	Equivalent I/O Schematic	Function
26	XGND		Crystal oscillator ground
27	AMUX1		Additional differential ADC standard input1 for external sensor, Analog Testsignal Port
28	AMUX2		Additional differential ADC standard input2 for external sensor, Analog Testsignal Port
29	xLF		Low Frequency Input

Pin No.	PAD name	Equivalent I/O Schematic	Function
30	LF		Low Frequency Input
31	VReg		Regulated Power supply
32	VDDD		Digital Supply
33	VDDA		Analog Supply

Pin No.	PAD name	Equivalent I/O Schematic	Function
34	GNDC		Ground
35	RD (sens.)		Connect to diagnostic resister on sensor bridge, otherwise no connection
36	V2P (sens.)		Channel 2 Positve Signal

Pin No.	PAD name	Equivalent I/O Schematic	Function
37	VM2 (sens.)		Channel 2 Negative Supply
38	V2N (sens.)		Channel 2 Negative Signal

2.2 Functional Block Diagram

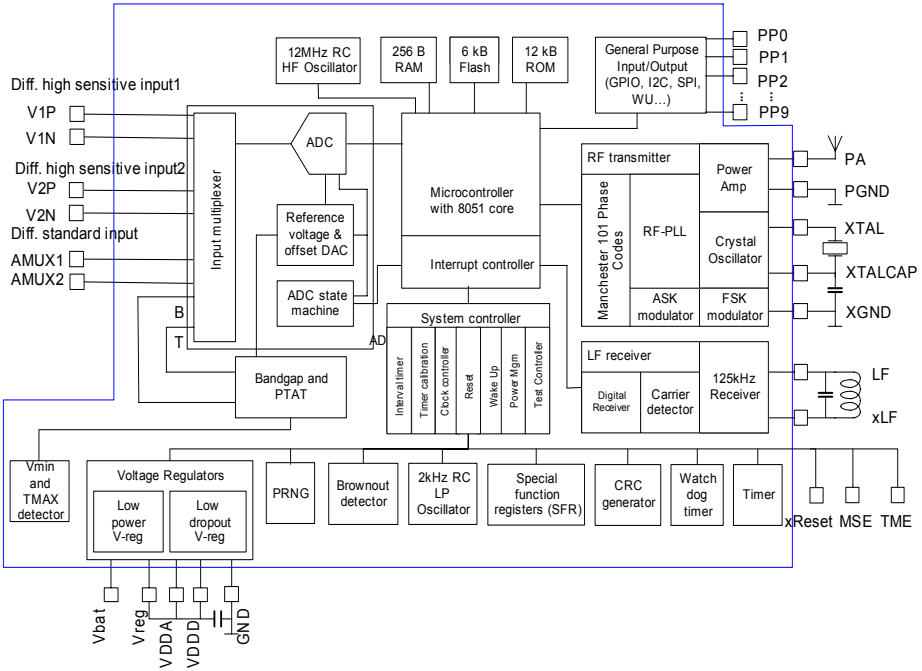


Figure 2 PMA7110 Block Diagram

2.3 Operating Modes and States

The PMA7110 can be operated in four different operating modes.

- NORMAL mode
- PROGRAMMING mode
- DEBUG mode
- (internal production TEST mode)

2.3.1 Operating mode selection

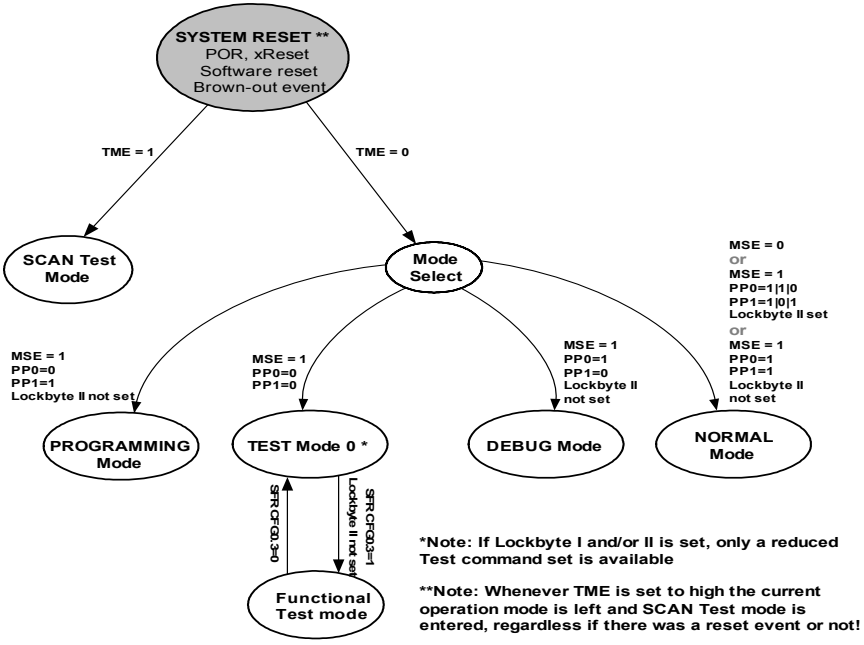


Figure 3 Operating mode selection of the PMA7110 after Reset

The Mode Select is entered after the System Reset expires and SCAN Test mode is not selected. The levels on the the I/O pins PP0 and PP1 are latched by the System controller and read by the operating system to determine the mode of operation of the device according to **Table 3 "Operating mode selection after Reset" on Page 30**. Therefore also the status of MSE and Lockbyte II from the FLASH are checked. The

MSE, PP0 and PP1 levels must not change after reset release during the whole t_{MODE} period (see **Figure 5 "Power On Reset - operating mode selection" on Page 32**).

Table 3 Operating mode selection after Reset

TME	MSE	Lock byte II	PP0	PP1	Operating mode	Devicecontrol	Hardware restrictions
1[3.)]	x	x	x	x	SCAN	external Test machine	n.a.
0	0	x	x	x	NORMAL	CPU executing from 4000h	Flash write disabled[2)]
0	1	x	0	0	TEST	TEST mode handler	None
0	1	not set	0	1	PROGRAMMING	PROGRAM mode handler	None
0	1	set	0	1	NORMAL	CPU executing from 4000h	Flash write disabled[2.)]
0	1	not set	1	0	DEBUG	DEBUG mode handler	Flash write disabled[2.)]
0	1	set	1	0	NORMAL	CPU executing from 4000h	Flash write disabled[2.)]
0	1	x	1	1	NORMAL	CPU executing from 4000h	Flash write disabled[2.)]

1.) Flash protection is done by hardware. In these modes setting the SFR bits FCS.3 [PROG] and FCS.2 [ERASE] is not possible.

2.) Flash programming and erasing is only possible via ROM Library functions.

3.) Whenever TME is set to high the current mode is left immediately and SCAN Test Mode is entered, regardless if there is a reset or not.

.

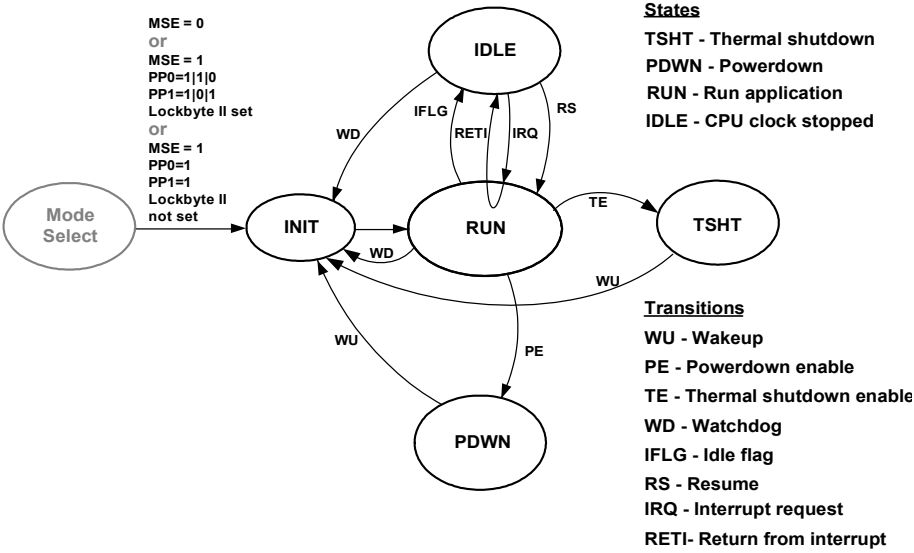


Figure 4 NORMAL Mode - State transistion diagram

For low power consumption and safety reasons the PMA7110 supports different operating states - *RUN* state, *IDLE* state and *POWER DOWN* mode and Thermal shutdown state. The device operation in these states is described below.

Transitions between these states are either application software controlled or managed automatically by the system controller.

- PDWN: Powerdown (CPU & Peripherrals stopped)
- IDLE: CPU clock stopped, peripherals are still running

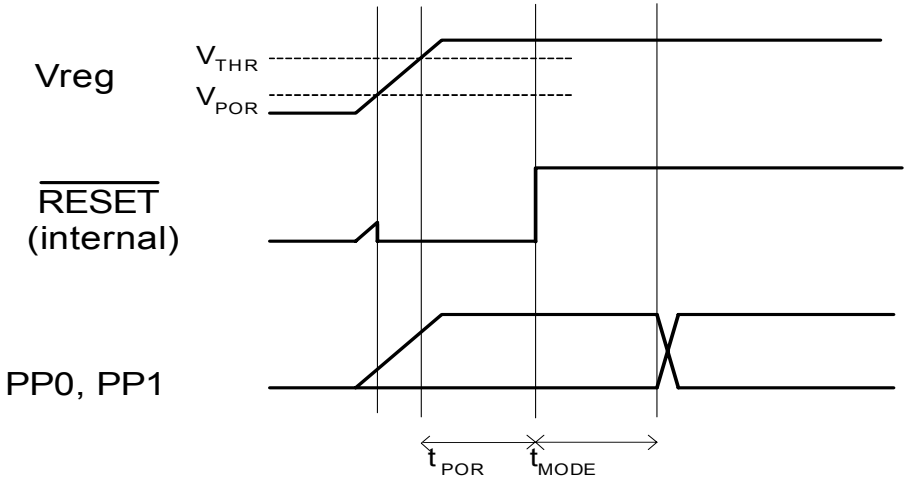


Figure 5 Power On Reset - operating mode selection

During the time t_{MODE}, the levels of PP0, PP1 and MSE are read, and being determined the operation mode of the device according to **Table 3 "Operating mode selection after Reset" on Page 30**. The levels on these pins must be stable during the whole t_{MODE} period.

The PMA7110's Power On Reset circuit is activated if Vreg rises above V_{POR}. The internal blocks are held in Reset state until Vreg has risen above V_{THR}.

When this Reset state is released, a further time of t_{MODE} is needed for reading the levels on PP0, PP1 and MSE. After t_{MODE} has elapsed, the device starts operation in the selected mode.

Note: See ***"Power On Reset" on Page 138*** *for details on Power On Reset characteristics.*

2.3.2 State Description

2.3.2.1 INIT State

This is a transient state which is entered when the settings of PP0, PP1, MSE, TSE and the Lockbyte II lead to Normal Mode (please refer to **Table 3 "Operating mode selection after Reset" on Page 30**). In this state, the SFRs which are not located in the System controller get reset and the ROM routines initializes the system to its default

values. Then the application Program in Flash is started at 4000h and the device enters RUN state.

2.3.2.2 RUN State

In RUN state the CPU8051 executes programs stored in ROM or FLASH memory. Peripherals are on or off according to the application program. The watchdog (WD) is active and automatically cleared when entering RUN state on a Wakeup event. The CPU clock frequency is selectable by software. All Wakeup events are ignored in RUN state but the corresponding flags get set and can be read and cleared.

2.3.2.3 IDLE State

In IDLE state, the CPU8051 clock is disabled but Peripherals (Timers, ADC, RF-TX, SPI, I^2C Interface and Manchester/Biphase Coder) continues normal operation. If a resume condition occurs the RUN state is reentered immediatelly. The watchdog (WD) is active and reset automatically when entering IDLE state. All wakeups are ignored in IDLE state but the corresponding flags are set if a wakeup occurs and can be evaluated once the device returns to the RUN state.

In case of a Peripheral requests, an interrupt or an External Interrupt occurs the IDLE state is left for RUN state, the Interrupt service routine is executed and on the next RETI (return from interrupt) instruction the IDLE State is re-entered in case no Resume event has occured in between.

Resume events:

The resume source can be identified by reading REF. Resume events may occur on following events:

- RF transmitter buffer empty.
- RF transmission finished.
- LF receiver buffer full.
- Timer 2 underflow.
- A/D conversion finished.
- RC-LP-Oscillator calibration finished.
- Clock change from RC-HF-Oscillator to Crystal-Oscillator finished.

Interrupt requests:

Interrupts during IDLE state may be requested by embedded peripherals or external events.

- External (Pin) Interrupt 0/1
- Timer 0/1/2/3

- I2C Interface
- SPI Interface
- LF Receiver
- RF Encoder

2.3.2.4 POWER DOWN State

In POWER DOWN state the CPU8051 and its peripherals are powered down. The system controller, its SFRs, the XData memory and optional the lower 128 byte internal RAM are kept powered. The LF receiver will be switched on periodically if the LF on/off timer is enabled. Wakeup flags are cleared automatically when going to POWER DOWN or THERMAL SHUTDOWN.

Wakeup Events:

A wakeup event occurs when a peripheral or external source causes the system to power up again. The wakeup source can be identified by reading SFRs WUF and ExtWUF. Wakeup Events may occur on following events:

- At least one of the External Wakeup Pins changed its state to the configured one
- Interval Timer underflow occured
- LF receiver carrier detected
- LF receiver pattern matched
- LF receiver sync matched
- Watchdog timer elapsed

2.3.2.5 THERMAL SHUTDOWN state

In THERMAL SHUTDOWN state, only the TMAX circuit can provide a wakeup event. All other wakeup sources are disabled. The device will remain in this state until the temperature falls below the T_{REL} threshold (see **“Functional Block Description” on Page 41** for details).

2.3.2.6 State Transitions

With reference to **Figure 4 "NORMAL Mode - State transistion diagram" on Page 31**, the following state transitions can occur:

Table 4 State Transitions in NORMAL mode

State transition	Description
RUN state => IDLE state (IFLG)	The application program can set SFR bit CFG0.5[IDLE][1] to enter IDLE state. Note that the next opcode should be a *NOP* instruction. (see **Table 11 "SFR Address $F8_H$: CFG0 - Configuration Register 0" on Page 58**) *Note: If no peripheral that can create a RESUME event is active, IDLE state will not be entered and the application will continue operation.*
IDLE state => RUN state (RS, IRQ)	**RS:** A peripheral unit (Timer 2, ADC, RF transmitter, LF receiver, System Clock source switch) creates a resume event. The application continues with the instruction after the Idle bit setting (see **Table 20 "SFR Address $D1_H$: REF - Resume Event Flag Register" on Page 67**). **IRQ:** An interrupt occurs. This interrupt allows the immediate execution of the interrupt service routine. With the return from interrupt instruction the device returns to IDLE state if no resume event has been generated in between.
IDLE state => INIT state (WD) **RUN state => INIT state (WD)**	Overflow of the watchdog timer. The application will restart by initialization of the SFRs that are located outside the SFR Container. No Mode selection is possible, the Normal Mode is not left. The watchdog wakeup may be identified by **Table 18 "SFR Address C0H: WUF - Wakeup Flag Register" on Page 65**
RUN state =>THERMAL SHUDOWN state (TE)	The application should enter Thermal Shutdown state whenever it detects that the specified operating temperature maximum of 125°C has been overreached to avoid malfunction of the device. This is done by setting the CFG0.6 [TSHDWN]. Alternatively this can be done via ROM library function. Note: If the temperature is below the TMAX threshold the device immediately generates a WU event and re-initializes the system
RUN state => POWER DOWN state (PDWN)	Entering this state is always software controlled by setting CFG0.7[PDWN]. The application program can call a ROM Library function to enter POWER DOWN state whenever needed.

State transition	Description
THERMAL SHUTDOWN state => RUN state (WU)	The TMAX circuit generates a wakeup event when the temperature falls below TMAX threshold.
POWER DOWN state => RUN state (WU)	A wakeup event will restart the application and set the SFR WUF resp. ExtWUF accordingly. The Watchdog timer is re-initialized (see **Table 19 "SFR Address F1H: ExtWUF - Wakeup Flag Register 2" on Page 65**). Wakeup duration from *POWER DOWN* mode to *RUN* state typically lasts 1410 µs. The time is the sum for the power supply to get stable (100µs), the startup time of the oscillator (1150 µs) and the time for the operating system to get initialized (160µs @12MHz CPU8051 clock).
INIT state => RUN state	This state change is initiated automatically by the system controller as soon as INIT state is finished.

1) [1] Note: It is mandatory that the instruction setting the CFG0.5[IDLE] is followed by a *NOP* instruction.

2.3.2.7 Status of PMA7110 Blocks in Different States

Depending of the actual state in NORMAL mode the internal blocks of the PMA7110 are active, inactive or have no supply to reduce power consumption. The next table gives an overview over the different blocks in the different device states.

Table 5 Status of important PMA7110 blocks in different states

Peripheral unit	RUN state	IDLE state	POWER DOWN state	THERMAL SHUTDOWN state
Power on reset	active	active	active	active
Brown-out detector	active	active	inactive power down	inactive power down
Power supply - Low drop voltage regulator	active	active	inactive power down (Remark: can be enabled by LF-RX)	inactive power down
Low power voltage supply	active	active	active	active
System controller	active	active	active	active
Wakeup Logic	active	active	active	active
CPU8051	active	inactive	no supply	no supply
Non-volatile SFRs (System Controller)	active	inactive content not lost	inactive content not lost	inactive content not lost
Peripheral core SFR's	active	inactive content not lost	no supply - content lost	no supply - content lost
Manchester/Biphase Coder, Timer	software selectable	software selectable	no supply	no supply
Pheripheral modules - CRC, MFLSR	software selectable	inactive	no supply	no supply
Peripheral modules -I2C, SPI, ADC	software selectable	software selectable	no supply	no supply
Watchdog	active	active	no supply	no supply

Peripheral unit	RUN state	IDLE state	POWER DOWN state	THERMAL SHUTDOWN state
RAM Lower 128Bytes	active	inactive content not lost	selectable power down (content lost) or inactive (content not lost)	selectable power down (content lost) or inactive (content not lost)
RAM Upper 128Bytes	active	inactive content not lost	no supply - content lost	no supply - content lost
XData 16 bytes	active	inactive content not lost	inactive content not lost	inactive content not lost
FLASH memory	active	inactive content not lost	no supply content not lost	no supply content not lost
ROM	active	inactive	no supply content not lost	no supply content not lost
Crystal oscillator	software selectable	software selectable	inactive power down	inactive power down
2kHz RC-Oscillator	active	active	active	inactive power down
12MHz RC-HF-Oscillator	software selectable	software selectable	power down (Remark: can be enabled by LF-RX)	power down
Interval timer	active	active	active	inactive
LF Receiver	software selectable	software selectable	software selectable	inactive power down
RF Transmitter	software selectable	software selectable	inactive power down	inactive power down

Peripheral unit	RUN state	IDLE state	POWER DOWN state	THERMAL SHUTDOWN state
Vmin Detector	software selectable	software selectable	no supply	inactive power down

Note: **active**: block is powered, is active and keeps its register contents. Power consumption is high
inactive: block is powered, cannot be used, but keeps its register contents. Power consumtion is low
no supply: block is not powered, connot be used and all register content is lost. Power consumption is zero

2.4 Fault protection

The PMA7110 features multiple fault protections which prevent the application from unexpected behavior and deadlocks. This chapter gives a brief overview of the available fault protections. Detailed explanation of the usage can be found later in this document and in [1] **“Reference SFR Registers” on Page 144**.

2.4.1 Watchdog Timer

For operation security a watchdog timer is available to avoid application deadlocks. The watchdog timer must be reset periodically by the microcontroller, otherwise the timer generates a software reset and forces a restart of PMA7110 program execution.
The watchdog timer duration is fixed to nominal 1 second. The accuracy depends on the accuracy of the 2 kHz RC LP Oscillator which is used to clock the watchdog timer.
Setting SFR bit CFG2.1[WDRES] resets the watchdog timer (see **Table 13 "SFR Address $D8_H$: CFG2 - Configuration Register 2" on Page 60**).

2.4.2 VMIN Detector

This circuit will detect if the supply voltage is below the minimum value required to guarantee the measurement accuracy. The ROM library functions which perform measurements will return the VMIN status in a statusbyte with the measurement result.

2.4.3 FLASH Memory Checksum

A CRC checksum is stored in the FLASH memory, and can be recalculated and checked by the application program for verification of program code if needed.

Flash bit FCSP.7[ECCErr]: If a single bit error in the Flash memory occurs it is corrected by the Flash internal Error Correction Coder, as an indication the FCSP.7[ECCErr] bit is set. (see **Table 101 "SFR Address $E9_H$: FCSP- Flash Control Register - Sector Protection Control" on Page 146** in **“Reference SFR Registers” on Page 144**)

2.4.4 ADC Measurement Overflow & Underflow

The ROM Library functions which perform measurements will return the over/underflow status in a statusbyte with the measurement result.

2.4.5 TMAX Detector

The TMAX detector is used to wakeup the PMA7110 from THERMAL SHUTDOWN state if the ambient temperature falls below the trigger level T_{REL}.
Entering THERMAL SHUTDOWN state can be initiated by a ROM Library function described in [1] **“Reference Documents” on Page 157**.

2.5 Functional Block Description

2.5.1 Sensor Interfaces and Data Acquisition

The PMA7110 has two internal sensors, two high sensitive differential analog interfaces 4 programmable gainfactors (from 76+-20%, 60+-20%, 50+-20% and 38+-20%) and one standard differential analog interface (gainfactor 1) to acquire environmental data:

- Temperature Sensor
- Battery Voltage Monitoring
- external data through analog interface

The analog data is aquired and digitalized by the internal 10 Bit ADC. Measurement routines for acquiring data are available within the ROM library functions that are described in [1] **“Reference Documents” on Page 157**.

2.5.1.1 Sensor Interface

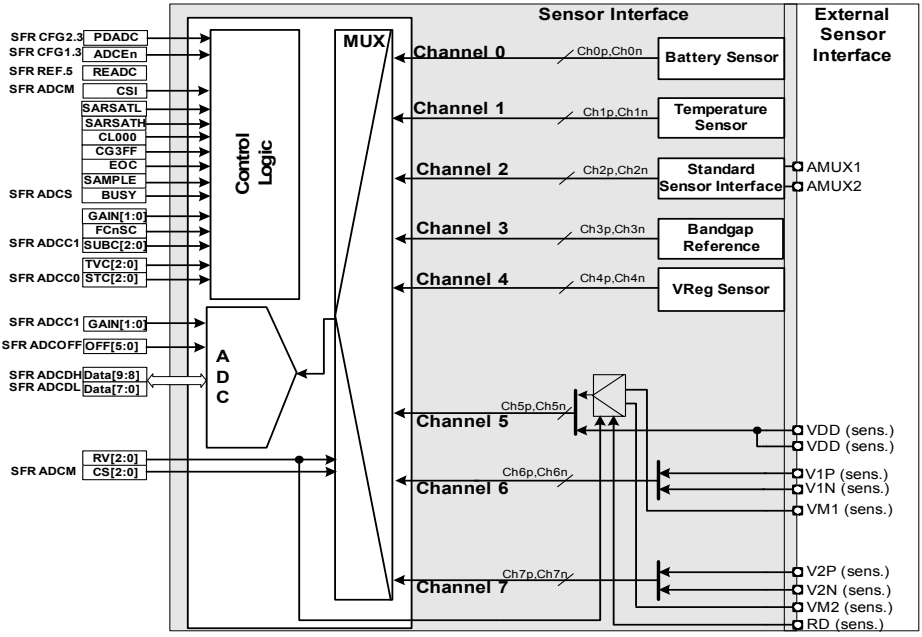


Figure 6 Block diagram Sensor Interface

The sensor interface connects to the external sensors and to the internal (on-chip) temperature and battery voltage sensors.

All signal channels can be configured for differential or single-ended operation. Differential operation is only recommended for signals where the common-mode voltage is stable, while the positive and negative signal voltages vary symmetrically around the common-mode voltage.

The input multiplexer selects one channel for the input signal and one channel for the reference voltage to the ADC. Any channel can be selected as reference, except channels 6 and 7, which are specially adapted to the low level signals from external sensors.

2.5.1.2 Two differential high sensitive interfaces to external Sensors

Differential high sensitive sensor interface 1((Channel 6)

V1P/V1N is the positve/negative differential voltage inputs of the first sensor bridge.

Differential high sensitive sensor interface 2 (Channel 7)

V2P/V2N is the positve/negative differential voltage inputs of the second sensor bridge.

Channel gain selection

The SFR Bit ADCC1.5-4 [GAIN1-0] gain factor selection allows the selection of the sensitivity of the analog input channels 6 and 7. The gain is one for all other input channels (see **Table 6**).

Table 6 Selection of the gain factor

Gain factor (gain)	Channel ADCM.CS2-0	GAIN1	GAIN0
76 +/- 20%	11X	0	0
60 +/- 20%	11X	0	1
50 +/- 20%	11X	1	0
38 +/- 20%	11X	1	1
1	others	0	0
1	others	0	1
1	others	1	0
1	others	1	1

Sensor Excitation

The two sensor bridges have a common positive supply which is always connected. When a sensor bridge is to be activated, its negative supply is pulled to ground by pad VM1 or VM2 for VMP or VMA. Otherwise, it is disconnected. In this way the power of a connected bridge can be supplied.

These two sensor interfaces are very adapted piezoresistive Wheatstone bridge sensors, whose output signal is differential and ratiometric (proportional to the bridge excitation voltage). The electrical configuration is shown as a example in figure below..

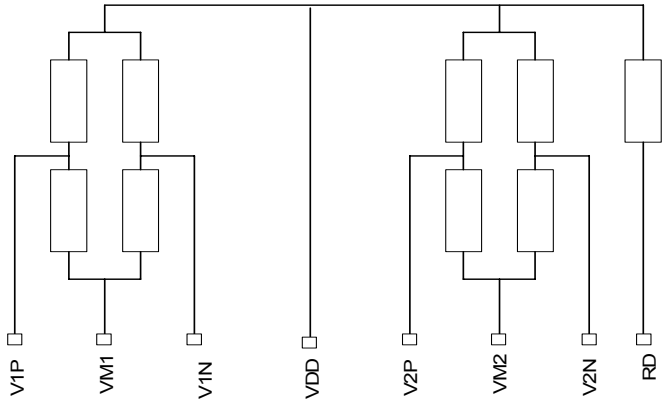


Figure 7 Wheatstone bridge sensor

2.5.1.3 Interface to other signals

Battery voltage Interface (Channel 0)

The positive input to the battery voltage signal is derived by dividing voltage V_{Bat} by 3.5. The negative input is connected to GND. The battery voltage is converted with a resolution of approximately 4.1mV, using channel 3 as reference.

Temperature Sensor Interface (Channel 1)

The temperature signal to the ADC is a single ended signal, with the PTAT voltage between 500 and 1100 mV. The temperature sensor signal is digitized with a resolution of approximately 0.5°C, using channel 3 as reference.

Standard sensor Interface (Channel 2)

The positive input signal is available at AMUX1, and the negative input at AMUX2.

2.5.1.4 Reference voltages

When channel 6 or 7 is selected as input to the ADC, and the negative external sensor supply is identical to the negative supply of ADC, this negative supply should be selected by the multiplexer as reference voltage on channel 5.

If the negative external sensor supply (which should be used as reference voltage to external sensor) is not identical to the negative supply of ADC, it should be connected to the Channel 2 so that it can be selected by multiplexer as reference voltage for channel 6 or 7. But the supply voltage of the external sensor must always be within the range GND to V_{BATT}

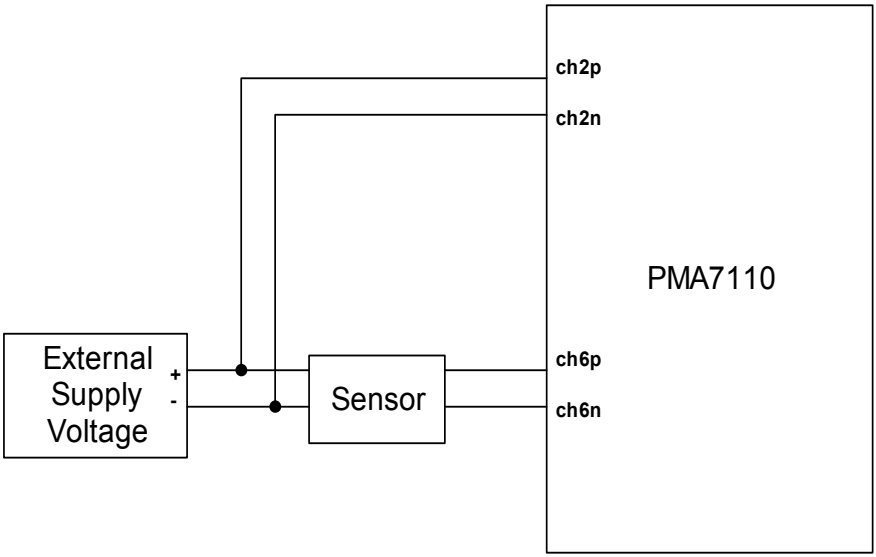


Figure 8 External Sensor use channel 2 as reference voltage

Additional 3 channels on ADC input multiplexer carry voltages which are intended as reference voltages for the converter:

BANDGAP Reference (Channel 3)

This reference is a nominal voltage of 1210 mV. It is intended as reference for the temperature and V_{Bat} measurements.

VREG Reference (Channel 4)

This reference is the V_{REG} voltage. This is the largest allowable input voltage to the ADC, and is meant as reference for the test signal, to allow as large test signal as possible.

BRIDGE SUPPLY Reference (Channel 5)

When channel 6 or 7 is selected as input to the ADC, the reference voltage is the bridge supply voltage. A multiplexer selects the appropriate negative bridge supply.

2.5.1.5 Temperature Sensor

Temperature measurement is performed by a dedicated ROM library function.

See **“Temperature Sensor Characteristics” on Page 128** for the sensor specification.

2.5.1.6 Battery Voltage Monitor

Battery Voltage measurement is performed by a dedicated ROM library function.

See **“Battery Sensor Characteristics” on Page 128** for the sensor specification.

2.5.2 Memory Organization and Special Function Registers (SFR)

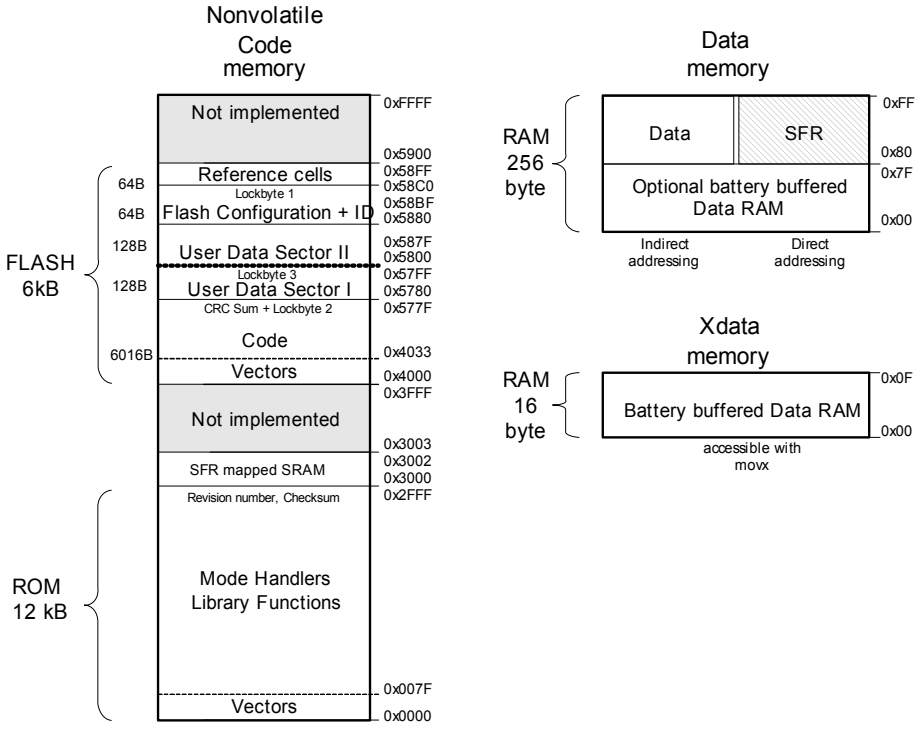


Figure 9 Memory map

The following memory blocks are implemented:

- 12 kByte ROM Memory
- 3 Byte SFR mapped Code Memory
- 6 kByte Flash Code Memory
- 2x128 Bytes FLASH User Data Memory
- 128 Bytes Flash Configuration, ID and Reference cells
- 2 x 128 Byte Data RAM / thereof 128 bytes battery buffered optionally
- 16 bytes battery buffered XData RAM

2.5.2.1 ROM

A 12 kB ROM memory is located in address range 0000_H to $2FFF_H$.

ROM library functions and Reset/Wakeup Handlers

The ROM contains the reset handler, the wakeup handler and the ROM Library functions (see [1] **“Reference SFR Registers” on Page 144**).

A hardware mechanism is implemented to prevent direct jumping into the ROM area, thus access to the ROM library functions is granted via a vector table at the bottom of the ROM address space.

ROM protection

To protect the ROM code against readout a hardware mechanism is implemented, thus a read operation from the ROM in the protected address area returns zero.

2.5.2.2 FLASH

FLASH Organization

The FLASH is divided into five sectors. Each sector can be erased and written individually (Bytewise erasing and writing is not possible).

- **4000_H -- $577F_H$ (6016 Bytes) code sector (sector 0):** This sector contains the Code sector for the application program.

- **5780_H -- $587F_H$ (2x128 Bytes) User Data sector I + User Data sector II (sector 1 + sector 2):** These two sectors contain the User Data Sector which can store individual device configuration data. It also contains the crystal frequency which is needed for the ROM Library functions.
- **5880_H -- $58BF_H$ (64 Bytes) configuration sector (sector 3):** This sector contains the FLASH configuration sector for FLASH driver parameters.

- **$58C0_H$ -- $58FF_H$ (64 Bytes) reference cells sector (sector 4):** This sector contains the reference current generator cells for FLASH reading.

FLASH protection

Write and erase operations on the Flash Code Sector are only allowed in PROGRAMMING mode. To protect the FLASH against unauthorized access three lockbytes can be set:

- **Lockbyte 1:** Address 0x58FF (Top address of Flash Configuration + Reference Cells Sector).
  This is written in the end of production test. Whenever the Resethandler detects this value the FCSP.0[ConfLock] gets set and the Reference Cells Sector, Flash Configuration Sector are irreversibly switched to read-only.
- **Lockbyte 2:** Address 0x577F (Top address of the Code Sector).
  This byte is written (also a ROM CRC) by the Programmer together with the Code download. When the Resethandler detects this byte it sets the FCSP.1[CodeLCK]. In addition the Debug Mode, Programming Mode and Test Mode are no longer accessible. Their pin settings lead to Normal Mode and reduced TM wherein the CRC can be checked (pass/fail) and the whole Flash can be erased to reset the chip to shipping state. This Lockbyte has to be set during programming the Code Sector to protect application code against undesired read-out.

- **Lockbyte 3:** Address 0x587F (Top address of the User Data Sector I and User Data Sector II).
  There is a ROM Library function for setting this byte. (Therefore the data in the User

Data Sector have to be captured into RAM, the Lockbyte added, the whole sector erased (Flash!) and re-written. Whenever the Resethandler detects this value DSR.0[FlashLCK] gets set. When not written together with the Code Sector the User Data Sector is planned to be written in Normal Mode (from the Customer) using ROM Library functions. There is a HW mechanism that blocks access to the Flash Registers when operating from the Flash (not ROM). In this way, the usage of ROM Library functions is guaranteed, they ensure several important details not to damage the chip. If Lockbyte 3 is set without setting Lockbyte 2, this byte shows no effect and will result a unlocked FLASH. How to set Lockbyte 3 is described in **“FLASH Set Lockbyte 3” on Page 121**.

2.5.2.3 RAM

The RAM is available as data storage for the application program. ROM library functions may use some RAM locations for passing parameters and internal calculations. The RAM area which is used for the ROM library functions is specified in [1] **“Reference Documents” on Page 157**.
The RAM is always powered in RUN state and IDLE state.
The upper 128 bytes of RAM are always switched off in POWER DOWN state and THERMAL SHUTDOWN state and lose their contents in these states.
SFR bit CFG2.4[PDLMB] determines if the lower 128 bytes of RAM are powered during POWER DOWN state and THERMAL SHUTDOWN state.
If not powered in these states, this RAM loses the content, otherwise it can be used as battery buffered storage beyond a POWER DOWN period.

Note: The RAM is not reset at a System Reset. After a Brown Out Reset this feature can be used to possibly recover data from RAM.
After Power On Reset the RAM is not initialized, thus it contains random data. The application has to initialize the RAM if needed.

2.5.2.4 Special Function Registers

Special Function Registers are used to control and monitor the state of the PMA7110 and its peripherals. The following table shows the naming convention for the SFR descriptions that are used throughout this document.

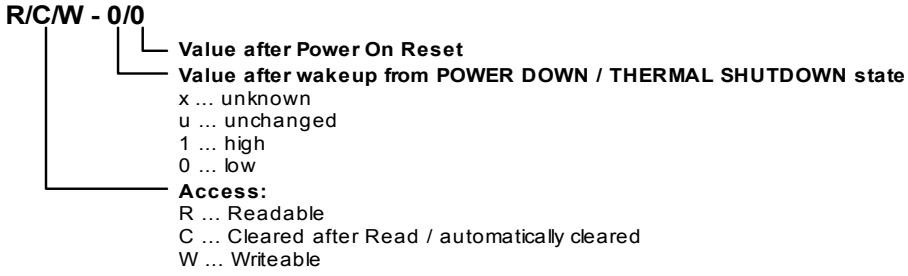


Figure 10 Naming convention for Register descriptions

Note: If a single bit or the whole byte value is declared as unchanged, it keeps its state even during POWER DOWN state or THERMAL SHUTDOWN state.

Table 7 "SFR Special Function Register Address Overview" on Page 53 shows all available registers of the PMA7110.

*Note: All SFRs that are listed in **Table 7 "SFR Special Function Register Address Overview" on Page 53** but not in **Table 8 "Status of SFR Registers in***

POWER DOWN state" on Page 53 should not be changed by the application since they could be damaged irreversibly. These are handled automatically by the ROM Library functions if needed.

Table 7 SFR Special Function Register Address Overview

Addr	Register	Addr	Register	Addr	Register	Addr	Register	Addr	Register	Addr	Register	Addr	Register	Addr	Register
F8	CFG0	F9	LFRXC	FA		FB		FC		FD		FE		FF	
F0	B	F1	EXTWUF	F2	EXTWUM	F3	SPIB	F4	SPIC	F5	SPID	F6	SPIM	F7	SPIS
E8	CFG1	E9	FCSP	EA	FCS	EB	P3DIR	EC	P3IN	ED	P3SENS	EE	RFC	EF	LBD
E0	ACC	E1	FCPP0	E2	FCPP1	E3	FCSERM	E4	FCTKAS	E5	FCSS	E6	RFS	E7	RFENC
D8	CFG2	D9	DSR	DA	ADCOFF	DB	ADCC0	DC	ADCC1	DD	ADWBC	DE	RFVCO	DF	RFFSLD
D0	PSW	D1	REF	D2	ADCM	D3	ADCS	D4	ADCDL	D5	ADCDH	D6	OSCCONF	D7	RFFSPLL
C8	TCON2	C9	TMOD2	CA	TL3	CB	TH3	CC	TL2	CD	TH2	CE	LFP1L	CF	LFP1H
C0	WUF	C1	WUM	C2	XTCFG	C3	XTAL1	C4	XTAL0	C5	LFOOTP	C6	LFOOT	C7	LFPCFG
B8	IP	B9	DIVIC	BA	ITPL	BB	ITPH	BC	ITPR	BD	TMAX	BE	LFPOL	BF	LFPOH
B0	P3Out	B1	I2CB	B2	LFCDFIt	B3	LFDIV0	B4	LFDIV1	B5	LFCDM	B6	LFRX1	B7	LFRX0
A8	IE	A9	CRCC	AA	CRCD	AB	RNGD	AC	CRC0	AD	CRC1	AE	RFTX	AF	LFSYNCFG
A0	P2 (reserved)	A1	P2Dir (reserved)	A2	I2CC	A3	I2CM	A4	LFRXS	A5	LFRXD	A6	LFSYN0	A7	LFSYN1
98	SCON (reserved)	99	SBUF (reserved)	9A	I2CD	9B	I2CS	9C	DBCL1	9D	DBCH1	9E	DBTL1	9F	DBTH1
90	P1OUT	91	P1DIR	92	P1IN	93	P1SENS	94	DBCL0	95	DBCH0	96	DBTL0	97	DBTH0
88	TCON	89	TMOD	8A	TL0	8B	TL1	8C	TH0	8D	TH1	8E	RFD	8F	IRQFR
80	P0 (reserved)	81	SP	82	DPL	83	DPH	84	MMR0	85	MMR1	86	MMR2	87	PCON

The following tabe shows which SFRs keep their content in POWER DOWN state *and THERMAL SHUTDOWN state* and gives a reference to the page within this document where a detailed description can be found.

Table 8 Status of SFR Registers in POWER DOWN state

SFR (Abbr.)	Addr	Register description	POWER SUPPLY		Description Page
			VDDD	VDDC Note:	
ACC	0xE0	Accumulator		n	Page 57
ADCC0	0xDB	ADC Configuration Register 0		n	Page 144
ADCC1	0xDC	ADC Configuration Register 1		n	Page 144
ADCDL	0xD4	ADC Result Register (low byte)		n	Page 151
ADCDH	0xD5	ADC Result Register (high byte)		n	Page 151.
ADCM	0xD2	ADC Mode Register		n	Page 145.
ADCOFF	0xDA	ADC Input Offset c-network configuration		n	Page 145.
ADCS	0xD3	ADC Status Register		n	Page 146.
ADWBC	0xDD	AD WBC Wire Bond Check		n	Page 146.
B	0xF0	Register B		n	Page 57.
CFG0	0xF8	Configuration Register 0	n		Page 58
CFG1	0xE8	Configuration Register 1	n		Page 59
CFG2	0xD8	Configuration Register 2	n		Page 60
CRCC	0xA9	CRC Control Register		n	Page 87
CRCD	0xAA	CRC Data Register		n	Page 151
CRC0	0xAC	CRC Shift Register (low byte)		n	Page 151
CRC1	0xAD	CRC Shift Register (high byte)		n	Page 152

SFR (Abbr.)	Addr	Register description	POWER SUPPLY		Description Page
			VDDD	VDDC Note:	
DBCL0	0x94	CPU Debug Compare Register 0 (low)		n	Page 152
DBCH0	0x95	CPU Debug Compare Register 0 (high)		n	Page 152
DBTL0	0x96	CPU Debug Target Register 0 (low)		n	Page 152
DBTH0	0x97	CPU Debug Target Register 0 (high)		n	Page 152
DBCL1	0x9C	CPU Debug Compare Register 1 (low)		n	Page 152
DBCH1	0x9D	CPU Debug Compare Register 1 (high)		n	Page 152
DBTL1	0x9E	CPU Debug Target Register 1 (low)		n	Page 153
DBTH1	0x9F	CPU Debug Target Register 1 (high)		n	Page 153
DIVIC	0xB9	Internal Clock Divider	n		Page 71
DPL	0x82	Data Pointer (low)		n	Page 57
DPH	0x83	Data Pointer (high)		n	Page 57
DSR	0xD9	Diagnosis and Status Register		n	Page 60
ExtWUF	0xF1	Wakeup Flag Register 2	n		Page 65
ExtWUM	0xF2	Wakeup Mask Register 2	n		Page 65
FCSP	0xE9	Flash Control Register - Sector Protection Control		n	Page 146
FCS	0xEA	Flash Control Register - Status Mode		n	Page 147.
FCPP0	0xE1	Flash Charge Pumps Power Control Register 0		n	Page 147
FCPP1	0xE2	Flash Charge Pumps Power Control Register 1		n	Page 147
FCSERM	0xE3	Flash Sector Erase and Read Margin Select Register		n	Page 148.
FCTKAS	0xE4	Flash Tkill and Analog Output Select Register		n	Page 153
FCSS	0xE5	Flash Control Register for Single-Step Mode		n	Page 154
I2CB	0xB1	I2C Baudrate Register		n	Page 112
I2CC	0xA2	I2C Control Register		n	Page 111
I2CD	0x9A	I2C Data Register		n	Page 112
I2CM	0xA3	I2C Mode Register		n	Page 113
I2CS	0x9B	I2C Status Register		n	Page 112
IE	0xA8	Interrupt Enable Register		n	Page 76
IP	0xB8	Interrupt Priority Register		n	Page 77
IRQFR	0x8F	Interrupt Request Flag Register (for extended interrupts)		n	Page 77
ITPL	0xBA	Interval Timer Precounter Register (Low Byte)	n		Page 69
ITPH	0xBB	Interval Timer Precounter Register (High Byte)	n		Page 69
ITPR	0xBC	Interval Timer Period Register	n		Page 68
LBD	0xEF	Low Battery Detector Control		n	Page 154
LFCDFlt	0xB2	t.b.d	n		t.b.d
LFCDM	0xB5	t.b.d	n		t.b.d
LFDIV0	0xB3	t.b.d	n		t.b.d
LFDIV1	0xB4	t.b.d	n		t.b.d
LFOOT	0xC6	t.b.d	n		t.b.d
LFOOTP	0xC5	t.b.d	n		t.b.d
LFPCFG	0xC7	t.b.d	n		t.b.d
LFP0L	0xBE	t.b.d	n		t.b.d
LFP0H	0xBF	t.b.d	n		t.b.d
LFP1L	0xCE	t.b.d	n		t.b.d

SFR (Abbr.)	Addr	Register description	POWER SUPPLY		Description Page
			VDDD	VDDC Note:	
LFP1H	0xCF	t.b.d	n		t.b.d
LFRX0	0xB7	t.b.d	n		t.b.d
LFRX1	0xB6	t.b.d	n		t.b.d
LFRXC	0xF9	t.b.d	n		t.b.d.
LFRXD	0xA5	t.b.d	n		t.b.d
LFRXS	0xA4	t.b.d	n		t.b.d.
LFSYNCFG	0xAF	t.b.d	n		t.b.d.
LFSYN0	0xA6	t.b.d	n		t.b.d
LFSYN1	0xA7	t.b.d	n		t.b.d
MMR0	0x84	Memory Mapped Register 0		n	Page 148
MMR1	0x85	Memory Mapped Register 1		n	Page 148
MMR2	0x86	Memory Mapped Register 2		n	Page 150
OSCCONF	0xD6	RC HF Oscillator Configuration Register	n		Page 155
P0 (reserved)	0x80	IO-Port 0 Data Register			n.u.
P1DIR	0x91	IO-Port 1 Direction Register	n		Page 106
P1IN	0x92	IO-Port 1 Data IN Register	n		Page 107
P1OUT	0x90	IO-Port 1 Data OUT Register	n		Page 106
P1SENS	0x93	IO-Port 1 Sensitivity Register	n		Page 107
P3DIR	0xEB	IO-Port 3 Direction Register	n		Page 106
P3IN	0xEC	IO-Port 3 Data IN Register	n		Page 107
P3OUT	0xB0	IO-Port 3 Data OUT Register	n		Page 106.
P3SENS	0xED	IO-Port 3 Sensitivity Register	n		Page 107
P2 (reserved)	0xA0	IO-Port 2 Data Register			n.u.
P2Dir (reserved)	0xA1	IO-Port 2 Direction Register			n.u.
PCON (reserved)	0x87	Power Control Register			n.u.
PSW	0xD0	Program Status Word		n	Page 57
REF	0xD1	Resume Event Flag Register		n	Page 67
RFC	0xEE	RF-Transmitter Control Register	n		Page 79
RFD	0x8E	RF-Encoder Tx Data Register		n	Page 82
RFENC	0xE7	RF-Encoder Tx Control Register		n	Page 82
RFFSPLL	0xD7	RF-Frequency Synthesizer PLL Configuration	n		Page 155.
RFS	0xE6	RF-Encoder Tx Status Register		n	Page 84
RFFSLD	0xDF	RF-Frequency Synthesizer Lock Detector Configuration	n		Page 151
RFTX	0xAE	RF-Transmitter Configuration Register	n		Page 79
RFVCO	0xDE	RF-Frequency Synthesizer VCO Configuration	n		Page 151
RNGD	0xAB	RNG Data Register	n		Page 89
SBUF (reserved)	0x99	Serial Interface Buffer			n.u.
SCON (reserved)	0x98	Serial Interface Control Register			n.u.
SP	0x81	Stack Pointer		n	Page 149.
SPIB	0xF3	SPI Baudrate Register (11 Bit cascaded register)		n	Page 117
SPIC	0xF4	SPI Control Register		n	Page 115
SPID	0xF5	SPI Data Register		n	Page 116
SPIM	0xF6	SPI Mode Register		n	Page 116

SFR (Abbr.)	Addr	Register description	POWER SUPPLY		Description Page
			VDDD	VDDC Note:	
SPIS	0xF7	SPI Status Register		n	Page 116
TCON	0x88	Timer Control Register (Timer 0/1)		n	Page 92
TCON2	0xC8	Timer Control Register 2 (Timer 2/3)		n	Page 93
TH0	0x8C	Timer 0 Register High Byte		n	Page 150
TH1	0x8D	Timer 1 Register High Byte		n	Page 149
TH2	0xCD	Timer 2 Register High Byte		n	Page 150
TH3	0xCB	Timer 3 Register High Byte		n	Page 150
TL0	0x8A	Timer 0 Register Low Byte		n	Page 150
TL1	0x8B	Timer 1 Register Low Byte		n	Page 150
TL2	0xCC	Timer 2 Register Low Byte		n	Page 150
TL3	0xCA	Timer 3 Register Low Byte		n	Page 150
TMOD	0x89	Timer Mode Register		n	Page 90
TMOD2	0xC9	Timer Mode Register 2 (Timer 2/3)		n	Page 91
TMAX	0xBD	TMAX Detector Control	n		Page 156
WUF	0xC0	Wakeup Flag Register	n		Page 65
WUM	0xC1	Wakeup Mask Register	n		Page 64
XTAL0	0xC4	XTAL Frequency Register (FSKLOW)	n		Page 73
XTAL1	0xC3	XTAL Frequency Register (FSKHIGH/ASK)	n		Page 73
XTCFG	0xC2	XTAL Configuration Register		n	Page 72

Note: Power Supply VDDC switched off during POWER DOWN state Register value will be lost.

2.5.3 Microcontroller

Central part of the PMA7110 is an CPU8051 instruction set compatible microcontroller. The CPU8051 offers an 8-bit datapath, an interrupt controller, several addressing modes (direct, register, register indirect, bit direct), and accesses peripheral components using Special Function Registers (SFR). The architecture of the CPU8051 is well known and not part of this discription. However some of the features are not needed or adapted to special product requirements. These features are described herein in detail.

The CPU8051 incorporates basic core internal registers. Accumulator (ACC), Register B (B) and Program Status Word (PSW) are bitaddressable registers used to perform arithmetical and logical operations. Stack Pointer (SP) and Data Pointer (DPL/DPH) are included to allow basic programming structures.

Table 9 8051 basic SFRs

SFR (Abbr)	Addr	Access	Default Value	Register
ACC	$E0_H$	rw	$00_H/00_H$	Accumulator
B	$F0_H$	rw	$00_H/00_H$	Register B
DPL	82_H	rw	$00_H/00_H$	Data Pointer (low)
DPH	83_H	rw	$00_H/00_H$	Data Pointer (high)
PSW	$D0_H$	rw	$00_H/00_H$	Program Status Word
SP	81_H	rw	$00_H/00_H$	Stack Pointer

SFR PSW holds the result of basic arithmetic operations.

Table 10 SFR Address $D0_H$: PSW - Program Status Word

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CY	**AC**	**F0**	**RS1**	**RS0**	**OV**	**F1**	**P**
rw 0/0	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**r 0/0**
CY		Carry Bit; set to '1' if accumulator changes signed number range through 0x00/0xFF (unsigned range overflow)					
AC		Auxillary Carry Bit; carry-out for BCD operations.					
F0		General Purpose Bit 0; may be freely used by the application					
RS1		Register Bank Select; bit 1					
RS0		Register Bank Select; bit 0					
OV		Overflow Bit; set to '1' if accu changes signed number range through 0x80/0x7F with arithmetic operations (signed range overflow)					
F1		Gereral Purpose Bit 1; may be freely used by the application					
P		reflects the number of 1s in the accumulator (set to '1' if accu contains an odd number of 1s)					

2.5.4 System Configuration Registers

The system configuration registers can be used for:

- Initiating state transitions
- System software reset
- Enabling or disabling peripherals
- Monitoring the operation mode, the system state and peripherals

Table 11 SFR Address $F8_H$: CFG0 - Configuration Register 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDWN	**TSHDWN**	**IDLE**	**n.u.**	**FTM**	**n.u.**	**n.u.**	**CLKSel0**
rw 0/0	**rw 0/0**	**rw 0/0**	**r 0/0**	**rw u/0**	**r 0/0**	**r 0/0**	**rw 0/0**
PDWN		POWER DOWN state If set to ’1’ by software the POWER DOWN state is entered; This bit is automatically reset to ’0’ by the system controller after a wakeup. *Note: Entering POWER DOWN state is handled by a ROM Library function. It is not recommended to set this bit manually.*					
TSHDWN		THERMAL SHUTDOWN state If set to ’1’ by software the THERMAL SHUTDOWN state is entered; This bit is automatically reset to '0' by the system controller after wakeup. *Note: Entering THERMAL SHUTDOWN state is handled by a ROM Library function. It is not recommended to set this bit manually.*					
IDLE		IDLE state If set to ’1’ by software the IDLE state is entered; This bit is automatically reset to ’0’ by the system controller after a resume event occurred.					
FTM		only used for internal production test mode, don’t care for application					
CLKSel0		Systemclock Source Select 1: Select crystal oscillator clock 0: Select 12MHz RC HF Oscillator *Note: Changing the systemclock is handled by a ROM Library function. It is not recommended to set this bit manually.*					

Table 12 SFR Address $E8_H$: CFG1 - Configuration Register 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PMWEn	**I2CEn**		**RfTXPEn**	**ADWBEn**	**SPIEn**	**ITInit**	**ITEn**
rw 0/0	**rw 0/0**	**r 0/0**	**rw u/0**	**rw 0/0**	**rw 0/0**	**r 0/0**	**r u/1**
PMWEn		Program Memory Write Enable. This bit is only used for PROGRAMMING mode: 0: No write access to FLASH program memory 1: Write access to FLASH program memory is allowed *Note: This bit is under control of ROM library functions. Don't care for application.*					
I2CEn		I^2C Enable 1: I^2C behavior on PINs PP1/SCL and PP2/SDA is enabled 0: Keeps standard I/O-Port functionality					
RfTXPEn		Transmitter Data Port Out Enable 1: The transmission data is strobed on port PP2/TXData 0: GPIO port functionality is provided.					
ADWBEn		ADC Conversion ENable. This is under control of ROM library functions. Don't change this bit by the application manually.					
ITInit		Interval Timer Initialization active This bit is '1' as long as the Interval-Timer is configured with the content of the ITPR register. This bit is automatically cleared after initialization completes.					
ITEn		Intervaltimer ENable (Test-, Debug-, Progmode only)					

Table 13 SFR Address $D8_H$: CFG2 - Configuration Register 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EnHFBYP	**n.u.**	**n.u.**	**PDLMB**	**PDADC**	**n.u.**	**WDRES**	**RESET**
rw 0/0	**r 0/0**	**r 0/0**	**rw u/1**	**rw 1/1**	**r 0/0**	**cw 0/0**	**cw 0/0**
EnHFBYP		Enable RF Vreg-HF bypass					
PDLMB		Power down RAM lower Memory Block (00_H - $7F_H$) 1: the lower 128 byte RAM is powered down in POWER DOWN state or THERMAL SHUTDOWN state 0: the lower memory block is always powered.					
PDADC		Power down ADC 1: ADC no supply 0: ADC active *Note: This bit is handled by the ROM Library functions automatically. It is not recommended to change this bit manually.*					
WDRES		*Reset Watchdog counter to 0*					
RESET		*Reset System (Software Reset)*					

Table 14 SFR Address $D9_H$: DSR -Diagnosis and System Status Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SCLK	**TMAX**	**OpMODE1**	**OpMODE0**	**FlashCP1**	**FlaschCP0**	**WUP**	**FlashLCK**
r 0/0	**r x/x**	**r u/x**	**r u/x**	**r 0/0**	**r 0/0**	**r x/0**	**rmw u/0**
SCLK		Status Flag indicating the current systemclock. 1: Crystal Oscillator clock 0: 12 MHz RC HF Oscillator					
TMAX		TMAX Detector Status Bit 1: Temperature < TMAX 0: Temperature > TMAX This bit should be polled by the application before entering THERMAL SHUTDOWN state *Note: Entering THERMAL SHUTDOWN state is handled by a ROM Library function. It is not needed to evaluate this bit manually.*					
OpMODE0-1		These bits indicate the current operation mode 11b: NORMAL mode 10b: PROGRAMMING mode 01b: DEBUG mode 00b: internal productionTEST mode					
FLASHCP1		Only used for internal production test mode, don't care for application					
FLASHCP0		Only used for internal production test mode, don't care for application					
WUP		Wakeup pending					
FLASHLCK		Flash Lock (0=full Flash-SFR access, 1=restricted write access) It is set to '1' by SW if Config-Magic-Number is detected. Self-holding when '1'!					

2.5.5 General Purpose Registers (GPR)

In PMA7110, XData Memory GPR1 - GPRF are used In NORMAL-, Debug- and Programming Mode as 16 GPR-General Purpose Register, which can be used by the application to store data beyond a POWER DOWN state period. They consume low leakage current compared to the whole lower memory block by storing low amounts of data. They can also be used as Testmode-Registers in Functional Testmode for building blocks and Test-Hardware, but they are not reseted in these modes to allow data retention even after Brown-out.

Table 15 GPR Registers

SFR (Abbr)	Addr	Register
GPR0	0x00 XDATA	General Purpose Register 0
GPR1	0x01 XDATA	General Purpose Register 1
GPR2	0x02 XDATA	General Purpose Register 2
GPR3	0x03 XDATA	General Purpose Register 3
GPR4	0x04 XDATA	General Purpose Register 4
GPR5	0x05 XDATA	General Purpose Register 5
GPR6	0x06 XDATA	General Purpose Register 6
GPR7	0x07 XDATA	General Purpose Register 7
GPR8	0x08 XDATA	General Purpose Register 8
GPR9	0x09 XDATA	General Purpose Register 9
GPRA	0x0A XDATA	General Purpose Register 10
GPRB	0x0B XDATA	General Purpose Register 11
GPRC	0x0C XDATA	General Purpose Register 12
GPRD	0x0D XDATA	General Purpose Register 13
GPRE	0x0E XDATA	General Purpose Register 14
GPRF	0x0F XDATA	General Purpose Register 15

Note: The GPRs are in the XData area and therefore not reset on a System Reset. After a Brownout Reset this feature can be used to possibly recover data from RAM. After Power On Reset the GPR Registers are not initialzed, thus they contain random data. The application has to initialize the GPR Registers if needed.

2.5.6 System Controller

While the microcontroller controls PMA7110 in RUN state, the system controller takes over control in POWER DOWN state, IDLE state and THERMAL SHUTDOWN state.

The system controller handles the system clock, wakeup events, and system resets.

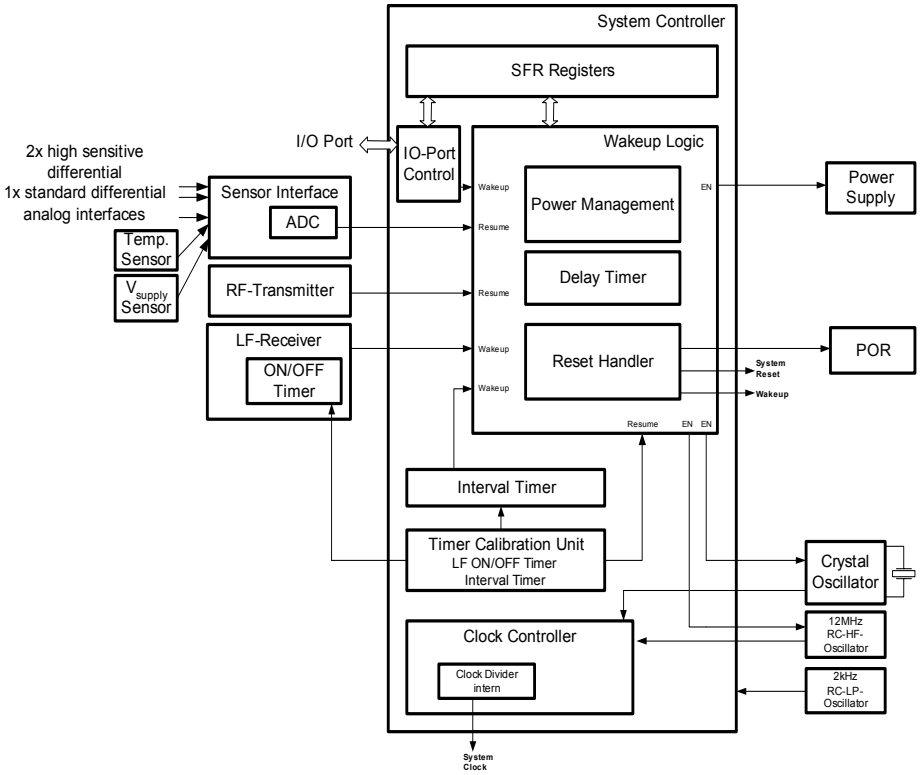


Figure 11 Block diagram of the system controller

2.5.6.1 Wakeup Logic

One of the key elements within the system controller is the wakeup logic, which is responsible for transitions from POWER DOWN state to RUN state via INIT state. The wakeup logic is clocked by the 2 kHz RC LP Oscillator, thus the wakeup logic is fully functional even when all other clock sources (12 MHz RC HF Oscillator and crystal oscillator) are switched off.

The difference between Reset and Wakeup:

- **Reset** - Either via Software Reset, Brownout or Reset pin, the digital circuit is reset. Program execution starts at address 0000_H to perform reset initialization routines (including operation mode selection) and will jump to the FLASH at address 4000_H in Normal Mode to execute the application program.

- **Wakeup** - Only the program counter of the microcontroller and its peripheral units are reset. Program Execution starts at address 0000_H to perform wakeup initialization routines (for evaluating the wakeup source) and jumps to the FLASH at 4000_H to execute the application program.

Wakeup Event Handling

Whenever a wakeup event occurs, the PMA7110 leaves POWER DOWN state and enters RUN state to execute the application code. This transition can be initiated from various sources. The wakeup source can be identified by reading SFR WUF and SFR ExtWUF.

A wakeup source can be enabled or disabled by setting the appropriate bits in SFR WUM and SFR ExtWUM. For security reasons the Interval Timer wakeup cannot be masked and the Interval Timer can not be disabled. The Watchdog, which is only active in RUN and Idle State can not be masked.

SFR WUF and SFR ExtWUF are read-only, thus no set/clear operations are possible. The wakeup source (except the Watchdog) is available during the whole RUN state. If an additional Wakeup event occurs during Run State, the appropriate flag will be set, but the device won't be forced through Init state.
It won't be cleared until POWER DOWN state is entered again.

Table 16 SFR Address $C1_H$: WUM - Wakeup Mask RegisterM

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MWDOG	**MTMAX**	**MLFCD**	**MLFSY**	**MLFPM1**	**MLFPM0**	**n.u.**	**MITIM**
rw u/1	**rw u/1**	**rw u/1**	**rw u/1**	**rw u/1**	**rw u/1**	**rw u/1**	**rw u/1**
MWDOG		Mask Watchdog Wakeup Watchdog Wakeup is not maskable in NORMAL mode This bit is only used for internal production test mode,Debug- and Prog. mode. don't care for application					
MTMAX		Mask TMAX Wakeup TMAX Wakeup is not maskable in NORMAL mode This bit is only used for internal production test mode,Debug- and Prog. mode. don't care for application					
MLFCD		Mask LF receiver Carrier detect 0: no Mask (enable wakeup source) 1: Mask (disable wakeup source)					
MLFSY		Mask LF receiver Sync match 0: no Mask (enable wakeup source) 1: Mask (disable wakeup source)					
MLFPM1		Mask LF receiver Pattern 1 match 0: no Mask (enable wakeup source) 1: Mask (disable wakeup source)					
MLFPM0		Mask LF receiver Pattern 0 match 0: no Mask (enable wakeup source) 1: Mask (disable wakeup source)					
ITIM		Mask Interval Timer Wakeup Interval Timer Wakeup is not maskable in NORMAL mode This bit is only used for internal production test mode, don't care for application					

Table 17 SFR Address $F2_H$: ExtWUM - Wakeup Mask Register 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MEXTWU7	**MEXTWU6**	**MEXTWU5**	**MEXTWU4**	**MEXTWU3**	**MEXTWU2**	**MEXTWU1**	**MEXTWU0**
rw u/1	**rw u/1**	**rw u/1**	**rw u/1**	**rw u/1**	**rw u/1**	**rw u/1**	**rw u/1**
MEXTWU7		Mask External Wakeup 7					
MEXTWU6		Mask External Wakeup 6					
MEXTWU5		Mask External Wakeup 5					
MEXTWU4		Mask External Wakeup 4					
MEXTWU3		Mask External Wakeup 3					
MEXTWU2		Mask External Wakeup 2					
MEXTWU1		Mask External Wakeup 1					
MEXTWU0		Mask External Wakeup 0					

Table 18 SFR Address $C0_H$: WUF - Wakeup Flag Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDOG	**TMU**	**LFCD**	**LFSY**	**LFPM1**	**LFPM0**	**n.u.**	**ITIM**
rc x/0	**rc x/0**	**rc x/0**	**rc x/0**	**rc x/0**	**rc x/0**	**r 0/0**	**rc x/0**
WDOG		Watchdog Wakeup					
TMU		TMAX Underflow Wakeup					
LFCD		LF receiver Carrier Wakeup					
LFSY		LF receiver Sync match Wakeup					
LFPM1		LF receiver Pattern 1 match Wakeup					
LFPM0		LF receiver Pattern 0 match Wakeup					
ITIM		Interval Timer Wakeup					

Table 19 SFR Address $F1_H$: ExtWUF - Wakeup Flag Register 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXTWU7	**EXTWU6**	**EXTWU5**	**EXTWU4**	**EXTWU3**	**EXTWU2**	**EXTWU1**	**EXTWU0**
r x/0	**r x/0**	**r x/0**	**r x/0**	**r x/0**	**r x/0**	**r x/0**	**r x/0**
EXTWU7		External Wakeup 7					
EXTWU6		External Wakeup 6					
EXTWU5		External Wakeup 5					
EXTWU4		External Wakeup 4					
EXTWU3		External Wakeup 3					

EXTWU2		External Wakeup 2
EXTWU1		External Wakeup 1
EXTWU0		External Wakeup 0

Watchdog Wakeup

A watchdog wakeup occurs after the watchdog timer has elapsed.
See **"Watchdog Timer" on Page 40** for details about the watchdog timer.

TMAX Wakeup

A TMAX wakeup occurs only if the device was in THERMAL SHUTDOWN state and the temperature falls below the threshold temperature T_{REL}.
See **"Functional Block Description" on Page 41** for details about the TMAX wakeup.

LF Receiver Wakeup Event

The LF receiver wakeup can be enabled by setting either:

- SFR bit WUM.5 [LFCD] or
- SFR bit WUM.4 [LFSY] or
- SFR bit WUM.3[LFPM1] and/or SFR bitWUM.2 [LFPM0]

The wakeup source can be read in the SFR WUF.

Note: The LF receiver has to be configured appropriate for the particular wakeup modes.
*See **"LF Receiver" on Page 85** for details.*

External Wakeup Event

I/O Port PP1-PP4 and PP6-PP9 can be configured to wakeup the PMA7110 from POWER DOWN state by an external source.

Note: PP1-PP4 and PP6-PP9 have to be configured according to ***"External Wakeup on PP1-PP4 and PP6-PP9" on Page 109*** *for this feature.*

Interval Timer Wakeup Event

When the Interval Timer elapses, a wakeup event is generated and POWER DOWN state is left. The wakeup can be identified by the application software reading SFR bit WUF.0[ITIM].
The Interval Timer is reloaded automatically with actual values from register ITPR and immediately restarted, so the Interval Timer is even working in RUN state.

Note: The Interval Timer is not maskable, so the application will get Interval Timer wakeup events periodically. If these Wakeup events occur during Run state, they will set the appropriate Flag but not force the device through Init state.

IDLE state and Resume Event Handling

If switched to IDLE state by setting SFR bit CFG0.5 [IDLE], the systemclock to the microcontoller is gated off.

Note: IDLE state will only be entered if one of the units providing a resume event is enabled and active. Otherwise the system will continue executing code in RUN state without entering IDLE state.

Only few peripherial components are still active in IDLE state. The watchdog is active and will be initialized automatically before entering IDLE state, thus IDLE state has a maximum duration of approx. 1 second before a watchdog wakeup occurs.
The systemclock to the microcontroller is re-enabled when a resume event occurs.
The program code continues working where it was suspended. SFR bit CFG0.5[IDLE] is automatically cleared after a resume event. The resume event source is available in SFR REF.

The Idle State will be left in case an interrupt event occurrs. After completion of the Interrupt service the Idle State will be re-entered in case no resume event is pending.

Table 20 SFR Address $D1_H$: REF - Resume Event Flag Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
REXTG	**n.u.**	**READC**	**RELFO**	**RERFU**	**RERFF**	**RERC**	**RET2**
rc 0/0	**0/0**	**rc 0/0**	**rc 0/0**	**rc 0/0**	**rc 0/0**	**rc 0/0**	**rc 0/0**
REXTG		Systemclock changed to crystal The PMA7110 can be put into IDLE state during crystal startup. After expiring of the crystal delay time the REXTG Flag is set. (see also SFR XTCFG.2-0 Bit XTDLY[2-0] in ***Table 26 "SFR Address $C2_H$: XTCFG - Crystal Config Register" on Page 72***).					
READC		ADC conversion complete (this bit is under control of ROM Library functions					
RELFO		LF receiver buffer full					
RERFU		RF transmit buffer empty					
RERFF		RF transmission finished					
RERC		2 kHz RC LP Oscillator calibration complete					
RET2		Timer 2 underflow					

2.5.6.2 Interval Timer

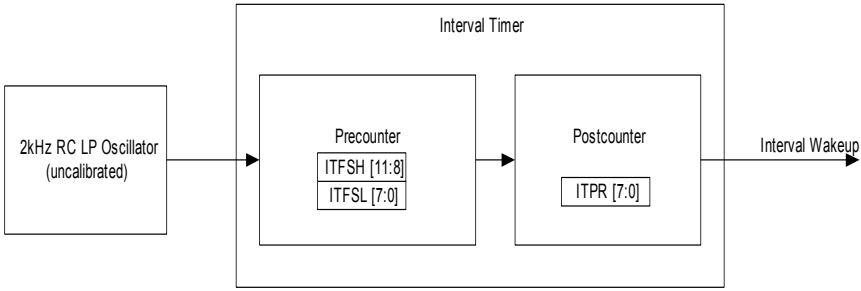


Figure 12 Interval Timer Block Diagram

The Interval Timer is responsible to wakeup the PMA7110 from the POWER DOWN state after a predefined time interval. It is clocked by the 2kHz RC LP Oscillator and incorporates two dividers:

- Precounter: can be calibrated to the systemclock and represents the timebase.
- Postcounter: configures the Interval Timer duration. It can be set from 1-256_{dec}.

Timing accuracy can be ensured by using a ROM library function which calibrates the precounter towards the accurate systemclock. See [1] **“Reference Documents” on Page 157**.

The Interval Timer duration is determined by the SFR ITPR. This value is calculated by using the following equation:

$$\text{Intervaltimeriod}[s] = \frac{\text{precounter}}{f_{2kHzRCLPOscillator}\left[\frac{1}{s}\right]} \bullet \text{postcounter}$$

The Postcounter (ITPR) is an 8 bit register. The maximum interval duration corresponds to 00_H (multiplication with 256_{dec}).
01_H up to FF_H corresponds to a multiplication with 1_{dec} up to 255_{dec}.

Note: After writing SFR ITPR some clock cyles are needed to activate the new setting. SFR bit CFG1.1[ITInit] is cleared automatically when the new setting is activated.

Table 21 SFR Address BC_H: ITPR - Interval Timer Period Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ITPR.7	ITPR.6	ITPR.5	ITPR.4	ITPR.3	ITPR.2	ITPR.1	ITPR.0
rw u/0	rw u/0	rw u/0	rw u/0	rw u/0	rw u/0	rw u/0	rw u/1

2.5.6.3 Interval Timer Calibration

Calibration is done by counting clock cycles from the crystal oscillator or the 12MHz RC HF Oscillator (depending on the current systemclock) during one 2kHz RC LP Oscillator period. The calibration is performed automatically by a ROM library function (see [1] **“Reference Documents” on Page 157**).

Note: If the crystal oscillator should be used for the calibration, the crystal frequency has to be stored in the FLASH User Data Sector.

Table 22 SFR Address BA_H: ITPL- Interval Timer Precounter (Low Byte)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ITP.7	ITP.6	ITP.5	ITP.4	ITP.3	ITP.2	ITP.1	ITP.0
rw u/1	rw u/1	rw u/1	rw u/0	rw u/1	rw u/0	rw u/0	rw u/0

Table 23 SFR Address BB_H: ITPH- Interal Timer Precounter (High Byte)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	n.u.	n.u.	n.u.	ITP.11	ITP.10	ITP.9	ITP.8
0/0	0/0	0/0	0/0	rw u/0	rw u/0	rw u/1	rw u/1

Note: These SFRs can be modified manually as well for using other (uncalibrated) precounter values.

2.5.7 Clock Controller

The Clock Controller for internal clock managment is part of the system controller.

The PMA7110 always starts up using the 12 MHz RC HF Oscillator to provide minimum startup time and minimum current consumption. Changing the systemclock from the 12 MHz RC HF Oscillator to the crystal (e.g. for RF Transmisssion) is performed automatically by a ROM library function (see [1] **"Reference Documents" on Page 157**). If the crystal is selected as systemclock, the 12 MHz RC HF Oscillator is automatically powered down.

Note: Since the external crystal needs some startup time, a 3 bit delay timer is integrated to delay the clock switching. Dependent on the used crystal the SFR bits XTCFG.2-0 [XTDLY2-0] can be set to delay from typ. 0µs up to 1750µs in 250µs steps.(see ***Table 26 "SFR Address C2$_H$: XTCFG - Crystal Config Register" on Page 72****).*

The following figure shows which clocks are used for which PMA7110 blocks. Details about the individual blocks can be found in the appropriate chapters of this document

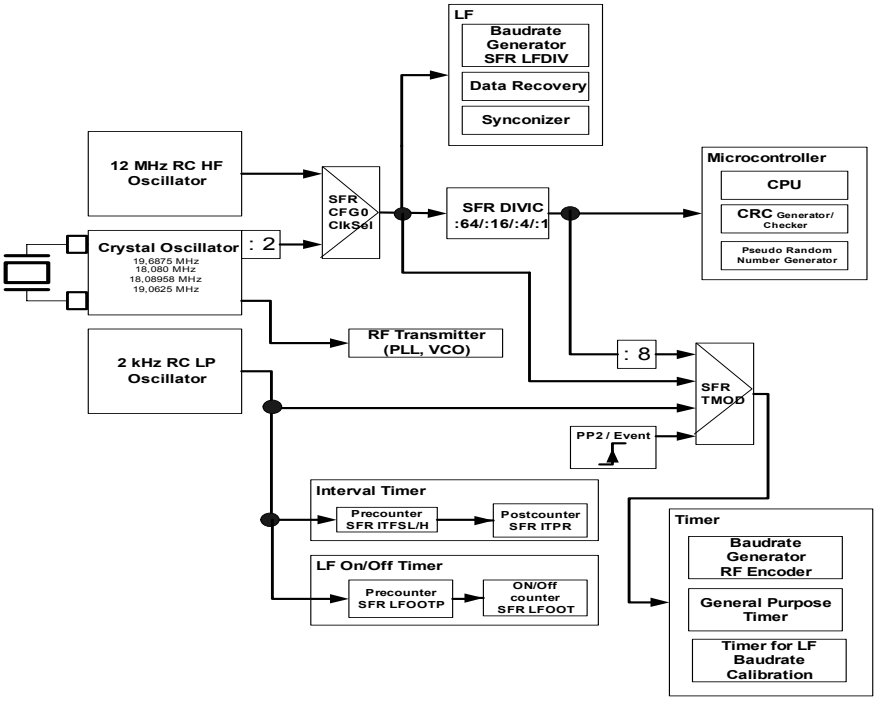


Figure 13 PMA7110 Clock Concept

PMA7110 Internal Clock Divider

For power saving it is possible to enable the internal clock divider, to reduce the systemclock by a prescaled factor. If SFR DIVIC is set to 00_H (default) the divider is disabled.

Table 24 SFR Address $B9_H$: DIVIC - Internal Clock Divider

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	n.u.	n.u.	n.u.	n.u.	n.u.	DIVIC1	DIVIC0
0/0	0/0	0/0	0/0	0/0	0/0	rw u/0	rw u/0
DIVIC1-0		"Internal Clock Divider" 11b: Divide by 64 10b: Divide by 16 01b: Divide by 4 00b: Divide by 1					

2.5.7.1 2 kHz RC LP Oscillator (Low Power)

The 2 kHz RC LP Oscillator stays active even in POWER DOWN state. The typical frequency of the oscillator is 2kHz.

2.5.7.2 12 MHz RC HF Oscillator (High Frequency)

The 12 MHz RC HF Oscillator runs at typ. 12MHz. It is used as the default clock source for the PMA7110 in RUN state and is calibrated in the Infineon production site.

2.5.7.3 Crystal Oscillator

The crystal oscillator is a Negative Impedance Converter (NIC) oscillator with a crystal operating in series resonance. The nominal crystal operating frequencies are between 18MHz and 20MHz depending on the RF-band used.

Table 25 Formulas for Crystal selection dependent of RF- Bands

$$868\text{MHz}, 915\text{MHz}\ldots\ldots f_{xtal} = f_{RF} \bullet \frac{1}{48}$$

$$434\text{MHz}\ldots\ldots f_{xtal} = f_{RF} \bullet \frac{2}{48}$$

$$315\text{MHz}\ldots\ldots f_{xtal} = f_{RF} \bullet \frac{3}{48}$$

Crystal startup time adjustment for different crystals is possible in steps of 250µs by using the SFR bits XTCFG.2-0 [XTDLY2-0].

Table 26 SFR Address $C2_H$: XTCFG - Crystal Config Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	n.u.	n.u.	n.u.	n.u.	XTDLY2	XTDLY1	XTDLY0
0/0	0/0	0/0	0/0	0/0	rw u/0	rw u/1	rw u/1
XTDLY2-0		Crystal Delay Timer delay time in steps of 250µs @ typ. 2 kHz RC LP Oscillator clcok = 2kHz 111b: typ. 1750µs 110b: typ. 1500µs 101b: typ. 1250µs 100b: typ. 1000µs 011b: typ. 750µs 010b: typ: 500µs 001b: typ. 250µs 000b: typ. 0µs					

Frequency pulling from the nominal crystal frequency can be achieved by the internal capacitor banks. This can be used for fine tuning the ASK carrier frequency and the lower and upper modulation frequencies for FSK modulation. Thus, frequency errors due to crystal or component tolerances can be trimmed away.

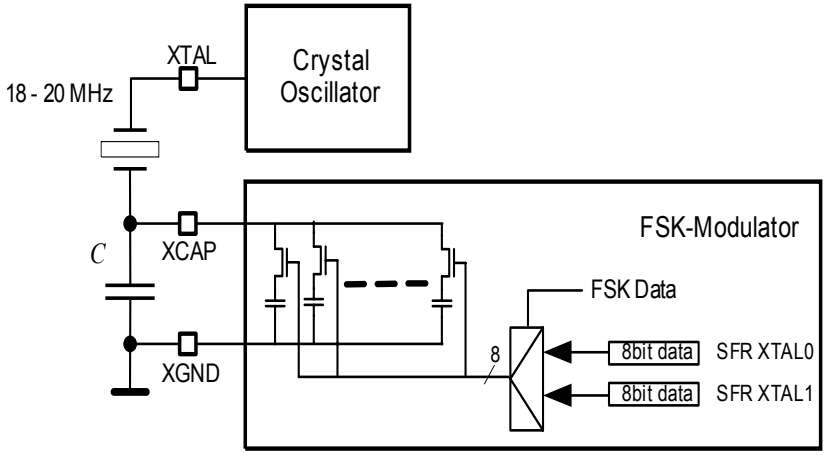


Figure 14 Crystal Oscillator and FSK-Modulator Block Diagram

The SFRs SFR XTAL0 and SFR XTAL1 allow the trimming of the crystal frequency in a broad range.

Table 27 SFR Address $C4_H$: XTAL0 - XTALConfiguration Register (FSKLOW)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FSKLOW7	FSKLOW6	FSKLOW5	FSKLOW4	FSKLOW3	FSKLOW2	FSKLOW1	FSKLOW0
w u/1	w u/1	w u/1	w u/1	w u/1	w u/1	w u/1	w u/1
FSKLOW7-0		FSK Low Frequency Capacitor select for lower FSK modulation frequency if RFENC.3==0[TXDD] and if RFTX.5==0[ASKFSK]. The capacitor array is binary weighted from FSKLOW7 = 20pF (MSB) FSKLOW0 = 156fF (LSB)					

Table 28 SFR Address $C3_H$: XTAL1-XTAL Config. Register (FSKHIGH/ASK)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FSKHASK7	FSKHASK6	FSKHASK5	FSKHASK4	FSKHASK3	FSKHASK2	FSKHASK1	FSKHASK0
w u/1	w u/1	w u/1	w u/1	w u/1	w u/1	w u/1	w u/1
FSKHASK7-0		FSK High Frequency / ASK Centre Frequency Capacitor select for upper FSK modulation frequency if RFENC.3===1[TXDD] and if RFTX.5==0[ASKFSK] or ASK center frequency fine tuning capacitor select if RFTX.5==1[ASKFSK]. The capacitor array is binary weighted from FSKHASK7 = 20pF (MSB) down to FSKHASK0 = 156fF (LSB).					

2.5.8 Interrupt Sources on the <Dev_NameShort1>

Similar to the CPU8051 the <Dev_NameShort1> supports interrupt events of several sources which are listed below.

When an interrupt occurs the PC is automatically set to the Vector assigned to the Interrupt source. From there the vector is forwarded via LJMP instruction into the Flash area and the offset of 4000_H is added.

When an an unmasked interrupt occurs while the device is in Idle State this state is immediately left and the PC continues operation on the appropriate interrupt vector (see **Figure 29**). After the processing of the Interrupt service routine (*RETI* instruction) the device automatically returns into Idle State in case no Resume Event has occured in between. If a Resume Event has been detected during the interrupt service routine the *RETI* instruction returns the PC to the location after the Idle Instruction. It is highly recommended that this instruction to be a *NOP*.

The priority of the Interrupts can be configured using the IP register. Setting a bit in IP to one assigns higher priority to the linked interrupt. A high priority interrups can then interrupt a service routine from a low priority interrupt.

Table 29 Interrupt Vector locations

Interrupt Vector	Vector Address	Forwarded Address	Interrupt source
Reset Vector	00_H	4000_H	
Vector 0	03_H	4003_H	External Interrupt 0 (PP9)
Vector 1	$0B_H$	$400B_H$	Timer 0 Interrupt
Vector 2	13_H	4013_H	External Interrupt 1 (PP7)
Vector 3	1B	401B	Timer 1 Interrupt
Vector 4	23_H	4023_H	I²C Interface Interrupt
Vector 5	$2B_H$	$402B_H$	SPI Interface Interrupt
Vector 6	33_H	4033_H	Extended Interrupt: the Flash software has to detect the Interrupt source peripheral from this Vector by reading IRQFR and the appropriate source within the peripheral from the various flag registers. – Timer 2 Interrupt – Timer 3 Interrupt – LF Receiver Interrupt – RF Encoder Interrupt

External Interrupts 0 and 1

The <Dev_NameShort1> has two external Interrupt sources Ext_Int0 on PP9 and Ext_Int1 on PP7. As in the CPU8051 the control bits and interrupt flags can be found in the TCON register (please refer to **Table 44 on Page 92**).

When enabled by setting IE.0 [EX0] for External Interrupt 0 (resp. IE.2 [EX1] for External Interrupt 1) interrupts can be generated from PP9 (resp. PP7).

The External Interrupts 0 and 1 can be programmed to be level-activated or negative-transition activated by clearing or setting bit TCON.0 [IT0], respectively TCON.2 [IT1]. If bit ITx = 0, the corresponding External Interrupt is triggered by a detected low level at the pin. If ITx = 1, the corresponding External Interrupt is negative edge-triggered. In this mode, if successive samples of the pin show a high in one cycle and a low in the next cycle, interrupt request flag IEx in TCON is set. Flag bit IEx=1 then requests the interrupt.

If the External Interrupt is level-activated, the external source has to hold the request active until the requested interrupt is actually generated. Then it has to deactivate the request before the interrupt service routine is completed, or else another interrupt will be generated.

Each of the External Interrupts has its own interrupt vector.

Timer Interrupts

All four timers on the <Dev_NameShort1> can be used as interrupt sources.

While Timer 0 and Timer 1 are fully compatible to the original CPU8051 (for a description please refer to **“Timer/counter interrupts” on Page 96**), Timer 2 and Timer 3 interrupts are treated as Extended Interrupts.

I²C Interface Interrupts

The data interface transfer on the I²C Module can be controlled via interrupts. This module has a separte interrupt vector (vector address 23_H) where the PC is automatically set whenever one of the interrupt flags active and unmasked.

In Test- , Debug- and Programming Mode the I²C interface handling is done by polling.

SPI Interface Interrupts

The data transfer on the SPI Interface can be controlled via Interrups. This module has a separte interrupt vector (vector address $2B_H$) where the PC is automatically set whenever one of the interrupt flags is active and unmasked.

LF Receiver Interrupts

While the main target for LF receiver operation is waking up the device, it is also possible to receive data via the LF interface in Run Mode. The Wake-up flags are used as Interrupt event flags and Wake-up mask bits are used as Interrupt Mask bits as well.

RF Encoder Interrupts

Note: It is recommended to keep the CPU in IDLE state during RF transmission whenever possible. Nevertheless, it is possible to coordinate the data transfer interrupt driven. Therefore, two interrupt sources are available for RF transmission:

Interrupt source flags:

- RFS.0 [RFBF] RF Encoder Buffer Full
- RFS.1 [RFSE] RF Encoder Shift Register Empty

Table 30 SFR Address $A8_H$: IE-Interrupt Enable Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EA	EID	ESPI	EI2C	ET1	EX1	ET0	EX0
rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0
EA		Global Interrupt Enable bit					
EID		Enable Extended Interrupts (Timer2/3, LF Receiver, RF Encoder)					
ESPI		Enable Interrupts from the SPI Interface					
EI2C		Enable Interrupts from I²C Interface					
ET1		Enable Interrupts from Timer 1					
EX1		Enable Interruots from External Interrupt 1 (PP7)					
ET0		Enable Interrupts from Timer 0					
EX0		Enable Interrupts from External Interrupt 0 (PP9)					

Table 31 SFR Address $B8_H$: IP-Interrupt Priority Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	PID	PSPI	PI2C	PT1	PX1	PT0	PX0
r 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0

PID		Priority level for Extended Interrupts (Timer2/3, LF Receiver, RF Encoder) 1: high priority Interrupt 0: low priority Interrupt
PSPI		Priority level for Interrupts from the SPI Interface
PI2C		Priority level for Interrupts from I²C Interface
PT1		Priority level for Interrupts from Timer 1
PX1		Priority level for Interruots from External Interrupt 1 (PP7)
PT0		Priority level for Interrupts from Timer 0
PX0		Priority level for Interrupts from External Interrupt 0 (PP9)

Table 32 SFR Address $8F_H$: IRQFR-Interrupt Request Flag Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	n.u.	n.u.	n.u.	IRQFMC	IRFLF	IRQFT3	IRQFT2
r 0/0	r 0/0	r 0/0	r 0/0	rc 0/0	rc 0/0	r 0/0	r 0/0

IRQFMC		Interrupt Request Flag RF Encoder
IRQFLF		Interrupt Request Flag LF Receiver
IRQFT3		Interrupt Request Flag Timer 3
IRQFT2		Interrupt Request Flag Timer 2

2.5.9 RF 315/434/868/915 MHz FSK/ASK Transmitter

The RF transmitter consists of a PLL Frequency synthesizer that is contained fully on chip, a lock detector and a power amplifier.

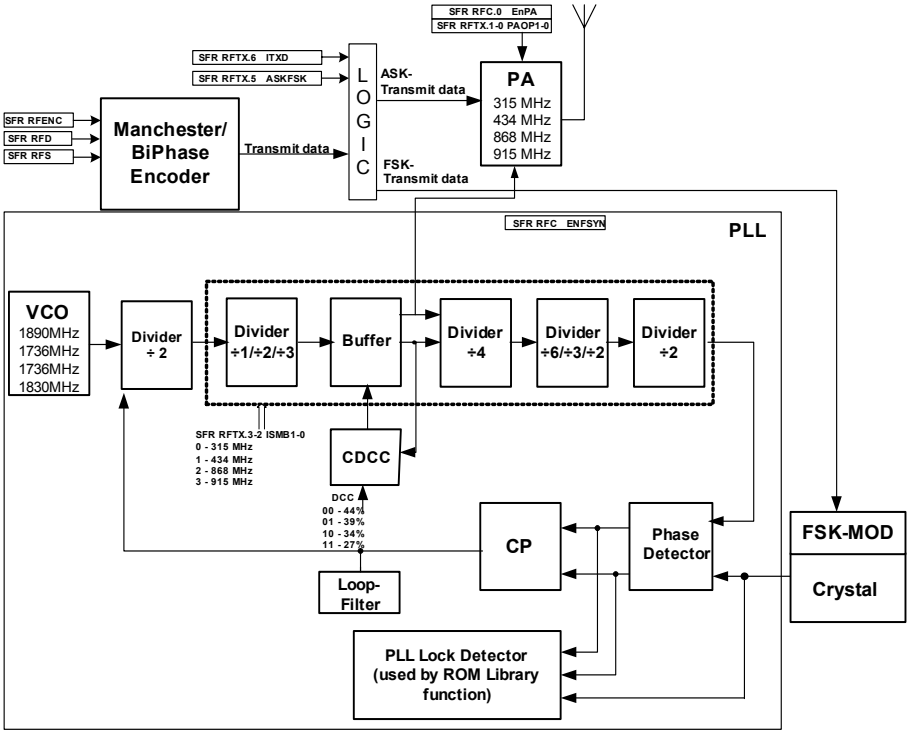


Figure 15 RF Transmitter Block Diagram

The RF-Transmitter can be configured for the 315/434/868/915 MHz ISM-Band frequencies by setting SFR bits RFTX.3-2[ISMB1-0] and choosing the proper crystal. Manchester/BiPhase/NRZ coded data with a bit rate up to 20kbit/s (40kchips/s) can be transmitted using ASK or FSK modulation.

Table 33 SFR Address AE_H: RFTX - RF Transmitter Control Register 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XCapSH	INVTXDAT	ASKFSK	n.u.	ISMB1	ISMB0	PAOP1	PAOP0
w 0/0	w u/0	w u/0	0/0	w u/0	w u/1	w u/1	w u/1
XCapSH		Enable XCAP short					
INVTXDAT		Invert TX Data					
ASKFSK		TX ASK/FSK Modulation Select 1: ASK 0: FSK					
ISMB1-0		RF Frequency Select 1xb: 868MHz/915MHz 01b: 434MHz 00b: 315MHz					
PAOP1-0		RF Power Amplifier Output Power Select 11b: 10dBm 10b: 8dBm 01b: 8dBm 00b: 5dBm					

The PLL synthesizer and the power amplifier can be enabled seperately by using the SFR RFC control register. The power amplifier should be switched on with a delay of at least 100µs after enabling the frequency synthesizer. This delay is needed for PLL locking.

Table 34 SFR Address EE_H: RFC - RF Transmitter Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	n.u.	n.u.	n.u.	n.u.	n.u.	ENFSYN	EnPA
0/0	0/0	0/0	0/0	0/0	0/0	rw 0/0	rw 0/0
ENFSYN		Enable RF Frequency Synthesizer					
EnPA		Enable RF Power Amplifier					

2.5.9.1 Phase Locked Loop PLL

The PLL consists of an on-chip VCO, an asynchronous divider chain with selectable overall division ratio, a phase detector with charge pump and an internal loop filter. (see **Table 118 "SFR Address DE_H: RFVCO -RF Frequency Synthesizer VCO Config" on Page 151**)

The PLL can be enabled manually by setting SFR bit RFC.1[ENFSYN]. The PLL lock frequency is determined by the used crystal (see **Table 25 "Formulas for Crystal selection dependent of RF- Bands" on Page 71**) and the appropriate configuration in the SFR bits RFTX.3-2[ISMB1-0].

2.5.9.2 Power Amplifier PA

The highly efficient power amplifier is enabled automatically if a byte is transmitted (RFS.1 [RFSE] is set to ’0’) and if TX data are not output on pin PP2 (CFG1.4 [RfTXPEn]). Alternatively the power amplifier is enabled immediately by using RFC.0 [ENPA]. The nominal transmit power levels are +5/8/10dBm into 50 Ohm load at a supply voltage of 3.0V. The power amplifier operating point must be optimized to the output power +5/8/10dBm regarding current consumption by properly setting the RFTX.1-0 [PAOP1-0], RFFSPLL.3-2 [DCC1-0] and using an optimal sized matching circuit. The power amplifier should be enabled at least 100µs after enabling the RF frequency synthesizer because of the PLL lock in time.

2.5.9.3 ASK Modulator

ASK modulation is done by turning on and off the power amplifier dependent on the baseband data to be transmitted (On/Off-Keying) by using RFENC.3 [TXDD] or the Manchester/BiPhase encoder (see also **“Manchester/BiPhase Encoder with bit Rate Generator” on Page 81**). About FSK modulation please see **“Crystal Oscillator” on Page 71**.

2.5.9.4 Voltage Controlled Oscillator (VCO)

The VCO is using on-chip inductors and varactors for tuning and has a nominal center frequency of 1750MHz. The tuning range VCO is split up into 16 frequency ranges.

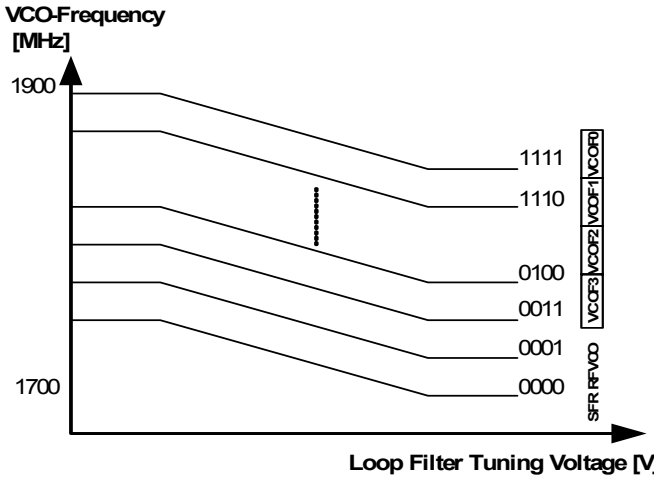


Figure 16 VCO tuning characteristic

automatically by the operating system after power up or a System Reset by using the PLL Lock detector and the PLL Lock detection routine. Additionally, the VCO is always recalibrated by firmware if the crystal oscillator is selected as clock source by setting CFG0.0 [ClkSel]. **Table 118 "SFR Address DE_H: RFVCO -RF Frequency Synthesizer VCO Config" on Page 151**

Additionally, the PLL Lock Detector for VCO tuning curve selection may be used by the user program code before RF data transmission. The PLL Lock Detection routine can be called by the user program for that reason. **Table 119 "SFR Address D4H: ADCDL - ADC Result Register (low Byte)" on Page 151**

A ROM library function is available which selects the tuning curve automatically dependent on environmental conditions (temperature, V_{bat}).

Note: Recalibration of the tuning curve is typically necessary when the supply voltage changes by more than 800mV or the temperature changes by more than 70 degrees.

For details on the ROM library functions please refer to [1] **"Reference SFR Registers" on Page 144**.

2.5.9.5 Manchester/BiPhase Encoder with bit Rate Generator

The interface between the CPU and the RF transmitter offers a Manchester/BiPhase encoder. The encoding bitrate can be set with Timer 3 (see **"Timer Unit (Timer 0, Timer 1, Timer 2, Timer 3)" on Page 90**) and may be programmed within a broad range.

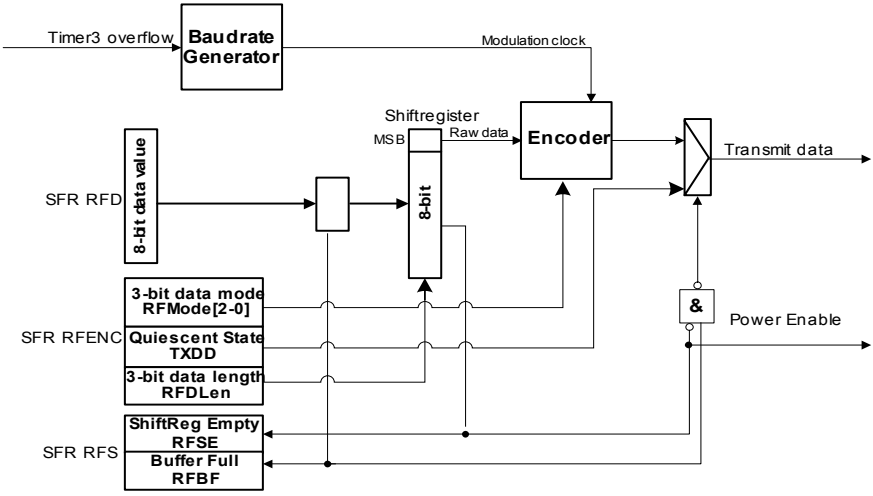


Figure 17 Manchester/BiPhase Encoder

The Manchester/BiPhase encoder automatically enables the power amplifier when a new databyte is written to SFR RFD. The power amplifier is disabled after transmitting the last data bit automatically as well.

It is also possible to send data with a user-defined encoding scheme, e.g. for sending a preamble. This can be achieved by using chipmode (SFR bits RFENC.2-0[RFMode2-0] = 101b). The chipmode sends each bit without encoding, but twice the data rate.

The encoding selection can be changed everytime before a data byte is written to the SFR RFD by adjusting SFR bits RFENC.2-0[RFMode2-0].

The SFR bit RFENC.3[TXDD] defines the data value assigned to Manchester/BiPhase encoder output when no data is available in the SFR RFD.

Note: If SFR bit RFC.1-0[ENFSYN EnPA] is set the SFR bit RFENC.3[TXDD] controls directly the transmitter state. By using this feature the user has full control of the transmit data without any restrictions in timing or protocol.

Table 35 SFR Address $E7_H$: RFENC - RF Encoder Tx Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFDLen2	RFDLen1	RFDLen0	RFMASK	TXDD	RFMode2	RFMode1	RFMode0
rw 1/1	rw 1/1	rw 1/1	rw 0/0	rw 0/0	rw =0/0	rw 0/0	rw 0/0
RFDLen2-0		RF Data Length - Number of bits to be transmitted from SFR RFD					
TXDD		Transmit data if SFR bit RFC.1-0 [ENFSYN EnPA] is set.					
RFMASK		RF Interrupt Mask Flag					
RFMode2-0		RF Encoder Mode 000b: Manchester: 0’ is encoded as Low-to-High, ’1’ as High-to-Low transition 001b: Inverted Manchester: ’0’ is encoded as High-to-Low, ’1’ as Low-to-High transition 010b: Differential Manchester ’0’ is encoded as transition 011b: BiPhase: ’0’ is encoded transition 100b: BiPhase: ’1’ is encoded transition 101b: Data bits are interpreted as chips 110b: reserved 111b: reserved					

By writing a databyte to the SFR RFD the data transmission is invoked automatically. Per default the transmission takes place byte-aligned. If less than 8 Bits should be transmitted, SFR bits RFENC.7-5[RFDLen2-0] can be set to determine the number of bits that should be transmitted.

Table 36 SFR Address $8E_H$: RFD - RF Encoder Tx Data Register

SFR (Abbr):	Addr	Access	Default Value	Register
RFD	$8E_H$	w	$u/00_H$	RF Encoder Data Register

The following figure shows the different timing diagrams for the different encoding schemes:

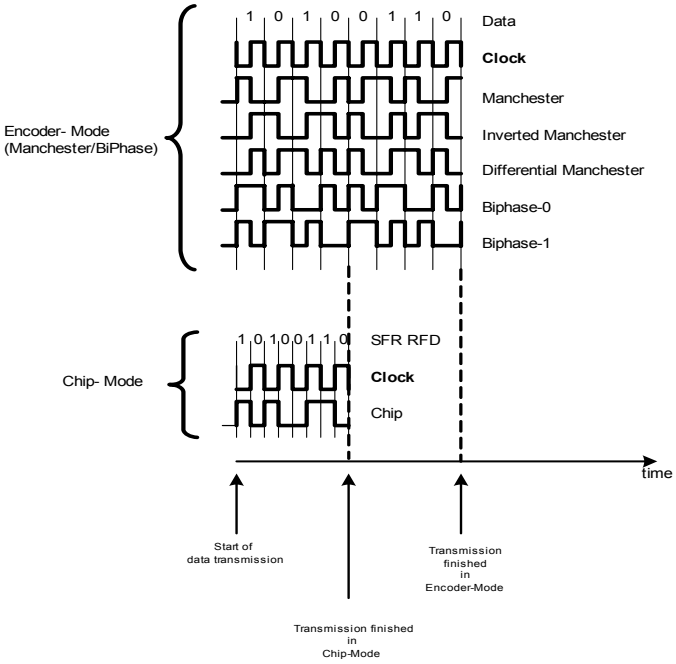


Figure 18 Diagram of the different RF Encoder modes.

Timer 3 (see **"Timer Unit (Timer 0, Timer 1, Timer 2, Timer 3)" on Page 90**) provides the bitrate clock and has to be set according to the desired bitrate. The bitrate timer value can be calculated with the following formula:

$$timervalue = \frac{f_{timerclocksource}[Hz]}{8 \bullet Bitrate\left[\frac{1}{s}\right]} - 1$$

This timervalue has to be written to the timer registers (see **Table 43 "SFR Address 8AH--8DH and CAH--CDH: Timer Registers" on Page 92**).

The SFR RFS represents the status of the RF Encoder.

After writing a databyte to SFR RFD, the SFR bit RFS.0[RFBF] is set. It is cleared automatically when the databyte in SFR RFD is transferred to the shiftregister.

The application should poll SFR bit RFS.0[RFBF] to determine when the data is transferred to the shiftregister and SFR RFD can take the next data byte for processing. It is necessary to provide the transmitter with a continous data stream to prevent the receiver from losing synchronization.

SFR bit RFS.1[RFSE] is set if there is no data available in the shiftregister and cleared if the shiftregister contains data that has to be transmitted.

Note: This flag is used internally to switch On/Off the Power Amplifier, thus is can be used by the application to determine if the Power Amplifier is currently active (SFR bit RFS.1[RFSE] == '0') or not active (SFR bit RFS.1[RFSE] == '1').

Table 37 SFR Address $E6_H$: RFS - RF Encoder Status Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	n.u.	n.u.	n.u.	n.u.	n.u.	RFSE	RFBF
0/0	0/0	0/0	0/0	0/0	0/0	r 1/1	r 0/0
RFSE		RF Encoder Shift-Register Empty Automatically set by hardware if no further bits are available in shift register.					
RFBF		RF Encoder Buffer Full Automatically set by hardware on write access to RFD register or cleared if data in register RFD is transferred to shift register respectively.					

2.5.10 LF Receiver

The LF receiver is used for data transmission to the PMA7110, as well as for waking up the PMA7110 from POWER DOWN state.
It can generate a wakeup directly by the carrier detector if the carrier amplitude is above a preset threshold, or it can decode the received data and not wake up the microcontoller until a predefined sync match pattern or wakeup pattern is detected in the data stream.

Data recovery using a synchronizer and a decoder is available for Manchester and BiPhase coded data. The synchronizer can also handle Manchester/BiPhase code violations. Any other coding scheme can be handled by the microcontroller on chip level, thus no limitations on data coding schemes apply.

A LF On/Off Timer is implemented to generate periodical On/Off switching of the LF receiver in POWER DOWN state. This can be done to reduce the current consumption.

2.5.11 16Bit CRC (Cyclic Redundancy Check) Generator/Checker

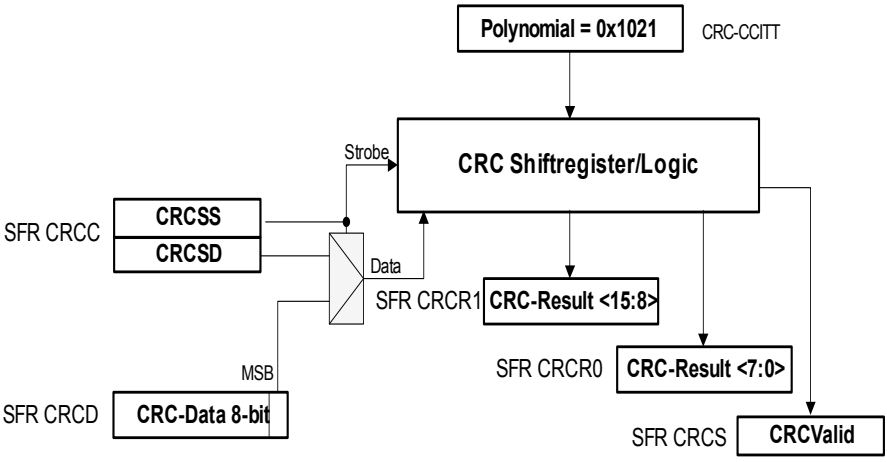


Figure 19 CRC (Cyclic Redundancy Check) Generator/Checker

CRC is a powerful method to detect errors in datapackets that have been transmitted over a distorted connection. The CRC Generator/Checker divides each byte of a datapacket that is transmitted/received, by a polynomial, leaving the remainder, which represents the checksum. The CRC-Generator/Checker is using the 16Bit CCITT polynomial 1021_H ($x^{16}+x^{12}+x^5+1$). The 16 bit start value is determined by SFR CRC0 and SFR CRC1.
The CRC Generator/Checker can process 8 bit parallel and/or serial data.

Table 38 CRC Data & Result Register

SFR (Abbr)	Addr	Access	Default Value	Register
CRCD	AA_H	rw	00_H	CRC Data Register
CRC0	AC_H	rw	00_H	CRC Result Register 0 low byte
CRC1	AD_H	rw	00_H	CRC Result Register 1 high byte

Table 39 SFR Address $A9_H$: CRCC - CRC Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	CRCSD	CRCSS	n.u.	n.u.	n.u.	CRCValid	n.u.
0/0	rw 0/0	w 0/0	0/0	0/0	0/0	r 1/1	0/0
CRCSD		CRC Serial Data					
CRCSS		CRC Serial Data Strobe use CRCSS to serial strobe data bit CRCSD into CRC encoding/decoding procedure.					
CRCValid		CRC Valid Is set by hardware on vaild CRC results, that means all CRC-bits are 0.					

Byte aligned CRC Generation

CRC generation is done executing the following steps:

- The CRC shiftregister has to be initialized e.g. with '1's by writing FF_H to both SFR CRC0 and SFR CRC1.
- The databytes which should be checked by the CRC Checker have to be shifted one after the other into the SFR CRCD. The process of CRC Generation is automatically invoked when data bytes are written to the SFR CRCD.
- The resulting checksum value is available in the CRC Result Register SFR CRC0 and SFR CRC1 after processing the last data byte.

Byte aligned CRC Checking

CRC checking is done in the following steps:

- The CRC shiftregister has to be initialized e.g. with '1's by writing FF_H to both SFR CRC0 and SFR CRC1.
- The databytes which should be checked by the CRC Checker have to be shifted serially (one after the other) into the SFR CRCD. It is important that the order (MSB-LSB) is the same as it was during the CRC Generation. The process of CRC Checking is automatically invoked when data bytes are written to the SFR CRCD.
- Write the 16 bit CRC-value to the SFR CRCD beginning with the high byte after processing all user-data.
- The SFR bit CRCC.1[CRCValid] indicates the correctness of the CRC calculation after processing the last data byte.

Serial bitstream CRC Generation/Checking

The CRC Generator/Checker features an additional serial mechanism to perform CRC generation and checking of non byte-aligned data streams. In this case SFR bit CRCC.5[CRCSS] and SFR bit CRCC.6[CRCSD] are used instead of SFR CRCD.

The data stream is written bit by bit into SFR bit CRCC.6[CRCSD]. Each bit is processed by forcing the flag SFR bit CRCC.5[CRCSS].

The following figure shows an example for the usage of SFR bit CRCC.5[CRCSS] and SFR bit CRCC.6[CRCSD].

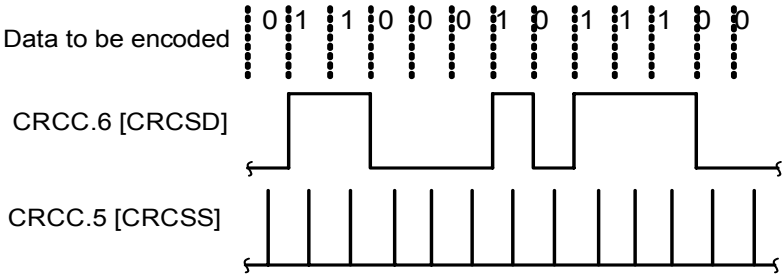


Figure 20 Example for serial CRC generation/checking

Note: The serial and byte-aligned generation/checking mechanism is interchangeable within the same generation/checking process. E.g. if a data packet consists of 18 bits , then 16 bits can be processed byte-aligned via SFR CRCD and the two remaining bits can be processed bit-aligned by using SFR bit CRCC.5[CRCSS] and SFR bit CRCC.6[CRCSD].

2.5.12 Pseudo Random Number Generator

For many applications a pseudo random number generator is needed, e.g. to vary the interval period between transmissions. For this purpose a Maximum Length linear Feedback Shift Register (MLFSR) is available as a hardware unit.

Table 40 SFR Address AB_H: SFR RNGD - Random Number Generator Data

SFR (Abbr)	Addr	Access	Default Value	Register
RNGD	AB_H	rw	u/55_H	Random Number Generator Data Register

A user-defined start value (except 00_H) can be written to SFR RNGD. The default value after startup is 55_H.

The generation of a new random number is initiated by setting SFR bit CFG1.5[RNGEn].

After the random number is generated, SFR bit CFG1.5[RNGEn] is reset automatically and the value is available in SFR RNGD.

2.5.13 Timer Unit (Timer 0, Timer 1, Timer 2, Timer 3)

The PMA7110 comprises four independent 16 bit timers. Timer 0/1 operate as up-counters, timer 2/3 operate as down-counters.

Timer / counter 0 and 1 are fully compatible with Timer / counter 0 and 1 of the Standard 8051 and can be used in the same four operating modes:

- Mode 0: 8-bit timer/counter with a divide-by-32 prescaler
- Mode 1: 16-bit timer/counter
- Mode 2: 8-bit timer/counter with 8-bit auto-reload
- Mode 3: Timer/counter 0 is configured as one 8-bit timer/counter and one 8-bit timer/counter 1 in this mode holds its count. The effect is the same as setting TR1 = 0.

The external inputs PP1 and PP9 can be programmed to function as a gate for timer/counters 0 and 1 to facilitate pulse width measurements. Each timer consists of two 8-bit registers (TH0 and TL0 for timer/counter 0, TH1 and TL1 for timer/counter 1) which may be combined to one timer configuration depending on the mode that is established. The functions of the timers are controlled by two special function registers TCON and TMOD. In the following descriptions the symbols TH0 and TL0 are used to specify the high-byte and the low-byte of Timer 0 (TH1 and TL1 for Timer 1, respectively). The operating modes are described and shown for Timer 0. If not explicity noted, this applies also to Timer 1.

2.5.13.1 Basic Timer Configuration

Timer 0 -Timer 3 comprise four fully programmable 16-bit timers, which can be used for time measurements as well as generating time delays. The clock source is selectable in order to enlarge the timer runtime.

SFR TMOD and SFR TMOD2 are used to select the clock source and the desired timer mode.

Table 41 SFR Address 89_H: TMOD - Timer Mode Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T1Gate	**T1C/T**	**T1M1**	**T1M0**	**T0Gate**	**T0C/T**	**T0M1**	**T0M0**
rw 0/0	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**
T1Gate		Timer 1 Gate Control bit (gating input: PP8)					
T1C/T		Timer 1 Counter / not Timer (count input: PP9)					
T1M1-0		Timer 1 Mode 00b: Mode 0. 8-bit timer with a divided-by-32 prescaler 01b: Mode 1.16-bit timer 10b: Mode 2. 8-bit timer with 8-bit auto-reload 11b: Mode 3. Timer 1 hold its count. The effect is the same like setting TR1=0					
T0Gate		Timer 0 Gate Control bit (gating input: PP0)					

T0C/T		Timer 0 Counter / not Timer (count input: PP1)
T0M1-0		Timer 0 Mode 00b: Mode 0. 8-bit timer with a divided-by-32 prescaler 01b: Mode 1.16-bit timer 10b: Mode 2. 8-bit timer with 8-bit auto-reload 11b: Mode 3. Two 8-bit timers.

Table 42 SFR Address $C9_H$: TMOD2 - Timer Mode Register 2 (Timer 2/3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T3Clk1	**T3Clk0**	**T2Clk1**	**T2Clk0**	**n.u.**	**TM2**	**TM1**	**TM0**
rw 0/0	**rw 0/0**	**rw 0/0**	**rw 0/0**	**0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**
T3Clk1-0		Timer 3 Clock Source Select 00b: undivided systemclock (see **Figure "PMA7110 Internal Clock Divider" on Page 71**) 01b: systemclock divided by 8 (see **Figure "PMA7110 Internal Clock Divider" on Page 71**) 10b: 2 kHz LP RC Oscillator clock 11b: PP2 event count (rising edge)					
T2Clk1-0		Timer 2 Clock Source Select 00b: undivided systemclock (see **Figure "PMA7110 Internal Clock Divider" on Page 71**) 01b: systemclock divided by 8 (see **Figure "PMA7110 Internal Clock Divider" on Page 71**) 10b: 2 kHz LP RC Oscillator clock 11b: Timer 3 overflow event count					
TM2-0		Timer Mode 000b: Mode 0 001b: Mode 1 010b: Mode 2 011b: Mode 3 100b: Mode 4 101b: Mode 5 110b: not used 111b: Mode 7					

The timer registers described in **Table 43 "SFR Address 8AH--8DH and CAH--CDH: Timer Registers" on Page 92** are used as start values and - once the timer is started - hold the actual counter values and can be read by the application at any time.

Note: The purpose of these registers depends on the selected timer mode.

Table 43 SFR Address $8A_H$--$8D_H$ and CA_H--CD_H: Timer Registers

SFR (Abbr)	Addr	Access	Default Value	Register
TH0	$8C_H$	rw	$00_H/00_H$	Timer 0 Register Upper Byte
TL0	$8A_H$	rw	$00_H/00_H$	Timer 0 Register Lower Byte
TH1	$8D_H$	rw	$00_H/00_H$	Timer 1 Register Upper Byte
TL1	$8B_H$	rw	$00_H/00_H$	Timer 1 Register Lower Byte
TH2	CD_H	rw	$00_H/00_H$	Timer 2 Register Upper Byte
TL2	CC_H	rw	$00_H/00_H$	Timer 2 Register Lower Byte
TH3	CB_H	rw	$00_H/00_H$	Timer 3 Register Upper Byte
TL3	CA_H	rw	$00_H/00_H$	Timer 3 Register Lower Byte

SFR TCON and SFR TCON2 are used for starting and stopping timers and for status indication of all timers.

Note: The purpose of this bits depends on the selected timer mode.

Table 44 SFR Address 88_H: TCON - Timer Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TF1	**TR1**	**TF0**	**TR0**	**IE1**	**IT1**	**IE0**	**IT0**
rw 0/0	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**
TF1		Timer 1 Overflow Flag					
TR1		Timer 1 Run control Bit					
TF0		Timer 0 Overflow Flag					
TR0		Timer 0 Run control Bit					
IE1		Interrupt 1 Edge Flag					
IT1		Interrupt 1 Type control bit					
IE0		Interrupt 0 Edge Flag					
IT0		Interrupt 0 Type control bit					

Setting the SFR bit TCON.4[TR0] (respectively SFR bit TCON.6[TR1]) starts Timer 0 (resp. Timer 1). It counts using the selected clock (see SFR TMOD) until the timer is elapsed. SFR bit TCON.5[TF0] (resp. SFR bit TCON.7[TF1] is set.
If the selected timer mode used timer reload, then the timer is automatically reloaded and restarted.

If the selected timer mode doesn't use timer reload, the timer is stopped and SFR bit TCON.4[TR0] (resp. SFR bit TCON.6[TR1]) is cleared.

Table 45 SFR Address $C8_H$: TCON2 - Timer Control Register 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T3Mask	**n.u.**	**T3Full**	**T3Run**	**T2Mask**	**n.u.**	**T2Full**	**T2Run**
rw 0/0	**0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**0/0**	**rw 0/0**	**rw 0/0**
T3Mask		Timer 3 Interrupt Mask Bit. When set to zero the Interrupt from Timer 3 is disabled					
T3Full		Timer 3 Full bit					
T3Run		Timer 3 Run bit					
T2Mask		Timer 2 Interrupt Mask Bit. When set to zero the Interrupt from Timer 2 is disabled					
T2Full		Timer 2 Full bit					
T2Run		Timer 2 Run bit					

Setting the SFR bit TCON2.0[T2Run] (respectively SFR bit TCON2.4[T3Run]) starts Timer 3 (resp. Timer 2). It counts using the selected clock (see SFR TMOD) until the timer is elapsed. SFR bit TCON2.1[T2Full] (resp. SFR bit TCON2.5[T3Full] is set.
If the selected timer mode used timer reload, then the timer is automatically reloaded and restarted.

If the selected timer mode doesn't use timer reload, the timer is stopped and SFR bit TCON2.0[T2Run] (resp. SFR bit TCON2.4[T3Run]) is cleared.

2.5.13.2 General Operation Description Timer 0 and Timer 1

Mode 0

When putting Timer/counter 0 (resp. Timer/counter 1) into Mode 0 the timer is configured as an 8-bit timer/counter with a divide-by-32 prescaler. **Figure 21 "Timer/Counter 0, Mode 0, 13-Bit Timer/Counter." on Page 94** shows the Mode 0 operation. In this mode, the timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the timer overflow flag TCON.5 [TF0] (resp. TCON.7 [TF1]). The overflow flag TCON.5 [TF0] (resp. TCON.7 [TF1]) can then be used to request an interrupt. The counted input is enabled to the timer when TCON.4 [TR0] = 1 and either TMOD.3 [T0Gate] = 0 or INT0 = 1 (setting T0Gate = 1 allows the timer to be controlled by external input PP1 (resp. PP9), to facilitate pulse width measurements).

The 13-bit register consists of all 8 bits of TH0 (resp. TH1) and the lower 5 bits of TL0 (resp TL1). The upper 3 bits of TL0 (resp. TL1) are indeterminate and should be ignored. Setting the run flag TCON.4 [TR0] (resp. TCON.6 [TR1]) does not clear the registers.

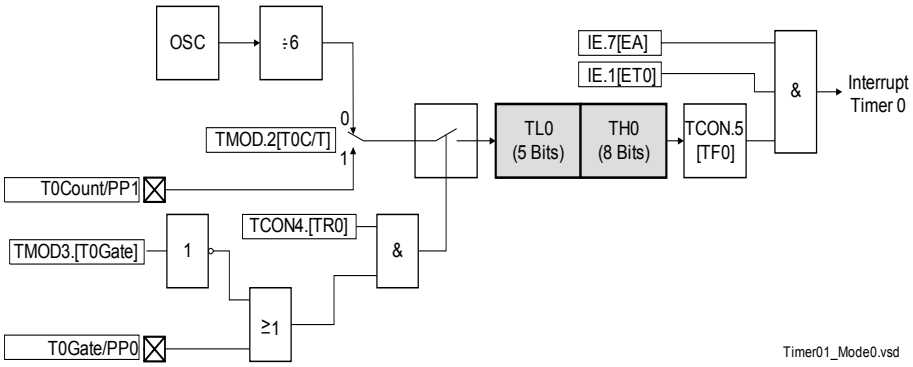


Figure 21 Timer/Counter 0, Mode 0, 13-Bit Timer/Counter.

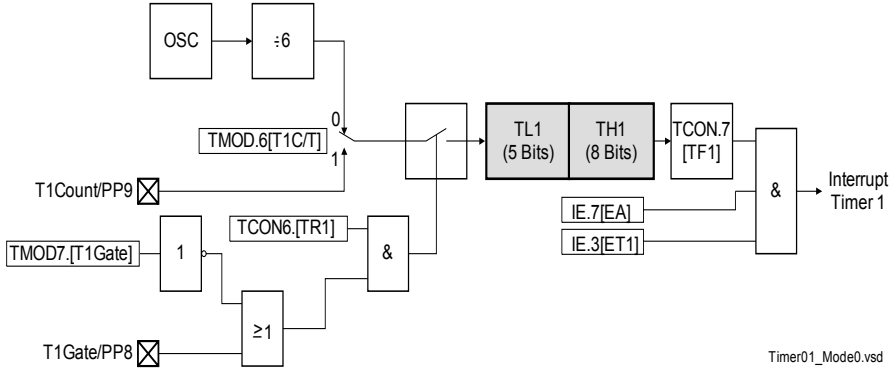


Figure 22 Timer/Counter 1, Mode 0, 13-Bit Timer/Counter

Mode 1

Mode 1 is equal to Mode 0 with the difference that the timer register is running with all 16 bits.

Mode 2

Mode 2 configures the timer registers as an 8-bit counter in TL0 (resp. TL1) with automatic reload, as shown in **Figure 23 "Timer/Counter 0, Mode 2: 8-Bit Timer/Counter with auto-reload" on Page 95**. Overflow from TL0 (resp. TL1) not only sets TCON.5 [TF0] (resp. TCON.7 [TF1]) , but also reloads TL0 (resp. TL1) with the

contents of TH0 (resp. TH1) , which is preset by software. The reload leaves TH0 (resp. TH1) unchanged.

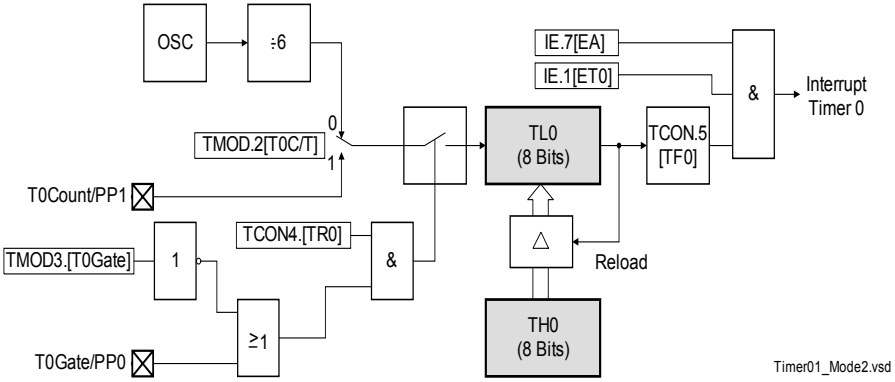


Figure 23 Timer/Counter 0, Mode 2: 8-Bit Timer/Counter with auto-reload

Mode 3

Mode 3 has different effects on Timer 0 and Timer 1. Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TCON.6 [TR1]=0. Timer 0 establishes TL0 and TH0 as two separate counters (**Figure 24 "Timer/Counter 0, Mode 3: Two 8-Bit Timers/Counters" on Page 96**). TL0 uses the Timer 0 control bits: TMOD.2 [T0C/T], TMOD.3 [T0Gate], TCON.4 [TR0], TCON.5 [TF0] and the pin status of PP0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TCON.6 [TR1] and TCON.7 [TF1] from Timer 1. Thus, TH0 now controls the Timer 1 interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer or counter. When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3, or in fact, in any application not requiring an interrupt from Timer 1 itself.

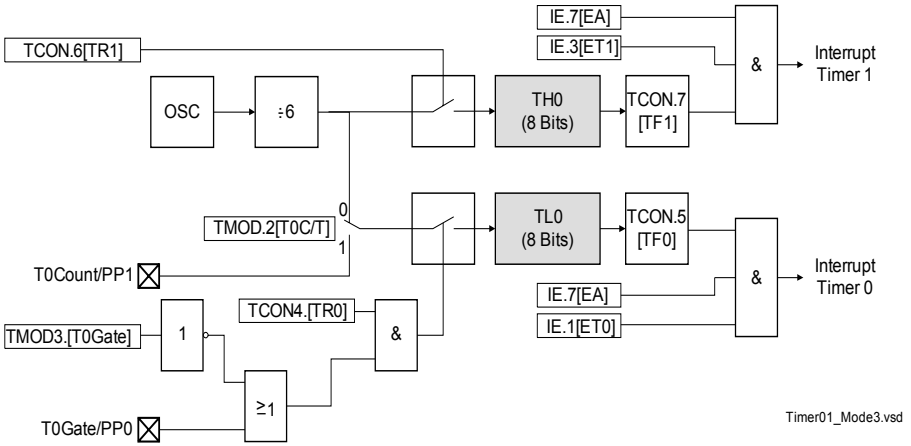


Figure 24 Timer/Counter 0, Mode 3: Two 8-Bit Timers/Counters

Interrupt support

This module supports interrupt generation on overrun of timer/counter 0 as well as timer/counter 1. Additional to these timer/counter interrupts, two external interrupts are handled by this unit, too (ref. to standard 8051).

When an Interrupt event occurs in Idle state, the device starts operation immediately and the PC is set to the appropriate interrupt vector.

Timer/counter interrupts

On overrun of the upcounting timer/counter from all ’1’ to all ’0’ the flag TCON.5 [TF0] or TCON.7 [TF1] is set by hardware. These flags acts as interrupt request flags: a ’1’ indicates a pending interrupt request. These flags are cleared by hardware as on Standard 8051 when the corresponding interrupt vector has been fetched by the CPU.

External interrupts 0 and 1

As on the Standard 8051, the interrupt control bits for the External Interrupts 0 and 1 are located in the TCON register. For a detailed description of the External Interrupts please refer to **“Interrupt Sources on the <Dev_NameShort1>” on Page 74**.

2.5.13.3 Timer Modes for Timer 2 and Timer 3

Timer mode 0

comprises:

- 16 bit timer with reload

The timer unit is configured as a 16 bit reloadable timer. SFR TL2 and SFR TH2 hold the start value. If SFR bit TCON2.0[T0Run] is set, the timer starts down counting. SFR bit TCON2.1[T0Full] is set when the timer is elapsed (underflow from 0 to 0xFF). The timer value is reloaded from SFR TL3 and SFR TH3 and the timer is restarted automatically. SFR bit TCON2.1[T0Full] has to be reset by software. It is not cleared on read-access.

Note: In this mode, both SFR bit TCON2.4[T1Run] and SFR bit TCON2.5[T1Full] are not used.

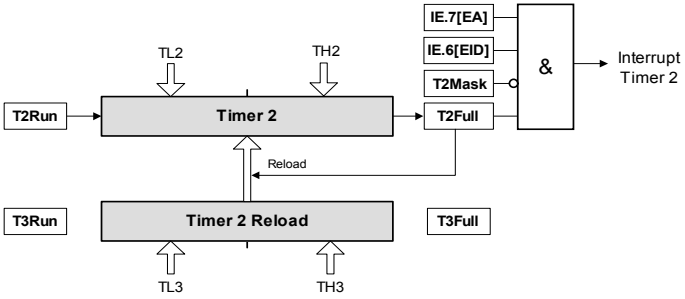


Figure 25 Timer mode 0

Timer mode 1

Comprises:

- 16 bit timer without reload
- 8 bit timer with reload and bitrate strobe signal for RF Transmitter

Timer 2 operates as 16 bit timer with start value in SFR TL2 and SFR TH2, timer run bit SFR bit TCON2.0[T0Run] and timer elapses indicator SFR bit TCON2.1[T0Full]. If the timer elapses, it stops, sets SFR bit TCON2.1[T0Full] and resets the timer run bit SFR bit TCON2.0[T0Run].

Timer 3 sets up a reloadable 8 bit timer holding the startup value in SFR TL3, timer reload value in SFR TH3, timer run bit in SFR bit TCON2.4[T1Run] and timer elapses indicator in SFR bit TCON2.5[T1Full].

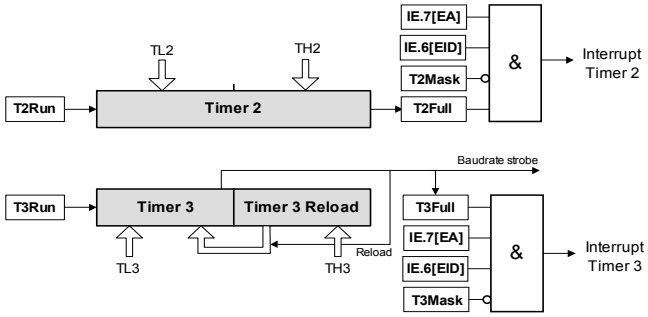


Figure 26 Timer mode 1

Timer mode 2

Comprises:

- 8 bit timer with reload
- 8 bit timer with reload and bitrate strobe signal for RF Transmitter

Timer 2 sets up a reloadable 8 bit timer holding the start value SFR TL0, timer reload value SFR TH0, timer run bit SFR bit TCON2.0[T0Run] and timer elapsed indicator SFR bit TCON2.1[T0Full].

Timer 3 sets up a reloadable 8 bit timer holding the start value SFR TL1, timer reload value SFR TH1, timer run bit SFR bit TCON2.4[T1Run] and timer elapsed indicator SFR bit TCON2.5[T1Full] .

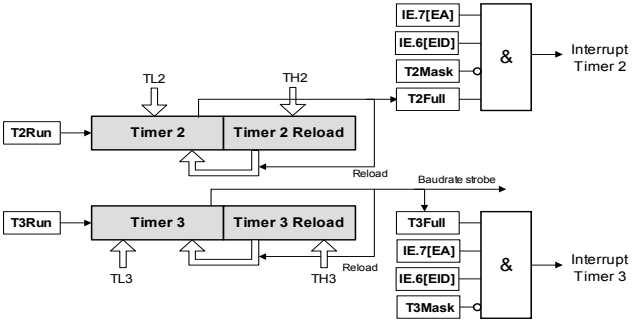


Figure 27 Timer mode 2

Timer mode 3

Comprises:

- 8 bit timer without reload (1)
- 8 bit timer without reload (2)
- 8 bit timer with reload and bitrate strobe signal for RF Transmitter

Timer 2 (1) utilizes SFR TL0 as starting value and T0Full as timer elapsed flag. Setting SFR bit TCON2.0[T0Run] starts the timer, and SFR bit TCON2.1[T0Full] is set when the timer is elapsed. SFR bit TCON2.0[T0Run] is reset automatically if the timer elapses.

Timer 3 (2) utilizes SFR TH0 as starting value and SFR bit TCON2.5[T1Full] as timer elapsed flag. Setting SFR bit TCON2.4[T1Run] starts the timer, and SFR bit TCON2.5[T1Full] is set when the timer is elapsed. SFR bit TCON2.4[T1Run] is reset automatically if the timer elapses.

Timer 3 operates exclusive as 8-bit bitrate timer for Manchester coding. Therefore the timer needs neither a run nor an elapsed bit. It is started automatically when the timer mode is set.

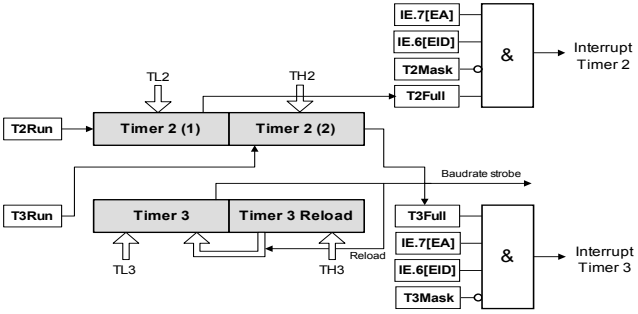


Figure 28 Timer mode 3

Timer mode 4

Comprises:

- 16 bit timer with reload and bitrate strobe signal for RF Transmitter

The timer unit is configured as a 16 bit reloadable timer. SFR TL1 and SFR TH1 hold the start value. If SFR bit TCON2.4[T1Run] is set, the timer starts counting. SFR bit TCON2.5[T1Full] is set when the timer is elapsed. The timer value is reloaded from SFR TL0 and SFR TH0 and the timer is restarted automatically. SFR bit TCON2.5[T1Full] has to be reset by software. It is not cleared on read-access.

Note: In this mode both SFR bit TCON2.0[T0Run] and SFR bit TCON2.1[T0Full] *are not used.*

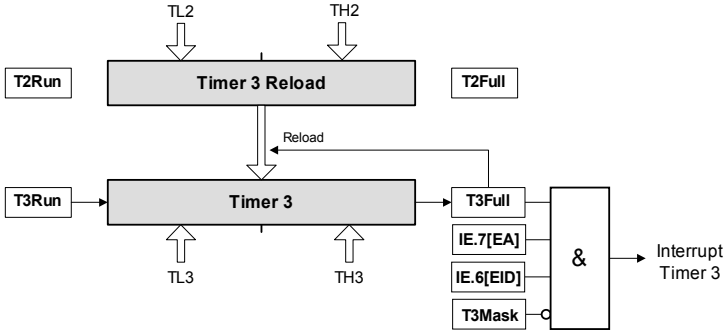


Figure 29 Timer mode 4

Timer mode 5

comprises:

- 8 bit timer with reload
- 16 bit timer without reload and bitrate strop signal for RF Transmitter

SFR bit TCON2.0[T0Run] starts the timer, and SFR bit TCON2.1[T0Full]

Timer 2 sets up a reloadable 8 bit timer holding the start value in SFR TL0, timer reload value in SFR TH0, timer run bit SFR bit TCON2.0[T0Run] and timer elapsed indicator in SFR bit TCON2.1[T0Full].

Timer 3 operates as a 16 bit timer with the start value in SFR TL1 and SFR TH1, timer run bit SFR bit TCON2.4[T1Run] and timer elapsed indicator SFR bit TCON2.5[T1Full]. If the timer elapses, the timer stops SFR bit TCON2.5[T1Full] is set and the timer run bit SFR bit TCON2.4[T1Run] is reset.

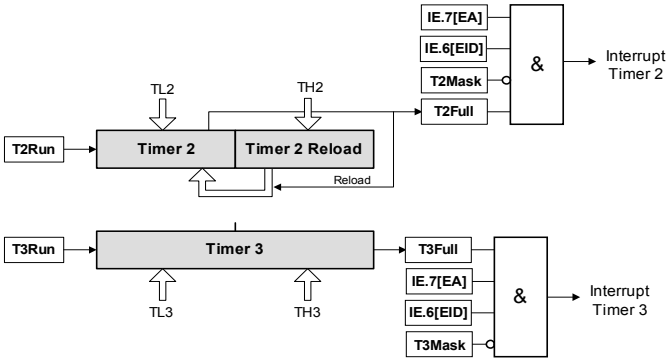


Figure 30 Timer mode 5

Timer mode 6

Comprises:

- 16 bit timer without reload
- 16 bit timer without reload and bitrate strobe signal for RF Transmitter

Timer 2 operates as a 16 bit timer with the start value in SFR TL0 and SFR TH0, timer run bit SFR bit TCON2.0[T0Run] and timer elapsed indicator SFR bit TCON2.1[T0Full]. If the timer is elapsed the timer is stopped, SFR bit TCON2.1[T0Full] is set and the timer run bit SFR bit TCON2.0[T0Run] is reset.

Timer 3 operates as a 16 bit timer with the start value in SFR TL1 and SFR TH1, timer run bit SFR bit TCON2.4[T1Run] and timer elapsed indicator SFR bit TCON2.5[T1Full]. If the timer elapses, the timer stops, SFR bit TCON2.5[T1Full] is set and the timer run bit SFR bit TCON2.4[T1Run] is reset.

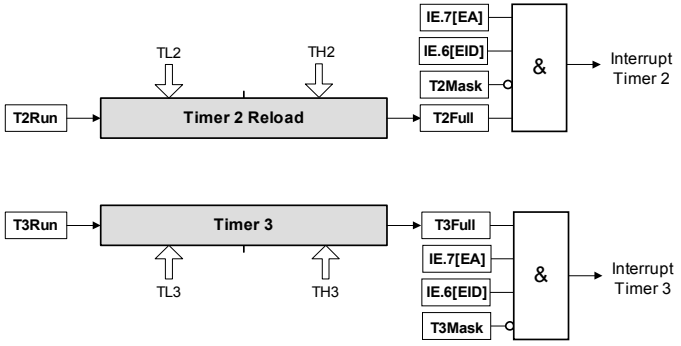


Figure 31 Timer mode 6

Timer mode 7

Comprises:

- 16 bit timer for Interval Timer calibration
- 8 bit timer with reload and bitrate strobe signal for RF Transmitter

Timer 2 operates as 16 bit clock counter during one 2 kHz RC LP Oscillator period with the counting value provided in SFR TL0 and SFR TH0, a timer run bit SFR bit TCON2.0[T0Run] and timer overflow indicator SFR bit TCON2.1[T0Full]. When SFR bit TCON2.0[T0Run] is set, the counter starts counting on the next rising edge of the 2 kHz RC LP Oscillator and is stopped at the subsequent rising edge. This Timer mode is used for e.g. Interval Timer Calbration by the ROM library functions (see [1] **“Reference SFR Registers” on Page 144**).

Timer 3 sets up a reloadable 8 bit Timer holding the startup value in SFR TL1, timer reload value in SFR TH1, timer run bit in SFR bit TCON2.4[T1Run] and timer elapsed indicator in SFR bit TCON2.5[T1Full].

Note: This timer mode is not recommended for application usage. It is used by the ROM library functions for calibration purpose.

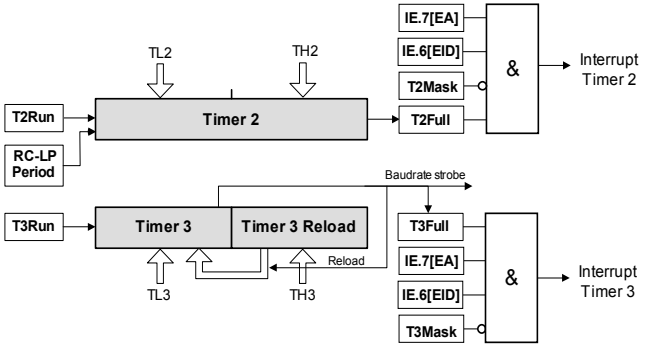


Figure 32 Timer mode 7

2.5.14 General Purpose Input/Output (GPIO)

Ten GPIO pins are available and can either be used by the application for general purposes or are fixed assigned to one peripheral (**"Alternative Port Functionality" on Page 109**). When used as GPIO pins they can be accessed directly by the processor. Pullup and pulldown resistors are configurable on demand to allow wired-AND and wired-OR functions. All peripheral port pins are configured as input with the pullup resistor which will be enabled after a Power On Reset. Pin-status will be kept during Powerdown.

2.5.14.1 Peripheral Port Basic Configuration

Table 46 Peripheral I/O Port Registers

SFR (Abbr)	Addr	Access	Default Value	Register
P1DIR	91_H	rwuu/	FF_H	PP0-7 Data Direction Register
P1IN	92_H	r	x/x	PP0-7 Data Input Register
P1OUT	90_H	rw	u/FF_H	PP0-7 Data OUT Register
P1SENS	93_H	rw	u/00_H	PP0-7 Sensitivity Register
P3DIR	EB_H	rw	u/03_H	PP8-9 Data Direction Register
P3IN	EC_H	r	x/x_H	PP8-9 Data Input Register
P3OUT	$B0_H$	rw	u/03_H	PP8-9 Data OUT Register
P3SENS	ED_H	rw	u/0_H	PP8-9 Sensitivity Register

The following table shows the different possible configurations for the GPIO- Port.

Table 47 GPIO Port Configuration

PPDx	PPOx	PPSx	I/O	pullup/ pulldown	Comment
0	0	-	Output	no	LOW (sink)
0	1	-	Output	no	HIGH (source)
1	0	-	Input	no	high-Z (Tri-State Bidirectional)
1	1	0	Input	pullup	Weak-High (Quasi Bidirectional)
1	1	1	Input	pulldown	Weak-Low (Quasi Bidirectional)

Note: In addition SFR bit PPSx defines the wakeup sensitivity for the external wakeup source (see ***"External Wakeup on PP1-PP4 and PP6-PP9" on Page 109****).*

The x in the table has to be replaced by any of 0 until 9(PP0 - PP9).

Table 48 SFR Address 91_H: P1DIR - IO-Port1 Direction Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD1_7	PD1_6	PD1_5	PD1_4	PD1_3	PD1_2	PD1_1	PD1_0
rw u/1	rw u/1	rw u/1	rw u/1	rw u/1	rw u/1	rw u/1	rw u/1
PD1_7 PD1_6 PD1_5 PD1_4 PD1_3		PP7 - PP3 I/O-Port configuration/Testmode(DMUX6-DMUX2 direction) 1: Input port 0: Output port					
PD1_2 PD1_1 PD1_0		PP2 - PP0 I/O-Port configuration 1: Input port 0: Output port					

Table 49 SFR Address EB_H: P3DIR - IO-Port3 Direction Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	n.u.	n.u.	n.u.	n.u.	n.u.	PPD9	PPD8
0/0	0/0	0/0	0/0	0/0	0/0	rw u/1	rw u/1
PPD9-8		PP-PP8 I/O-Port configuration 1: Input port 0: Output port					

T

Table 50 SFR Address 90_H: P1OUT - I/O-Port1 Data Out Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1_7	P1_6	P1_5	P1_4	P1_3	P1_2	P1_1	P1_0
rw u/1	rw u/1	rw u/1	rw u/1	rw u/1	rw u/1	rw u/1	rw u/1
P1_7-P1_2		PP7 - PP2 Data Out/DMUX6-DMUX1 (Data Out/PullUp enable) 1: Input port 0: Output port					
P1_1-P1_0		PP1 - PP0 Data Out / PullUp enable					

Table 51 SFR Address $B0_H$: P3OUT - I/O-Port3 Data Out Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	n.u.	n.u.	n.u.	n.u.	n.u.	P3_1	P3_0
r 0/0	r 0/0	r 0/0	r 0/0	r 0/0	r 0/0	rw u/1	rw u/1
P3_1 P3_0		PP9 Data Out / PullUp enable PP8 Data Out / PullUp enable					

Table 52 SFR Address 93_H: P1SENS - IO-Port1 Sensitivity Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PS1_7	PS1_6	PS1_5	PS1_4	PS1_3	PS1_2	PS1_1	PS1_0
rw u/0	rw u/0	rw u/0	rw u/0	rw u/0	rw u/0	rw u/0	rw u/0
PS1_x		PPx I/O-Port sensitivity 1b: Pulldown is enabled if SFR P1DIR.x==1 and P1OUT.x==1 0b: Pullup is enable if SFR P1DIR.x==1 and P1OUT.x==1					

The x in the table has to be replaced by either of 0 until 7.

Table 53 SFR Address ED_H: P3SENS - IO-Port3 Sensitivity Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	n.u.	n.u.	n.u.	n.u.	n.u.	PS3_1	PS3_0
r0/0	r0/0	r0/0	r0/0	r0/0	r0/0	rw u/0	rw u/0
PS3_1		PP9 I/O-Port sensitivity 1b: Pulldown 0b: Pullup					
PS3_0		PP8 I/O-Port sensitivity 1b: Pulldown 0b: Pullup					

Table 54 SFR Address 92_H: P1IN - IO-Port1 Data In Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PI1_7	PI1_6	PI1_5	PI1_4	PI1_3	PI1_2	PI1_1	PI_0
r x/x	r x/x	r x/x	r x/x	r x/x	r x/x	r x/x	r x/x
PI1_7-PI1_2		PP7-PP2 data In / Testmode (DMUX7-DMUX2 in)					
PI1_1-PI1_0		PP1-PP0 data In					

Table 55 SFR Address EC_H: P3IN - IO-Port3 Data In Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	n.u.	n.u.	n.u.	n.u.	n.u.	PI3_1	PI3_0
0/0	0/0	0/0	0/0	0/0	0/0	r x/x	r x/x
PI3_1		PP9 data In					
PI3_0		PP8 data In					

2.5.14.2 Spike Suppression on Input Pins

To avoid metastabilities when reading the GPIO pins, a synchronization stage is included and a two-stage spikefilter suppresses spikes, thus data is available to be read after a delay of maximum 2 systemclock periods.

Due to the synchronization stage the following possibilities might occur:

- Signal duration (T_{SIGNAL}) < 1 systemclock period (1 T_{CLK}): Signal is surpressed
- 1 T_{CLK} < T_{SIGNAL} < 2 T_{CLK}: undefined if supressed or passed
- T_{SIGNAL} > 2 T_{CLK}: Signal is available in P1IN register

2.5.14.3 External Wakeup on PP1-PP4 and PP6-PP9

PP1-PP4 and PP6-PP9 can additionally be used as external wakeup sources if enabled by the Wakeup-Mask SFR bit ExWUM.x[MEXTWUx] and configured as input pin by setting SFR bit P1DIR.x[PPDx].
The internal pullup/pulldown resistor is enabled if SFR bit P1OUT.x[PPOx] is set. SFR bit P1SENS.x[PPSx] selects the sensitivity (high active/low active):

Table 56 External Wakeup Configuration

SFR Settings	Description
SFR bit P1DIR.x[PPDx] = 1 SFR bit P1OUT.x[PPOx]=1 SFR bit P1SENS.x[PPSx] = 0 SFR bit ExWUM.x[MEXTWUx] = 0	PPx configured as Input, pullup enabled, Wakeup occurs if PPx is forced to LOW externally.
SFR bit P1DIR.x[PPDx] = 1 SFR bit P1OUT.x[PPOx] =1 SFR bit P1SENS.x[PPSx] = 1 SFR bit ExWUM.x[MEXTWUx] = 0	PPx configured as Input, pulldown enabled, Wakeup occurs if PPx is forced to HIGH externally.

The x in the table has to be replaced by either 1-4 or 5-9 (PP0-PP4, PP6-PP9).

2.5.14.4 Alternative Port Functionality

In the following table, the alternative port functionality is shown - which has higher priority than standard I/O port functionality.

Table 57 I/O Port 1 - Alternative Functionality

Pin	Function	I/O	Description
PP0	I2C-SCL	I	I2C Serial Clock Line Configured to I2C clock pin if SFR bit CFG1.6 [I2CEn] is set. Weak-High has to be provided by an external pullup resistor or by the I2C master device.
	Port Pin I/O	I/O	Standard I/O port functionality
	OPMode1	I/O	Select operation mode
PP1	I2C-SDA	I/O	I2C Serial Data Configured to I2C data pin if bit CFG1.6 [I2CEn] is set. Weak-High has to be provided either by the internal pullup resistor, by an external pullup resistor or by the I2C master device.
	Port Pin I/O	I/O	Standard I/O port functionality
	WU0	I/O	Wake up by external wake up source
	OPMode2	I/O	Select operation mode

Pin	Function	I/O	Description
PP2	TX Data Out	O	If bit CFG1.4[RfTXPEn] is set to one, the Manchester/BiPhase encoded data is delivered serial to PP2. An external device can process the data.
	Port Pin I/O	I/O	Standard I/O port functionality
	WU1	I/O	Wake up by external wake up source
PP3	SPI_CS	I/O	SPI bus interface chip select
	Port Pin I/O	I/O	Standard I/O port functionality
	WU2	I/O	Wake up by external wake up source
PP4	SPI_MISO	I/O	SPI bus interface master in slave out
	Port Pin I/O	I/O	Standard I/O port functionality
	WU3	I/O	Wake up by external wake up source
PP5	SPI_MOSI	I/O	SPI bus interface master out slave in
	Port Pin I/O	I/O	Standard I/O port functionality
PP6	SPI_Clk	I/O	SPI bus interface clock
	Port Pin I/O	I/O	Standard I/O port functionality
	WU4	I/O	Wake up by external wake up source
PP7	Port Pin I/O	I/O	Standard I/O port functionality
	WU5	I/O	Wake up by external wake up source
PP8	Port Pin I/O	I/O	Standard I/O port functionality
	WU6	I/O	Wake up by external wake up source
PP9	Ext_Int	I/O	Interrupt by external interrupt source
	Port Pin I/O	I/O	Standard I/O port functionality
	WU7	I/O	Wake up by external wake up source

2.5.15 I²C- Interface

For communication between a external hardware and the PMA7110, a I²C master/slave interface is implemented.

- PP1 is used as a serial data line (SDA)
- PP0 is used as a serial clock line (SCL)
- PMA7110 responds to I²C- Address $6C_H$ or to a general call if enabled by addressing slave address 00_H. General call is enabled by setting SFR bit I2CC.6[GCEn].
- Data transfer up to 100 kbit/s in standard mode, or 400 kbit/s in fast mode.

To control I²C master/slave interface, the following registers are implemented:

Table 58 SFR I²C Control, Status und DataRegister

SFR (Abbr)	Addr	Access	Default Value	Register
I2CB	$B1_H$	rw	$00/001_H$	I²C Bitrate Register.
I2CC	$A2_H$	rw	$00/00_H$	I²C Control Register.
I2CS	$9B_H$	r/rc	$00/00_H$	I²C Status Register.
I2CD	$9A_H$	rw	$00/00_H$	I²C DataIn / DataOut Register. If written, data are stored in the I²C internal data transmit register - if read, data is read from the data receive register. Flags TBF and RBF are available in status register.
I2CM	$A3_H$	rw	$6C/6C_H$	I²C Mode Register.

The basic I²C-bus configuration is set for both master- and slave mode. To allow bitlogic operations this register is readable and writeable. The contained bits are partially set by software and reset by hardware resp. set and reset by software itself. The control register is only applicable in master mode; in slave mode all functional steps are done automatically without external control.

Table 59 SFR Address $A2_H$: I2CC - I²C Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	GCEn	INP	ACKDT	ACKEN	PEN	RSEN	SEN
0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0
GCEN		I²C General Call Enable.					
INP		I²C interrupt/not-polling handling (0: interrupt, 1: polling mode).					
ACKDT		I²C acknowledge data (0: ACK, 1: nACK).					
ACKEN		I²C acknowledge sequence enable.					
PEN		I²C STOP condition enable.					

RSEN		I^2C repeated START condition enable.
SEN		I^2C START condition enable.

Table 60 SFR Address $9B_H$: I2CS - I^2C Status Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AM	**CD**	**OV**	**S**	**RnW**	**RAck**	**TBF**	**RBF**
rc 0/0	**rc 0/0**	**rc 0/0**	**rc 0/0**	**r 0/0**	**r 0/0**	**r 0/0**	**r 0/0**
AM		Address match - set if device address matches with received address byte					
CD		I2C bus collision detected					
OV		Overflow Bit - set if received byte has not been read out before next byte received; also set if byte has not been transmitted after writing new byte to register I2CD. In both cases, the old byte value is kept, the new byte is rejected. The bit is automatically cleared by hardware if I2CS is read.					
S		I2C transmission in progress - set on occurrance of start condition and reset on occurrance of stop condition.					
RnW		Read/Write Bit Information - states the actual state received with device address					
RAck		Received Acknowledge Level - states the actual level of the received acknowledge (’0’ if acknowledge, ’1’ if not-acknowledge received).					
TBF		Transmit Buffer Full - set by hardware if register I2CD is written; cleared automatically if data byte is taken over by the shift register to be transmitted.					
RBF		Receive Buffer Full - set by hardware if a full data byte is received; cleared automatically if register I2CD is read.					

Table 61 SFR Address $9A_H$: I2CD - I2C Data Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I2CD.7	**I2CD.6**	**I2CD.5**	**I2CD.4**	**I2CD.3**	**I2CD.2**	**I2CD.1**	**I2CD.0**
rw 0/0	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**
I2CD.7-0		8 bit Read/Write Data. Access should be done after reading I2CS Bits [TBD, RBF]					

Table 62 SFR Address $B1_H$: I2CB - I2C Bitrate Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPIB.7	**SPIB.6**	**SPIB.5**	**SPIB.4**	**SPIB.3**	**SPIB.2**	**SPIB.1**	**SPIB.0**
rw 0/0	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**
I2CB.7-0		8 bit Bitrate Data.					

Table 63 SFR Address $A3_H$: I2CM - I2C Mode Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A7	A6	A5	A4	A3	A2	A1	n.u.
rw 0/0	rw 1/1	rw 1/1	rw 0/0	rw 1/1	rw 1/1	rw 0/0	r 0/0
I2CM.0-7		8 bit Address Data.					

2.5.15.1 Slave mode sequence

Programming the slave I^2C interface

To enable the I^2C interface, the SFR bit I2CC.6[GCEn] has to be set. Once the I^2C interface has been enabled, the PMA7110 waits for a start condition to occur. After the PMA7110 received a start condition, the following received 7 bits are compared to the device address. When the address matches, the hardware automatically generates an acknowledge and sets SFR bit I2CS.7[AM] and SFR bit I2CS.3[RnW].

Depending on SFR bit I2CS.3[RnW], the following two different actions are executed:

Receive I^2C-data

- If SFR bit I2CS.0[RBF] is set, one byte has been shifted to SFR I2CD.
  An acknowledge is automatically set by hardware as long as no receive buffer overflow (SFR bit I2CS.5[OV]) has occurred.
- If SFR bit I2CS.4[S] is set, a stop condition has occurred; the transmission is closed by the master device.
- If SFR bit I2CS.7[AM] is set, a restart condition has been set and a matching address has been received; in case of a write access, a branch to the transmit data subroutine has to be performed.

Transmit I^2C data

- Data to be transmitted has to be written to SFR I2CD.
  SFR bit I2CS.1[TBF] is reset if data is taken over by the shift-register and new data may be written to SFR I2CD. If no data is provided, the I^2C interface automatically sets line SCL to low until data is written to SFR I2CD (slave device gains access over line SCL).
- If SFR bit I2CS.4[S] is set, the transmission process has been terminated by the master and the transmission subroutine can be left.

2.5.15.2 General call sequence

If a general call address is sent and bit I2CC.6 [GCEn] in control register is set the I2C-bus behaves like a slave receiver, i.e. the same procedure may be taken. The defined general call protocol has to be done by software.

2.5.15.3 Master mode sequence

After enabling the I^2C bus module and configuration as master device, it waits for further actions given by the control register (I2CC and simultaneously for a start condition from other master devices; in the later case the master behaves like a slave, i.e. the same procedure described above may be taken. Control over the I2C-bus is only taken if the I2C-bus is in idle state and bit I2CC.0 [SEN] (start enable in the control register plus the address of the wanted device including the access direction bit RnW in status register (I2CS.3 is set by software. The start condition and the following address byte is transmitted immediately on SCL and SDA. An existing slave with the according device address responds with an acknowledge, whereby bits IE.4 [EI2C] and I2CS.2 [RAck] in status register will be set accordingly. After that the master may transmit (write data to data register) or receive (read data register after reception) data. After data reception the master has to set an acknowledge. This is done by setting bit I2CC.3 [ACKEN] and I2CC.4 [ACKDT] in control register.

Please see **Table 30 "SFR Address $A8_H$: IE-Interrupt Enable Register" on Page 76** and **Table 31 "SFR Address $B8_H$: IP-Interrupt Priority Register" on Page 77**.

2.5.16 Serial Peripheral Interface SPI

The PMA7110 supports a 2, 3 or 4 wires bus protocol.

- High speed synchronous data transfer (up to 1.125 Mbit @ 18 MHz clock)
- Four programmable bit rates through prescaler
- 2-wire bus for half duplex transmission; a serial clock line (SPI_Clk) and concatenated data line (SPI_MISO,SPI_MOSI)
- 3-wire bus for full duplex transmission; a serial clock line (SPI_Clk) and two serial data lines (SPI_MISO,SPI_MOSI)
- A 4-wire bus for full duplex transmission plus handshaking can be implemented by utilizing also the Chip Select (SPI_CS). This pin can be used for indicating the beginning of a new byte sequence
- Master or Slave Operation

- Clock Control - Polarity (idle low/high) and Phase (sample data with rising/falling clock edge) are programmable
- Bit Width (1 to 8 bits) and Bit Order (MSB or LSB first) are configurable
- Compatible to SSC (High Speed Synchronous Serial Interface) and standard SPI interfaces
- Protocol is defined by software

The Serial Peripherial Interface, also known as SPI, is a very simple synchronous interface to transfer data on a serial bus, connecting an intelligent master controller with general-purpose slave circuits like slave controller, RAMs, memories and so on. A simple 2-wire (half duplex mode) or 3-wire (full duplex mode) bus is used for communication.

The SPI will operate in the master mode normally, thus the SPI has to drive the clock line (SPI_Clk). Therefore the SPI encloses a dedicated bit rate generator.

Table 64 SFR Address $F4_H$: SPIC - SPI Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	**CSMON**	**DORD**	**MSTR**	**CPOL**	**CPHA**	**n.u.**	**n.u.**
0/0	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**0/0**	**0/0**
DORD		“Data Order” DORD = 0 ... LSB is transmitted and received first DORD = 1 ... MSB is transmitted and received first					
MSTR		“Master/Slave Select” MSTR = 0 ... SPI is configured as slave device (controls port MISO) MSTR = 1 ... SPI is configured as master device (controls port SCK, MOSI)					
CPOL		“Clock Polarity” - defines the initial state of SPI clock line SCK CPOL = 0 ... idle clock line is low and leading clock edge is a low to high transition CPOL = 1 ... idle clock line is high and leading clock edge is a high to low transition					
CPHA		“Clock Phase” determines whether data is active with rising or falling edge of SPI clock SCK. CPHA = 0 ... transmission starts without a rising or falling edge on SPI clock; with first edge detected, the first data bit is latched, with the following edge data are shifted. CPHA = 1 ... a rising or falling edge is generated on SPI clock before data are set; with the following clock edge data are latched before shifted on with consecutive one.					

Table 65 SFR Address $F5_H$:SPID - SFR SPI Data Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPID.7	SPID.6	SPID.5	SPID.4	SPID.3	SPID.2	SPID.1	SPID.0
rw 0/0	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**

Table 66 SFR Address $F6_H$: SPIM - SPI Mode Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FL	**n.u.**	**n.u.**	**ALGN**	**n.u.**	**DWS2**	**DWS1**	**DWS0**
rw 0/0	**0/0**	**0/0**	**rw 0/0**	**0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**
FL		SPI force level FL=0 ... SPI_MISO, SPI_MOSI and SPI_CLK pullup driven weak high level FL=1 ... SPI_MISO, SPI_MOSI and SPI_CLK active driven high level					
DWS2-0		“Data Width Selection (bit 2-0)” Defines the amount of transmitted bits per data byte. If set to “000”, a whole data byte (8 bits) is transmitted (SPI standard). If only a byte fragment should be transferred, it depends on SPIC.5 [DORD] whether the upper DWS.2-0 bits of data register SPID are transmitted or the lower one					
ALGN		Data allign (0: right, 1: left)					

Table 67 SFR Address $F7_H$: SPIS - SPI Status Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRE	**STE**	**SPE**	**SSCC**	**SCSD**	**SCSS**	**SRBF**	**STBE**
rc 0/0	**r 1/1**	**rc 0/0**	**rc 0/0**	**rc 0/0**	**rc 0/0**	**rc 0/0**	**r 1/1**
SRE		“SPI Receive Error” Is set by hardware if a new data frame is completely received but the previous data was not read out from the receive data buffer SPID (data will be overwritten).					
STE		“SPI Transmit Completed” (no further data to transmit)					
SPE		“SPI Phase Error” Is set by hardware if the incoming data at pin MISO (master mode) respectively MOSI (slave mode) sampled with CPU clock, changes between 1 sample before and 2 samples after latching edge of the clock signal.					
SSCC		“SPI Slave Communication Corrupt”					
SCSS		“SPI Chip Select latch Status” If register SPIC is read, this bit is set with the actual state of PP5/SPI-MOSI. CSS is set, if an rising edge is detected on PP5/SPI-MOSI pin (SPI transmission completed).					
SCSD		“SPI Chip Select detected”					

SRBF		"SPI Receive Buffer Full" Is set by hardware if a data byte is received completely; the receive buffer is ready to beread.
STBE		"SPI Transmit Buffer Empty" Is reset by hardware if register SPID is written and automatically set if data byte is transferred to SPI internal shift register.

Table 68 SFR Address $F3_H$: SPIB - SPI Bitrate Register (11 Bit cascaded register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPIB.7	**SPIB.6**	**SPIB.5**	**SPIB.4**	**SPIB.3**	**SPIB.2**	**SPIB.1**	**SPIB.0**
w 0/0	**w 0/0**	**w 0/0**	**w 0/0**	**w 0/0**	**w 0/0**	**w 0/0**	**w 0/0**
SPIB.7 - SPIB.0		Bit 7 - Bit 0					

2.5.17 PROGRAMMING mode Operation

In PROGRAMMING mode the PMA7110 is accessible as a slave using the I²C Interface. The device is operating using the 12 MHz RC HF Oscillator as clock source.

To avoid programming failures all PROGRAMMING mode commands are protected by a 16 bit CRC at the end of each command (**"16Bit CRC (Cyclic Redundancy Check) Generator/Checker" on Page 86** shows details about the used CRC polynom).
The checksum has to be calculated over all bytes in the command excluding the PMA7110 I²C device address.

PROGRAMMING mode commands:

- FLASH Write Line
- FLASH Erase
- FLASH Check Erase Status
- FLASH Read Line
- FLASH Set Lockbyte 3
- Read Status

2.5.17.1 FLASH Write Line

The FLASH Write Line command writes 32 bytes to the FLASH, start address is a multiple of 20_H.

- If transferring the start address, the lower 5 bits are cleared automatically.
- If less than 32 data bytes are received, the contents of the previous write access are written into the FLASH.

- If an already written section in the FLASH gets re-written (without being erased before), the resulting data is undefined.

Note: After the Stop condition (P) is received the data is programmed into the FLASH. During the programming time incoming I²C commands are not acknowledged.

Figure 33 FLASH Write Line Command

AdrHi: MSB of the FLASH address to write to.

AdrLo: LSB of the FLASH address to write to (has to be a multiple of 20_H).

Data0 ... Data31: This data is written into the FLASH memory starting at the specified address. Data0 is written at the lowest specified address.

CRCH: MSB of the CRC sum.

CRCL: LSB of the CRC sum.

2.5.17.2 FLASH Erase

The FLASH Erase command erases 1 to 5 sectors of the FLASH.

Note: After the Stop condition (P) is received the selected FLASH sectors are being erased. During the erase time incoming I²C commands are not acknowledged.

Figure 34 FLASH Erase Command

Table 69 Parameter: Sect

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	n.u.	n.u.	Sector4	Sector3	Sector2	Sector1	Sector0
Sector4		protected area, don't care					
Sector3		protected area, don't care					
Sector2		protected area, don't care					

Sector1		1: erase User Data Sector 0: don't erase User Data Sector
Sector0		1: erase Code sector 0: don't erase Code sector

CRCH: MSB of the CRC sum

CRCL: LSB of the CRC sum

2.5.17.3 FLASH Check Erase Status

This function returns the status of the selected FLASH sector(s). The time required for the checking of the sectors depends on the selected sectors.

Note: After the first Stop condition (P) is received the selected FLASH sectors are checked. During this time incoming I²C commands are not acknowledged.

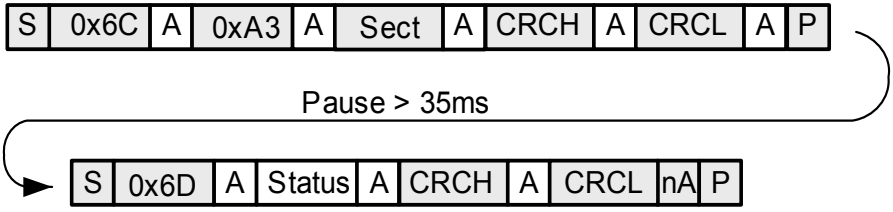


Figure 35 FLASH Check Erase Status Command

Table 70 Parameter: Sect

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	n.u.	n.u.	Sector4	Sector3	Sector2	Sector1	Sector0
Sector4		protected area, thus don't care					
Sector3		protected area, thus don't care					
Sector2		protected area, thus don't care					
Sector1		1: check if User Data Sector is erased 0: don't check User Data Sector					
Sector0		1: check if Code sector is erased 0: don't check Code sector					

CRCH: MSB of the CRC sum.

CRCL: LSB of the CRC sum.

Table 71 Return Value: Status

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	n.u.	n.u.	Sector4	Sector3	Sector2	Sector1	Sector0
Sector4		1: at least one bit is set in the sector 0: sector is erased or untested					
Sector3		1: at least one bit is set in the sector 0: sector is erased or untested					
Sector2		1: at least one bit is set in the sector 0: sector is erased or untested					
Sector1		1: at least one bit is set in the sector 0: sector is erased or untested					
Sector0		1: at least one bit is set in the sector 0: sector is erased or untested					

2.5.17.4 FLASH Read Line

The contents of the FLASH memory can be read out via the I²C interface. If Lockbyte 2 is set, reading of code sector will only yield 0_H, but the Lockbyte 2 itself can still be read for validating the result.

Figure 36 FLASH Read Line Command

AdrHi: MSB of the address to start the read access.

AdrLo: LSB of the read address.

Data0: Value that has been read from the specifed address

Data31: Value that has been read from the specified address + 31.

CRCH: MSB of the CRC sum.

CRCL: LSB of the CRC sum.

2.5.17.5 FLASH Set Lockbyte 2

Lockbyte 2 protect the Code sector. After the Lockbyte 2 is set by the Keil programmer, a startup in DEBUG mode or PROGRAMMING mode is not possible any more.

2.5.17.6 FLASH Set Lockbyte 3

This command sets the Lockbyte 3 protecting the FLASH User Configuration Sector (Sector 1). After the Lockbyte 3 is set, a startup in DEBUG mode or PROGRAMMING mode is not possible any more (see**“” on Page 121** for details).

Note: It is required to set Lockbyte 2 (Code Sector) to enable Lockbyte 3 to become effective.

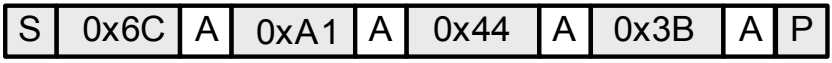


Figure 37 FLASH Set Lockbyte 3 Command

2.5.17.7 Read Status

This function is intended to read out the status of the previous executed functions (pass/fail). It can be called whenever desired to verify if there were errors since the last Read Status call.

.

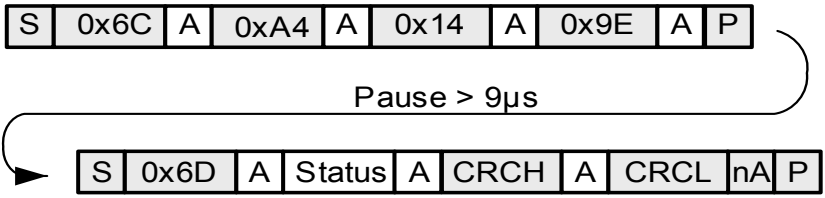


Figure 38 Read Status Command

Table 72 Return Value: Status

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CmdCnt3	**CmdCnt2**	**CmdCnt1**	**CmdCnt0**	**ErrCnt1**	**ErrCnt0**	**InvCmdL**	**CRCFail**
CmdCnt3-0		Counter indicates the number of executed commands since the first detected error. 1111b: 15 commands or more 1110b: 14 commands ... 0001b: 1 command 0000b: error occured in last command					
ErrCnt1-0		Counter of erroneous events since the last Read Status call 11b: three or more errors 10b: two errors 01b: one error 00b: no error					
InvCmdL		1: Invalid command length or execution fail since the last Read Status call 0: no Invalid command length or execution fail occured since the last Read Status call					
CRCFail		1: CRC Failure detected since the last Read Status call 0: no CRC Error occured since the last Read Status call					

CRCH: MSB of the CRC sum

CRCL: LSB of the CRC sum.

☐	**from master to slave**	**S**	**start condition**	**nA**	**not acknowledge**
☐	**from slave to master**	**P**	**stop condition**	**A**	**acknowledge**

SR repeated start condition, may be replaced by Stop-Start condition

Figure 39 I²C-Commands Legend

2.5.18 DEBUG mode Operation

2.5.18.1 Debug Special Function Registers

Table 73 DEBUG mode SFRs:

SFR (Abbr)	Addr	Access	Default Value	Register
DBCL0	94_H	rw	$00_H/00_H$	Debug Compare Register 0 (low)
DBCH0	95_H	rw	$00_H/00_H$	Debug Compare Register 0 (high)
DBTL0	96_H	rw	$00_H/00_H$	Debug Target Register 0 (low)
DBTH0	97_H	rw	$00_H/00_H$	Debug Target Register 0 (high)
DBCL1	$9C_H$	rw	$00_H/00_H$	Debug Compare Register 1(low)
DBCH1	$9D_H$	rw	$00_H/00_H$	Debug Compare Register 1 (high)
DBTL1	$9E_H$	rw	$00_H/00_H$	Debug Target Register 1 (low)
DBTH1	$9F_H$	rw	$00_H/00_H$	Debug Target Register 1 (high)

2.5.18.2 Debugging Facility

During program execution, the Program Counter (PC) of the microcontroller is continuously compared with the contents of the DBCHx + DBCLx registers.
The DBCHx + DBCLx registers can be set to addresses in the FLASH or the ROM code area. In case of a match, the PC is automatically set to the address given in DBTHx + DBTLx, and program execution is continued.

The x in the upper content is 0 or 1.

ROM Debug Function

The debug function mainly consists of a debug handler and a single stepper. The debug handler processes the I^2C communication and debug command interpretation. The debug commands **SetSFR**, **ReadSFR**, **SetData, ReadData** and **SetPC, ReadPC** are executed directly by the debug handler.

The debug commands **Single Step**, **Run Interruptible** and **Run until Breakpoint** are executed by the single stepper. The single stepper fetches the current opcode and enables opcode execution depending on the debug command. To enable single stepping of branch instructions, two sets of debug registers are implemented. Afterwards, the debug handler is entered again.

2.5.18.3 Debugger Commands

SetSFR: Set an SFR to a user-defined value. Exception: It is not possible to set the SFRs used by the Debug Function itself (GPR3, GPR4, GPR5, DBCxx).

Adr: represents the address of the SFR to be set.
Data: this value has to be put into the SFR address specified by *Adr*.

ReadSFR: Read the value of one SFR.

Adr: represents the address of the SFR to be read.
Data: this value was read on the SFR address specified by *Adr*.

SetData: Set one Byte in RAM to a user-defined value.

Adr: represents the address of the Internal data memory to be set.
Data: this value that has to be written into the internal data memory byte specified by *Adr*.

ReadData: Read one Byte of the RAM.

Adr: represents the address of the Internal data memory location to be read.
Data: this value was read from the internal data memory address specified by *Adr*.

SetPC: Set the Program Counter to a user-defined value.

AdrHi: MSB of the new Program Counter.
AdrLo: LSB of the new Program Counter.

ReadPC: Reads the Program Counter

PCHi: MSB of the Program Counter.
PCLo: LSB of the Program Counter.

SingleStep: Execute one Opcode Instruction and return to the debug handler

Run Interruptible: The function consists of device internal consecutive single steps until any I²C command is received on the bus. Compared to running the program in realtime this function has a slower execution speed by a factor of about 1/50, dependent on the executed program.

Run until Breakpoint: The debugged program is executed without single steps in realtime. This enables debugging of runtime critical functions like RF transmission or LF data receiving. The execution is stopped when the PC matches one of the two hardware breakpoints. If none of these breakpoints is hit the communication to the debugger is lost.

BP0 H: MSByte of the Breakpoint Register 0.
BP0 L: LSByte of the Breakpoint Register 0.

from master to slave	S start condition	nA	not acknowledge
from slave to master	P stop condition	A	acknowledge

SR repeated start condition, may be replaced by Stop-Start condition

Figure 40 I²C-Commands Legend

3 Reference

3.1 Electrical Data

3.1.1 Absolute Maximum Ratings

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 74 Absolute Maximum Ratings

#	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
A1	Supply Voltage	V_{batmax}	-0.3	+4.0	V	
A2	Operating Temperature	T_j	-40	+125	°C	Max 24 hrs accumulated over life time
A3	Storage Temperature	T_s	-40	+100	°C	Max 1000 hours
A5	ESD HBM integrity	V_{HBM}	2		kV	all pins According to ESD Standard JEDEC EIA / JESD22-A114-B
A6	ESD CDM integrity	V_{CBM}		500	V	all pins (According to ESDA STM 5.3.1)
				750	V	corner pins (According to ESDA STM 5.3.1)
A7	Latch up	I_{LU}	-100	+100	mA	AEC-Q100 (transient current)
A8	Input voltage at digital input pins	V_{inmax}	-0.3	V_{Bat}+0.3	V	
A9	Input and Output current for digital I/O pins	I_{IOmax}		4	mA	
A10	LF Receiver Input current	I_{LFIN}		4	mA	
A11	XTAL input volage	V_{InXT}	-0.3	V_{REG}+0.3	V	

3.1.2 Operating Range

Within the operational range the IC operates as explained in the circuit description.

Table 75 Operating Range

#	Parameter	Symbol	Limit Values			Unit	Remarks
			min.	typ.	max.		
B1	Supply voltage	V_{Bat1}	2.1		3.6	V	Measurement of, temperature and external sensor. Operation of LF receiver
		V_{Bat2}	1.9		3.6	V	Battery measurements, microcontroller, RF transmitter
		V_{BatFL}	2.5		3.6	V	FLASH programming
B4	Ambient temperature	T_{amb}	-40		85	°C	Normal operation
		T_{FLC}	0	0~35		°C	FLASH code sector programming
		T_{FLD}	0	0~35		°C	FLASH data sector programming

3.1.3 Product Characteristics

Product characteristics involve the spread of values guaranteed within the specified voltage and ambient temperature range.

Typical characteristics are the median of the production.

Supply voltage: V_{bat} = 1.9V ... 3.6V, unless otherwise specified

Ambient temperature: T_{amb} = -40°C ... +85°C, unless otherwise specified

Table 76 Temperature Sensor Characteristics

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks
			min.	typ.	max.		
Q1	Measurement error	T_{Error}	-3		+3	°C	T=-20 ... 70°C V_{bat} = 2.1 ... 3.6V
Q2	Measurement error		-5		+5	°C	T=-40 ... 85°C V_{bat} = 2.1 ... 3.6V

Table 77 Battery Sensor Characteristics

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks
			min.	typ.	max.		
P1	Measurement error	V_{Error}	-100		100	mV	

Table 78 Supply Currents

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks
			min.	typ.	max.		
C1a	Supply Current RF Transmission FSK modulation	$I_{FSK5dbm}$ $I_{FSK8dbm}$ $I_{FSK10dbm}$		8,9 11 12	9 12 15	mA mA mA	@Pout=5/8/10dBm, V_{Bat}=3V, T=-40°C SFR DIVIC = 0x03, f=315MHz
C1b	Supply Current RF Transmission FSK modulation	$I_{FSK5dbm}$ $I_{FSK8dbm}$ $I_{FSK10dbm}$		9,2 11,5 12,9	9,5 12 15	mA mA mA	@Pout=5/8/10dBm, V_{Bat}=3V, T=-40°C SFR DIVIC = 0x03, f=434MHz
C2a	Supply Current RF Transmission FSK modulation	$I_{FSK5dbm}$ $I_{FSK8dbm}$ $I_{FSK10dbm}$		9,7 12,2 12,8	10 14 18	mA mA mA	@Pout=5/8/10dBm, V_{Bat}=3V, T=25°C SFR DIVIC = 0x03, f=315MHz

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks
			min.	typ.	max.		
C2b	Supply Current RF Transmission FSK modulation	$I_{FSK5dbm}$ $I_{FSK8dbm}$ $I_{FSK10dbm}$		9,9 12,3 13,8	10 14 18	mA mA mA	@Pout=5/8/10dBm, V_{Bat}=3V, T=25°C SFR DIVIC = 0x03, f=434MHz
C3a	Supply Current RF Transmission FSK modulation	$I_{FSK5dbm}$ $I_{FSK8dbm}$ $I_{FSK10dbm}$		tbd tbd tbd	tbd tbd tbd	mA mA mA	@Pout=5/8/10dBm, V_{Bat}=3V, T=85°C SFR DIVIC = 0x03, f=315MHz
C3b	Supply Current RF Transmission FSK modulation	$I_{FSK5dbm}$ $I_{FSK8dbm}$ $I_{FSK10dbm}$		tbd tbd tbd	tbd tbd tbd	mA mA mA	@Pout=5/8/10dBm, V_{Bat}=3V, T=85°C SFR DIVIC = 0x03, f=434MHz
C4a	Supply Current RF Transmission FSK modulation	$I_{FSK5dbm}$ $I_{FSK8dbm}$ $I_{FSK10dbm}$		11,3 12,8 16,8	tbd tbd tbd	mA mA mA	@Pout=5/8/10dBm, V_{Bat}=3V, T=-40°C SFR DIVIC = 0x03, f=868MHz
C4b	Supply Current RF Transmission FSK modulation	$I_{FSK5dbm}$ $I_{FSK8dbm}$ $I_{FSK10dbm}$		11,3 13,4 16,7	tbd tbd tbd	mA mA mA	@Pout=5/8/10dBm, V_{Bat}=3V, T=-40°C SFR DIVIC = 0x03, f=915MHz
C4c	Supply Current RF Transmission FSK modulation	$I_{FSK5dbm}$ $I_{FSK8dbm}$ $I_{FSK10dbm}$		11,8 12,9 16,9	14 18 24	mA mA mA	@Pout=5/8/10dBm, V_{Bat}=3V, T=25°C SFR DIVIC = 0x03, f=868MHz
C4d	Supply Current RF Transmission FSK modulation	$I_{FSK5dbm}$ $I_{FSK8dbm}$ $I_{FSK10dbm}$		12,6 15,3 17,1	14 18 24	mA mA mA	@Pout=5/8/10dBm, V_{Bat}=3V, T=25°C SFR DIVIC = 0x03, f=915MHz
C4e	Supply Current RF Transmission FSK modulation	$I_{FSK5dbm}$ $I_{FSK8dbm}$ $I_{FSK10dbm}$		tbd tbd tbd	tbd tbd tbd	mA mA mA	@Pout=5/8/10dBm, V_{Bat}=3V, T=85°C SFR DIVIC = 0x03, f=868MHz
C4f	Supply Current RF Transmission FSK modulation	$I_{FSK5dbm}$ $I_{FSK8dbm}$ $I_{FSK10dbm}$		tbd tbd tbd	tbd tbd tbd	mA mA mA	@Pout=5/8/10dBm, V_{Bat}=3V, T=85°C SFR DIVIC = 0x03, f=915MHz

Note: Matching circuit as used in the 50 Ohm-Output evaluation board at the specified frequency. Tolerances of the passive elements not taken into account

C5	Supply Current POWER DOWN	I_{PD}		500	700	nA	V_{bat}= 3.0V, T= 25°C
				2.6	9	µA	V_{bat}= 3.0V, T= 85°C

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks
			min.	typ.	max.		
C7	Supply Current THERMAL SHUTDOWN	I_{TSHD}	n.u.	n.u.	n.u.	µA	
C8	Supply Current IDLE (SFR DIVIC = 0x00, systemclock = 12 MHz RC Osc.)	I_{IDLE}			tbd	mA	V_{bat}= 3.0V, T= 25°C
					tbd	mA	V_{bat}= 3.0V, T= 85°C
C9	Supply Current RUN (SFR DIVIC = 0x00, systemclock = 12 MHz RC Osc.)	I_{RUN}			tbd	mA	V_{bat}= 3.0V, T= 25°C
					tbd	mA	V_{bat}= 3.0V, T= 85°C

Table 79 RF Transmitter Characteristics

The RF Transmitter is characterized on the testboard with 50 Ohm matching network for specified frequency. Tolerances of the passive elements not taken into accoun. Under this condition, the application is compliant to standards ETSI EN 300 220 and FCC 15.231a/b/e.

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks
			min.	typ.	max.		
D1	Transmit frequency	f_{TX}	300 433 865 902		320 450 870 928	MHz MHz MHz MHz	
D2	Output power transformed to 50 Ohm	P_{5dBm} P_{8dBm} P_{10dBm}	4 7 9	5 8 10	6 9 11	dBm dBm dBm	V_{Bat}=3V, T=25°C
D3	Low temp. output power change	dP_{LT}			1	dB	V_{Bat}=3V, T=-40°C, nominal output power P_{5dBm}
D4	High temp. output power change	dP_{HT}			-1.5	dB	V_{Bat}=3V, T=85°C, nominal output power P_{5dBm}
D5	Supply voltage dependent output power change	dP_{V1V9}		-5.5		dB	V_{Bat}=1.9V, T=25°C, nominal output power P_{5dBm}
D6	Supply voltage dependent output power change	dP_{V2V5}		-1.8		dB	V_{Bat}=2.5V, T=25°C, nominal output power P_{5dBm}
D7	Supply voltage dependent output power change	dP_{V3V6}		1.8		dB	V_{Bat}=3.6V, T=25°C nominal output power P_{5dBm}
D8	Data rate				32	kBps	64kChips/s
D9	Carrier to spurious ratio (incl. harmonics) @D1=315/915MHz				-28	dBc	FCC 15.231a/e RBW=100kHz 2nd -10th harmonic
D10	carrier to noise ratio @D1=315/915MHz				-20	dBc	FCC 15.231a/e RBW=100kHz measured at frequency edge: 0,25%*f_c for 315MHz 0,5%*f_c for 915MHz f_c: carrier frequency

D11	SSB Phase Noise @D1=315MHz			 -95 -93 -97 -120 -136	 tbd tbd tbd tbd tbd	 dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz	RBW = 100kHz, +25°C @ 10kHz offset, @ 100kHz offset, @ 250kHz offset, @ 1MHz offset, @ 10MHz offset,
D12	SSB Phase Noise @D1=434MHz			 -93 -90 -91 -113 -132	 tbd tbd tbd tbd tbd	 dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz	RBW = 100kHz, +25°C @ 10kHz offset, @ 100kHz offset, @ 250kHz offset, @ 1MHz offset, @ 10MHz offset,
D13	SSB Phase Noise @D1=868MHz			 -87 -85 -88 -110 -134	 tbd tbd tbd tbd tbd	 dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz	RBW = 100kHz, +25°C @ 10kHz offset, @ 100kHz offset, @ 250kHz offset, @ 1MHz offset, @ 10MHz offset,
D14	SSB Phase Noise @D1=915MHz			 -86 -85 -87 -109 -135	 tbd tbd tbd tbd tbd	 dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz	RBW = 100kHz, +25°C @ 10kHz offset, @ 100kHz offset, @ 250kHz offset, @ 1MHz offset, @ 10MHz offset,
D15	Spurious and Out Band Emission @D1=434/868MHz				-54	dBm	EN300220 (EUR) RBW = 10kHz 47-74MHz, 87.5-118MHz, 174-230MHz, 470-862MHz
D16	Spurious and Out Band Emission @D1=434/868MHz				-36	dBm	EN300220 (EUR) RBW = 10kHz other < 1GHz
D17	Spurious and Out Band Emission @D1=434/868MHz				-30	dBm	EN300220 (EUR) RBW=10kHz other >1GHz

Note: Matching circuit as used in the 50 Ohm-Output Testboard at the specified frequency. Tolerances of the passive elements not taken into account

Table 80 LF Receiver, V_{bat}=2.1-3.6V

#	Parameter	Symbol	Limit Values			Unit	Test Conditions, Remarks
			min.	typ.	max.		
E1	LF Baseband Sensitivity Gain setting 1	S_{LF1}			1.2	mV_{pp}	Input signal level required to achieve a BER better than 0.1% (100% square AM modulation, Datarate 4000 Bit/s) SFR LFRX0: tbd SFR LFCDM: tbd SFR LFCDFLT: tbd
E2	LF Baseband Sensitivity Gain setting 2	S_{LF2}			120	mV_{pp}	Input signal level required to achieve a BER better than 0.1% (100% square AM modulation, Datarate 4000 Bit/s) SFR LFRX0: tbd SFR LFCDM: tbd SFR LFCDFLT: tbd
E3	Datarate	DR_{LF}	2000		4000	Bit/s	
E4	Datarate error	DR_{error}			2	%	
E5	Carrier frequency	f_{CLF}	120	125	130	kHz	
E6	LF Current consumption	I_{LF_AFE}			2	µA	V_{Bat}= 3.0V, T= 25°C, LF Input signal smaller than Carrier Detection level (12 MHz RC HF Osc. and LF Baseband OFF)
		I_{LF_BB}			tbd	µA	V_{Bat}= 3.0V, T= 25°C, LF Input signal higher than Carrier Detection level or enabled by SFR Bit LFCDFLT.[CDFM1-0] = 11b (12 MHz RC HF Osc. and LF Baseband ON)
E7	Input dynamic range	DR_{LF}	70			dB	Sensitivity Gain setting 1 (#E1), AGC enabled
E9	AGC attack time	T_{AGCATT}		200	900	µs	@continous wave signal

#	Parameter	Symbol	Limit Values			Unit	Test Conditions, Remarks
			min.	typ.	max.		
E10	AGC decay slew rate	T_{AGCDEC}		35		V/s	SFR bit LFRX0.7-6[AGCTCD1-0] = 00b
				70		V/s	SFR bit LFRX0.7-6[AGCTCD1-0] = 01b
				140		V/s	SFR bit LFRX0.7-6[AGCTCD1-0] = 10b
E11	Settling time	T_{SET}			4	ms	power on settling time of internal nodes. 6 x 2 kHz RC Oscillator cycles. Min/Max Tolerances from Table 83 apply.
E12	Input capacitance	C_{inLF}	t.b.d	10	t.b.d	pF	
E13	Differential Input resistance	R_{inLF}	t.b.d	420	t.b.d	kOhm	AGC disabled
E14	Preamble length	$T_{preamble}$	3			ms	Manchester coded input signal. Datarate 4kBit/s
F1	LF Carrier Detector threshold Gain setting 1.	DL_{CD1}	0.2	tbd	2.5	mV_{pp}	Minimum Carrier Pulse length 1ms SFR LFRX0: tbd SFR LFCDM: tbd SFR LFCDFLT: tbd
			1.2	3	7.5	mV_{pp}	Minimum Carrier Pulse length 1ms SFR LFRX0: tbd SFR LFCDM: tbd SFR LFCDFLT: tbd
F2	LF Carrier Detector threshold Gain setting 2	DL_{CD2}	20	50	120	mV_{pp}	Minimum Carrier Pulse length 1ms SFR LFRX0: tbd SFR LFCDM: tbd SFR LFCDFLT: tbd
			80	200	480	mV_{pp}	Minimum Carrier Pulse length 1ms SFR LFRX0: tbd SFR LFCDM: tbd SFR LFCDFLT: tbd
F3	Carrier Detector Freeze Hold Time	T_{CDCFH}			50	ms	worst case @ 85°C if Calibration Freeze Bit SFR bit LFCDM.3[LFENFCTC] is set

#	Parameter	Symbol	Limit Values			Unit	Test Conditions, Remarks
			min.	typ.	max.		
F4	Carrier Detector Filter time	T_{CDFLT}	tbd		tbd	µs	SFR bit LFCDFLT.4-5[CDFT1-0] = 00b
			tbd		tbd	µs	SFR bit LFCDFLT.4-5[CDFT1-0] = 01b
			tbd		tbd	µs	SFR bit LFCDFLT.4-5[CDFT1-0] = 10b
			tbd		tbd	µs	SFR bit LFCDFLT.4-5[CDFT1-0] = 11b

Table 81 Crystal Oscillator

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks
			min.	typ.	max.		
G1	Crystal startup time	t_{XTAL}		1.2		ms	IFX Testboard with Crystal NX5032SD EXS00A-02825 C_L=12pF , $f_{Crystal}$ = 18,08MHz
G2	Crystal oscillator startup delay time	$t_{XTALADJ}$	0		1750	µs	Progammable in 250µs steps SFR XTCFG
G3	Crystal frequency	f_{XTAL}	18		20	MHz	
G4	Paracitic capacitance	C_{PCBmax}			4	pF	determined by PCB Layout
G5	Serial resistance of the crystal	R_{Rmax}	-	-	60	Ohm	$f_{crystal}$=19~20MHz
		R_{Rmax}	-	-	80	Ohm	$f_{crystal}$=18~19MHz
G6	Input inductance XTALOUT	L_{OSC}		2.2		uH	
G7	Crystal fine tuning capacitance	C_{tune}		40		pF	Selectable with 156 fF resolution (8 bits)

Table 82 12 MHz RC HF Oscillator

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks
			min.	typ.	max.		
H1	Operating frequency	f_{RCHF}	11.64	12.00	12.36	MHz	V_{Bat}= 3.0V, T= 25°C
H3	Overall drift	df_{RCHF}			+/- 5	%	

Table 83 2kHz RC LP Oscillator

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks
			min.	typ.	max.		
J1	Operating frequency	f_{RCLP}	1.3	2	2.8	kHz	V_{Bat}= 3.0V, T= 25°C
J2	Overall drift	df_{RCLP}			+/- 7	%	

Table 84 Interval Timer

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks
			min.	typ.	max.		
K1	Wake up interval timer range	T_{WU}	0.035		332.8	s	Adjustble with resolution of 8 bit.
K2	Wake up interval timer step	T_{WUST}	0.05		1	s	
K3	Frequency calibration error	f_{ITCE}			+/- 5	%	T_{WUST}=0.5s, systemclock = XTAL

Table 85 Power On Reset

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks
			min.	typ.	max.		
L1	Power On Reset level	V_{POR}	0.2	0.4	1.7	V	Minimum supply voltage level measured at Pin V_{REG} for a valid logic LOW at Power On Reset circuit
L2	Power On release level	V_{THR}	1.7		1.8	V	measured at Pin V_{REG}
L3	Power On reset time	t_{POR}	0.25		10	ms	
L4	Brown Out detect level in RUN state	V_{BRD}	1.7		1.8	V	measured at Pin V_{REG}
L5	Brown Out detect level in POWER DOWN and THERMAL SHUTDOWN	V_{PDBR}	0.7		1.7	V	measured at Pin V_{REG}
L6	Mode selection time	t_{MODE}			2.5	ms	
L7	Minimum detectable Brown Out glitch in RUN state	t_{brd}			1	µs	
L8	Minimum detectable Brown Out glitch in POWER DOWN and THERMAL SHUTDOWN	t_{brdpd}				µs	not used

Table 86 Voltage Regulator

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks
			min.	typ.	max.		
M1	Regulated output voltage in RUN state	V_{REG}	2.3	2.5	2.75	V	V_{Bat} = 2.5V-3.6V, I_{REG}=0.1-10mA 1)
M2	Regulated output voltage at low battery in RUN state	V_{REGLOW}	1.8		2.5	V	V_{Bat} = 1.9V-2.5V, I_{REG}=0.1-8.5mA 1)
M4	Regulated output voltage in POWER DOWN THERMAL SHUT DOWN	V_{regLP}	1.7		2.75	V	I_{REGPD}= max. 40uA 1)

1) The voltage regulator is designed to supply only the internal blocks of the PMA7110 and not designed to drive any external circuitry, thus only the decoupling cap may be connected to the pin V_{REG}.
A 100nF decoupling cap is recommended for proper operation.

Table 87 VMIN detector

#	Parameter	Symbol	Limit Values			Unit	Test Conditions, Remarks
			min.	typ.	max.		
N1	Low battery threshold warning level	TH_{LBat}	2.0	2.1	2.2	V	used by ROM Library functions only

Table 88 6k FLASH Code memory data

#	Parameter	Symbol	Limit Values[1]			Unit	Test Conditions Remarks
			min.	typ.	max.		
O1	Temperature range Erase/program	TR_{FL}	0	0 ~ 35		°C	
O2	Erase/Program Supply voltage range regulated @pad VDDD @pad VBat	V_{FLVDDD} V_{FLBat}	2.3 2.5	2.5		V V	
O3	Endurance Data Retention @25°C	En_{FLCode} t_{RCode}	400k 40	1M		cycles yrs	programming /erase cycles per sector or wordline
O4	Erase time			102		ms	RC-HF-Oscillator @12MHz
O5	Write time/line			2.2		ms	RC-HF-Oscillator @12MHz Line=32byte

1) This is only valid for storage temperature from -40°C to +125°C for max. 1000 hours.

Table 89 2 times 128 byte FLASH User Data memory

#	Parameter	Symbol	Limit Values[1]			Unit	Test Conditions Remarks
			min.	typ.	max.		
O6	Temperature range Erase/program	TR_{FL}		0~35		°C	
O7	Erase/Program Supply voltage range regulated @pad VDDD @pad VBat	V_{FLVDDD} V_{FLBat}	2.3 2.5	2.5		V V	
O8	Endurance Data Retention	En_{FLCode}@25°C t_{RCode}@85°C	100 40	500		kcycles yrs	programming /erase cycles per sector or wordline retention is a function of Endurance

O9	Erase time			102		ms	RC-HF-Oscillator @12MHz
O10	Write time/line			2.2		ms	RC-HF-Oscillator @12MHz Line=32byte

1) This is only valid for storage temperature from -40°C to +125°C for max. 1000 hours.

Table 90 ADC Interface

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks
			min.	typ.	max.		
P1	ADC input voltage range	VR_{ADC}	GND		VADC		
P2	ADC resolution	R_{ADC}	10			bit	
P3	Offset correction range	R_{OFFC}			6	bit	
P4	ADC clock frequency	f_{ADC}	0.5	1	20	MHz	
P5	Differential non-linearity	DNL	-0.5		0.5	lsb	
P6	Integral non-linearity	INL	-1		1	lsb	
P7	Noise	N_{ADC}			15	μV_{rms}	
P8	Non-ratiometric offset voltage with supply voltage[1]	OV_{NR}	-1.5		1.5	lsb	Measured at any constant temperature between -20 and 70°C

1.) Extrapolate offset voltage vs. supply voltage to find the intersection with the y-axis (supply voltage =0). This is the non-ratiometric part of the offset voltage.

Table 91 TMAX Detector

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks
			min.	typ.	max.		
T1	THERMAL SHUTDOWNrelease temperature	T_{REL}	tbd	tbd	tbd	°C	used by ROM Library functions only

Table 92 Digital I/O Pin

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks
			min.	typ.	max.		
U1	Input low voltage	V_{IL}	-0.2		0.4	V	
U2	Input high voltage	V_{IH}	V_{Bat} -0.4		V_{Bat} + 0.2	V	
U3	Output low voltage	V_{OL}			0.5	V	I_{OL}= 1.6mA

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks
			min.	typ.	max.		
U4	Output high voltage	V_{OH}	V_{Bat} -0.5			V	I_{OH}= -1.6mA
U6	Output transition time	t_{THL}, t_{TLH}			30	ns	20pF load, 10% ... 90%
U7	Input capacitance	C_{pad}			2	pF	
U8	Internal pullup or pulldown resistor	R_{uPPx}, $R_{downPPx}$ 1)	35	50	65	kOhm	
U9	Internal pullup or pulldown resistor	R_{upPPy}, $R_{downPPy}$ 2)	175	250	325	kOhm	

1) PPx are: PP0, PP1, PP4, PP5, PP6, PP7
2) PPy are: PP2, PP3, PP8, PP9

3.2 Reference SFR Registers

This section contains detailed description about SFRs which are shown in **Figure 7 "SFR Special Function Register Address Overview" on Page 53** but not described in Chapter **"Functional Description**.

Table 93 SFR Address DB_H: ADCC0- ADC Configuration Register 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	TVC2	TVC1	TVC0	n.u.	STC2	STC1	STC0
0/0	rw 0/0	rw 0/0	rw 0/0	0/0	r/w 0/0	rw 0/0	rw 0/0
TCV2		Internal Clock Divider Bit 2					
TCV1		Internal Clock Divider Bit 1					
TCV0		Internal Clock Divider Bit *0*					
STC2		*Sample Time Adjustment Bit 2*					
STC1		*Sample Time Adjustment Bit 1*					
STC0		*Sample Time Adjustment Bit 0*					

Table 94 SFR Address DC_H: ADCC1- ADC Configuration Register 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SeDC	CSI	GAIN1	GAIN0	FCnSC	SUBC2	SUBC1	SUBC0
rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	r/w 0/0	rw 0/0	rw 0/0
SeDC		Single ended/differential conversion					
CSI		Comparator signal inversion					
GAIN1		*Gain setting of the 10-bit c-network Bit 1*					
GAIN0		*Gain setting of the 10-bit c-network Bit 0*					
FCnSC		*Full conversion or subconversion*					
SUBC2		*Subconversion Bit 2*					
SUBC1		*Subconversion Bit 1*					
SUBC0		*Subconversion Bit 0*					

Table 95 SFR Address $D4_H$: ADCCL- ADC Configuration Register (low byte)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCD.7	ADCD.6	ADCD.5	ADCD.4	ADCD.3	ADCD.2	ADCD.1	ADCD.0
r 0/0	r 0/0	r 0/0	r 0/0	r 0/0	r 0/0	r 0/0	r 0/0
ADCD.7 - ADCD.0		Bit 7 - Bit 0					

Table 96 SFR Address $D5_H$: ADCCH- ADC Configuration Register (high byte)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	n.u.	n.u.	n.u.	n.u.	n.u.	ADCD.9	ADCD.8
0/0	0/0	0/0	0/0	0/0	0/0	r 0/0	r 0/0
ADCD.9		Bit 9					
ADCD.8		Bit 8					

Table 97 SFR Address $D2_H$: ADCM- ADC Mode Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCStart	RV2	RV1	RV0	WBCStart	CS2	CS1	CS0
rcw 0/0	rw 1/1	rw 1/1	rw 1/1	rcw 0/0	rw 1/1	rw 1/1	rw 1/1
ADCStart		ADC conversion start					
RV2		Reference voltage select bit 2					
RV1		Reference voltage select bit 1					
RV0		Reference voltage select bit 0					
WBCStart		WBC start					
CS2		Analog channel select bit 2					
CS1		Analog channel select bit 1					
CS0		Analog channel select bit 0					

Table 98 SFR Address DA_H: ADCOFF- ADC Input Offset c-network configuration

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OFF5	OFF5	OFF5	RV0	WBCStart	CS2	CS1	CS0
r 0/0	r 0/0	rw 0/0	rw 1/1	rcw 0/0	rw 1/1	rw 1/1	rw 1/1
OFF5		Bit 5 (extended)					
OFF5		Bit 5 (extended)					
OFF5		Input of Offset c-network Bit 5					
OFF4		Input of Offset c-network Bit 4					
OFF3		Input of Offset c-network Bit 3					
OFF2		Input of Offset c-network Bit 2					
OFF1		Input of Offset c-network Bit 1					
OFF0		Input of Offset c-network Bit 0					

Table 99 SFR Address $D3_H$: ADCS- ADC Startus Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	SARSATL	SARSATH	CL000	CG3FF	n.u.	SAMPLE	BUSY
0/0	r 0/0	r 0/0	r 0/0	r 0/0	0/0	r 0/0	r 0/0
SARSATL		negative saturation of SAR					
SARSATH		positive saturation of SAR					
CL000		0x000 saturation of c-net control word					
CG3FF		0x3FF saturation of c-net control word					
SAMPLE		Sample/Hold					
BUSY		Busy					

Table 100 SFR Address DD_H: ADWBC- AD WBC Wire Bond Check

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	n.u.	n.u.	n.u.	STAT3	STAT2	DREF	WBEF
0/0	0/0	0/0	0/0	r 0/0	r 0/0	r 0/0	r 0/0
STAT3		reserved					
STAT2		reserved					
DREF		Diagnostic Resistor Error Flag					
BUSY		Wire Bond Error Flagl					

Table 101 SFR Address $E9_H$: FCSP- Flash Control Register - Sector Protection Control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ECCErr	ECCLeft	ECCOff	WLO	WLE	SingleStep	CodeLCK	ConfLCK
rc 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rmw u/0	rmw u/0
ECCErr		ECC Error Detected Bit (0=no error, 1=error detected)					
ECCLeft		ECC vector selection for read/write (0=select lower 8-bit, 1=selects LEFT 4 bits)					
ECCOff		Bypass ECC					
WLO		Selects all odd wordlines					
WLE		Selects all even wordlines					
SingleStep		Flash Single-Step Mode					
CodeLCK		Code-sector Lock Bit (0=programmable & erasable; 1=read only)					
ConLCK		Config-sector Lock Bit (0=programmable & erasable; 1=read only)					

Table 102 SFR Address EA_H: FCS- Flash Control Register - Status Model

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IPROG	**IERASE**	**IREAD**	**IPDWN**	**PROG**	**ERASE**	**READ**	**PDWN**
r 0/0	**r 0/0**	**r 0/0**	**r 1/1**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 1/1**
IPROG		Indicates that the Flash is in Program Mode					
IERASE		Indicates that the Flash is in Erase Mode					
IREAD		Indicates that the Flash is in Read Mode					
IPDWN		Indicates that the Flash is in PowerDown Mode					
PROG		Program Enable Bit: 0->1: Starts transition into Program Mode					
ERASE		Erase Enable Bit: 0->1: Starts transition into Erase Mode					
READ		Read Enable Bit: 0->1: Starts transition into Read Mode					
PDWN		CPDWN Enable Bit: 0->1: Starts transition into PowerDown Mode					

Table 103 SFR Address $E1_H$: FCPP0- Flash Charge Pumps Power Control Register 0l

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VProgN1	**VProgN0**	**VProgNen**	**VPP3**	**VPP2**	**VPP1**	**VPP0**	**VPPen**
rw 0/0	**rw 0/0**	**rw 0/0**	**rw0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**
VProgN1		also used for SSDI<7> and DisConCG					
VProgN0		also used for SSDI<6>					
VProgNen		also used for SSDI<5>					
VPP3		also used for SSDI<4> and DMux <3> and LongEval					
VPP2		also used for SSDI<3> and DMux <2>					
VPP1		also used for SSDI<2> and DMux <1>					
VPP0		also used for SSDI<1> and DMux <0>					
VPPen		also used for SSDI<0>					

Table 104 SFR Address $E2_H$: FCPP1- Flash Charge Pumps Power Control Register 1l

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VReadHi	**IBiasHi**	**VProgPBit4**	**VProgPBit3**	**VProgPBit2**	**VProgPBit1**	**VProgPBit0**	**VProgPEn**
rw 0/0	**rw 0/0**	**rw 0/0**	**rw0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**
VReadHi		increases CG-voltage from 1.8 V to 2.5 V during read					
IBiasHi		increases bias currents by 66% (from 5 uA to 8.33 uA)					
VProgPBit4							
VProgPBit3							
VProgPBit2		also used for SSDI<11>					

VProgPBit1		also used for SSDI<10>
VProgPBit0		also used for SSDI<9>
VProgPEn		also used for SSDI<8>

Table 105 SFR Address $E3_H$: FCSERM- Flash Sector Erase and Read Margin Select Registerl

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UseVEXT	**REFCURMAG1**	**REFCURMAG0**	**ERSELREF**	**ERSELCONF**	**ERSELS2**	**ERSELS1**	**ERSELS0**
rw 0/0	**rw 0/0**	**rw 1/1**	**rw0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**
UseVEXT		uses voltage at VEXT to increase VProgP current					
REFCURMAG1		Reference current magnitude, bit 1					
REFCURMAG0		Reference current magnitude, bit 0					
ERSELREF		Selects Reference cells for Erase					
ERSELCONF		Selects Config-sector for Erase					
ERSELS2		Selects ID-sector for Erase					
ERSELS1		Selects Data-sector for Erase					
ERSELS0		Selects Code-sector for Erase					

Table 106 SFR Address 84_H: MMR0 - Memory Mapped Register 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
rw 0/0	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**
Bit 7 - Bit 0		general / programming & debugging purposes					

Table 107 SFR Address 85_H: MMR1 - Memory Mapped Register 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
rw 0/0	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**
Bit 7 - Bit 0		general / programming & debugging purposes					

Table 108 SFR Address 86_H: MMR2 - Memory Mapped Register 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0
Bit 7 - Bit 0		general / programming & debugging purposes					

Table 109 SFR Address 81_H: SP - Stack Pointer

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0
0/0	0/0	0/0	0/0	0/0	rw 0/0	rw 0/0	rw 1/1
SP.7 -SP. 0		Stackpointer Bit 7 - Bit 0					

Table 110 SFR Address $8C_H$: TH0 - Timer 0 Register High Byte

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0
Bit 7 - Bit 0		Bit 7 - Bit 0					

Table 111 SFR Address $8D_H$: TH1 - Timer 1Register High Byte

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0
Bit 7 - Bit 0		Bit 7 - Bit 0					

Table 112 SFR Address CD_H: TH2 - Timer 2 Register High Byte

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
rw 0/0	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**
Bit 7 - Bit 0		Bit 7 - Bit 0					

Table 113 SFR Address CB_H: TH3 - Timer 3Register High Byte

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
rw 0/0	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**
Bit 7 - Bit 0		Bit 7 - Bit 0					

Table 114 SFR Address $8A_H$: TL0 - Timer 0 Register Low Byte

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
rw 0/0	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**
Bit 7 - Bit 0		Bit 7 - Bit 0					

Table 115 SFR Address $8B_H$: TL1 - Timer 1 Register Low Byte

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
rw 0/0	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**
Bit 7 - Bit 0		Bit 7 - Bit 0					

Table 116 SFR Address CC_H: TL2 - Timer 2 Register Low Byte

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
rw 0/0	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**
Bit 7 - Bit 0		Bit 7 - Bit 0					

Table 117 SFR Address CA_H: TL3 - Timer 3 Register Low Byte

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
rw 0/0	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**
Bit 7 - Bit 0		Bit 7 - Bit 0					

Table 118 SFR Address DE_H: RFVCO -RF Frequency Synthesizer VCO Config

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCOCC3	VCOCC2	VCOCC1	VCOCC0	VCOF3	VCOF2	VCOF1	VCOF0
rw u/1	rw u/0	rw u/0	rw u/1	rw u/0	rw u/0	rw u/0	rw u/0
Bit 7-4	VCOCC3-0	VCO Core Current Select VCOCC3 ... 1600µA (MSB) VCOCC2 ... 800µA VCOCC1 ... 400µA VCOCC0 ... 200µA (LSB)					
Bit 3-0	VCOF3-0	VCO Frequency range adjustment VCO Tuning Curve Select					

Table 119 SFR Address $D4_H$: ADCDL - ADC Result Register (low Byte)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCD.7	ADCD.6	ADCD.5	ADCD.4	ADCD.3	ADCD.2	ADCD.1	ADCD.0
r 0/0	r 0/0	r 0/0	r 0/0	r 0/0	r 0/0	r 0/0	r 0/0

Table 120 SFR Address $D5_H$: ADCDH - ADC Result Register (high Byte)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	n.u.	n.u.	n.u.	n.u.	n.u.	ADCD.9	ADCD.8
0/0	0/0	0/0	0/0	0/0	0/0	r 0/0	r 0/0
Bit 1	ADCD.9	Bit 9					
Bit 0	ADCD.8	Bit 8					

Table 121 SFR Address AA_H: CRCD - CRC Data Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRCD.7	CRCD.6	CRCD.5	CRCD.4	CRCD.3	CRCD.2	CRCD.1	CRCD.0
rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0

Table 122 SFR Address AC_H: CRC0 - CRC Shift Register(low byte)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRC.7	CRC.6	CRC.5	CRC.4	CRC.3	CRC.2	CRC.1	CRC.0
rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0

Table 123 SFR Address AD_H: CRC1 - CRC Shift Register(high byte)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRC.15	CRC.14	CRC.13	CRC.12	CRC.11	CRC.10	CRC.9	CRC.8
rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0

Table 124 SFR Address 94_H: DBCL0- CPU Debug Compare Register 0 (Low)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DBCL.7	DBCL.6	DBCL.5	DBCL.4	DBCL.3	DBCL.2	DBCL.1	DBCL.0
rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0

Table 125 SFR Address 95_H: DBCH0- CPU Debug Compare Register 0 (High)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DBCH.7	DBCH.6	DBCH.5	DBCH.4	DBCH.3	DBCH.2	DBCH.1	DBCH.0
rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0

Table 126 SFR Address 96_H: DBTL0- CPU Debug Target Register 0 (Low)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DBTL.7	DBTL.6	DBTL.5	DBTL.4	DBTL.3	DBTL.2	DBTL.1	DBTL.0
rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0

Table 127 SFR Address 97_H: DBTH0- CPU Debug Target Register 0 (High)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DBTH.7	DBTH.6	DBTH.5	DBTH.4	DBTH.3	DBTH.2	DBTH.1	DBTH.0
rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0

Table 128 SFR Address $9C_H$: DBCL1- CPU Debug Compare Register 1 (Low)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DBCL.7	DBCL.6	DBCL.5	DBCL.4	DBCL.3	DBCL.2	DBCL.1	DBCL.0
rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0

Table 129 SFR Address $9D_H$: DBCH1- CPU Debug Compare Register 1 (High)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

DBCH.7	DBCH.6	DBCH.5	DBCH.4	DBCH.3	DBCH.2	DBCH.1	DBCH.0
rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0

Table 130 SFR Address $9E_H$: DBTL1- CPU Debug Target Register 1 (low)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DBTL.7	DBTL.6	DBTL.5	DBTL.4	DBTL.3	DBTL.2	DBTL.1	DBTL.0
rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0

Table 131 SFR Address $9F_H$: DBTH1- CPU Debug Target Register 1 (High)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DBTH.7	DBTH.6	DBTH.5	DBTH.4	DBTH.3	DBTH.2	DBTH.1	DBTH.0
rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0	rw 0/0

Table 132 SFR Address $E4_H$: FCTKAS- Flash Tkill and Analog Output Select Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read0V9	CLKSEL	ANSEL3	ANSEL2	ANSEL1	ANSEL0	TKILL1	TKILL0
rw 0/0	rw 0/0	rw 1/1	rw 1/1	rw 1/1	rw 1/1	rw 1/1	rw 1/1
Bit 7	Read0V9	sets the read voltage to 0.9 V					
Bit 6	CLKSEL	Read clock select (0:g_Clk, 1:MemClk)					
Bit 5	ANSEL3	Analog Output Select, bit 3					
Bit 4	ANSEL2	Analog Output Select, bit 2					
Bit 3	ANSEL1	Analog Output Select, bit 1					
Bit 2	ANSEL0	Analog Output Select, bit 0					
Bit 1	TKILL1	Tkill-Time, bit 1					
Bit 0	TKILL0	Tkill-Time, bit 0					

Table 133 SFR Address $E5_H$: FCSS- Flash Control Register for Single-Step Mode

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SelRefCell1	**SelRefCell0**	**VPPCh**	**VProgPCh**	**VProgNCh**	**SSCSB**	**SSALE**	**SSWRB**
rw 1/1	**rw 1/1**	**r 0/0**	**r 0/0**	**r 0/0**	**rw 0/0**	**rw 0/0**	**rw 0/0**
Bit 7	SelRefCell1	Selects RefCells#3 and #2					
Bit 6	SelRefCell0	Selects RefCells#1 and #0					
Bit 5	VPPCh	Charge pump charging indicator for VPP					
Bit 4	VProgPCh	Charge pump charging indicator for VProgP					
Bit 3	VProgNCh	Charge pump charging indicator for VProgN					
Bit 2	SSCSB	Single-Step-Chip-Select-Bar					
Bit 1	SSALE	Single-Step-Address-Latch-Enable					
Bit 0	SSWRB	Single-Step-Write-Read-Bar					

Table 134 SFR Address EF_H: LBD- Low Battery Detector Control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	**n.u.**	**n.u.**	**n.u.**	**LBD2V1**	**LBDF**	**LBDEn**	**LBDMen**
0/0	**0/0**	**0/0**	**0/0**	**rw 1/1**	**rc 0/0**	**rw 1/1**	**rw 1/1**
Bit 3	LBD2V1	Low Battery Voltage Switch (1…2.1V VEXT, 0…2.4V VDDC)					
Bit 2	LBDF	Low Battery Detector Flag (1..Supply Voltage below threshold)					
Bit 1	LBDEn	Low Battery Detector enable					
Bit 0	LBDMen	Low Battery Detector measurement enable					

Table 135 SFR Address $D6_H$: OSCCONF- RC HF Oscillator Configuration Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Rneg2	**Rneg1**	**Rneg0**	**RCOFT4**	**RCOFT3**	**RCOFT2**	**RCOFT1**	**RCOFT0**
rw u/0	**rw u/0**	**rw u/0**	**rw u/0**	**rw u/0**	**rw u/0**	**rw u/0**	**rw u/0**
Bit 7	Rneg2	Rneg setting of XtalOsc (bit 2)					
Bit 6	Rneg1	Rneg setting of XtalOsc (bit 1)					
Bit 5	Rneg0	Rneg setting of XtalOsc (bit 0)					
Bit 4	RCOFT4	RC Oscillator Frequency Tuning (bit 4)					
Bit 3	RCOFT3	RC Oscillator Frequency Tuning (bit 3)					
Bit 2	RCOFT2	RC Oscillator Frequency Tuning (bit 2)					
Bit 1	RCOFT1	RC Oscillator Frequency Tuning (bit 1)					
Bit 0	RCOFT0	RC Oscillator Frequency Tuning (bit 0)					

Table 136 SFR Address $D7_H$: RFFSPLL- RF- Frequency Synthesizer PLL Configuration

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FPDPOL	**DDCC**	**ABLP1**	**ABLP0**	**DCC1**	**DCC0**	**CPCU1**	**CPCU0**
w 1/1	**0/0**	**w 0/0**	**w 0/0**	**0/0**	**0/0**	**w 1/1**	**w 0/0**
Bit 7	FPDPOL	Frequency-Phase-Detector polarity - must be '1'					
Bit 6	DDCC	Disable RF divider duty cycle control					
Bit 5	ABLP1	Antibacklash pulse width select (bit 1)					
Bit 4	ABLP0	Antibacklash pulse width select (bit 0)					
Bit 3	DCC1	RF divider duty cycle control (bit 1)					
Bit 2	DCC0	RF divider duty cycle control (bit 0)					
Bit 1	CPCU1	Charge pump current select (bit 1)					
Bit 0	CPCU0	Charge pump current select (bit 0)					

Table 137 SFR Address DE_H: RFVCO- RF- Frequency Synthesizer VCO Configuration

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCOCC3	VCOCC2	VCOCC1	VCOCC0	VCOF3	VCOF2	VCOF1	VCOF0
rw u/1	rw u/0	rw u/0	rw u/1	rw u/0	rw u/0	rw u/0	rw u/0
Bit 7 - Bit 0	VCOCC3 - VCOCC0	VCO Core Current Select (bit 3 - bit 0)					
Bit 6	VCOCC2	VCO Core Current Select (bit 2)					
Bit 5	VCOCC1	VCO Core Current Select (bit 1)					
Bit 4	VCOCC0	VCO Core Current Select (bit 0)					
Bit 3	VCOF3	VCO Tuning Curve Select (bit 3 - bit 0)					
Bit 2	VCOF2	VCO Tuning Curve Select (bit 2)					
Bit 1	VCOF1	VCO Tuning Curve Select (bit 1)					
Bit 0	VCOF0	VCO Tuning Curve Select (bit 0)					

Table 138 SFR Address DF_H: RFFSLD- RF- Frequency Synthesizer Lock Detector Configuration

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	n.u.	NOLOCK	ENLOCKDET	LL3	LL2	LL1	LL0
0/0	0/0	rc 0/0	w u/0	w u/1	w u/0	w u/0	w u/0
Bit 5	NOLOCK	PLL Lock Indicator					
Bit 4	ENLOCKDET	Enable Lock Detector					
Bit 3 - Bit 0	LL3 -LL0	Lock Limit Select (bit 3 - bit 0)					

Table 139 SFR Address BD_H: TMAX - TMAX Detector Control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD_TMAX	n.u.	TMTR5	TMTR4	TMTR3	TMTR2	TMTR1	TMTR0
rw u/1	0/0	rw u/0	rw u/0	rw u/0	rw u/0	rw u/0	rw u/0
Bit 7	PD_TMAX	Power down TMAX Detector in RUN state if set. Please note, TMAX Detector is always active in THERMAL SHUTDOWN state					
Bit 5 - Bit 0	TMTR5 - TMTR0	TMAX Detector Shut Down Trigger/Release Tempr.Trimming (LSB~1°C nonlinear charcteristic) 000000b = min. temp. threshold (~90°C) 111111b = max. temp. threshold (~135°C)					

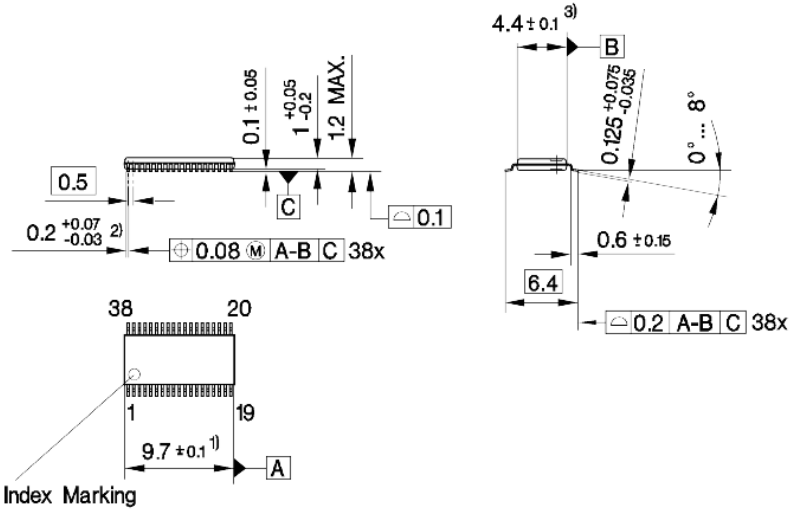
3.3 Reference Documents

This section contains documents used for cross- reference throughout this document.

Table 140 Reference Documents

Reference Number	Document description
[1]	PMA5110 ROM Library function Guide

4 Package Outlines



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.08 max. per side
3) Does not include plastic or metal protrusion of 0.25 max. per side

Figure 41 Package Outline P-TSSOP-38

Table 141 Order Information

Type	Ordering Code	Package
PMA7110	tbd	TSSOP38

You can find all of our packages, sorts of packing and others on our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

www.infineon.com

Published by Infineon Technologies AG