

PMBT3906VS

40 V, 200 mA PNP/PNP switching transistor

Rev. 01 — 20 August 2009

Product data sheet

1. Product profile

1.1 General description

PNP/PNP double switching transistor in a SOT666 ultra small and flat lead Surface-Mounted Device (SMD) plastic package.

Table 1. Product overview

Type number	Package		NPN/NPN complement	NPN/PNP complement
	NXP	JEITA		
PMBT3906VS	SOT666	-	PMBT3904VS	PMBT3946VPN

1.2 Features

- Double general-purpose switching transistor
- Board-space reduction
- AEC-Q101 qualified
- Ultra small and flat lead SMD plastic package

1.3 Applications

- General-purpose switching and amplification

1.4 Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
V_{CE0}	collector-emitter voltage	open base	-	-	-40	V
I_C	collector current		-	-	-200	mA
h_{FE}	DC current gain	$V_{CE} = -1\text{ V};$ $I_C = -10\text{ mA}$	100	180	300	

2. Pinning information

Table 3. Pinning			
Pin	Description	Simplified outline	Graphic symbol
1	emitter TR1		
2	base TR1		
3	collector TR2		
4	emitter TR2		
5	base TR2		
6	collector TR1		
		sym018	

3. Ordering information

Table 4. Ordering information			
Type number	Package		
	Name	Description	Version
PMBT3906VS	-	plastic surface-mounted package; 6 leads	SOT666

4. Marking

Table 5. Marking codes	
Type number	Marking code
PMBT3906VS	ZD

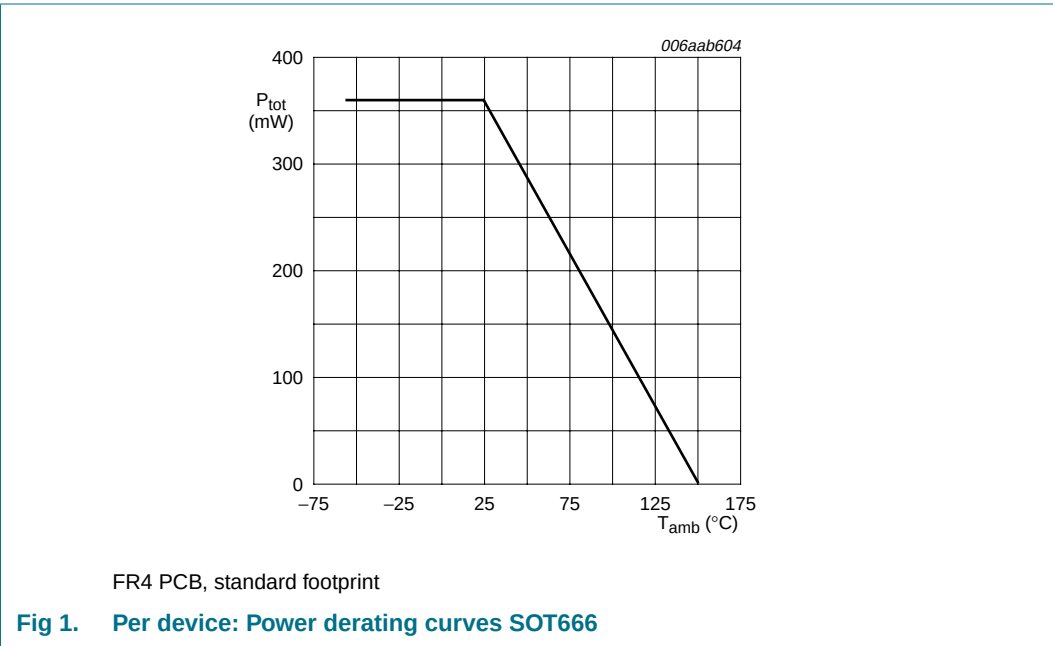
5. Limiting values

Table 6. Limiting values					
In accordance with the Absolute Maximum Rating System (IEC 60134).					
Symbol	Parameter	Conditions	Min	Max	Unit
Per transistor					
V _{CBO}	collector-base voltage	open emitter	-	-40	V
V _{CEO}	collector-emitter voltage	open base	-	-40	V
V _{EBO}	emitter-base voltage	open collector	-	-6	V
I _C	collector current		-	-200	mA
I _{CM}	peak collector current	single pulse; t _p ≤ 1 ms	-	-200	mA
I _{BM}	peak base current	single pulse; t _p ≤ 1 ms	-	-100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1] [2]	240	mW
Per device					
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1] [2]	360	mW

Table 6. Limiting values ...continued
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
T _j	junction temperature		-	150	°C
T _{amb}	ambient temperature		-55	+150	°C
T _{stg}	storage temperature		-65	+150	°C

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [2] Reflow soldering is the only recommended soldering method.

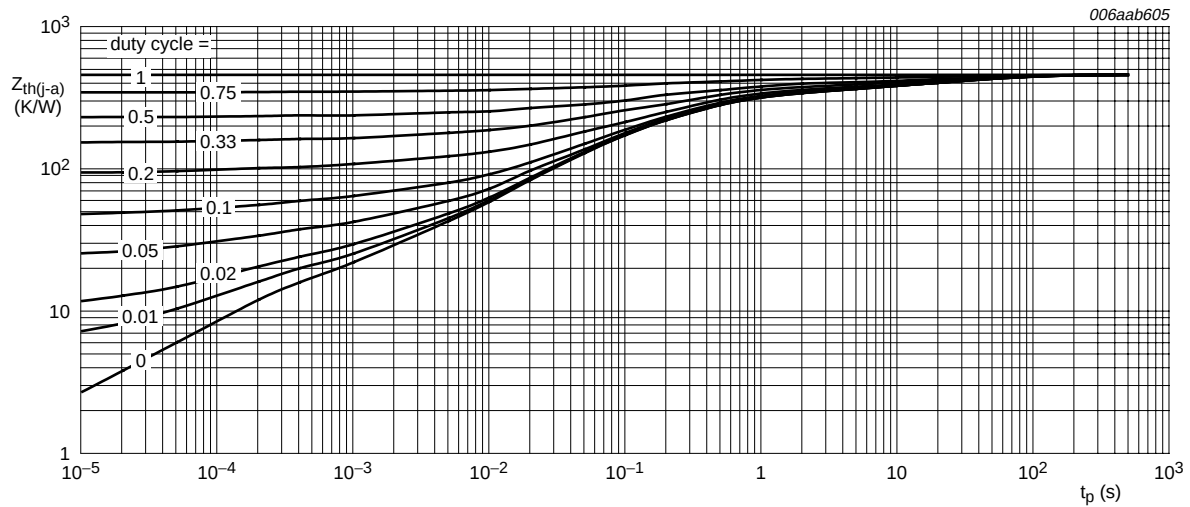


6. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1][2] -	-	521	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point		-	-	100	K/W
Per device						
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1][2] -	-	347	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Reflow soldering is the only recommended soldering method.



FR4 PCB, standard footprint

Fig 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

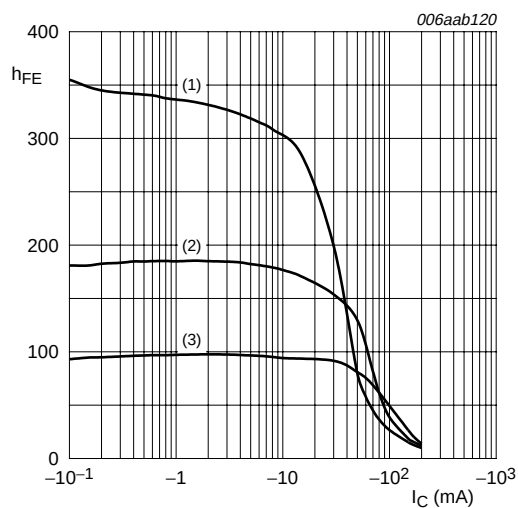
Table 8. Characteristics

$T_{amb} = 25^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
I_{CBO}	collector-base cut-off current	$V_{CB} = -30\text{ V}; I_E = 0\text{ A}$	-	-	-50	nA
I_{EBO}	emitter-base cut-off current	$V_{EB} = -6\text{ V}; I_C = 0\text{ A}$	-	-	-50	nA
h_{FE}	DC current gain	$V_{CE} = -1\text{ V}$				
		$I_C = -0.1\text{ mA}$	60	180	-	
		$I_C = -1\text{ mA}$	80	180	-	
		$I_C = -10\text{ mA}$	100	180	300	
		$I_C = -50\text{ mA}$	60	130	-	
		$I_C = -100\text{ mA}$	30	50	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -10\text{ mA}; I_B = -1\text{ mA}$	-	-100	-250	mV
		$I_C = -50\text{ mA}; I_B = -5\text{ mA}$	-	-165	-400	mV
V_{BEsat}	base-emitter saturation voltage	$I_C = -10\text{ mA}; I_B = -1\text{ mA}$	-	-750	-850	mV
		$I_C = -50\text{ mA}; I_B = -5\text{ mA}$	-	-850	-950	mV
t_d	delay time	$V_{CC} = -3\text{ V};$	-	-	35	ns
t_r	rise time	$I_C = -10\text{ mA};$	-	-	35	ns
t_{on}	turn-on time	$I_{Bon} = -1\text{ mA};$	-	-	70	ns
		$I_{Boff} = 1\text{ mA}$				
t_s	storage time		-	-	225	ns
t_f	fall time		-	-	75	ns
t_{off}	turn-off time		-	-	300	ns

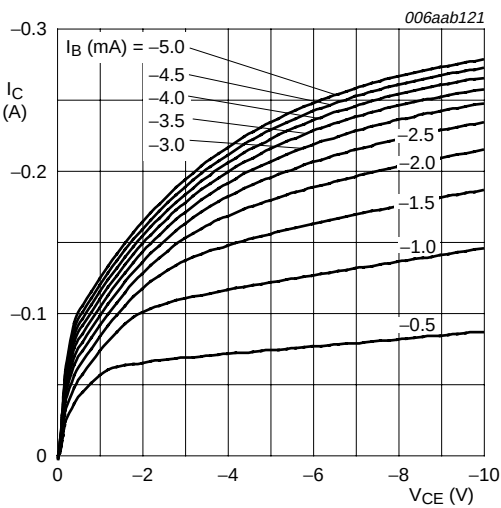
Table 8. Characteristics ...continued
T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C _c	collector capacitance	V _{CB} = -5 V; I _E = i _e = 0 A; f = 1 MHz	-	-	4.5	pF
C _e	emitter capacitance	V _{EB} = -500 mV; I _C = i _c = 0 A; f = 1 MHz	-	-	10	pF
f _T	transition frequency	V _{CE} = -20 V; I _C = -10 mA; f = 100 MHz	250	-	-	MHz
NF	noise figure	V _{CE} = -5 V; I _C = -100 µA; R _S = 1 kΩ; f = 10 Hz to 15.7 kHz	-	-	4	dB



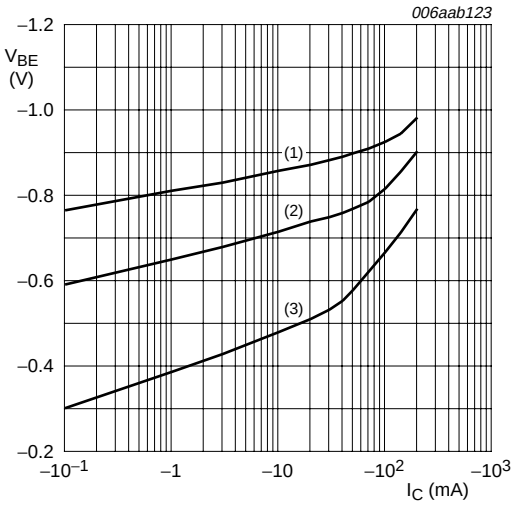
V_{CE} = -1 V
(1) T_{amb} = 150 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -55 °C

Fig 3. Per transistor:
DC current gain as a function of collector current; typical values



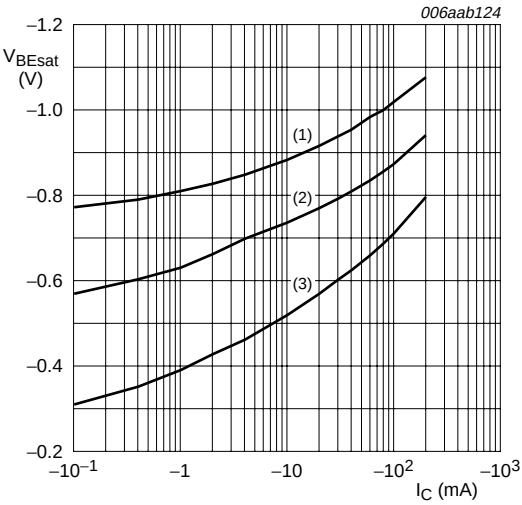
T_{amb} = 25 °C

Fig 4. Per transistor:
Collector current as a function of collector-emitter voltage; typical values



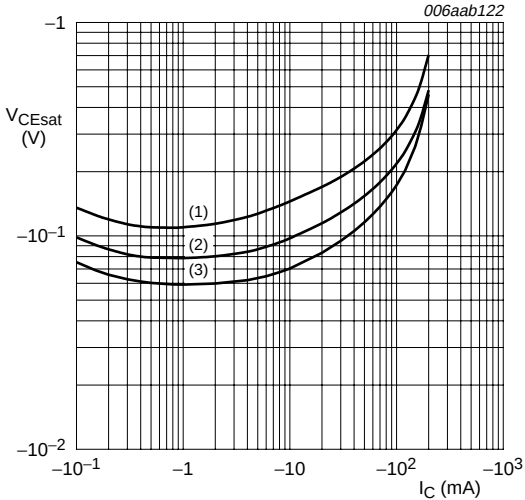
$V_{CE} = -1\text{ V}$
(1) $T_{amb} = -55\text{ }^{\circ}\text{C}$
(2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
(3) $T_{amb} = 150\text{ }^{\circ}\text{C}$

Fig 5. Per transistor:
Base-emitter voltage as a function of collector current; typical values



$I_C/I_B = 10$
(1) $T_{amb} = -55\text{ }^{\circ}\text{C}$
(2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
(3) $T_{amb} = 150\text{ }^{\circ}\text{C}$

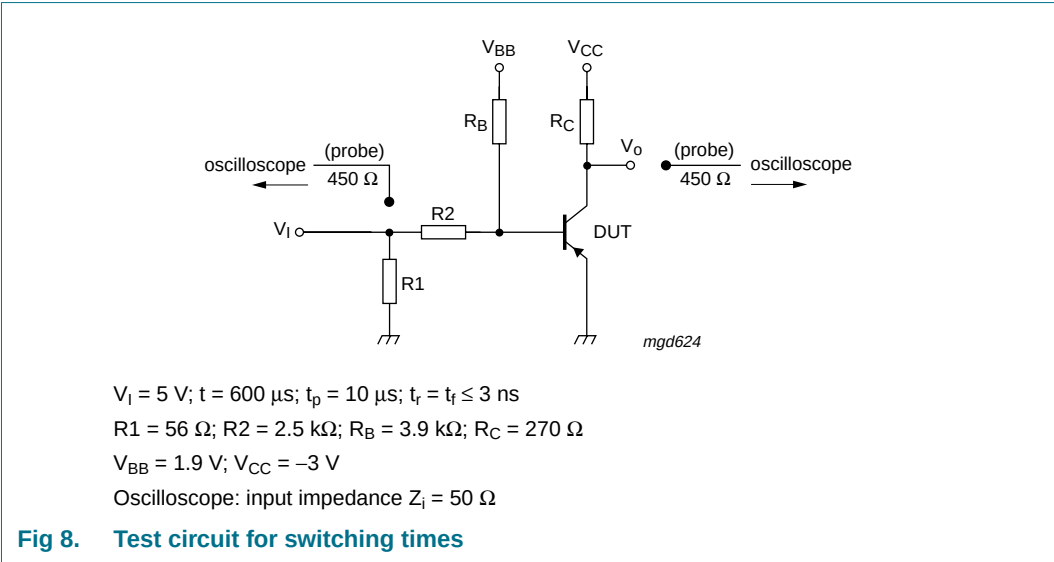
Fig 6. Per transistor:
Base-emitter saturation voltage as a function of collector current; typical values



$I_C/I_B = 10$
(1) $T_{amb} = 150\text{ }^{\circ}\text{C}$
(2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
(3) $T_{amb} = -55\text{ }^{\circ}\text{C}$

Fig 7. Per transistor: Collector-emitter saturation voltage as a function of collector current; typical values

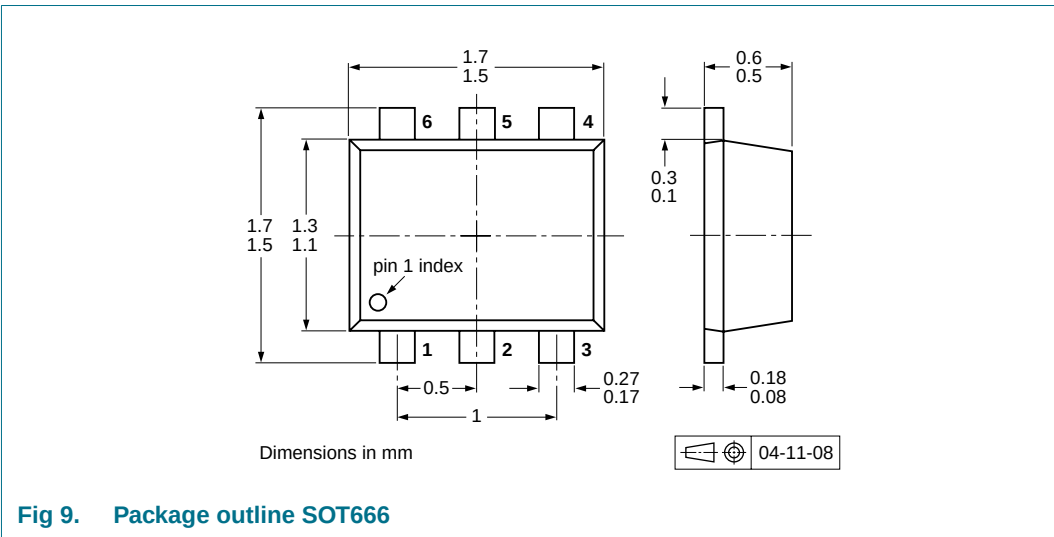
8. Test information



8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

9. Package outline



10. Packing information

Table 9. Packing methods
The indicated -xxx are the last three digits of the 12NC ordering code.[\[1\]](#)

Type number	Package	Description	Packing quantity	
			4000	8000
PMBT3906VS	SOT666	2 mm pitch, 8 mm tape and reel	-	-315
		4 mm pitch, 8 mm tape and reel	-115	-

[1] For further information and the availability of packing methods, see [Section 14](#).

11. Soldering

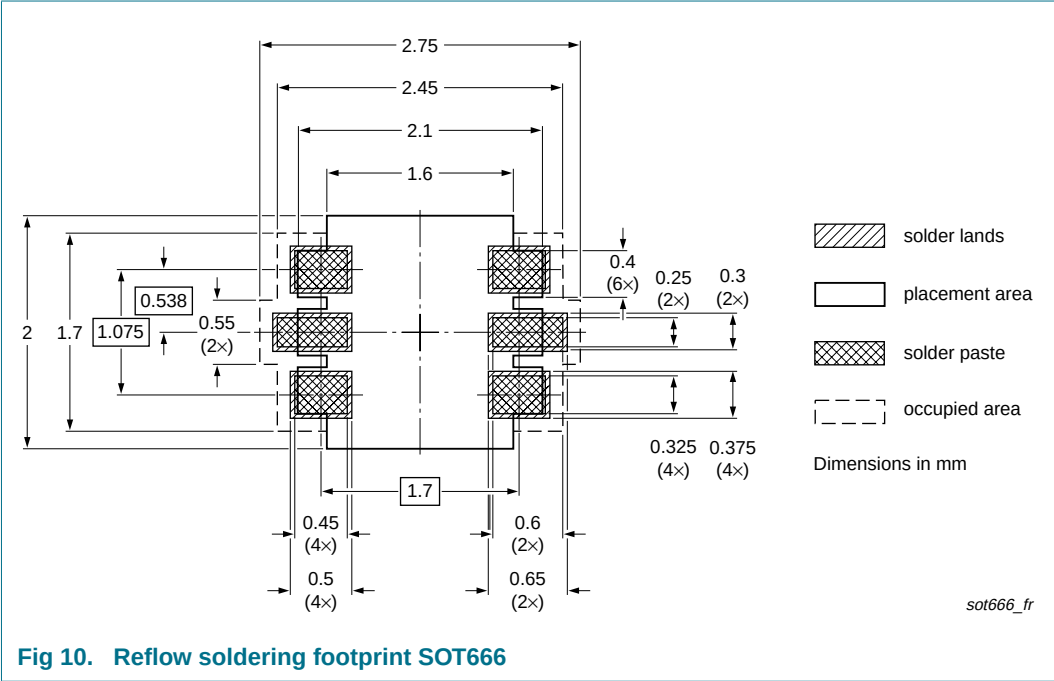


Fig 10. Reflow soldering footprint SOT666

12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMBT3906VS_1	20090820	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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