



# PMCM950ENE

60 V, N-channel Trench MOSFET

13 May 2019

Product data sheet

## 1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a 9 bumps Wafer Level Chip-Size Package (WLCSP) using Trench MOSFET technology.

## 2. Features and benefits

- Low threshold voltage
- Ultra small package:  $1.48 \times 1.48 \times 0.35$  mm
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection  $> 2$  kV HBM

## 3. Applications

- High-speed line driver
- Low-side load switch
- Switching circuits

## 4. Quick reference data

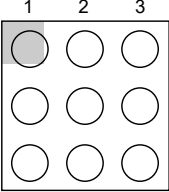
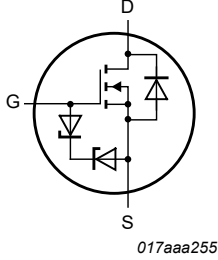
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ }^{\circ}\text{C}$		-	-	60	V
$V_{GS}$	gate-source voltage			-20	-	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}; t \leq 5\text{ s}$	[1]	-	-	6.1	A
<b>Static characteristics</b>							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 3\text{ A}; T_j = 25\text{ }^{\circ}\text{C}$		-	28	41	m $\Omega$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain  $6\text{ cm}^2$ .

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
A1	G	gate	 <p>Transparent top view <b>WLCSP9 (WLCSP9_3x3)</b></p>	
A2	S	source		
A3	S	source		
B1	S	source		
B2	S	source		
B3	S	source		
C1	D	drain		
C2	D	drain		
C3	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMCM950ENE	WLCSP9	WLCSP9: wafer level chip-size package; 9 bumps (3 x 3)	WLCSP9_3x3

7. Marking

Table 4. Marking codes

Type number	Marking code
PMCM950ENE	A1

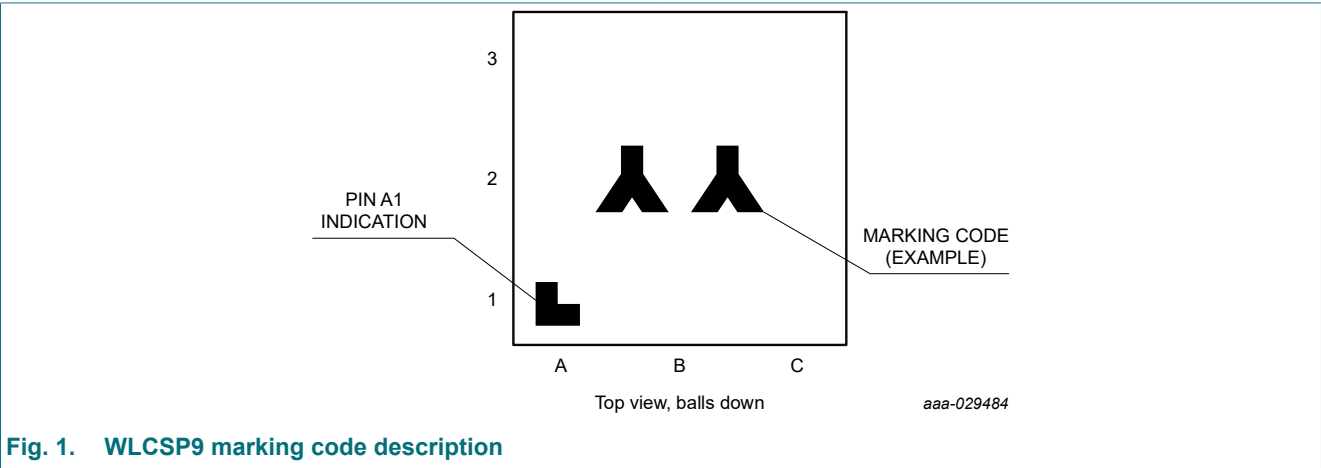


Fig. 1. WLCSP9 marking code description

## 8. Limiting values

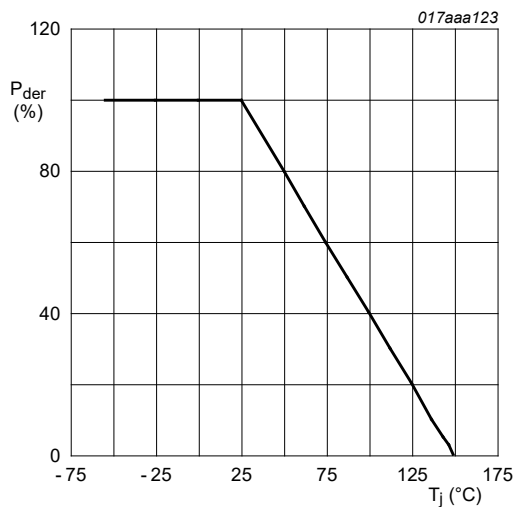
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C		-	60	V
V <sub>GS</sub>	gate-source voltage			-20	20	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>amb</sub> = 25 °C; t ≤ 5 s	[1]	-	6.1	A
		V <sub>GS</sub> = 10 V; T <sub>amb</sub> = 25 °C	[1]	-	4.8	A
		V <sub>GS</sub> = 10 V; T <sub>amb</sub> = 100 °C	[1]	-	3	A
I <sub>DM</sub>	peak drain current	T <sub>amb</sub> = 25 °C; single pulse; t <sub>p</sub> ≤ 10 μs		-	19	A
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[2]	-	780	mW
			[1]	-	1.4	W
		T <sub>sp</sub> = 25 °C		-	12.5	W
T <sub>j</sub>	junction temperature			-55	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C
<b>Source Drain Diode</b>						
I <sub>S</sub>	source current	T <sub>amb</sub> = 25 °C	[1]	-	1.4	A

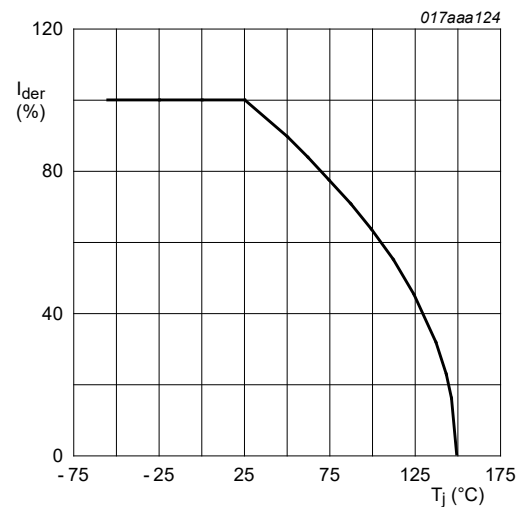
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100 \%$$

**Fig. 2. Normalized total power dissipation as a function of junction temperature**



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100 \%$$

**Fig. 3. Normalized continuous drain current as a function of junction temperature**

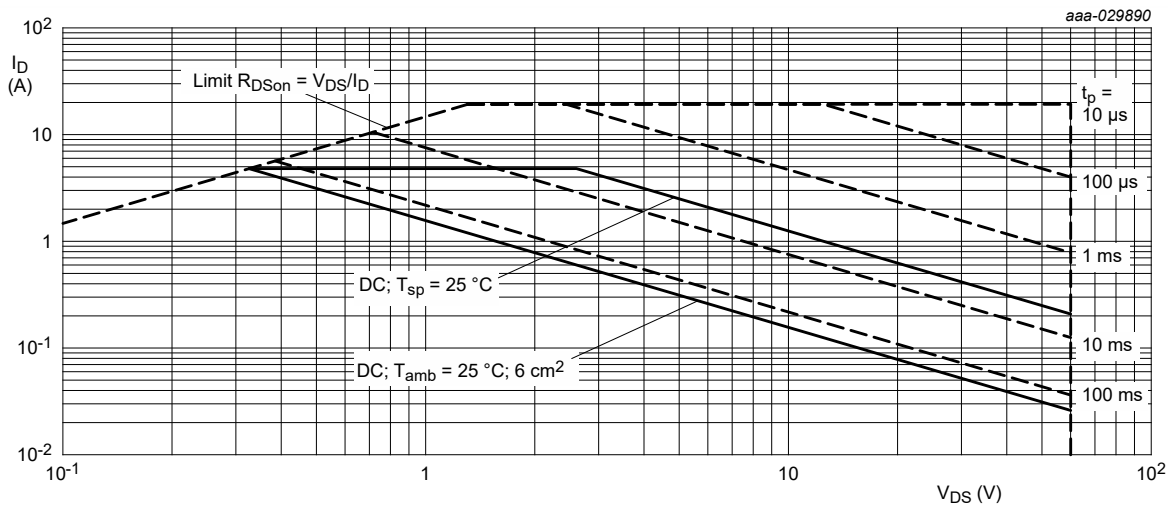


Fig. 4. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	130	160	K/W
			[2]	-	50	60	K/W
			[3]	-	65	80	K/W
		$t \leq 5$ s	[3]	-	42	50	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	5	10	K/W

- [1] Device mounted on an FR4 PCB, single sided-copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain, 4 layer, 1 cm<sup>2</sup>.
- [3] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.

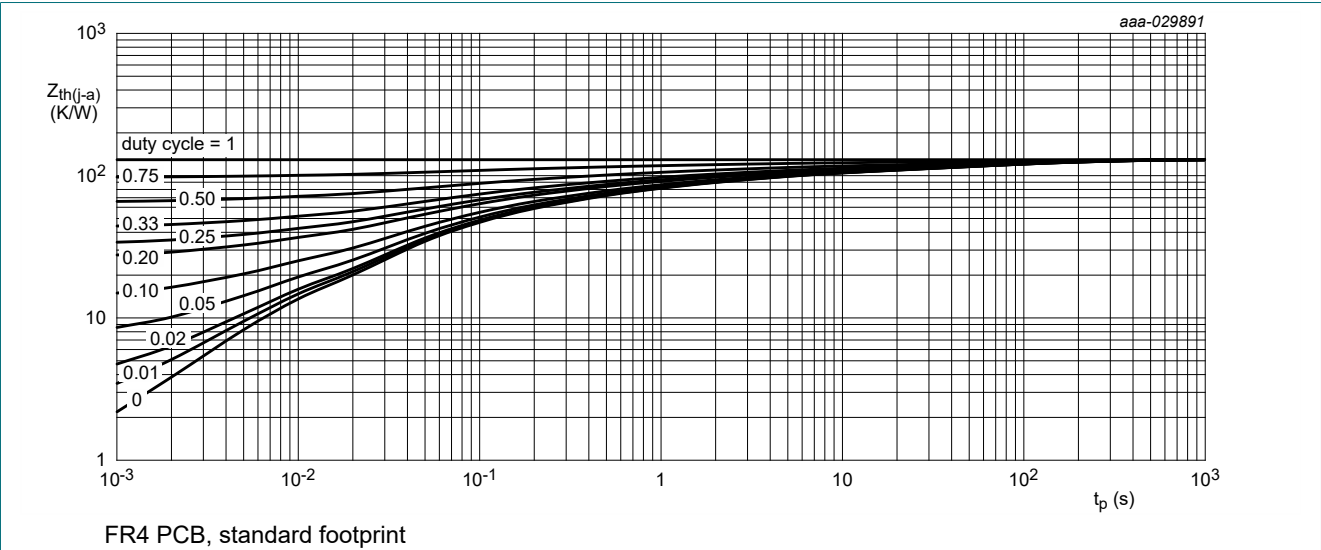


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

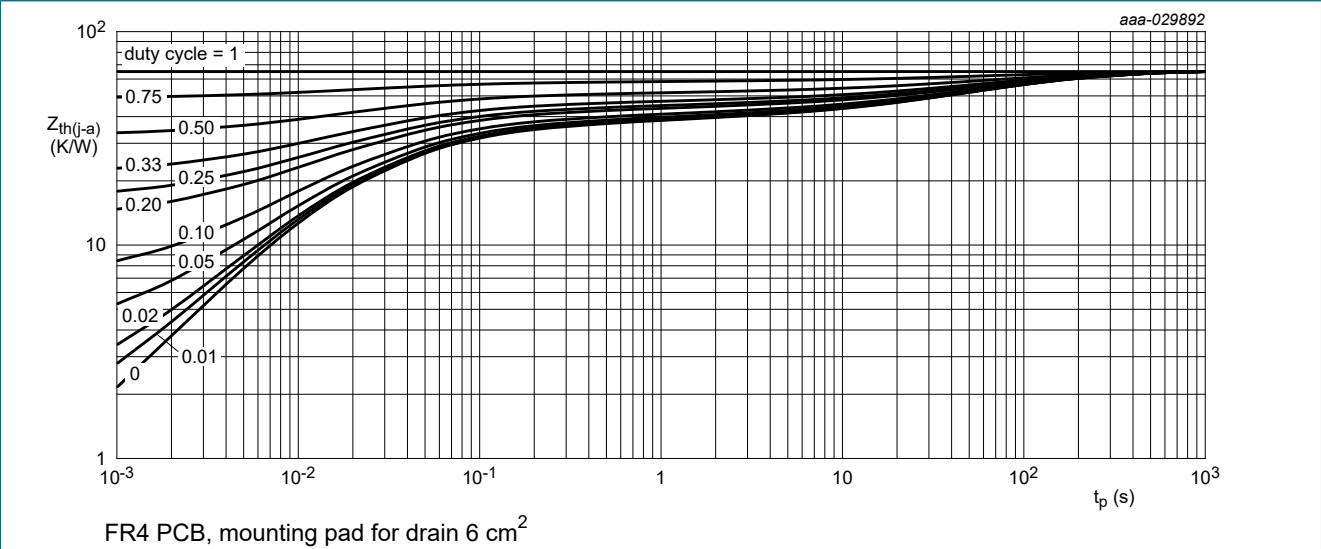


Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		60	-	-	V
V <sub>GSth</sub>	gate-source threshold voltage	I <sub>D</sub> = 250 μA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 25 °C		0.9	1.2	1.5	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 60 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	1	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	10	μA
		V <sub>GS</sub> = -20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	-10	μA
		V <sub>GS</sub> = 8 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	1	μA
		V <sub>GS</sub> = -8 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	-1	μA
		V <sub>GS</sub> = 4.5 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	200	nA
		V <sub>GS</sub> = -4.5 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	-200	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 3 A; T <sub>j</sub> = 25 °C		-	28	41	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 3 A; T <sub>j</sub> = 150 °C		-	46	68	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 3 A; T <sub>j</sub> = 25 °C		-	31	47	mΩ
g <sub>fs</sub>	forward transconductance	V <sub>DS</sub> = 5 V; I <sub>D</sub> = 3 A; T <sub>j</sub> = 25 °C		-	20	-	S
R <sub>G</sub>	gate resistance	f = 1 MHz		-	5.7	-	Ω
Dynamic characteristics							
Q <sub>G(tot)</sub>	total gate charge	V <sub>DS</sub> = 30 V; I <sub>D</sub> = 3 A; V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C		-	30	45	nC
Q <sub>GS</sub>	gate-source charge			-	2.3	-	nC
Q <sub>GD</sub>	gate-drain charge			-	5.9	-	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 30 V; f = 1 MHz; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	1160	-	pF
C <sub>oss</sub>	output capacitance			-	71	-	pF
C <sub>rss</sub>	reverse transfer capacitance			-	62	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 30 V; I <sub>D</sub> = 3 A; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 6 Ω; T <sub>j</sub> = 25 °C		-	2	-	ns
t <sub>r</sub>	rise time			-	4	-	ns
t <sub>d(off)</sub>	turn-off delay time			-	70	-	ns
t <sub>f</sub>	fall time			-	17	-	ns
Source-drain diode							
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 1.4 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	0.7	1.2	V

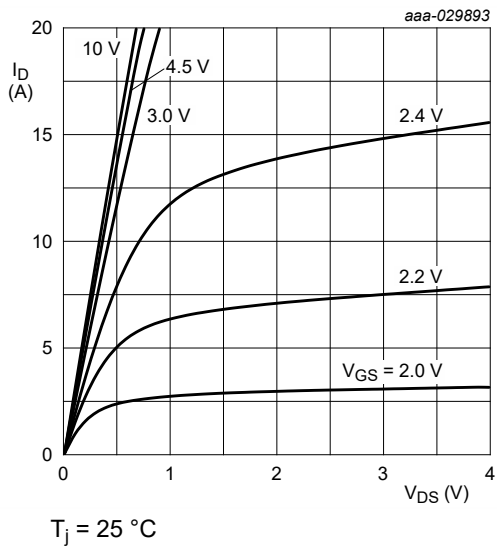


Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values

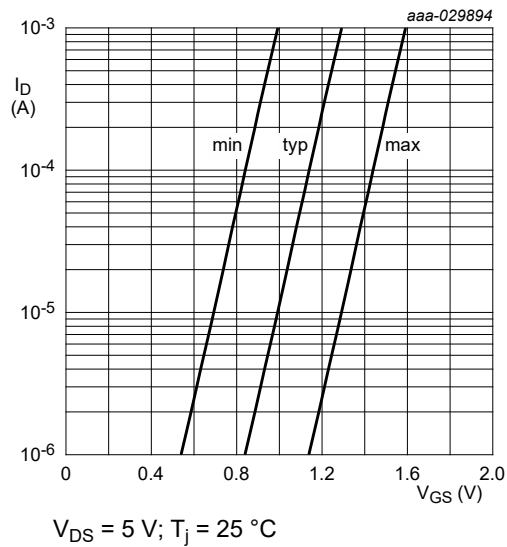


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

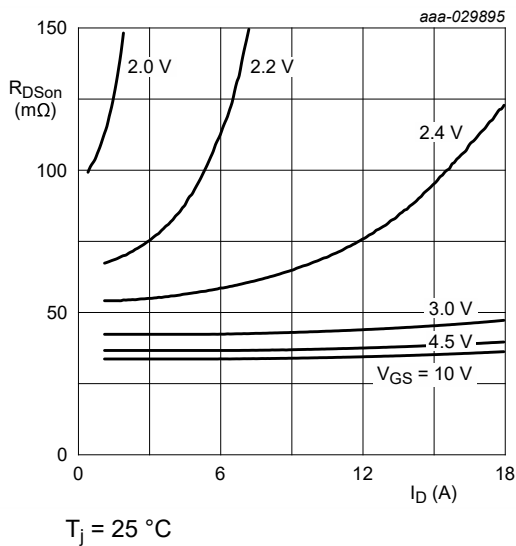


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

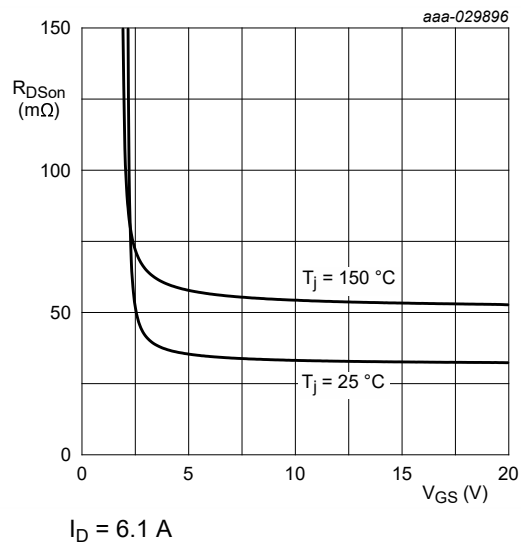


Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values

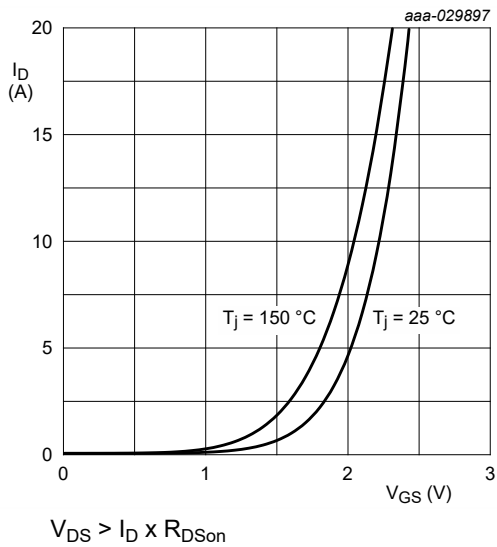


Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values

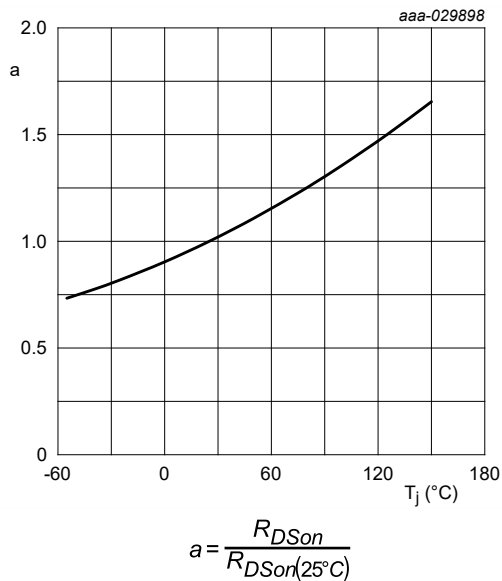


Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values

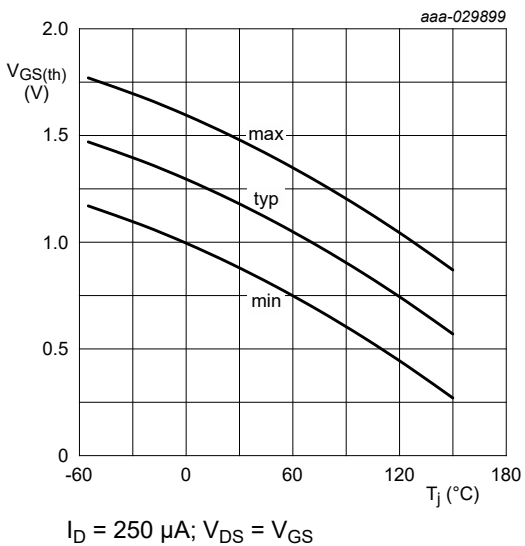


Fig. 13. Gate-source threshold voltage as a function of junction temperature

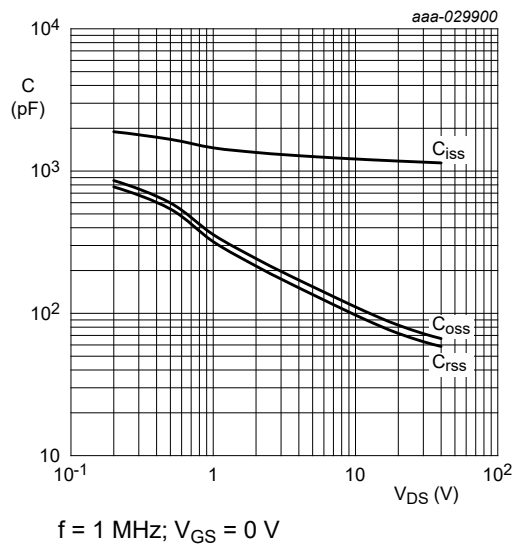
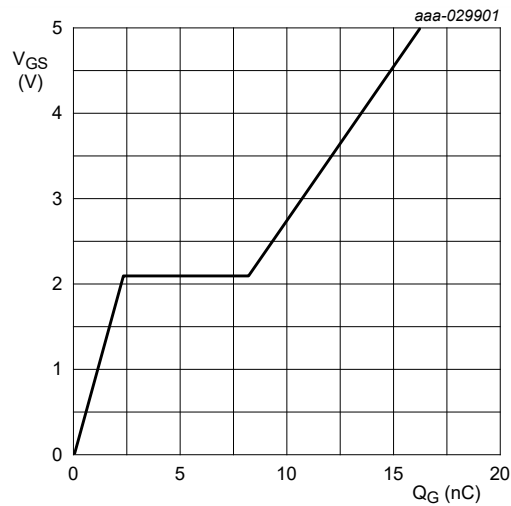


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values





$V_{DS} = 30\text{ V}$ ;  $I_D = 3\text{ A}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$

Fig. 15. Gate-source voltage as a function of gate charge; typical values

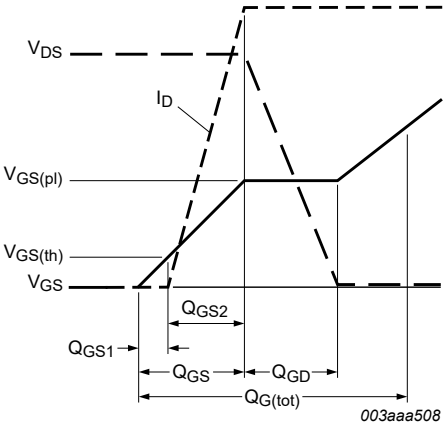
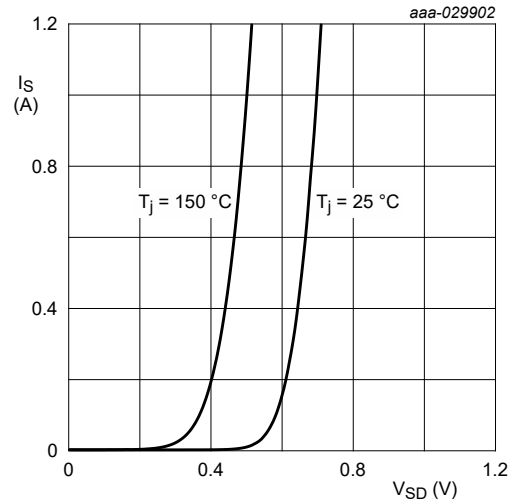


Fig. 16. Gate charge waveform definitions



$V_{GS} = 0\text{ V}$

Fig. 17. Source current as a function of source-drain voltage; typical values

11. Test information

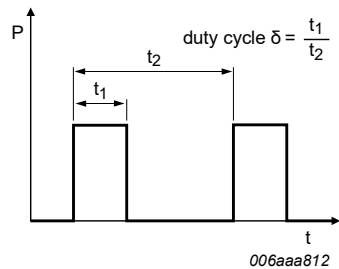


Fig. 18. Duty cycle definition

12. Package outline

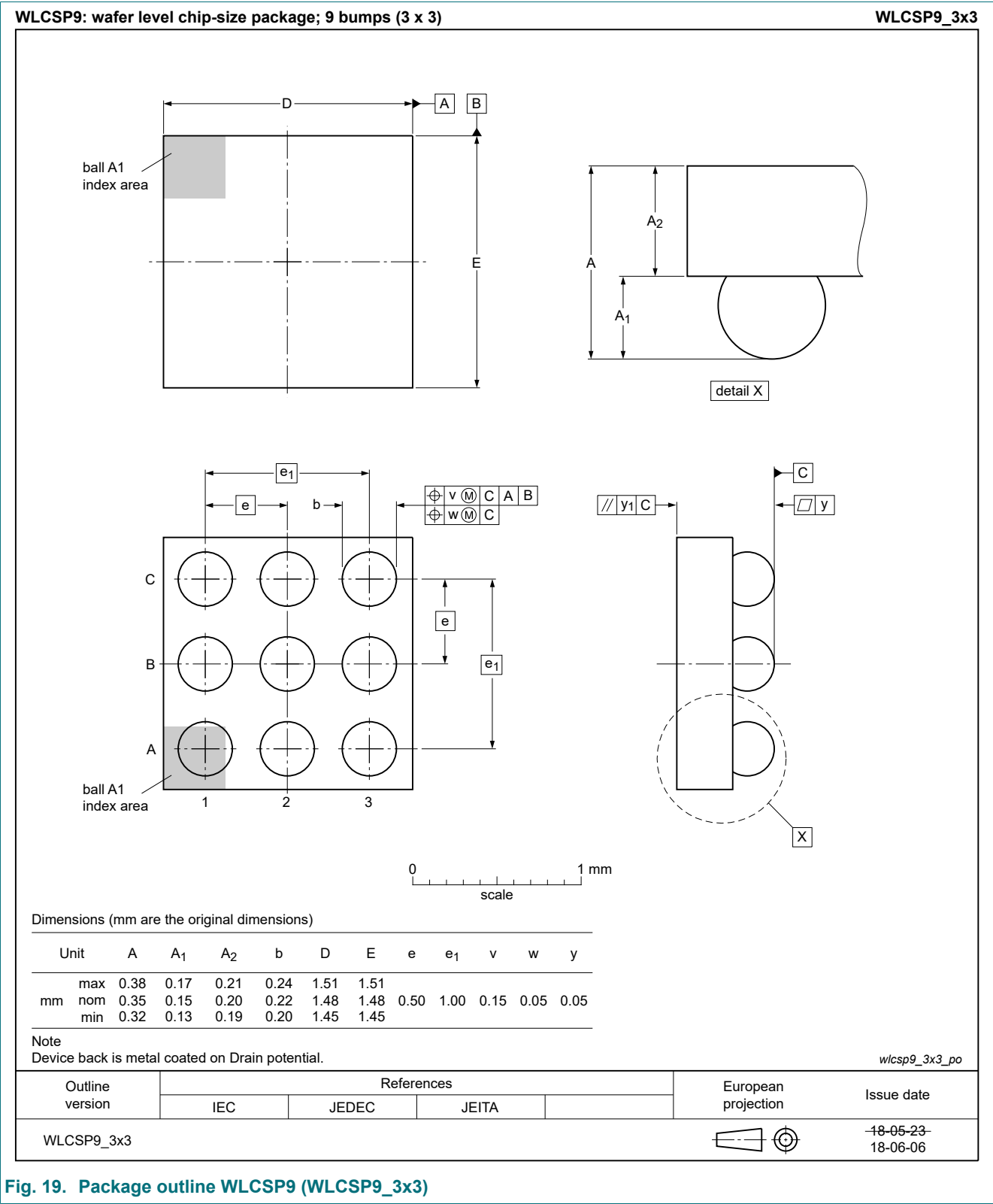


Fig. 19. Package outline WLCSP9 (WLCSP9\_3x3)

13. Soldering

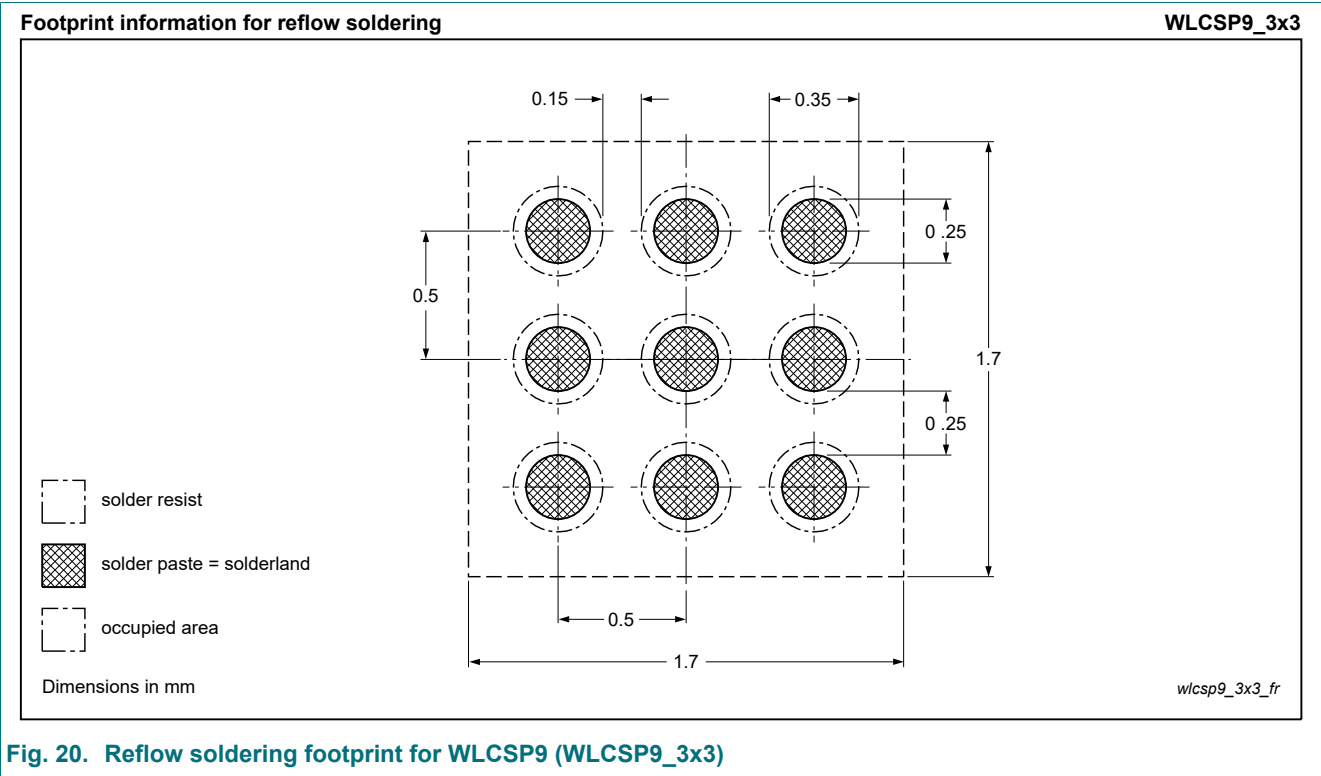


Fig. 20. Reflow soldering footprint for WLCSP9 (WLCSP9\_3x3)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMCM950ENE v.1	20190513	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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