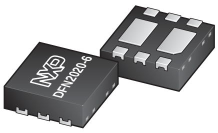


PMDPB42UN

20 V, dual N-channel Trench MOSFET

Rev. 1 — 16 May 2012 Product data sheet

1. Product profile

1.1 General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in a small and leadless ultra thin DFN2020-6 (SOT1118) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Very fast switching
- Trench MOSFET technology
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- Exposed drain pad for excellent thermal conduction

1.3 Applications

- Charging switch for portable devices
- DC-to-DC converters
- Small brushless DC motor drive
- Power management in battery-driven portables
- Hard disc and computing power management

1.4 Quick reference data

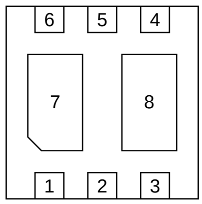
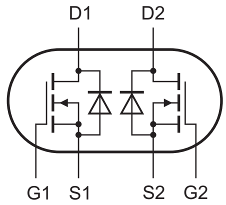
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
V_{DS}	drain-source voltage	T_j = 25 °C		-	-	20	V
V_{GS}	gate-source voltage			-8	-	8	V
I_D	drain current	V_{GS} = 4.5 V; T_{amb} = 25 °C; t ≤ 5 s	[1]	-	-	5.1	A
Static characteristics (per transistor)							
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 3.9 A; T_j = 25 °C		-	40	50	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 Transparent top view **SOT1118 (DFN2020-6)**	 *017aaa254*
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		
7	D1	drain TR1		
8	D2	drain TR2		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMDPB42UN	DFN2020-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1118

4. Marking

Table 4. Marking codes

Type number	Marking code
PMDPB42UN	1L

5. Limiting values

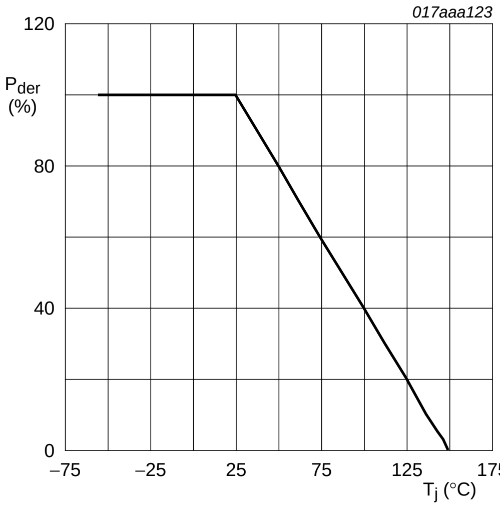
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V_{DS}	drain-source voltage	T_j = 25 °C		-	20	V
V_{GS}	gate-source voltage			-8	8	V
I_D	drain current	V_{GS} = 4.5 V; T_{amb} = 25 °C; t ≤ 5 s	[1]	-	5.1	A
		V_{GS} = 4.5 V; T_{amb} = 25 °C	[1]	-	3.9	A
		V_{GS} = 4.5 V; T_{amb} = 100 °C	[1]	-	2.5	A
I_{DM}	peak drain current	T_{amb} = 25 °C; single pulse; t_p ≤ 10 µs		-	15.6	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	[2]	-	510	mW
			[1]	-	1165	mW
		T_{sp} = 25 °C		-	8330	mW
Source-drain diode						
I_S	source current	T_{amb} = 25 °C	[1]	-	1.2	A
Per device						
T_j	junction temperature			-55	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C

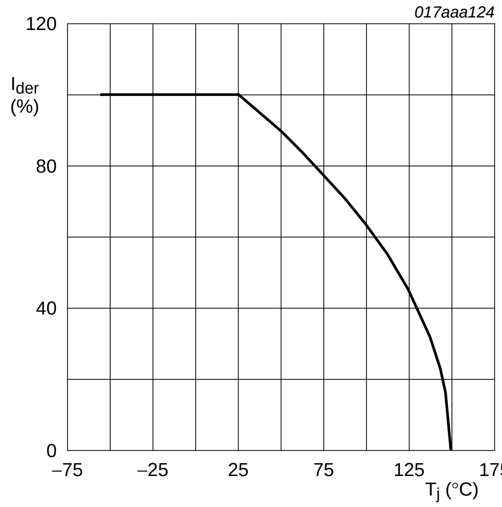
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2.

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



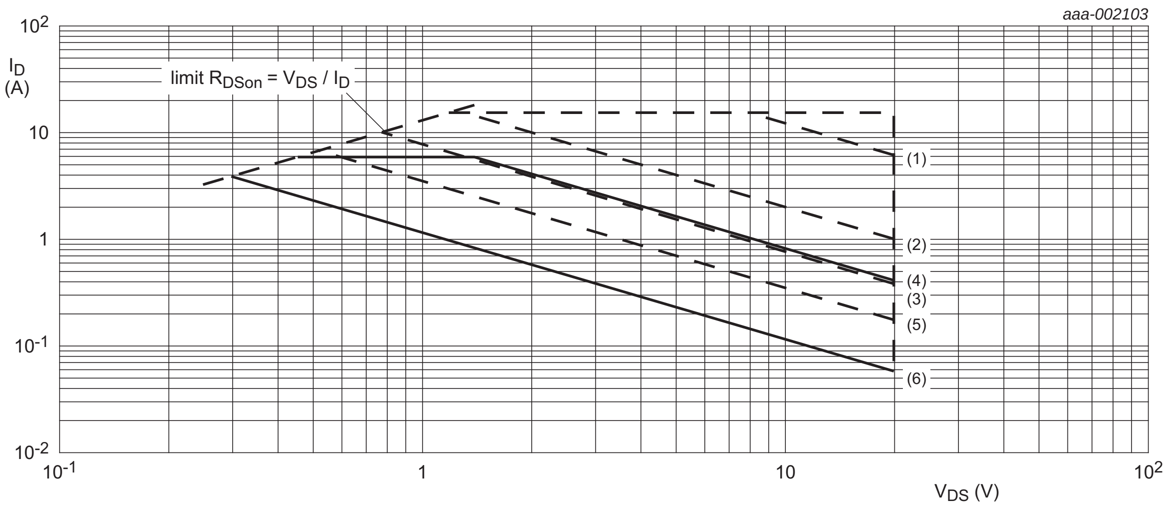
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

Fig 1. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\ \%$$

Fig 2. Normalized continuous drain current as a function of junction temperature



I_{DM} is single pulse

(1) t_p = 100 µs

(2) t_p = 1 ms

(3) t_p = 10 ms

(4) DC; T_{sp} = 25 °C

(5) t_p = 100 ms

(6) DC; T_{amb} = 25 °C; drain mounting pad 6 cm^2

Fig 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

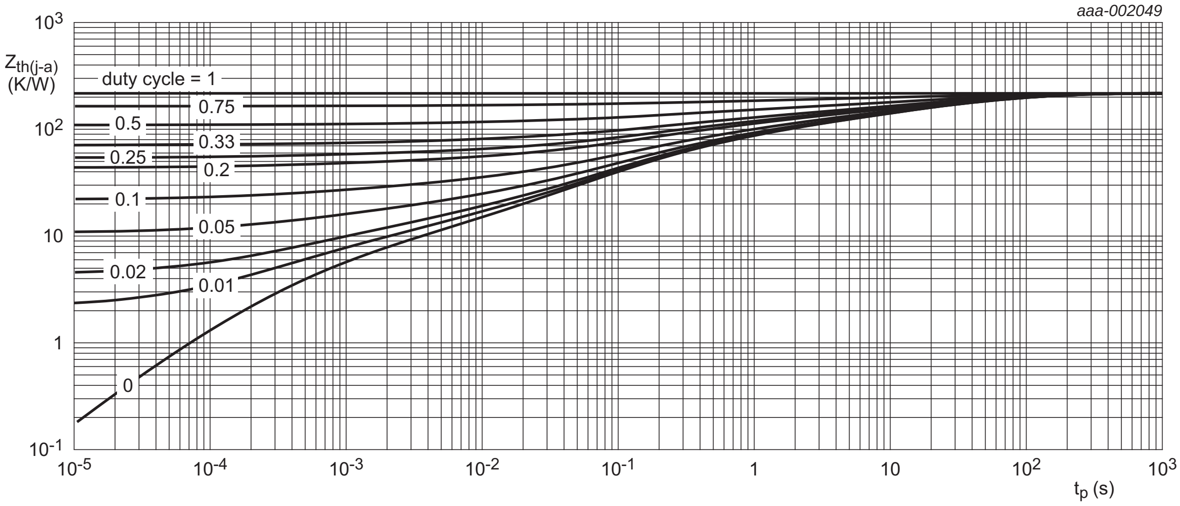
6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	213	245	K/W
			[2]	-	93	107	K/W
		in free air; t ≤ 5 s	[2]	-	55	64	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	12	15	K/W

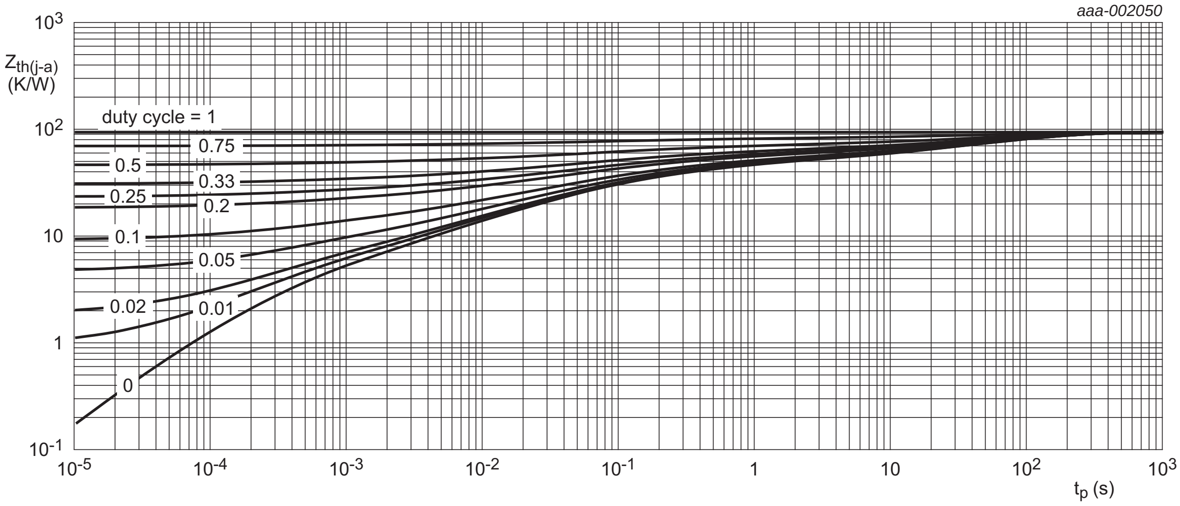
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm^2.



FR4 PCB standard footprint

Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



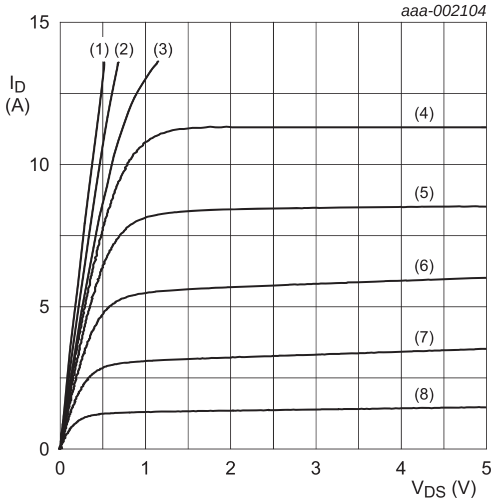
FR4 PCB, mounting pad for drain 6 cm^2

Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics (per transistor)						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 μA; V_{GS} = 0 V; T_j = 25 °C	20	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = 250 μA; V_{DS} = V_{GS}; T_j = 25 °C	0.4	0.7	1	V
I_{DSS}	drain leakage current	V_{DS} = 20 V; V_{GS} = 0 V; T_j = 25 °C	-	-	1	μA
		V_{DS} = 20 V; V_{GS} = 0 V; T_j = 150 °C	-	-	20	μA
I_{GSS}	gate leakage current	V_{GS} = 8 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
		V_{GS} = -8 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 3.9 A; T_j = 25 °C	-	40	50	mΩ
		V_{GS} = 4.5 V; I_D = 3.9 A; T_j = 150 °C	-	61	76	mΩ
		V_{GS} = 2.5 V; I_D = 3.2 A; T_j = 25 °C	-	53	70	mΩ
		V_{GS} = 1.8 V; I_D = 0.8 A; T_j = 25 °C	-	82	123	mΩ
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 3.9 A; T_j = 25 °C	-	11	-	S
Dynamic characteristics (per transistor)						
$Q_{G(tot)}$	total gate charge	V_{DS} = 10 V; I_D = 3.9 A; V_{GS} = 4.5 V; T_j = 25 °C	-	2	3.5	nC
Q_{GS}	gate-source charge		-	0.4	-	nC
Q_{GD}	gate-drain charge		-	0.6	-	nC
C_{iss}	input capacitance	V_{DS} = 10 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25 °C	-	185	-	pF
C_{oss}	output capacitance		-	55	-	pF
C_{rss}	reverse transfer capacitance		-	25	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 10 V; I_D = 3.9 A; V_{GS} = 4.5 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C	-	6	-	ns
t_r	rise time		-	30	-	ns
$t_{d(off)}$	turn-off delay time		-	20	-	ns
t_f	fall time		-	15	-	ns
Source-drain diode (per transistor)						
V_{SD}	source-drain voltage	I_S = 1.2 A; V_{GS} = 0 V; T_j = 25 °C	-	0.8	1.2	V



T_j = 25 °C

(1) V_{GS} = 4.5 V

(2) V_{GS} = 3.0 V

(3) V_{GS} = 2.4 V

(4) V_{GS} = 2.2 V

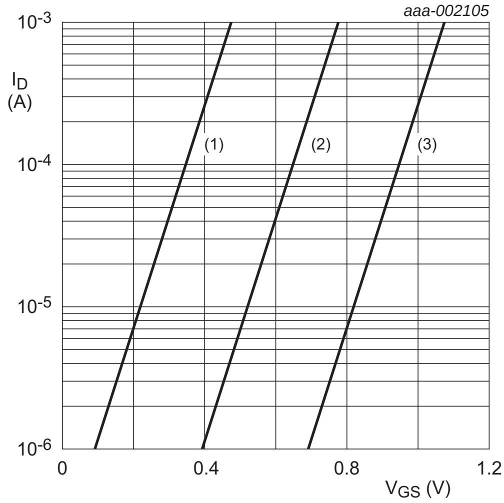
(5) V_{GS} = 2.0 V

(6) V_{GS} = 1.8 V

(7) V_{GS} = 1.6 V

(8) V_{GS} = 1.4 V

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values



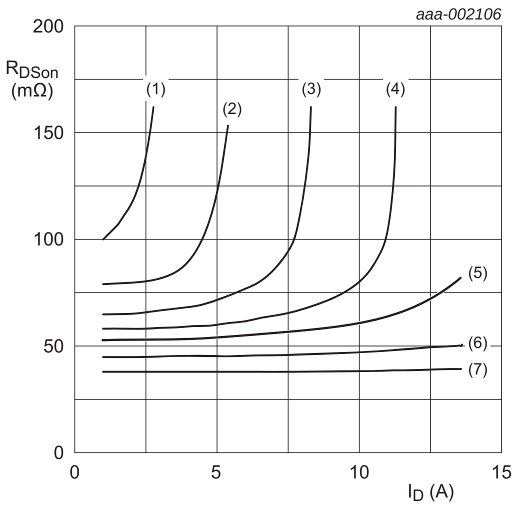
T_j = 25 °C; V_{DS} = 15 V

(1) minimum values

(2) typical values

(3) maximum values

Fig 7. Subthreshold drain current as a function of gate-source voltage



T_j = 25 °C

(1) V_{GS} = 1.6 V

(2) V_{GS} = 1.8 V

(3) V_{GS} = 2.0 V

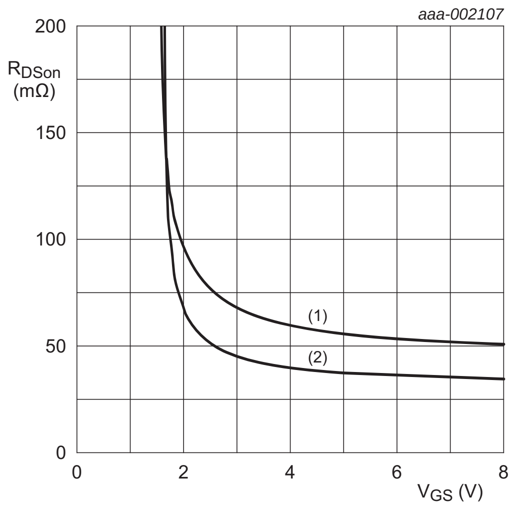
(4) V_{GS} = 2.2 V

(5) V_{GS} = 2.4 V

(6) V_{GS} = 3.0 V

(7) V_{GS} = 4.5 V

Fig 8. Drain-source on-state resistance as a function of drain current; typical values

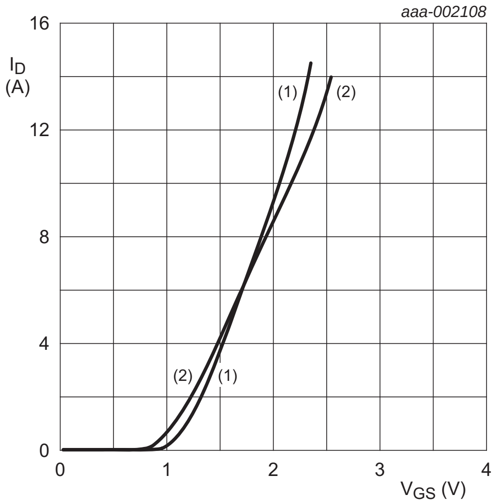


I_D = 3.4 A

(1) T_j = 150 °C

(2) T_j = 25 °C

Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

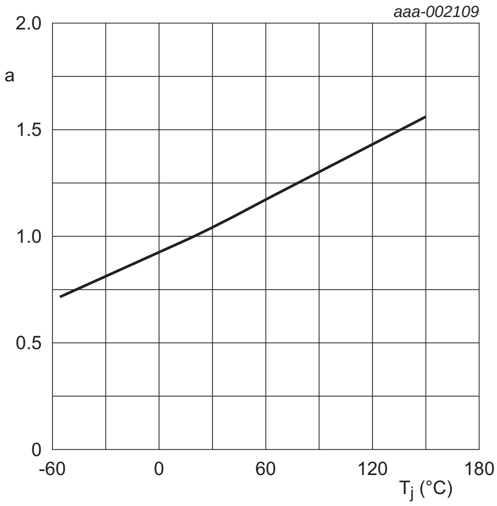


$V_{DS} > I_D \times R_{DSon}$

(1) T_j = 25 °C

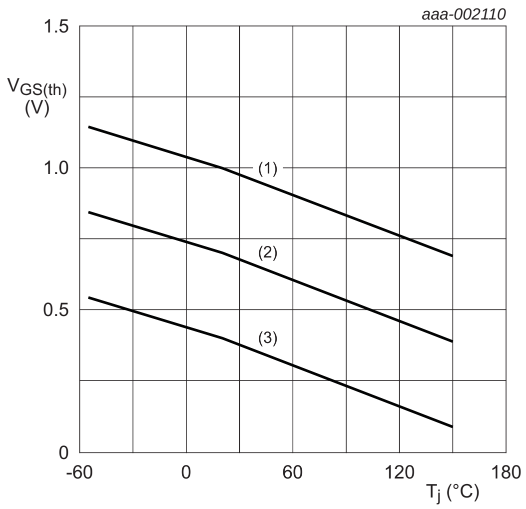
(2) T_j = 150 °C

Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values



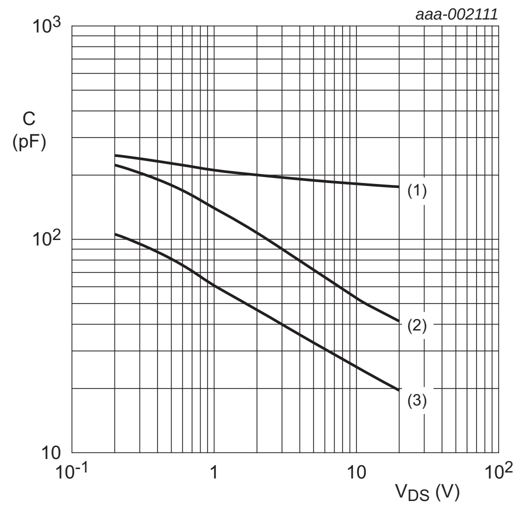
I_D = 0.25 mA; V_{DS} = V_{GS}

(1) maximum values

(2) typical values

(3) minimum values

Fig 12. Gate-source threshold voltage as a function of junction temperature



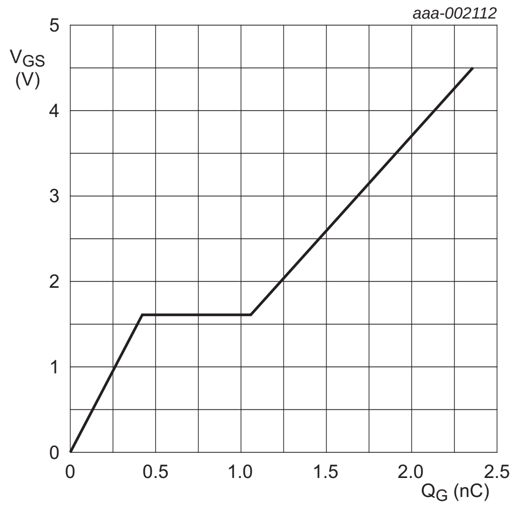
f = 1 MHz; V_{GS} = 0 V

(1) C_{iss}

(2) C_{oss}

(3) C_{rss}

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



I_D = 3.9 A; V_{DS} = 15 V; T_{amb} = 25 °C

Fig 14. Gate-source voltage as a function of gate charge; typical values

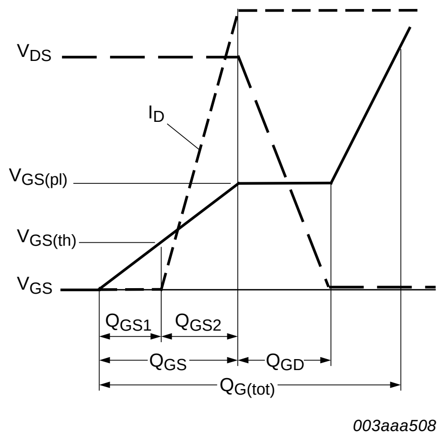
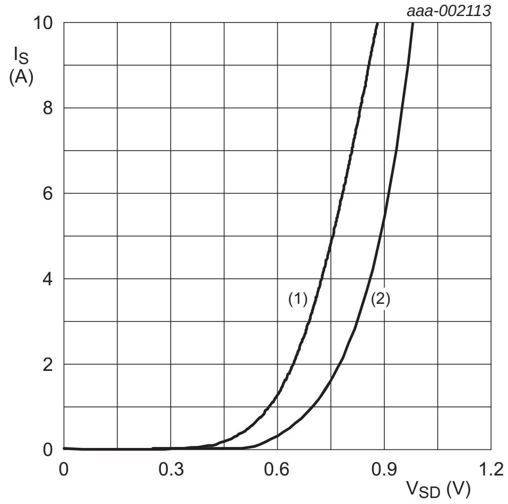


Fig 15. Gate charge waveform definitions



V_{GS} = 0 V

(1) T_j = 150 °C

(2) T_j = 25 °C

Fig 16. Source current as a function of source-drain voltage; typical values

8. Test information

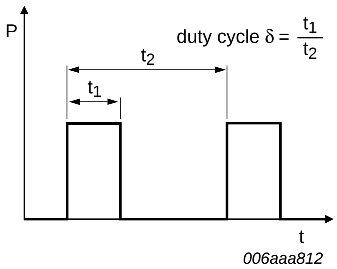


Fig 17. Duty cycle definition

9. Package outline

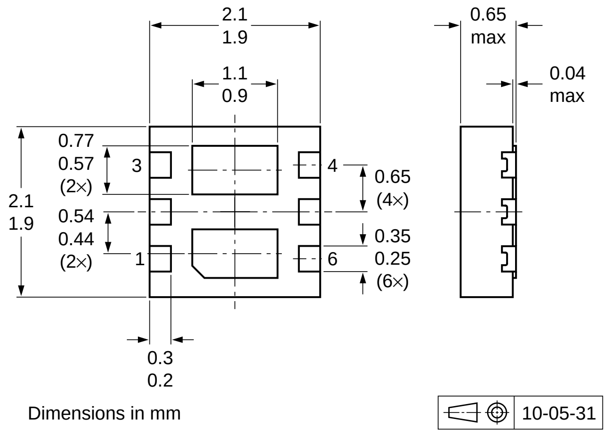


Fig 18. Package outline SOT1118 (DFN2020-6)

10. Soldering

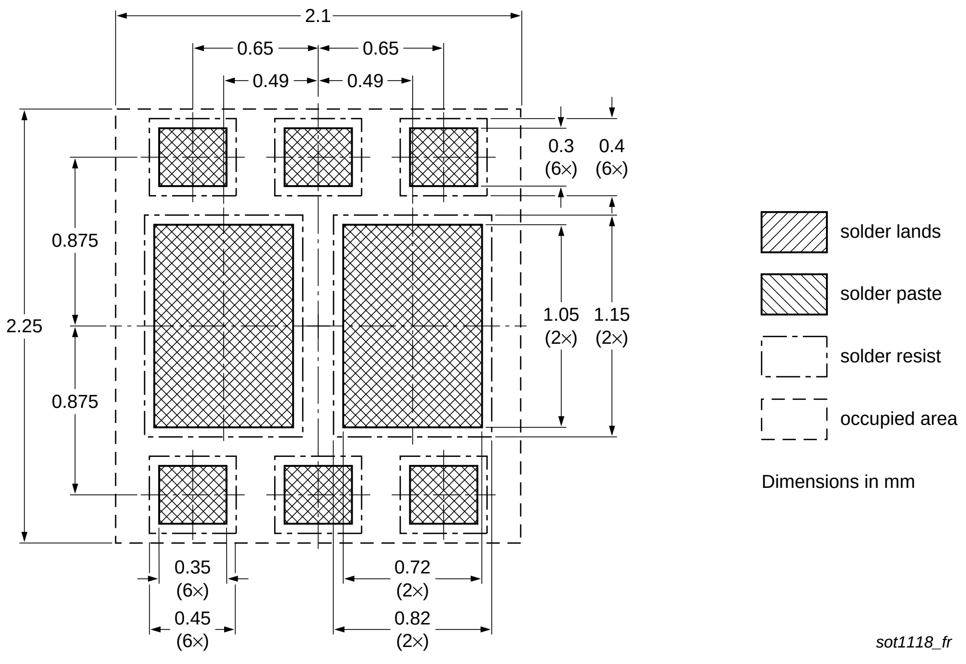


Fig 19. Reflow soldering footprint for SOT1118 (DFN2020-6)

11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMDPB42UN v.1	20120516	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1] [2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URLhttp://www.nxp.com.

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14. Contents

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