

PMF3800SN

N-channel TrenchMOS standard level FET

Rev. 02 — 1 July 2005

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

1.2 Features

- Logic level compatible
- Very fast switching
- Subminiature surface-mounted package
- Gate-source ESD protection diodes

1.3 Applications

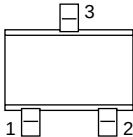
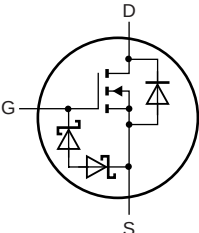
- Relay driver
- High-speed line driver

1.4 Quick reference data

- $V_{DS} \leq 60 \text{ V}$
- $I_D \leq 260 \text{ mA}$
- $R_{DS(on)} \leq 4.5 \text{ } \Omega$
- $P_{tot} \leq 0.56 \text{ W}$

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1	gate (G)		
2	source (S)		
3	drain (D)		
		SOT323 (SC-70)	03ab60

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3. Ordering information

Table 2: Ordering information

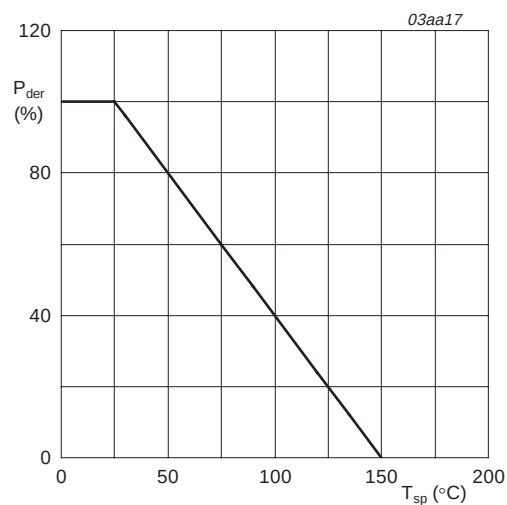
Type number	Package		
	Name	Description	Version
PMF3800SN	SC-70	plastic surface mounted package; 3 leads	SOT323

4. Limiting values

Table 3: Limiting values

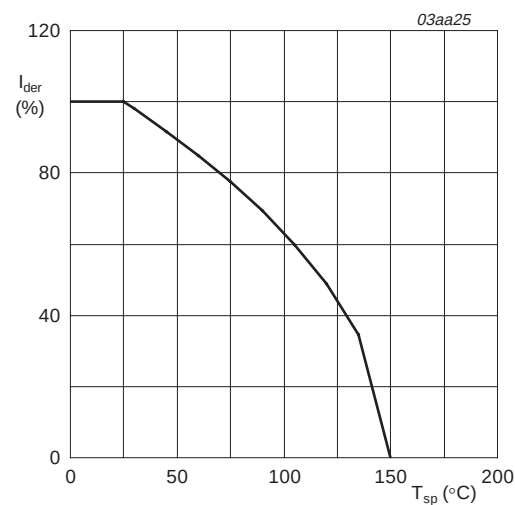
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	60	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	60	V
V_{GS}	gate-source voltage		-	± 15	V
I_D	drain current	$T_{sp} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2 and 3	-	260	mA
		$T_{sp} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2	-	165	mA
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	-	560	mA
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; Figure 1	-	0.56	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C
Source-drain diode					
I_S	source (diode forward) current	$T_{sp} = 25\text{ °C}$	-	280	mA
I_{SM}	peak source (diode forward) current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	560	mA
Electrostatic discharge voltage					
V_{esd}	electrostatic discharge voltage	Human body model 1; $C = 100\text{ pF}$; $R = 1.5\text{ k}\Omega$	-	1	kV



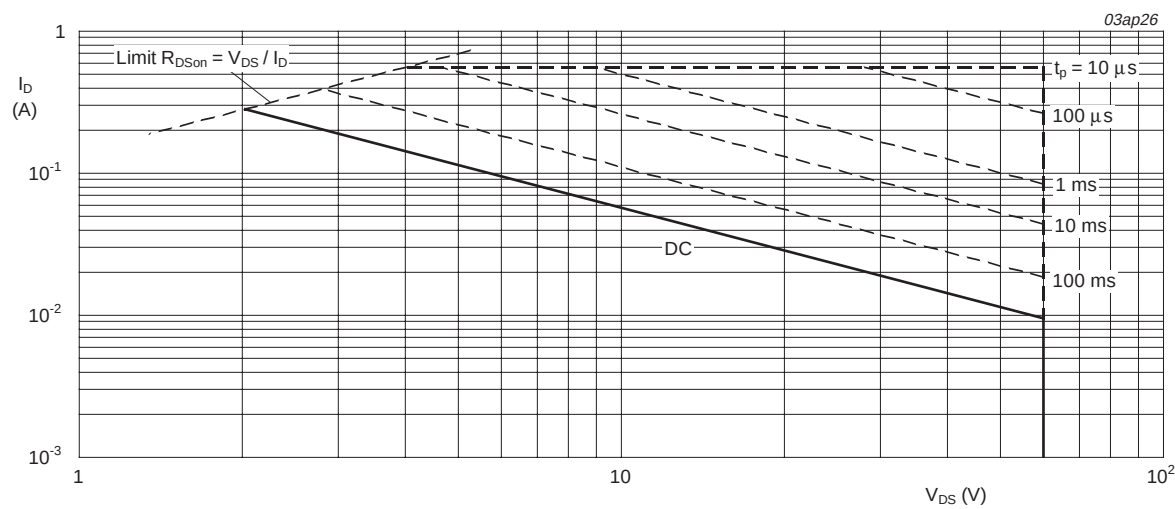
$$P_{der} = \frac{P_{tot}}{P_{tot(25\text{ }^{\circ}\text{C})}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature



$$I_{der} = \frac{I_D}{I_{D(25\text{ }^{\circ}\text{C})}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature



T_{sp} = 25 °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Figure 4	-	-	220	K/W

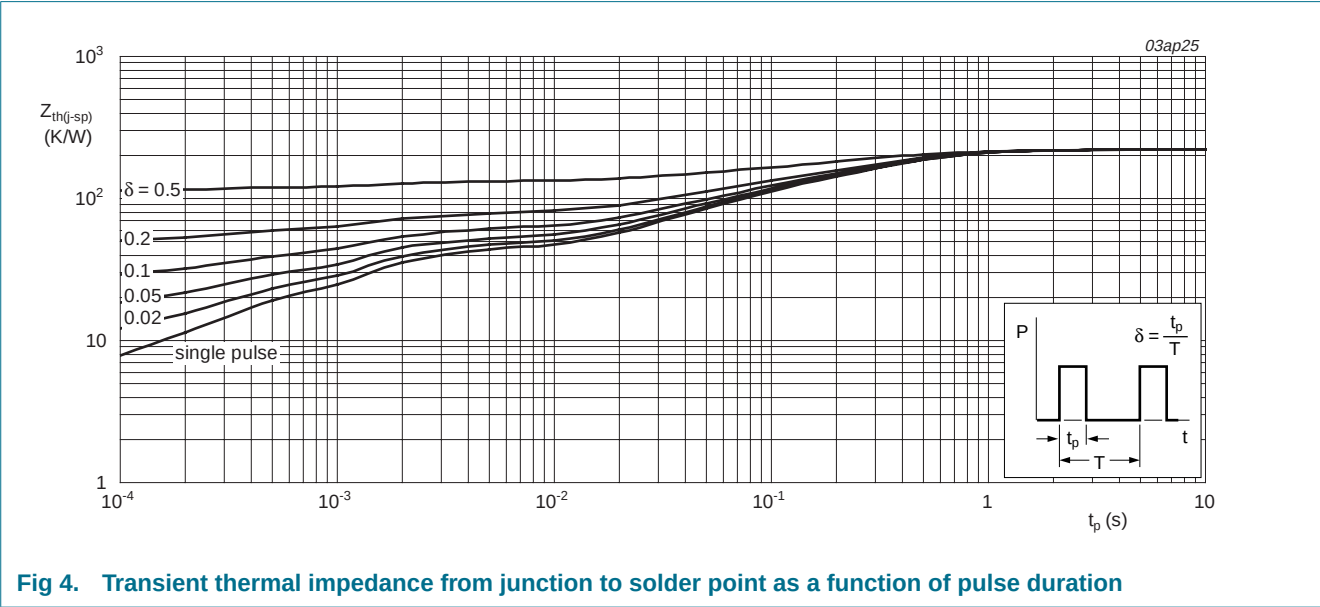


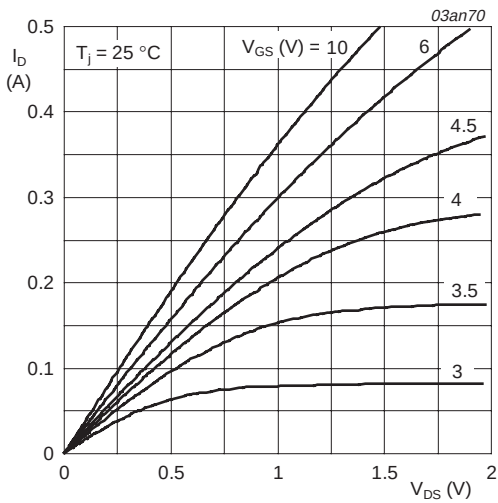
Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

Table 5: Characteristics

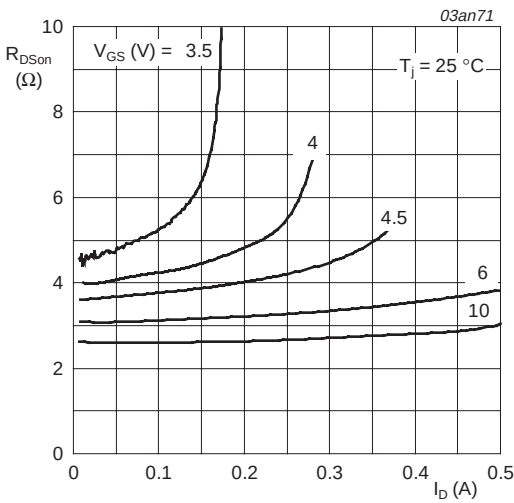
$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^{\circ}\text{C}$	60	-	-	V
		$T_j = -55\text{ }^{\circ}\text{C}$	55	-	-	V
$V_{(BR)GSS}$	gate-source breakdown voltage	$I_G = \pm 1\text{ mA}$; $V_{DS} = 0\text{ V}$	16	22	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; Figure 9 and 10				
		$T_j = 25\text{ }^{\circ}\text{C}$	1	2	-	V
		$T_j = 150\text{ }^{\circ}\text{C}$	0.6	-	-	V
		$T_j = -55\text{ }^{\circ}\text{C}$	-	-	3.5	V
I_{DSS}	drain leakage current	$V_{DS} = 48\text{ V}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^{\circ}\text{C}$	-	-	1	μA
		$T_j = 150\text{ }^{\circ}\text{C}$	-	-	10	μA
I_{GSS}	gate leakage current	$V_{GS} = \pm 10\text{ V}$; $V_{DS} = 0\text{ V}$	-	50	500	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 500\text{ mA}$; Figure 6 and 8				
		$T_j = 25\text{ }^{\circ}\text{C}$	-	2.8	4.5	m Ω
		$T_j = 150\text{ }^{\circ}\text{C}$	-	5.2	8.4	m Ω
		$V_{GS} = 4.5\text{ V}$; $I_D = 200\text{ mA}$; Figure 6 and 8	-	3.8	5.3	m Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 0.5\text{ A}$; $V_{DS} = 48\text{ V}$; $V_{GS} = 10\text{ V}$; Figure 11	-	0.85	-	nC
Q_{GS}	gate-source charge		-	0.55	-	nC
Q_{GD}	gate-drain (Miller) charge		-	0.07	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 10\text{ V}$; $f = 1\text{ MHz}$; Figure 13	-	13	40	pF
C_{oss}	output capacitance		-	8	30	pF
C_{rss}	reverse transfer capacitance		-	4	10	pF
t_{on}	turn-on time	$V_{DS} = 50\text{ V}$; $R_L = 250\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $R_G = 50\text{ }\Omega$; $R_{GS} = 50\text{ }\Omega$	-	3	-	ns
t_{off}	turn-off time		-	9	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 300\text{ mA}$; $V_{GS} = 0\text{ V}$; Figure 12	-	0.93	1.5	V
t_{rr}	reverse recovery time	$I_S = 300\text{ mA}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_R = 25\text{ V}$	-	30	-	ns
Q_r	recovered charge		-	30	-	nC



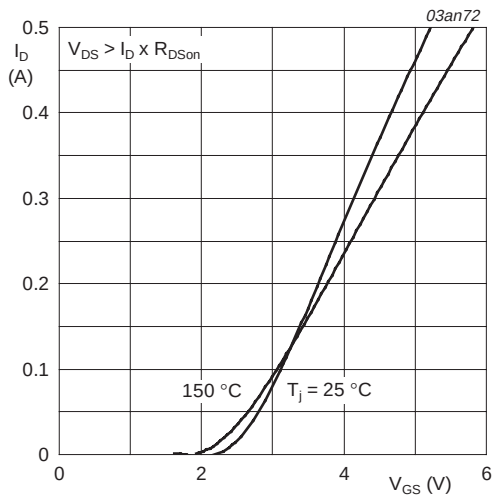
$T_j = 25\text{ °C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



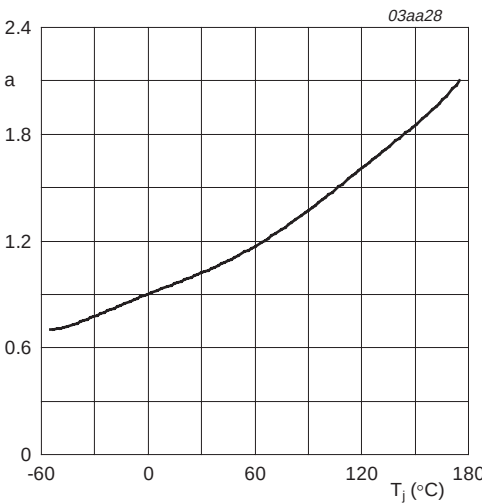
$T_j = 25\text{ °C}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



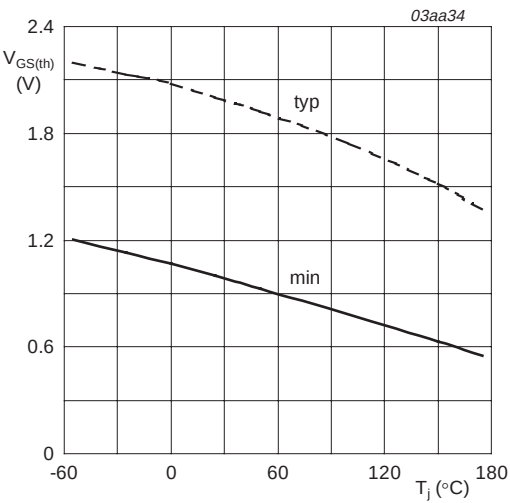
$T_j = 25\text{ °C}$ and 150 °C ; $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



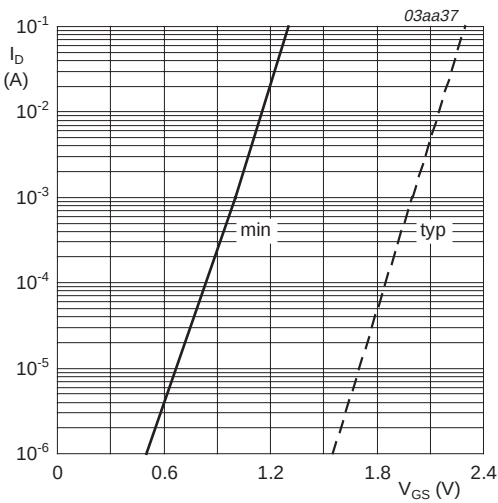
$$a = \frac{R_{DSon}}{R_{DSon(25\text{ °C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



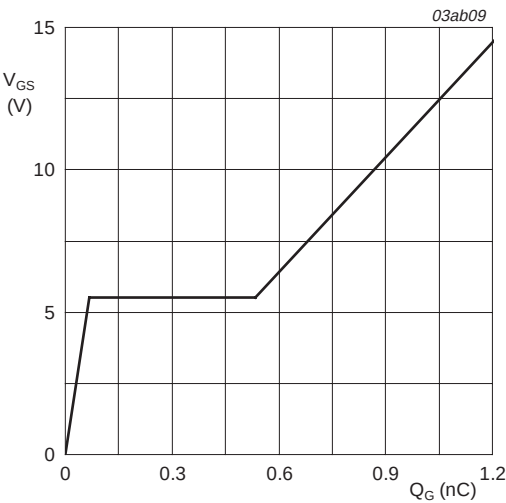
$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



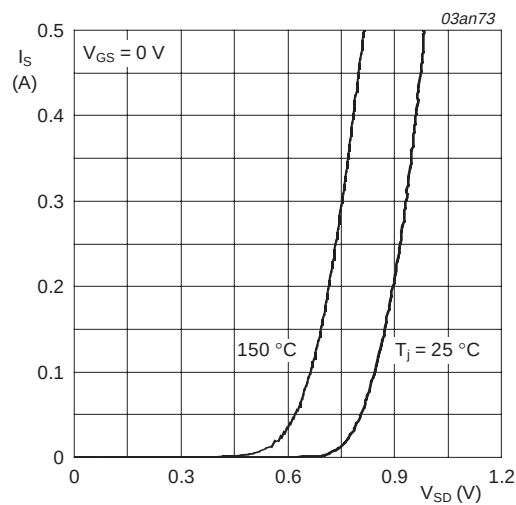
$T_J = 25\text{ }^{\circ}C$; $V_{DS} = 5\text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



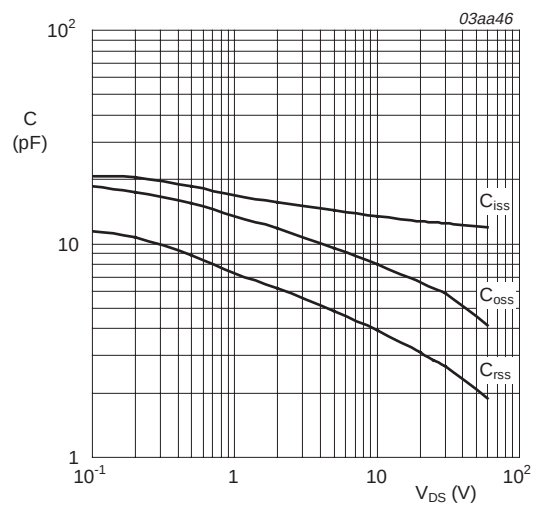
$I_D = 0.5\text{ A}$; $V_{DS} = 48\text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values



$T_j = 25\text{ °C}$ and 150 °C ; $V_{GS} = 0\text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values



$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

7. Package outline

Plastic surface mounted package; 3 leads

SOT323

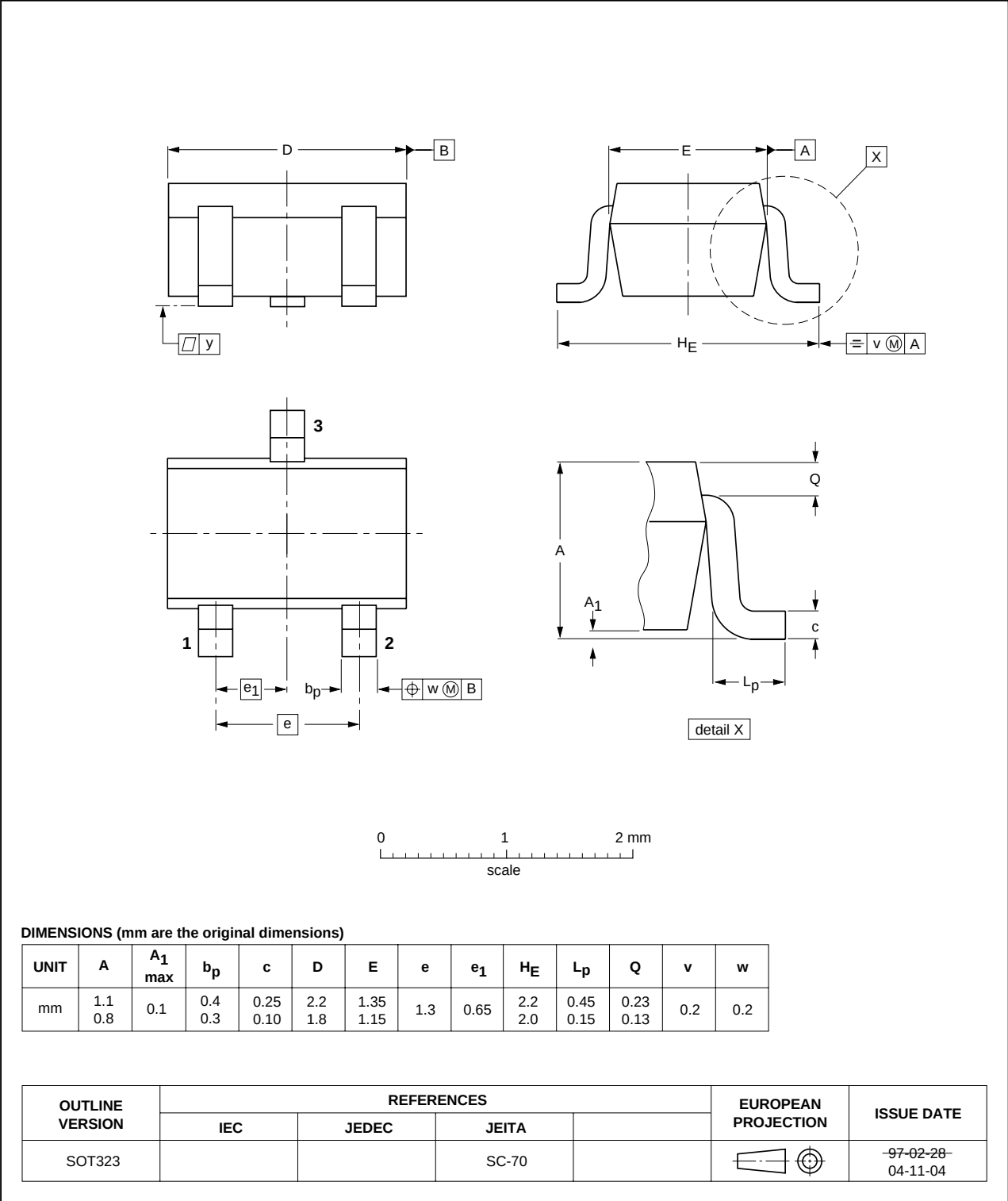


Fig 14. Package outline SOT323 (SC-70)

8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PMF3800SN_2	20050701	Product data sheet	-	9397 750 15218	PMF3800SN_1
Modifications:					
• Table 5 "Characteristics" : Addition of Q _G data to table.					
PMF3800SN_1	20050208	Product data sheet	-	9397 750 14255	-

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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