



PMGD290UCEA

20 / 20 V, 725 / 500 mA N/P-channel Trench MOSFET

28 March 2014

Product data sheet

1. General description

Complementary N/P-channel enhancement mode Field-Effect Transistor (FET) in a very small SOT363 Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Very fast switching
- Trench MOSFET technology
- 2 kV ESD protection
- AEC-Q101 qualified

3. Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits
- Automotive applications

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR1 (N-channel), Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 500 \text{ mA}; T_j = 25 \text{ }^\circ\text{C}$	-	290	380	m Ω
TR2 (P-channel), Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}; I_D = -400 \text{ mA}; T_j = 25 \text{ }^\circ\text{C}$	-	670	850	m Ω
TR1 (N-channel)						
V_{DS}	drain-source voltage	$T_j = 25 \text{ }^\circ\text{C}$	-	-	20	V
V_{GS}	gate-source voltage		-8	-	8	V
I_D	drain current	$V_{GS} = 4.5 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$	[1]	-	725	mA
TR2 (P-channel)						
V_{DS}	drain-source voltage	$T_j = 25 \text{ }^\circ\text{C}$	-	-	-20	V

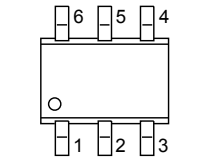
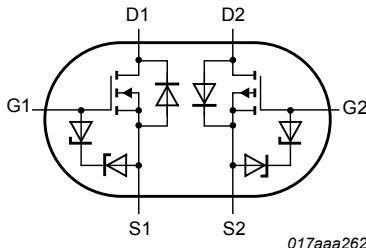


Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{GS}	gate-source voltage		-8	-	8	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-500	mA

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 <p>TSSOP6 (SOT363)</p>	 <p>017aaa262</p>
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PMGD290UCEA	TSSOP6	plastic surface-mounted package; 6 leads	SOT363

7. Marking

Table 4. Marking codes

Type number	Marking code
PMGD290UCEA	YD% [1]

[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
TR1 (N-channel)					
V _{DS}	drain-source voltage	T _j = 25 °C	-	20	V
V _{GS}	gate-source voltage		-8	8	V

Symbol	Parameter	Conditions		Min	Max	Unit
I _D	drain current	V _{GS} = 4.5 V; T _{amb} = 25 °C	[1]	-	725	mA
		V _{GS} = 4.5 V; T _{amb} = 100 °C	[1]	-	450	mA
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	3	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	280	mW
			[1]	-	320	mW
		T _{sp} = 25 °C		-	990	mW
TR1 (N-channel), Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	370	mA
TR1 N-channel), ESD maximum rating						
V _{ESD}	electrostatic discharge voltage	HBM	[3]	-	2000	V
TR2 (P-channel)						
V _{DS}	drain-source voltage	T _j = 25 °C		-	-20	V
V _{GS}	gate-source voltage				-8	8
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-500	mA
		V _{GS} = -4.5 V; T _{amb} = 100 °C	[1]	-	-320	mA
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	-2	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	280	mW
			[1]	-	320	mW
		T _{sp} = 25 °C		-	990	mW
TR2 (P-channel), Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	-370	mA
TR2 (P-channel), ESD maximum rating						
V _{ESD}	electrostatic discharge voltage	HBM	[3]	-	2000	V
Per device						
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	445	mW
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm².

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper; tin-plated and standard footprint.

[3] Measured between all pins.

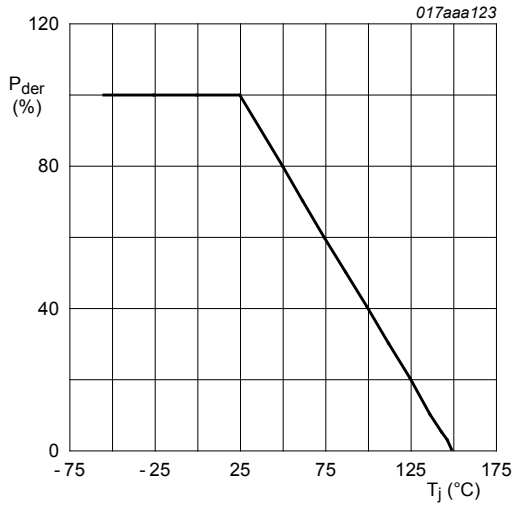


Fig. 1. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

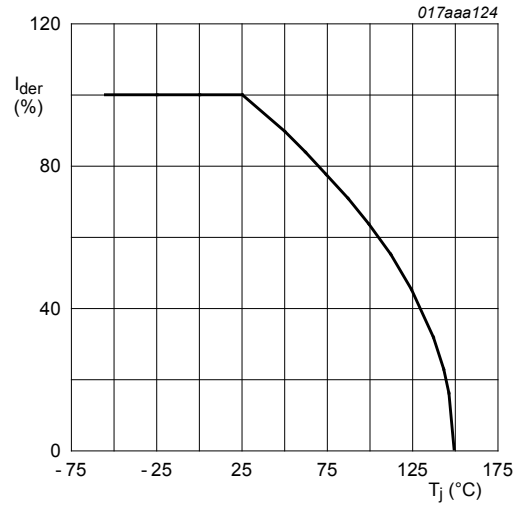
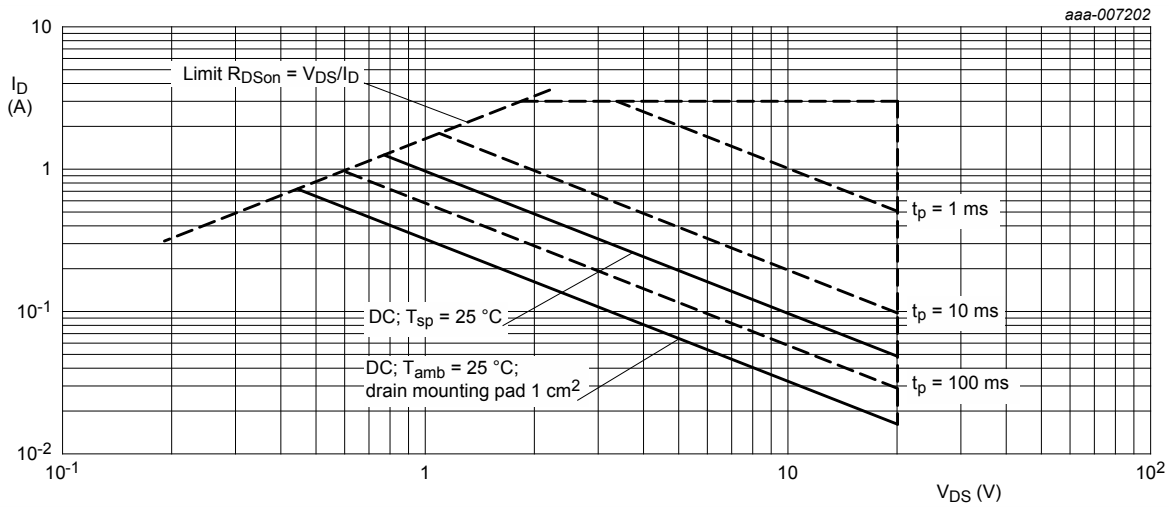


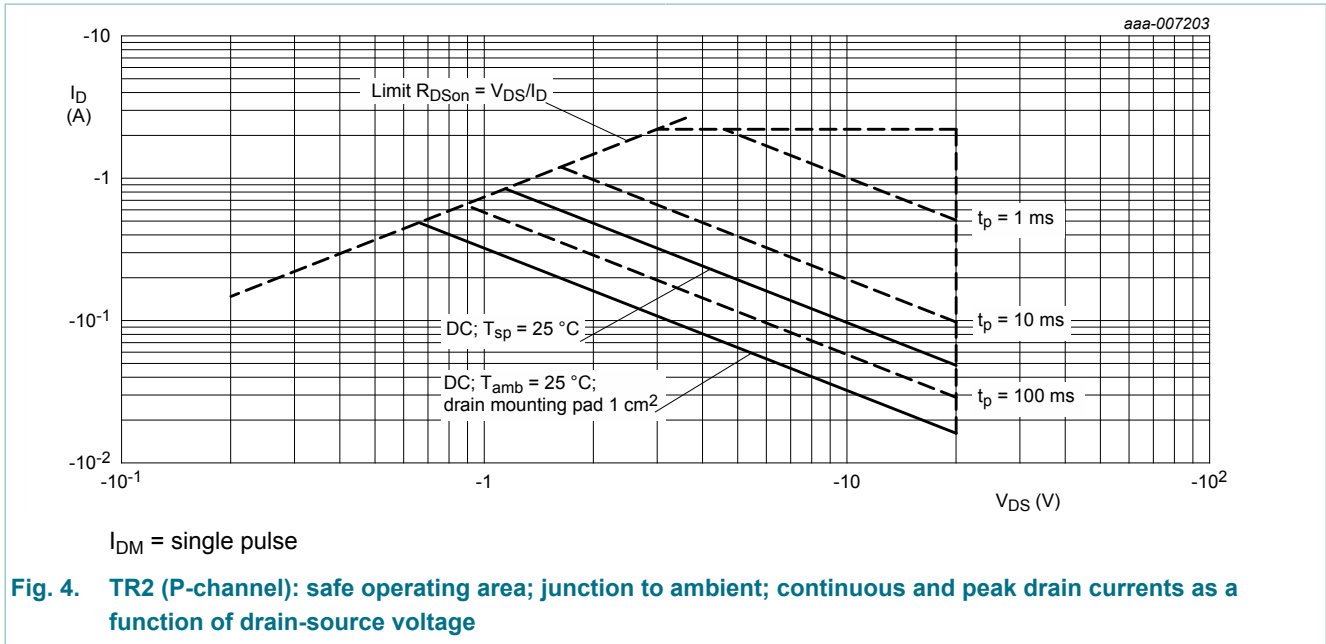
Fig. 2. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100 \%$$



I_{DM} = single pulse

Fig. 3. TR1 (N-channel): safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TR1 (N-channel)							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	390	445	K/W
			[2]	-	340	390	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	-	130	K/W
TR2 (P-channel)							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	390	445	K/W
			[2]	-	340	390	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	-	130	K/W
Per device							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	300	K/W

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper; tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm².

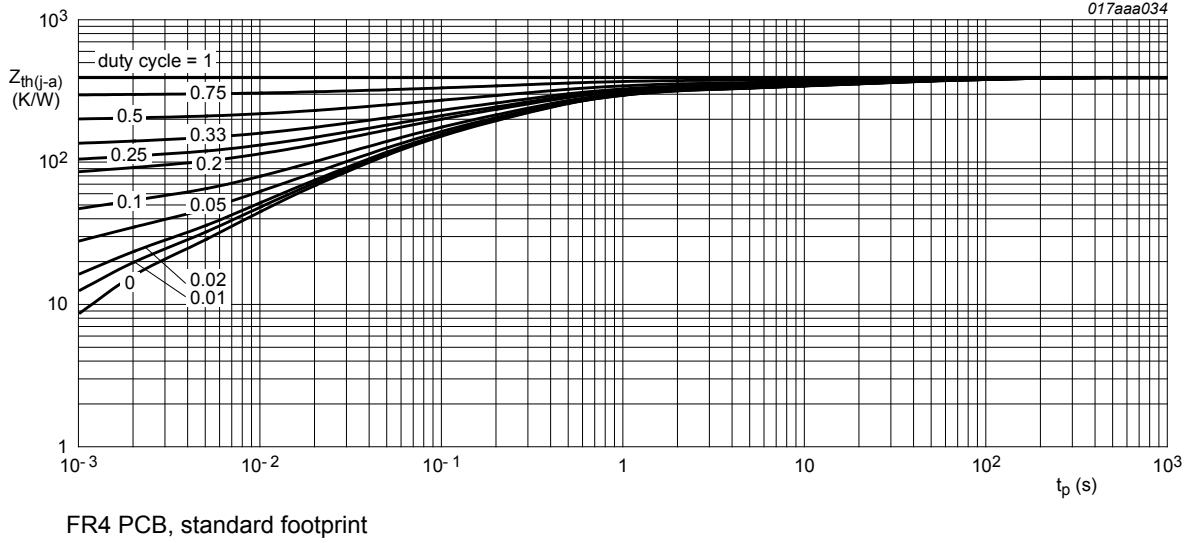


Fig. 5. TR1: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

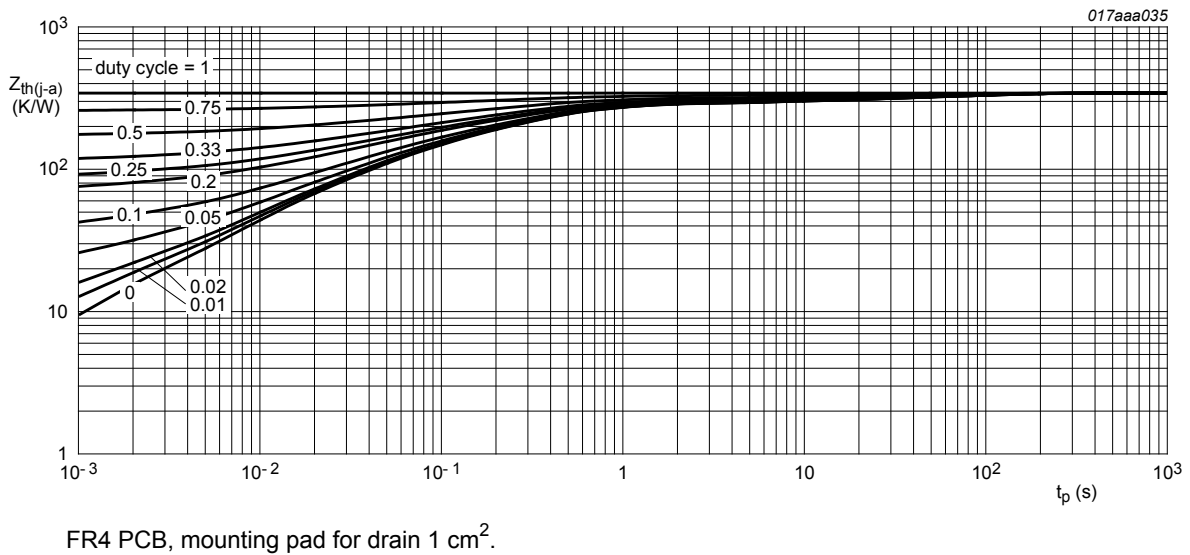
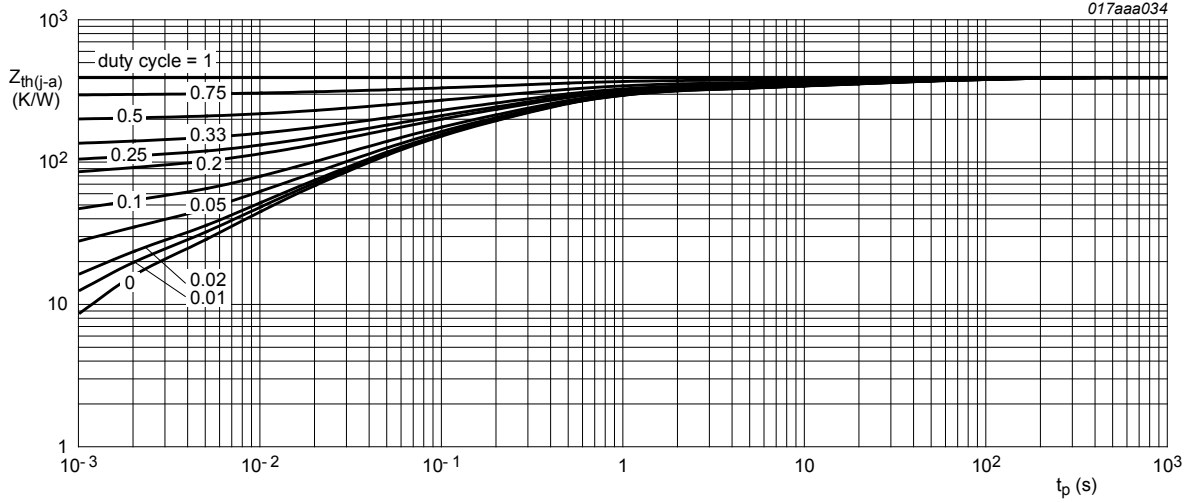
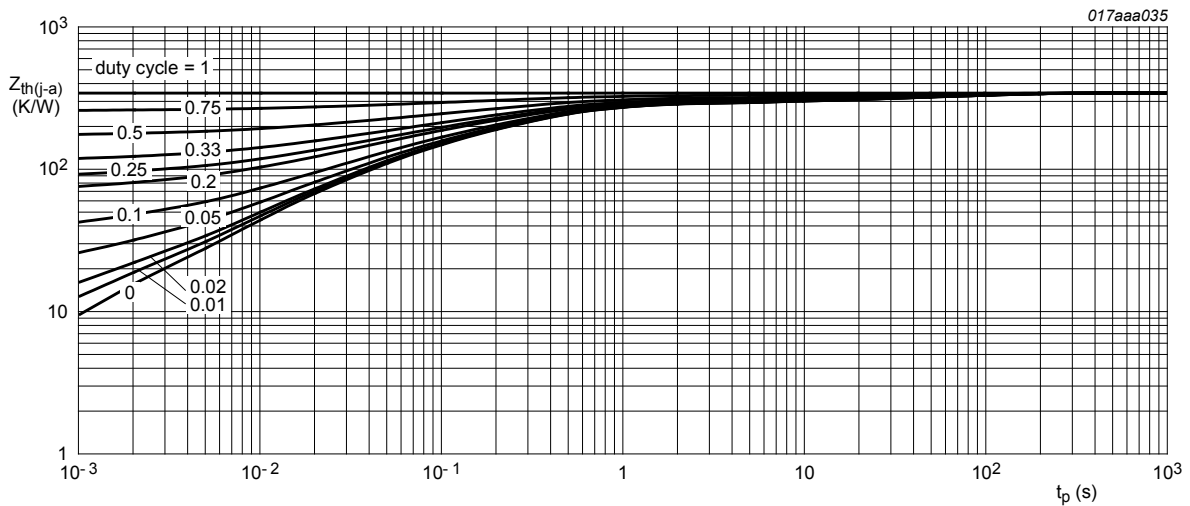


Fig. 6. TR1: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, standard footprint

Fig. 7. TR2: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 1 cm²

Fig. 8. TR2: transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR1 (N-channel), Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	0.5	0.75	0.95	V
I_{DSS}	drain leakage current	$V_{DS} = 20 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{DS} = 20 V; V_{GS} = 0 V; T_j = 150 \text{ }^\circ C$	-	-	10	μA
I_{GSS}	gate leakage current	$V_{GS} = 8 V; V_{DS} = 0 V; -40 \text{ }^\circ C < T_j < 150 \text{ }^\circ C$	-	-	10	μA
		$V_{GS} = -8 V; V_{DS} = 0 V; -40 \text{ }^\circ C < T_j < 150 \text{ }^\circ C$	-	-	-10	μA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 V; I_D = 500 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	290	380	m Ω
		$V_{GS} = 4.5 V; I_D = 500 \text{ mA}; T_j = 150 \text{ }^\circ C$	-	460	610	m Ω
		$V_{GS} = 2.5 V; I_D = 200 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	420	620	m Ω
		$V_{GS} = 1.8 V; I_D = 10 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	0.6	1.1	Ω
g_{fs}	transfer conductance	$V_{DS} = 10 V; I_D = 200 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	1.6	-	S
TR1 (N-channel), Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 10 V; I_D = 500 \text{ mA}; V_{GS} = 4.5 V; T_j = 25 \text{ }^\circ C$	-	0.45	0.68	nC
Q_{GS}	gate-source charge		-	0.15	-	nC
Q_{GD}	gate-drain charge		-	0.15	-	nC
C_{iss}	input capacitance	$V_{DS} = 10 V; f = 1 \text{ MHz}; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	55	83	pF
C_{oss}	output capacitance		-	15	-	pF
C_{rss}	reverse transfer capacitance		-	7	-	pF
$t_{d(on)}$	turn-on delay time		$V_{DS} = 10 V; R_L = 250 \Omega; V_{GS} = 4.5 V; R_{G(ext)} = 6 \Omega; T_j = 25 \text{ }^\circ C$	-	6	12
t_r	rise time	-		4	-	ns
$t_{d(off)}$	turn-off delay time	-		86	172	ns
t_f	fall time	-		31	-	ns
TR1 (N-channel), Source-drain diode characteristics						
V_{SD}	source-drain voltage	$I_S = 300 \text{ mA}; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	0.48	0.77	1.2	V
TR2 (P-channel), Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-20	-	-	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{GSth}	gate-source threshold voltage	$I_D = -250 \mu A$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ }^\circ\text{C}$	-0.5	-0.8	-1.3	V
I_{DSS}	drain leakage current	$V_{DS} = -20 \text{ V}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-1	μA
		$V_{DS} = -20 \text{ V}$; $V_{GS} = 0 \text{ V}$; $T_j = 150 \text{ }^\circ\text{C}$	-	-	-10	μA
I_{GSS}	gate leakage current	$V_{GS} = 8 \text{ V}$; $V_{DS} = 0 \text{ V}$; $-40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$	-	-	10	μA
		$V_{GS} = -8 \text{ V}$; $V_{DS} = 0 \text{ V}$; $-40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$	-	-	-10	μA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}$; $I_D = -400 \text{ mA}$; $T_j = 25 \text{ }^\circ\text{C}$	-	670	850	m Ω
		$V_{GS} = -4.5 \text{ V}$; $I_D = -400 \text{ mA}$; $T_j = 150 \text{ }^\circ\text{C}$	-	1.1	1.4	Ω
		$V_{GS} = -2.5 \text{ V}$; $I_D = -200 \text{ mA}$; $T_j = 25 \text{ }^\circ\text{C}$	-	1.2	1.5	Ω
		$V_{GS} = -1.8 \text{ V}$; $I_D = -10 \text{ mA}$; $T_j = 25 \text{ }^\circ\text{C}$	-	1.8	2.8	Ω
g_{fs}	transfer conductance	$V_{DS} = -10 \text{ V}$; $I_D = -200 \text{ mA}$; $T_j = 25 \text{ }^\circ\text{C}$	-	610	-	mS
TR2 (P-channel), Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -10 \text{ V}$; $I_D = -400 \text{ mA}$; $V_{GS} = -4.5 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	0.76	1.14	nC
Q_{GS}	gate-source charge		-	0.28	-	nC
Q_{GD}	gate-drain charge		-	0.18	-	nC
C_{iss}	input capacitance	$V_{DS} = -10 \text{ V}$; $f = 1 \text{ MHz}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	58	87	pF
C_{oss}	output capacitance		-	21	-	pF
C_{rss}	reverse transfer capacitance		-	12	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -10 \text{ V}$; $R_L = 250 \text{ }^\circ\Omega$; $V_{GS} = -4.5 \text{ V}$; $R_{G(ext)} = 6 \text{ }^\circ\Omega$; $T_j = 25 \text{ }^\circ\text{C}$	-	18	36	ns
t_r	rise time		-	30	-	ns
$t_{d(off)}$	turn-off delay time		-	80	160	ns
t_f	fall time		-	72	-	ns
TR2 (P-channel), Source-drain diode characteristics						
V_{SD}	source-drain voltage	$I_S = -300 \text{ mA}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-0.48	-0.84	-1.2	V

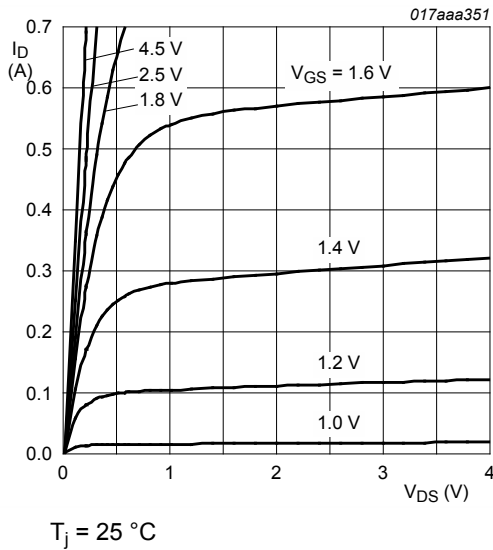


Fig. 9. TR1; Output characteristics: drain current as a function of drain-source voltage; typical values

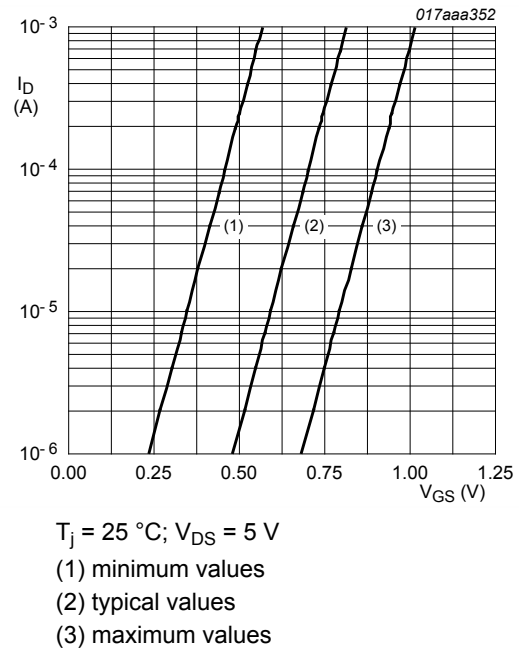


Fig. 10. TR1; Sub-threshold drain current as a function of gate-source voltage

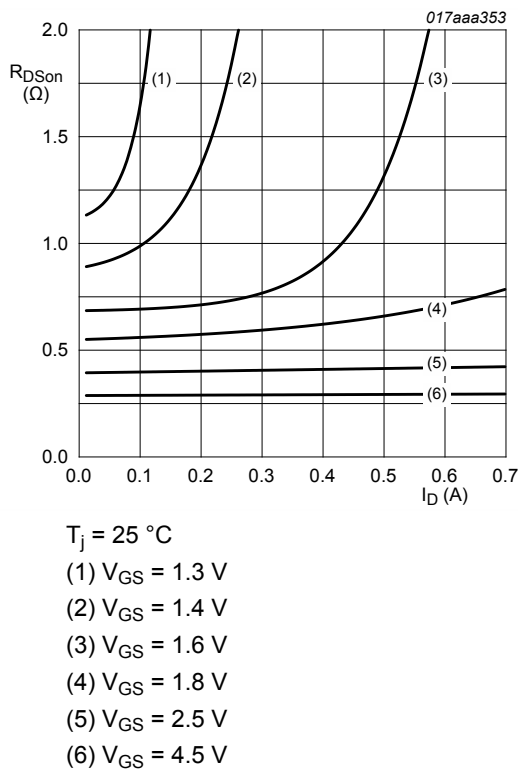


Fig. 11. TR1; Drain-source on-state resistance as a function of drain current; typical values

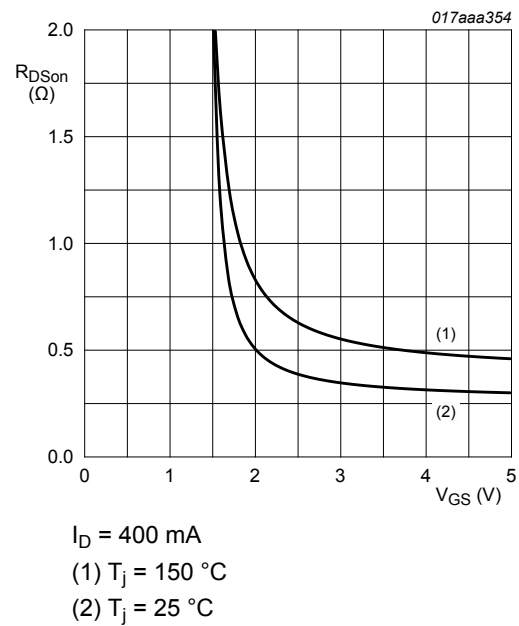
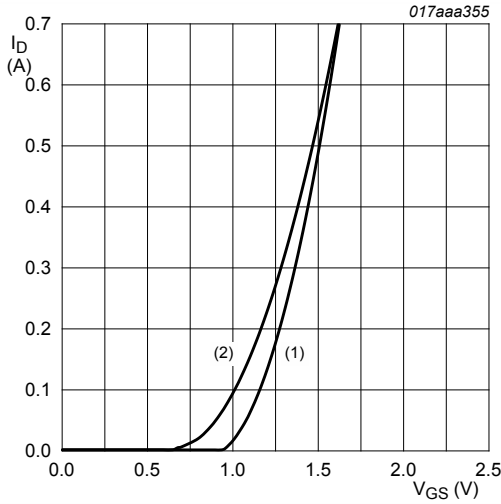


Fig. 12. TR1; Drain-source on-state resistance as a function of gate-source voltage; typical values



$V_{DS} > I_D \times R_{DSon}$
 (1) $T_j = 25\text{ °C}$
 (2) $T_j = 150\text{ °C}$

Fig. 13. TR1; Transfer characteristics: drain current as a function of gate-source voltage; typical values

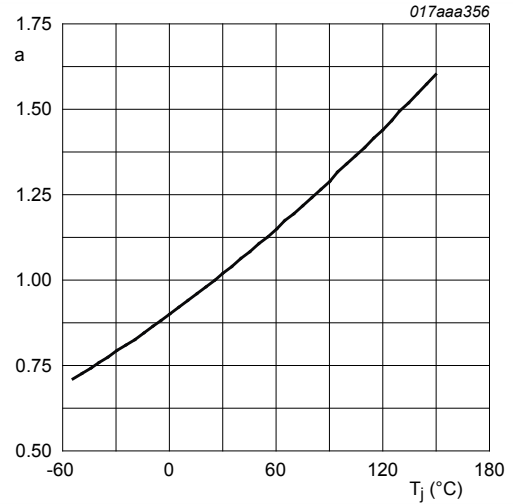
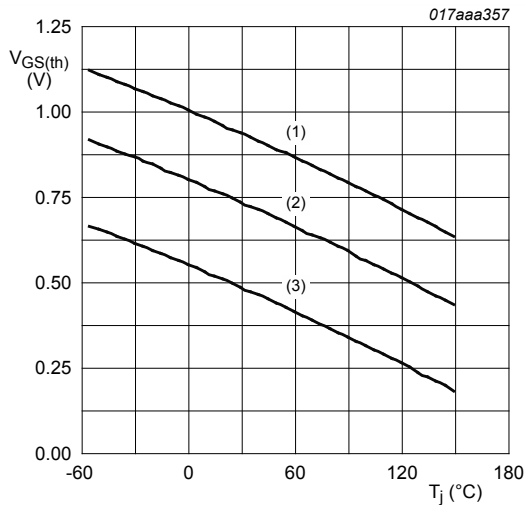


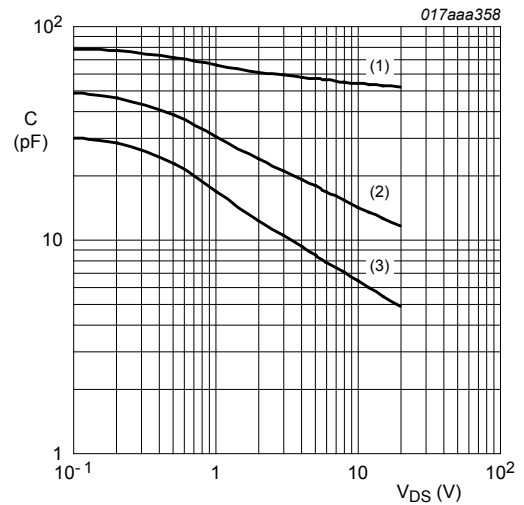
Fig. 14. TR1; Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$



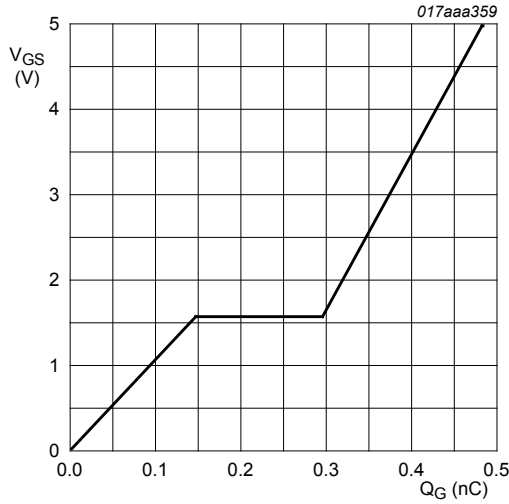
$I_D = 0.25\text{ mA}; V_{DS} = V_{GS}$
 (1) maximum values
 (2) typical values
 (3) minimum values

Fig. 15. TR1; Gate-source threshold voltage as a function of junction temperature



$f = 1\text{ MHz}; V_{GS} = 0\text{ V}$
 (1) C_{iss}
 (2) C_{oss}
 (3) C_{rss}

Fig. 16. TR1; Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = 0.5 \text{ A}; V_{DS} = 10 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 17. TR1; Gate-source voltage as a function of gate charge; typical values

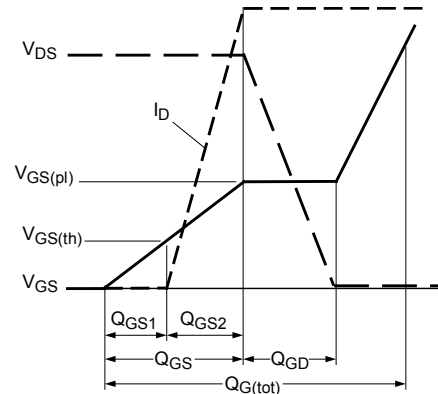
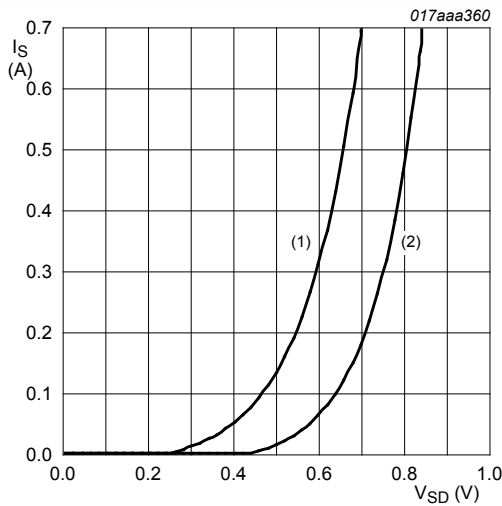
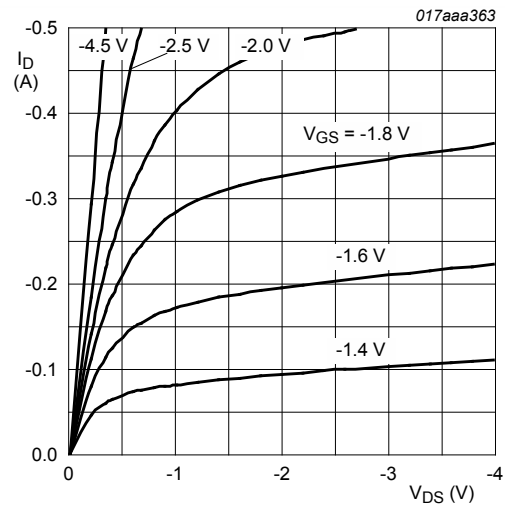


Fig. 18. Gate charge waveform definitions



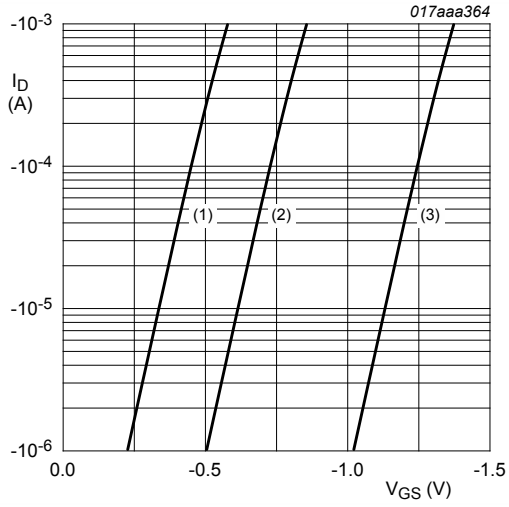
$V_{GS} = 0 \text{ V}$
 (1) $T_j = 150 \text{ }^\circ\text{C}$
 (2) $T_j = 25 \text{ }^\circ\text{C}$

Fig. 19. TR1; Source current as a function of source-drain voltage; typical values



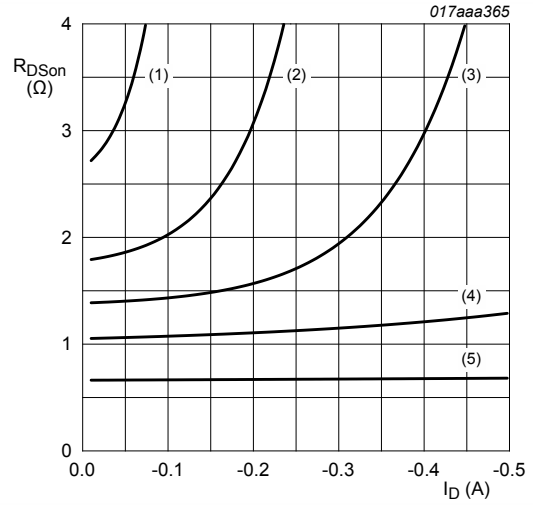
$T_j = 25 \text{ }^\circ\text{C}$

Fig. 20. TR2; Output characteristics: drain current as a function of drain-source voltage; typical values



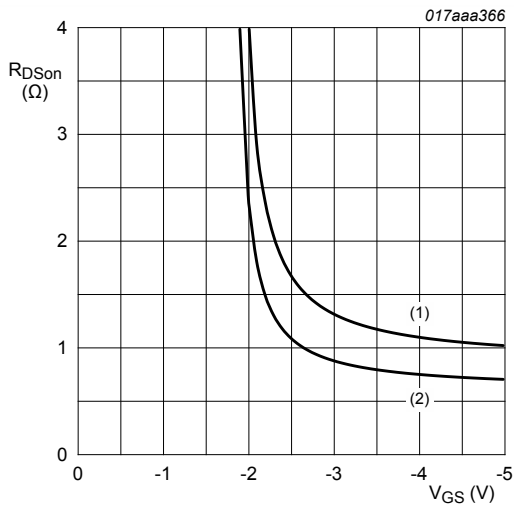
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = -5\text{ V}$
 (1) minimum values
 (2) typical values
 (3) maximum values

Fig. 21. TR2; Sub-threshold drain current as a function of gate-source voltage



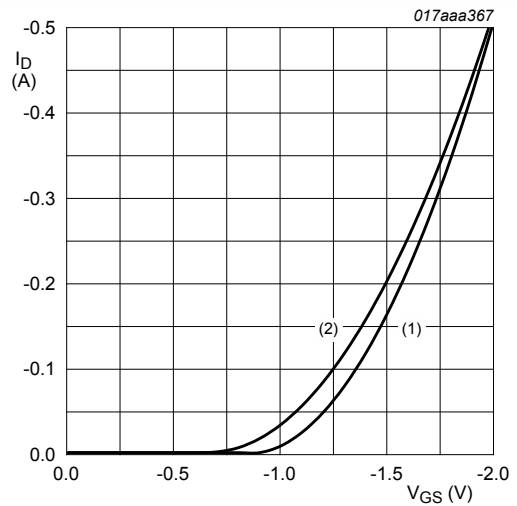
$T_j = 25\text{ }^\circ\text{C}$
 (1) $V_{GS} = -1.5\text{ V}$
 (2) $V_{GS} = -1.8\text{ V}$
 (3) $V_{GS} = -2.0\text{ V}$
 (4) $V_{GS} = -2.5\text{ V}$
 (5) $V_{GS} = -4.5\text{ V}$

Fig. 22. TR2; Drain-source on-state resistance as a function of drain current; typical values



$I_D = -400\text{ mA}$
 (1) $T_j = 150\text{ }^\circ\text{C}$
 (2) $T_j = 25\text{ }^\circ\text{C}$

Fig. 23. TR2; Drain-source on-state resistance as a function of gate-source voltage; typical values



$V_{DS} > I_D \times R_{DSon}$
 (1) $T_j = 25\text{ }^\circ\text{C}$
 (2) $T_j = 150\text{ }^\circ\text{C}$

Fig. 24. TR2; Transfer characteristics: drain current as a function of gate-source voltage; typical values

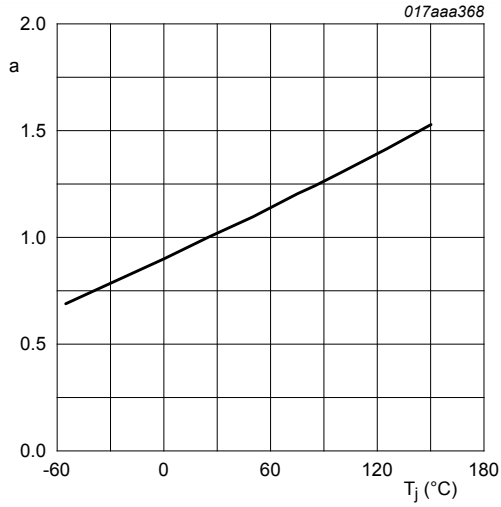
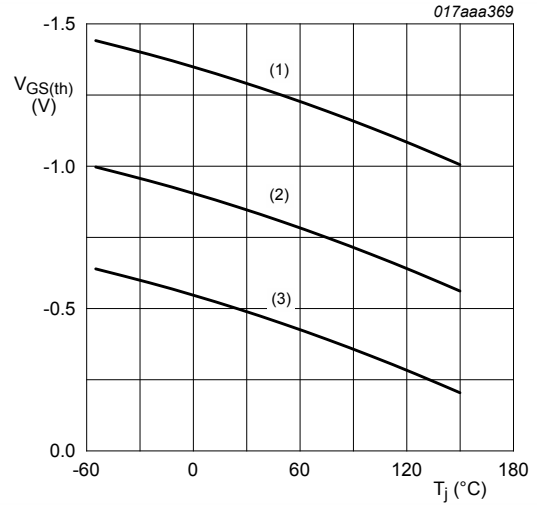


Fig. 25. TR2; Normalized drain-source on-state resistance as a function of ambient temperature; typical values

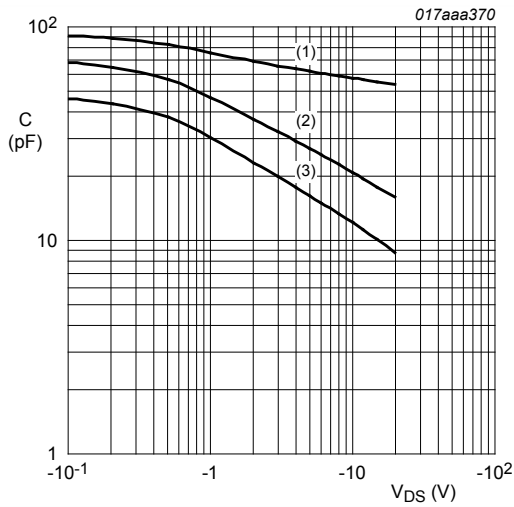
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$



$I_D = -0.25 \text{ mA}; V_{DS} = V_{GS}$

- (1) maximum values
- (2) typical values
- (3) minimum values

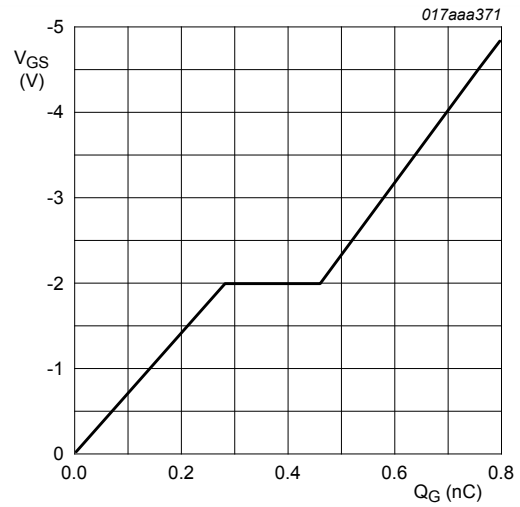
Fig. 26. TR2; Gate-source threshold voltage as a function of junction temperature



$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$

- (1) C_{iss}
- (2) C_{oss}
- (3) C_{rss}

Fig. 27. TR2; Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = -0.4 \text{ A}; V_{DD} = -10 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 28. TR2; Gate-source voltage as a function of gate charge; typical values

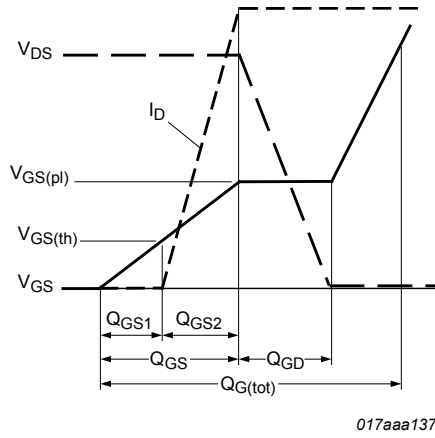
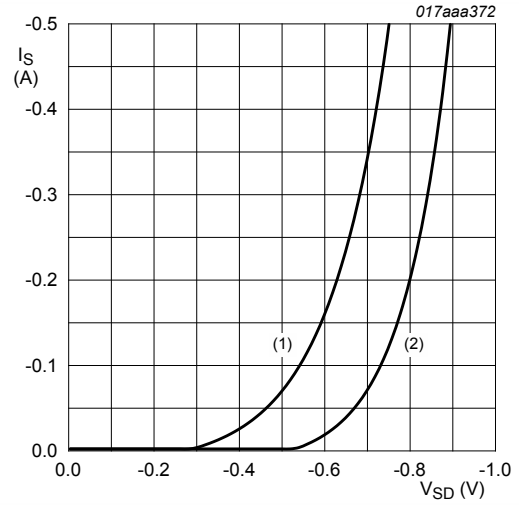


Fig. 29. Gate charge waveform definitions



$V_{GS} = 0\text{ V}$
 (1) $T_{amb} = 150\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$

Fig. 30. TR2; Source current as a function of source-drain voltage; typical values

11. Test information

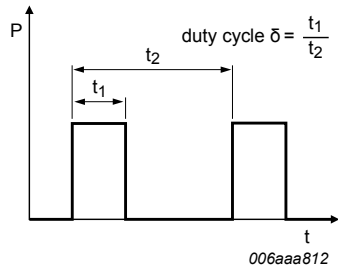


Fig. 31. Duty cycle definition

11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

12. Package outline

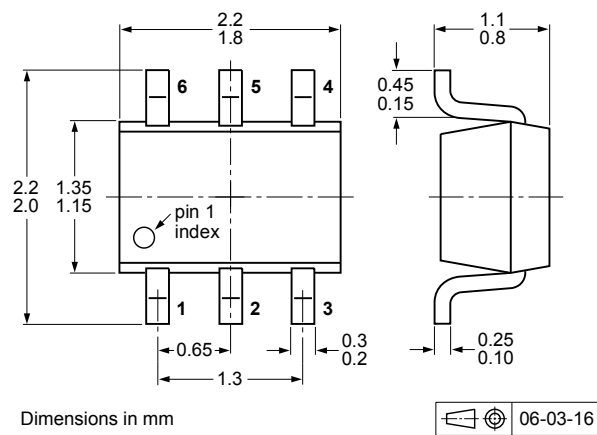


Fig. 32. Package outline TSSOP6 (SOT363)

13. Soldering

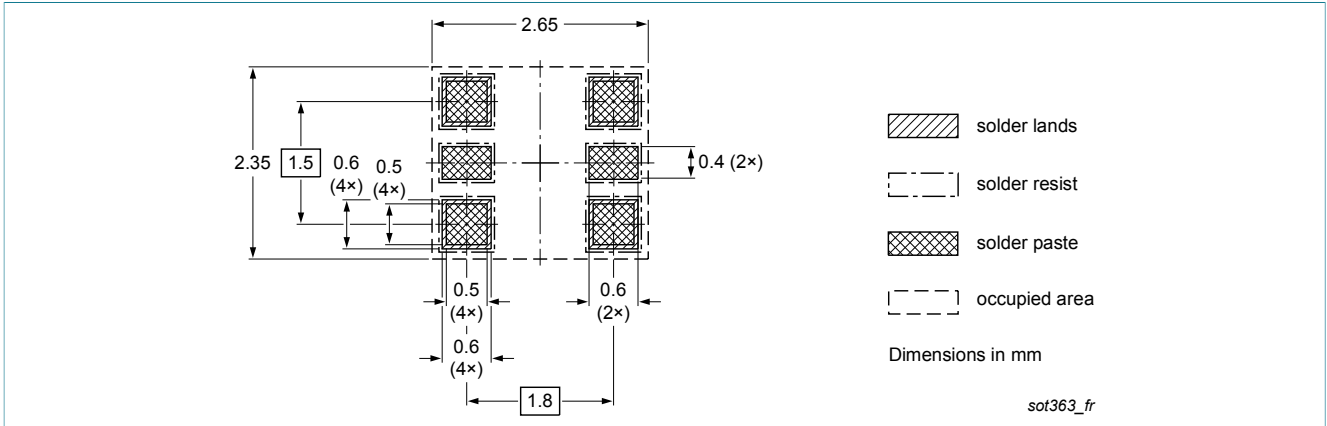


Fig. 33. Reflow soldering footprint for TSSOP6 (SOT363)

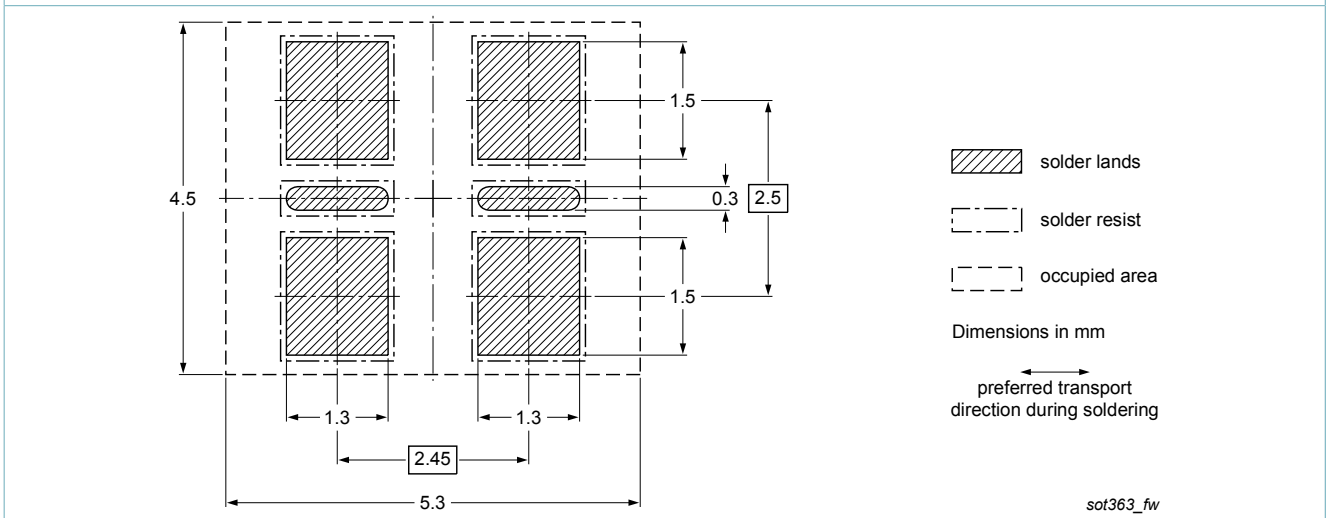


Fig. 34. Wave soldering footprint for TSSOP6 (SOT363)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMGD290UCEA v.3	20140328	Product data sheet	-	PMGD290UCEA v.2
Modifications:	• Table 7: I _{GSS} parameter unit corrected			
PMGD290UCEA v.2	20130418	Product data sheet	-	PMGD290UCEA v.1
PMGD290UCEA v.1	20130415	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

15.2 Definitions

Preview — The document is a preview version only. The document is still subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

15.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Adelante, Bitport, Bitsound, CoolFlux, CoReUse, DESFire, EZ-HV, FabKey, GreenChip, HiPerSmart, HITAG, I²C-bus logo, ICODE, I-CODE, ITEC, Labelution, MIFARE, MIFARE Plus, MIFARE Ultralight, MoReUse, QLPAK, Silicon Tuner, SiliconMAX, SmartXA, STARplug, TOPFET, TrenchMOS, TriMedia and UCODE — are trademarks of NXP Semiconductors N.V.

HD Radio and **HD Radio** logo — are trademarks of iBiquity Digital Corporation.

16. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Quick reference data	1
5	Pinning information	2
6	Ordering information	2
7	Marking	2
8	Limiting values	2
9	Thermal characteristics	5
10	Characteristics	8
11	Test information	16
11.1	Quality information	16
12	Package outline	16
13	Soldering	17
14	Revision history	18
15	Legal information	19
15.1	Data sheet status	19
15.2	Definitions	19
15.3	Disclaimers	19
15.4	Trademarks	20

© NXP Semiconductors N.V. 2014. All rights reserved

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 28 March 2014