

PMN27UN

TrenchMOS™ ultra low level FET

Rev. 01 — 27 September 2002

Product data

1. Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PMN27UN in SOT457 (TSOP6).

2. Features

- TrenchMOS™ technology
- Very fast switching
- Low threshold voltage
- Surface mount package.

3. Applications

- Battery powered motor control
- Load switch in notebook computers
- High speed switch in set top box power supplies
- Driver FET in DC to DC converters.

4. Pinning information

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Table 1: Pinning - SOT457 (TSOP6), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,5,6	drain (d)	Top view MBK092 SOT457 (TSOP6)	MBB076
3	gate (g)		
4	source (s)		

5. Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	20	V
I_D	drain current (DC)	$T_{sp} = 25\text{ °C}; V_{GS} = 4.5\text{ V}$	-	5.7	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$	-	1.75	W
T_j	junction temperature		-	150	°C
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 2\text{ A}; T_j = 25\text{ °C}$	27	34	mΩ
		$V_{GS} = 2.5\text{ V}; I_D = 2\text{ A}; T_j = 25\text{ °C}$	32	40	mΩ
		$V_{GS} = 1.8\text{ V}; I_D = 1.5\text{ A}; T_j = 25\text{ °C}$	39	56	mΩ

6. Limiting values

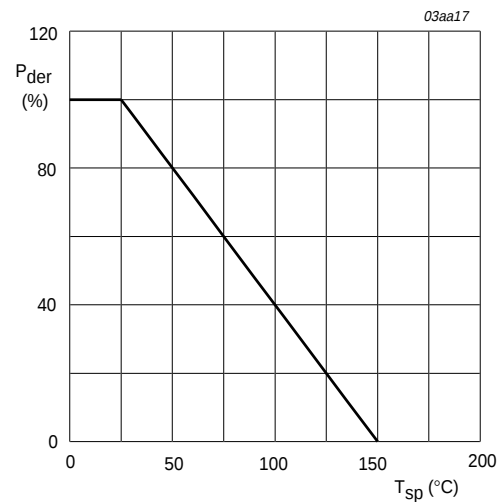
Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	20	V
V_{GS}	gate-source voltage (DC)		-	±8	V
I_D	drain current (DC)	$T_{sp} = 25\text{ °C}; V_{GS} = 4.5\text{ V}; \text{Figure 2 and 3}$	-	5.7	A
		$T_{sp} = 70\text{ °C}; V_{GS} = 4.5\text{ V}; \text{Figure 2}$	-	4.5	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}; \text{pulsed}; t_p \leq 10\text{ }\mu\text{s}; \text{Figure 3}$	-	22.9	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}; \text{Figure 1}$	-	1.75	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C

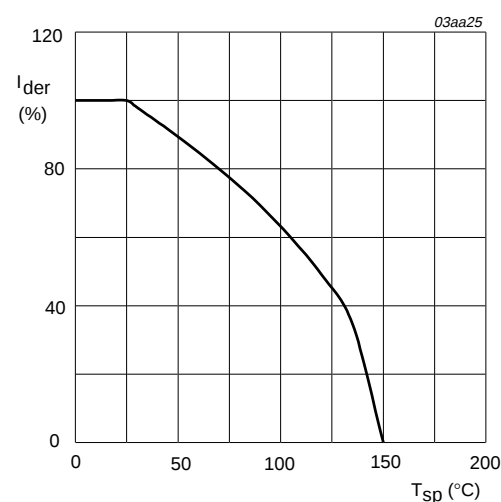
Source-drain diode

I_S	source (diode forward) current (DC)	$T_{sp} = 25\text{ °C}$	-	1.45	A
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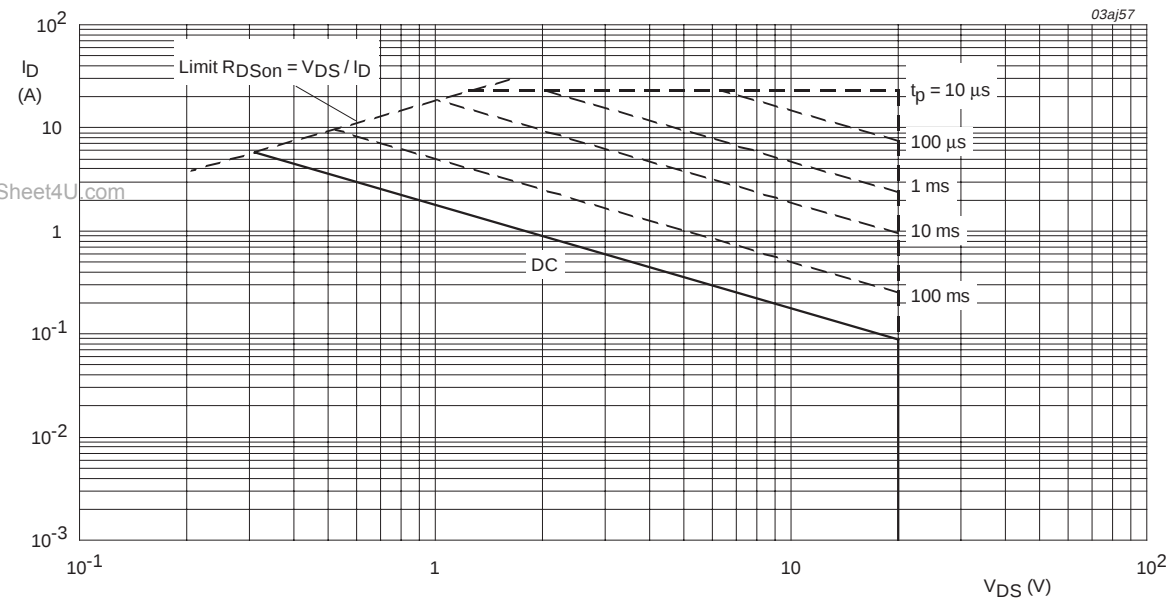
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



$T_{sp} = 25$ °C; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	mounted on a metal clad board; Figure 4	-	-	70	K/W

7.1 Transient thermal impedance

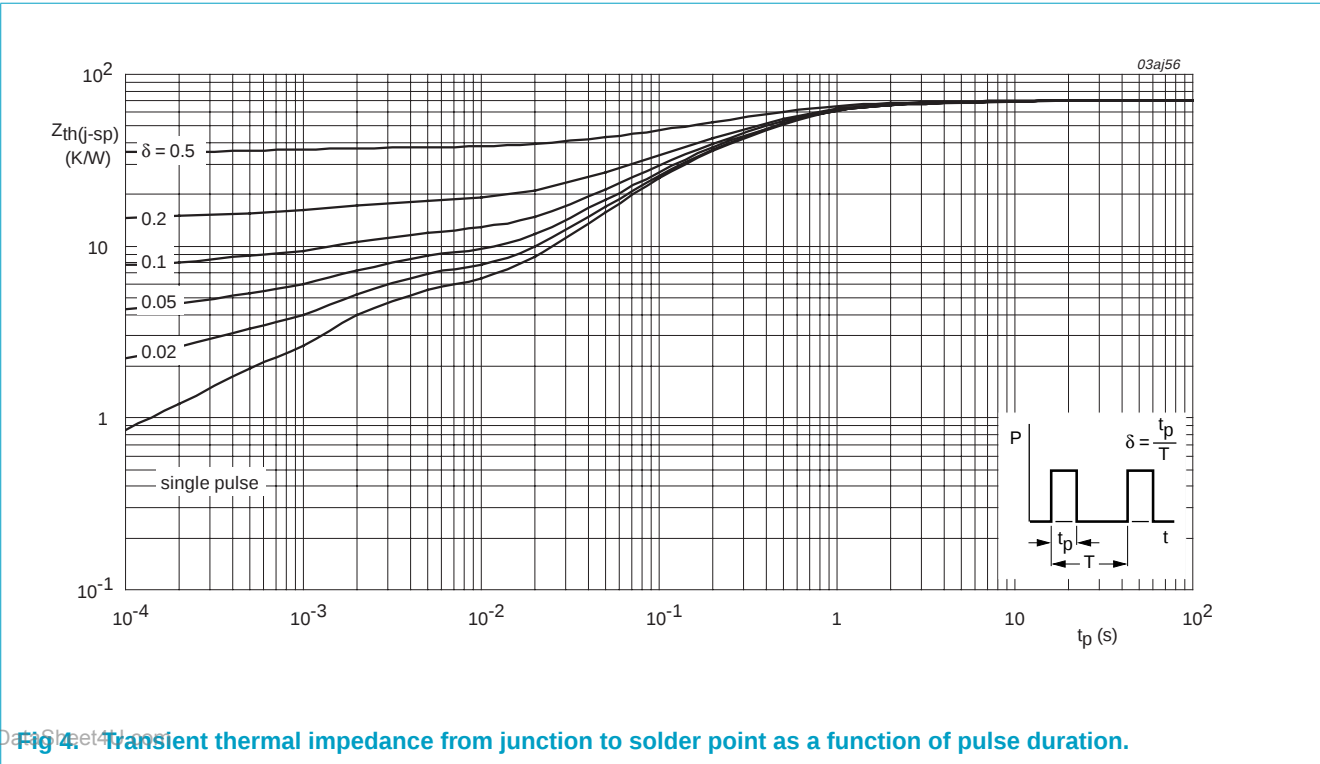


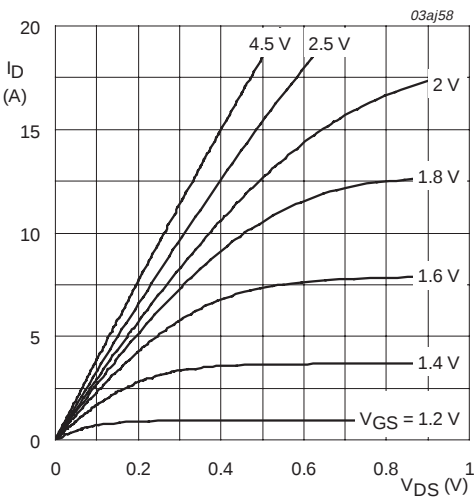
Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration.

8. Characteristics

Table 5: Characteristics

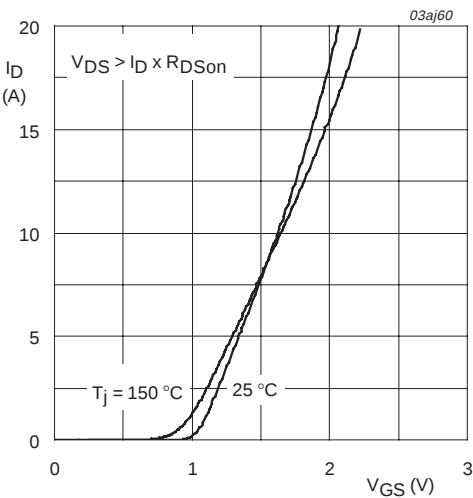
$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V	20	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; Figure 9	0.4	0.7	-	V
I _{DSS}	drain-source leakage current	V _{DS} = 16 V; V _{GS} = 0 V				
		T _j = 25 °C	-	0.01	1.0	μA
		T _j = 55 °C	-	-	10	μA
I _{GSS}	gate-source leakage current	V _{GS} = ±8 V; V _{DS} = 0 V	-	10	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 2 A; Figure 7 and 8	-	27	34	mΩ
		V _{GS} = 2.5 V; I _D = 2 A; Figure 7 and 8	-	32	40	mΩ
		V _{GS} = 1.8 V; I _D = 1.5 A; Figure 7 and 8	-	39	56	mΩ
Dynamic characteristics						
Q _{g(tot)}	total gate charge	V _{DD} = 10 V; V _{GS} = 4.5 V; I _D = 3.8 A; Figure 13	-	10.6	-	nC
Q _{gs}	gate-source charge		-	1.8	-	nC
Q _{gd}	gate-drain (Miller) charge		-	2.1	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 10 V; f = 1 MHz; Figure 11	-	740	-	pF
C _{oss}	output capacitance		-	185	-	pF
C _{rss}	reverse transfer capacitance		-	125	-	pF
t _{d(on)}	turn-on delay time	V _{DD} = 10 V; R _D = 10 Ω; V _{GS} = 4.5 V; R _G = 6 Ω	-	8.5	-	ns
t _r	rise time		-	14.5	-	ns
t _{d(off)}	turn-off delay time		-	55	-	ns
t _f	fall time		-	16	-	ns
Source-drain diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 1.7 A; V _{GS} = 0 V; Figure 12	-	0.8	1.2	V



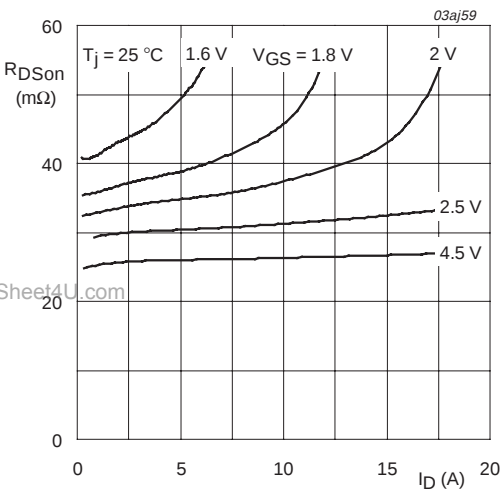
$T_J = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



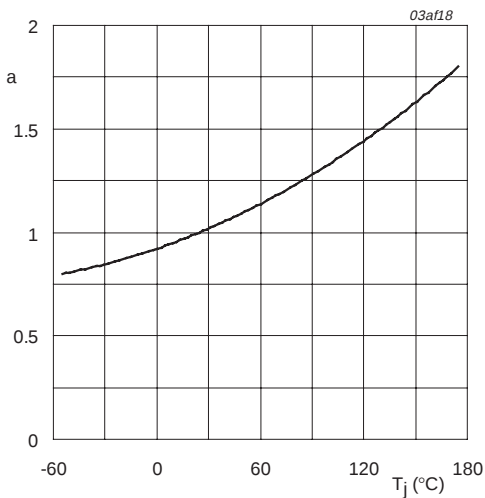
$T_J = 25^\circ\text{C}$ and 150°C ; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



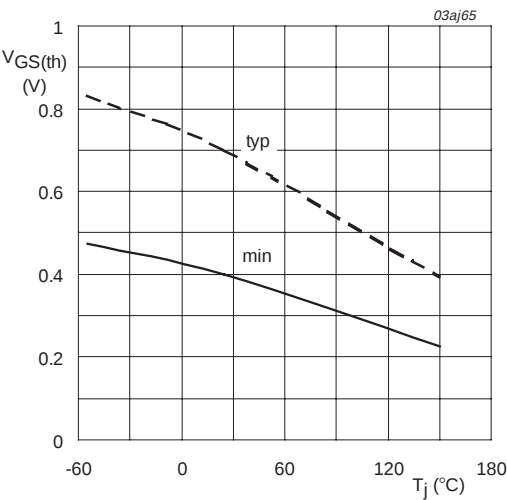
$T_J = 25^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



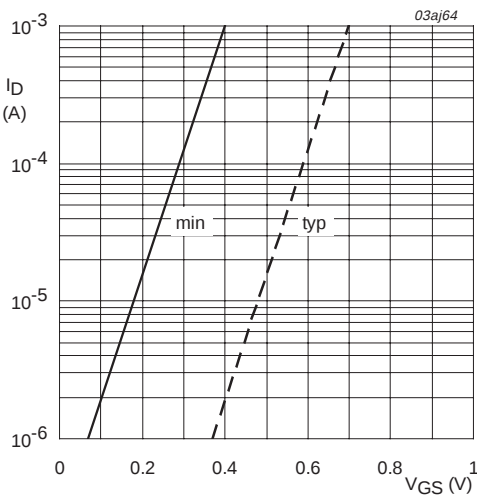
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



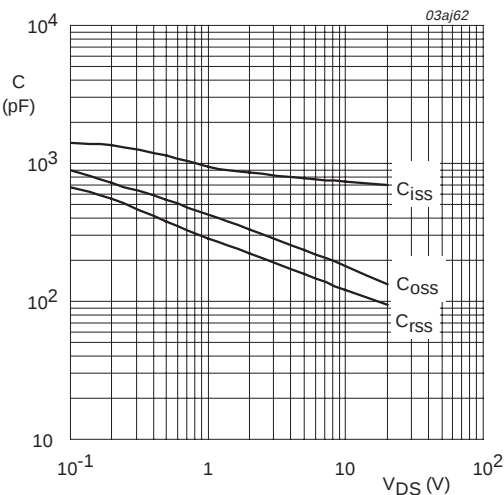
$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



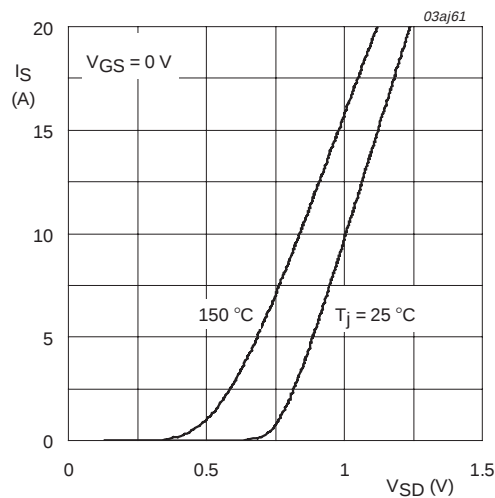
$T_j = 25 \text{ °C}$; $V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



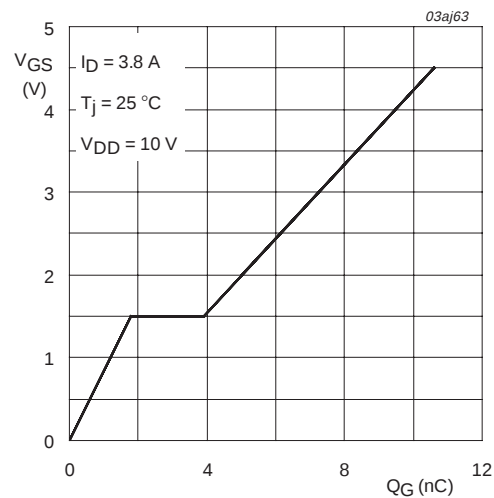
$V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25$ °C and 150 °C; $V_{GS} = 0$ V

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



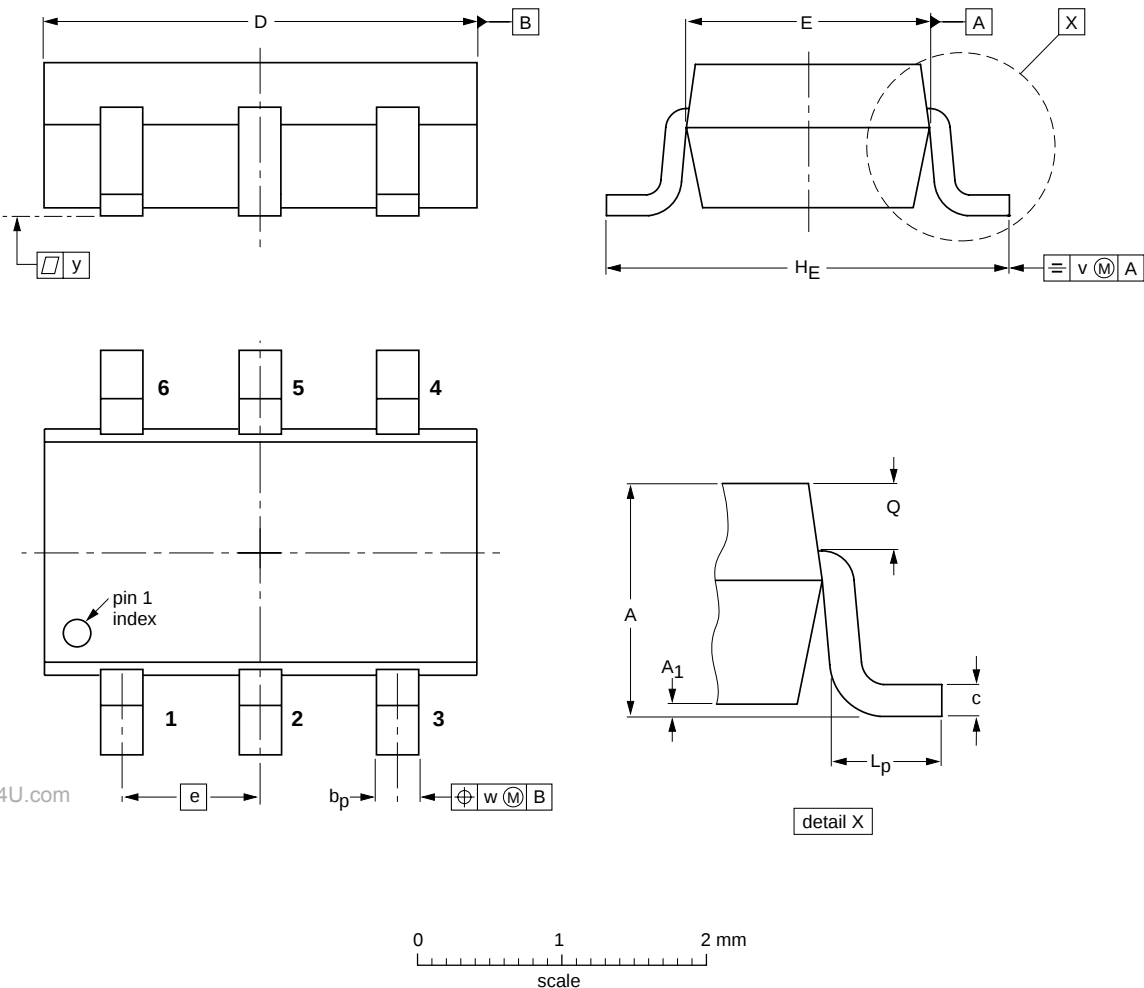
$I_D = 3.8$ A; $V_{DD} = 10$ V

Fig 13. Gate-source voltage as a function of gate charge; typical values.

9. Package outline

Plastic surface mounted package; 6 leads

SOT457



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b _p	c	D	E	e	H _E	L _p	Q	v	w	y
mm	1.1 0.9	0.1 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT457			SC-74			-97-02-28 01-05-04

Fig 14. SOT457 (TSOP6).

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20020927	-	Product data (9397 750 10189)

11. Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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