**Product data sheet** 

## 1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a small SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

### 2. Features and benefits

- Trench MOSFET technology
- Low threshold voltage
- Very fast switching
- Enhanced power dissipation capability of 1240 mW
- ElectroStatic Discharge (ESD) protection > 1 kV HBM

## 3. Applications

- LED driver
- Power management
- Low-side loadswitch
- Switching circuits

### 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C		-	-	20	V
$V_{GS}$	gate-source voltage			-8	-	8	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 4.5 V; T <sub>amb</sub> = 25 °C; t ≤ 5 s	[1]	-	-	6	Α
Static characteristics							,
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 4.8 \text{ A}; T_j = 25 ^{\circ}\text{C}$		-	28	36	mΩ

<sup>[1]</sup> Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.



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# 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	<u> </u>	D I
2	D	drain		
3	G	gate	1 12 13	G T
4	S	source	TSOP6 (SOT457)	
5	D	drain		
6	D	drain		S 017aaa255

# 6. Ordering information

Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
PMN30UNE	TSOP6	plastic surface-mounted package (TSOP6); 6 leads	SOT457			

# 7. Marking

Table 4. Marking codes

Type number	Marking code
PMN30UNE	G8

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## 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C		-	20	V
$V_{GS}$	gate-source voltage			-8	8	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 4.5 V; T <sub>amb</sub> = 25 °C; t ≤ 5 s	[1]	-	6	Α
		V <sub>GS</sub> = 4.5 V; T <sub>amb</sub> = 25 °C	[1]	-	4.8	Α
		V <sub>GS</sub> = 4.5 V; T <sub>amb</sub> = 100 °C	[1]	-	3	Α
I <sub>DM</sub>	peak drain current	$T_{amb}$ = 25 °C; single pulse; $t_p \le 10 \mu s$		-	19	Α
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[2]	-	530	mW
			[1]	-	1.24	W
		T <sub>sp</sub> = 25 °C		-	4.46	W
T <sub>j</sub>	junction temperature			-55	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C
Source-dra	in diode		1		1	
Is	source current	T <sub>amb</sub> = 25 °C	[1]	-	1.2	Α
		I				

- Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

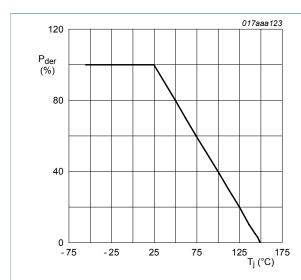


Fig. 1. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

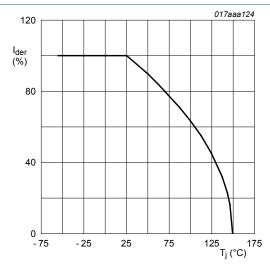


Fig. 2. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100 \%$$

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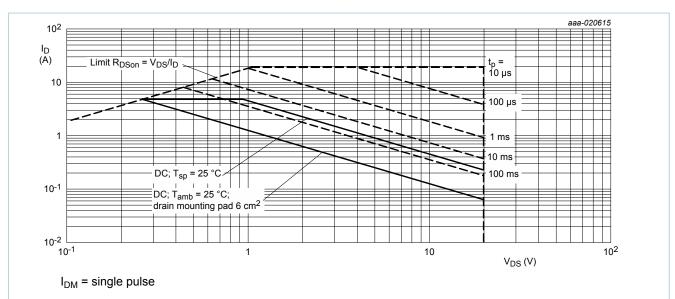


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

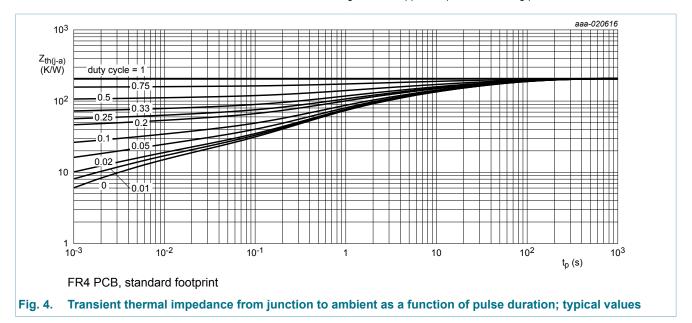
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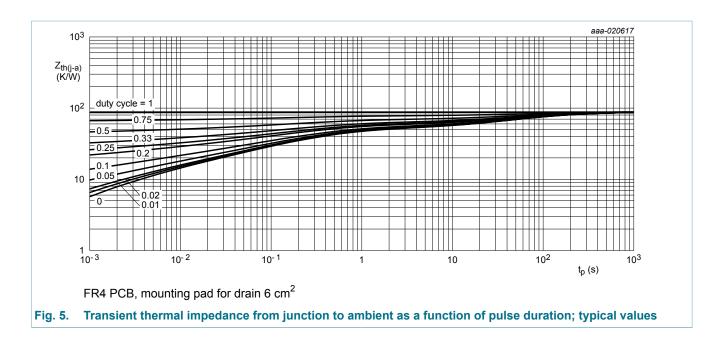
### 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
R <sub>th(j-a)</sub> thermal resistar from junction to ambient	thermal resistance		[1]	-	205	235	K/W
			[2]	-	88	101	K/W
	ambient	in free air; t ≤ 5 s	[2]	-	55	63	K/W
R <sub>th(j-sp)</sub>	thermal resistance from junction to solder point			-	24	28	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.





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## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	racteristics					
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	20	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ °C}$	0.4	0.65	0.9	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	1	μΑ
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 8 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	10	μA
		V <sub>GS</sub> = -8 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	-10	μA
		V <sub>GS</sub> = 4.5 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	2	μA
		V <sub>GS</sub> = -4.5 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	-2	μA
		V <sub>GS</sub> = 2.5 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	200	nA
		V <sub>GS</sub> = -2.5 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	-200	nA
R <sub>DSon</sub>	drain-source on-state	$V_{GS}$ = 4.5 V; $I_D$ = 4.8 A; $T_j$ = 25 °C	-	28	36	mΩ
	resistance	V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 4.8 A; T <sub>j</sub> = 150 °C	-	43	55	mΩ
		V <sub>GS</sub> = 2.5 V; I <sub>D</sub> = 4.2 A; T <sub>j</sub> = 25 °C	-	38	47	mΩ
		V <sub>GS</sub> = 1.8 V; I <sub>D</sub> = 0.9 A; T <sub>j</sub> = 25 °C	-	42	60	mΩ
		V <sub>GS</sub> = 1.5 V; I <sub>D</sub> = 0.1 A; T <sub>j</sub> = 25 °C	-	52	105	mΩ
g <sub>fs</sub>	forward transconductance	$V_{DS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ °C}$	-	19	-	S
$R_G$	gate resistance	f = 1 MHz; T <sub>j</sub> = 25 °C	-	0.8	-	Ω
Dynamic o	haracteristics			'	'	,
Q <sub>G(tot)</sub>	total gate charge	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 4.8 A; V <sub>GS</sub> = 4.5 V;	-	5.1	9	nC
$Q_{GS}$	gate-source charge	T <sub>j</sub> = 25 °C	-	0.6	-	nC
$Q_{GD}$	gate-drain charge		-	0.9	-	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 10 V; f = 1 MHz; V <sub>GS</sub> = 0 V;	-	558	-	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C	-	56	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	45	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 4.8 A; V <sub>GS</sub> = 4.5 V;	-	5.5	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 6 \Omega; T_j = 25 °C$	-	24	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	22	-	ns
t <sub>f</sub>	fall time		-	6	-	ns

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Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Source-drain diode							
$V_{SD}$	source-drain voltage	$I_S = 1.2 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}$		-	0.7	1.2	V

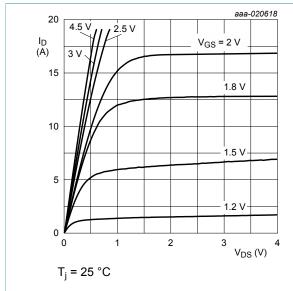


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

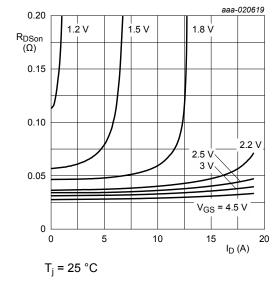


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

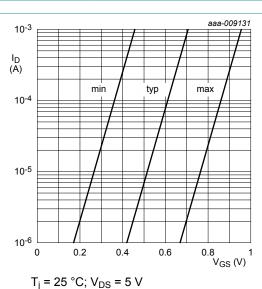


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

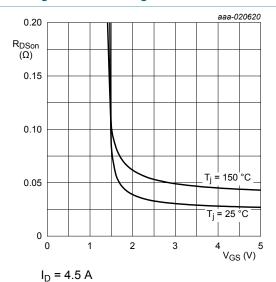


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

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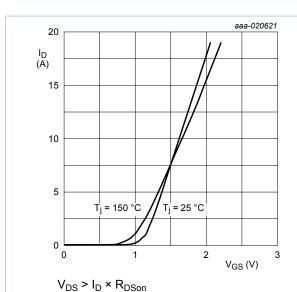


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

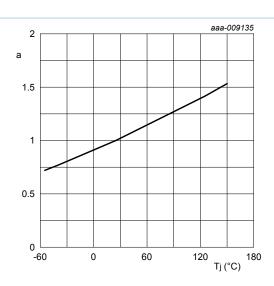


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

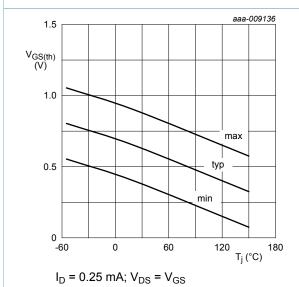


Fig. 12. Gate-source threshold voltage as a function of junction temperature

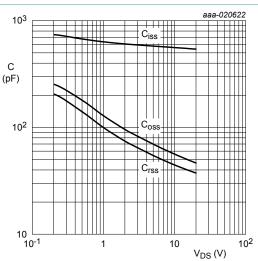


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

 $f = 1 MHz; V_{GS} = 0 V$ 

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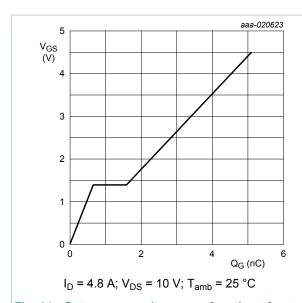


Fig. 14. Gate-source voltage as a function of gate charge; typical values

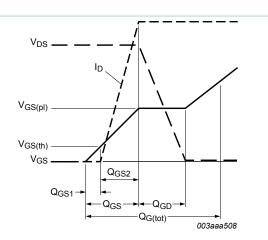


Fig. 15. MOSFET transistor: Gate charge waveform definitions

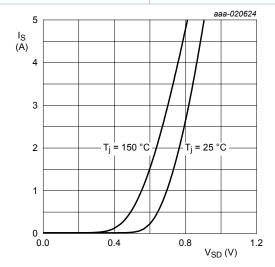
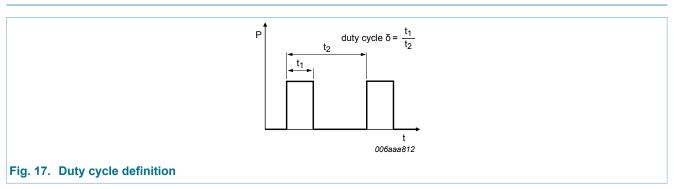


Fig. 16. Source current as a function of source-drain voltage; typical values

### 11. Test information

 $V_{GS} = 0 V$ 



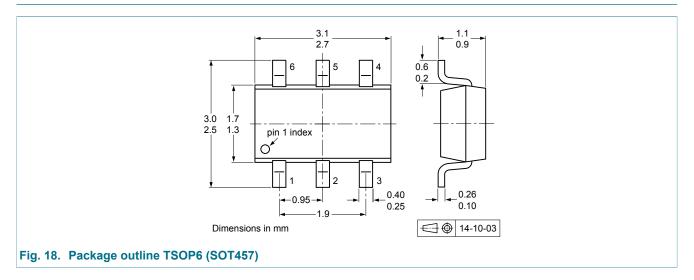
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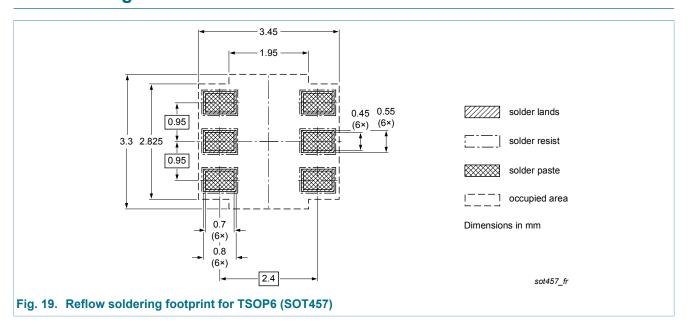
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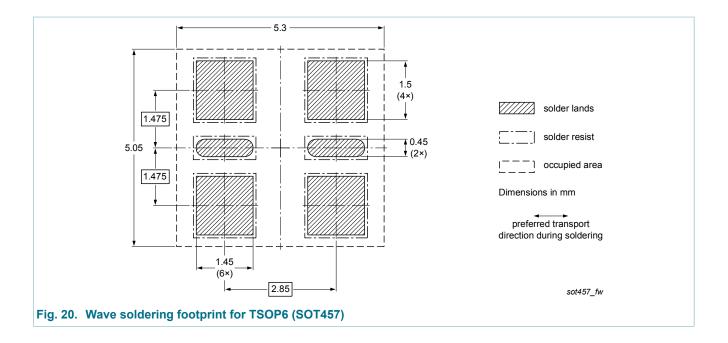
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# 12. Package outline



# 13. Soldering





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# 14. Revision history

### Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMN30UNE v.1	20160129	Product data sheet	-	-

#### 20 V, N-channel Trench MOSFET

### 15. Legal information

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Document status [1][2]	Product status [3]	Definition
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