

PMN50XP

P-channel TrenchMOS extremely low level FET

Rev. 01 — 23 January 2006

Product data sheet

1. Product profile

1.1 General description

P-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

1.2 Features

- Low threshold voltage
- Low on-state losses

1.3 Applications

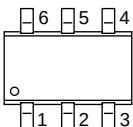
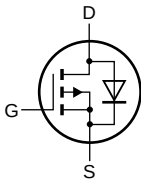
- Low power DC-to-DC converters
- Battery management
- Load switching
- Battery powered portable equipment

1.4 Quick reference data

- $V_{DS} \leq -20 \text{ V}$
- $I_D \leq -4.8 \text{ A}$
- $R_{DS(on)} \leq 60 \text{ m}\Omega$
- $Q_{GD} = 1.3 \text{ nC (typ)}$

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1, 2, 5, 6	drain (D)	 SOT457 (TSOP6)	
3	gate (G)		
4	source (S)		

003aaa671

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3. Ordering information

Table 2: Ordering information

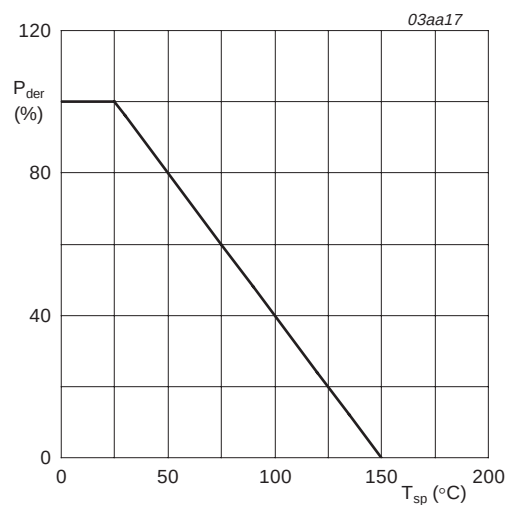
Type number	Package		
	Name	Description	Version
PMN50XP	TSOP6	plastic surface mounted package (TSOP6); 6 leads	SOT457

4. Limiting values

Table 3: Limiting values

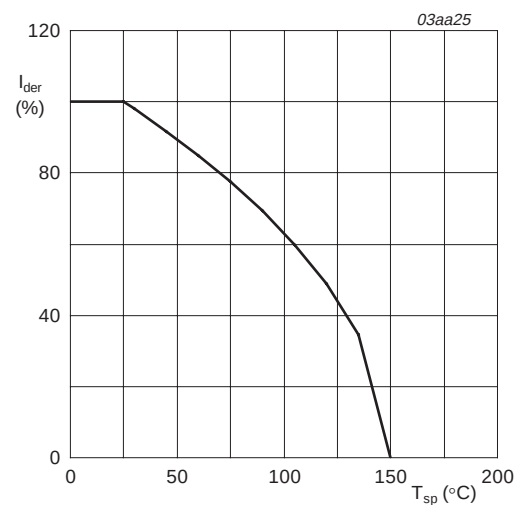
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	-20	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	-20	V
V_{GS}	gate-source voltage		-	± 12	V
I_D	drain current	$T_{sp} = 25\text{ °C}$; $V_{GS} = -4.5\text{ V}$; see Figure 2 and 3	-	-4.8	A
		$T_{sp} = 100\text{ °C}$; $V_{GS} = -4.5\text{ V}$; see Figure 2	-	-3	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; see Figure 3	-	-19.4	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; see Figure 1	-	2.2	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C
Source-drain diode					
I_S	source current	$T_{sp} = 25\text{ °C}$	-	-1.9	A
I_{SM}	peak source current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	-7.5	A



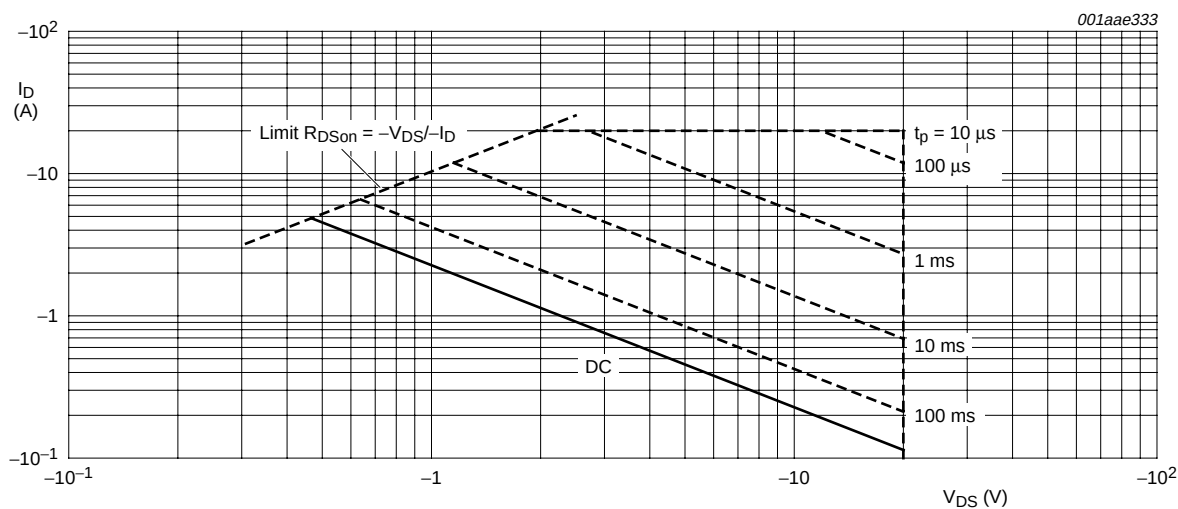
$$P_{der} = \frac{P_{tot}}{P_{tot(25\text{ }^{\circ}\text{C})}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature



$$I_{der} = \frac{I_D}{I_{D(25\text{ }^{\circ}\text{C})}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature



T_{sp} = 25 °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see Figure 4	-	-	55	K/W

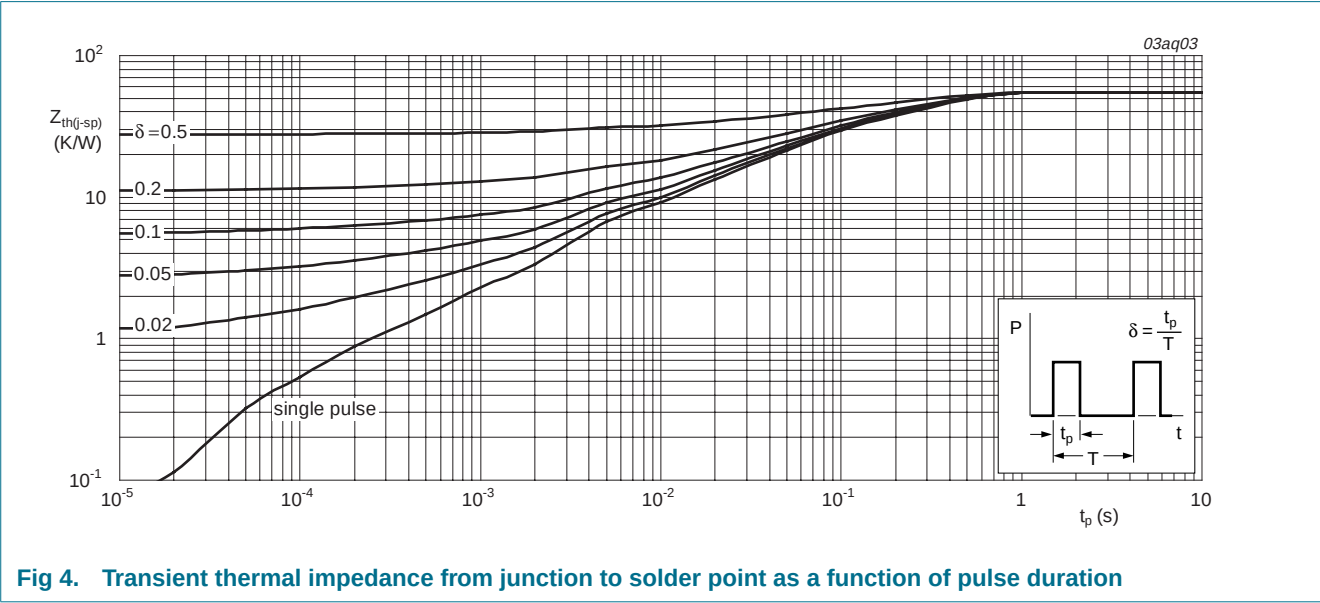


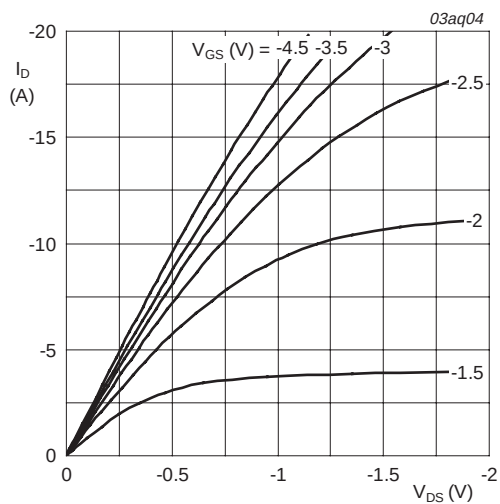
Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

Table 5: Characteristics

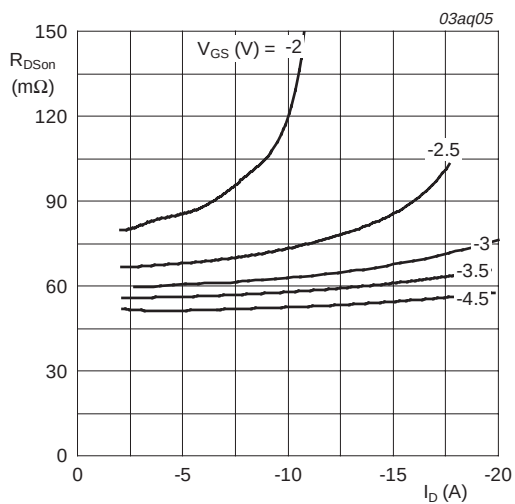
$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^{\circ}\text{C}$	-20	-	-	V
		$T_j = -55\text{ }^{\circ}\text{C}$	-18	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = -0.25\text{ mA}$; $V_{DS} = V_{GS}$; see Figure 9 and 10				
		$T_j = 25\text{ }^{\circ}\text{C}$	-0.55	-0.75	-0.95	V
		$T_j = 150\text{ }^{\circ}\text{C}$	-0.35	-	-	V
		$T_j = -55\text{ }^{\circ}\text{C}$	-	-	-1.1	V
I_{DSS}	drain leakage current	$V_{DS} = -20\text{ V}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^{\circ}\text{C}$	-	-	-1	μA
		$T_j = 70\text{ }^{\circ}\text{C}$	-	-	-5	μA
I_{GSS}	gate leakage current	$V_{GS} = \pm 12\text{ V}$; $V_{DS} = 0\text{ V}$	-	-10	-100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}$; $I_D = -2.8\text{ A}$; see Figure 6 and 8				
		$T_j = 25\text{ }^{\circ}\text{C}$	-	48	60	m Ω
		$T_j = 150\text{ }^{\circ}\text{C}$	-	77	96	m Ω
		$V_{GS} = -2.5\text{ V}$; $I_D = -2.3\text{ A}$; see Figure 6 and 8	-	65	80	m Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = -4.7\text{ A}$; $V_{DS} = -10\text{ V}$; $V_{GS} = -4.5\text{ V}$; see Figure 11 and 12	-	10	-	nC
Q_{GS}	gate-source charge		-	2.2	-	nC
Q_{GD}	gate-drain charge		-	1.3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage		-	-1.6	-	V
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = -20\text{ V}$; $f = 1\text{ MHz}$; see Figure 14	-	1020	-	pF
C_{oss}	output capacitance		-	140	-	pF
C_{rss}	reverse transfer capacitance		-	100	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -10\text{ V}$; $R_L = 10\text{ }\Omega$; $V_{GS} = -4.5\text{ V}$; $R_G = 6\text{ }\Omega$	-	8.5	-	ns
t_r	rise time		-	7.5	-	ns
$t_{d(off)}$	turn-off delay time		-	82	-	ns
t_f	fall time		-	35	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = -1.7\text{ A}$; $V_{GS} = 0\text{ V}$; see Figure 13	-	-0.77	-1.2	V



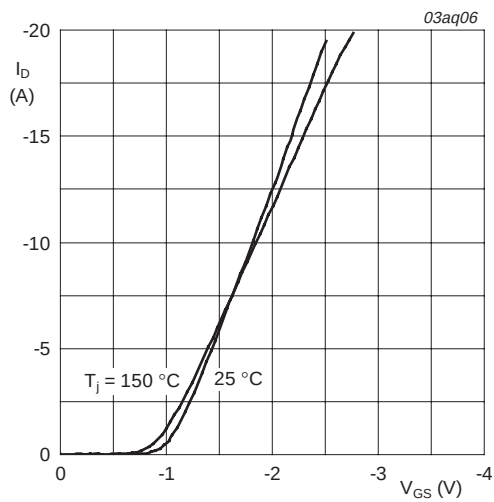
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



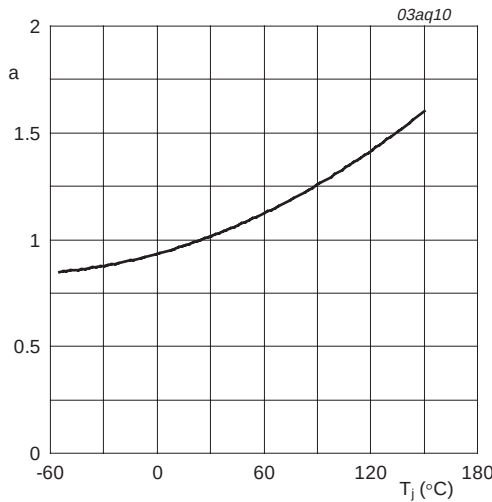
T_j = 25 °C

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



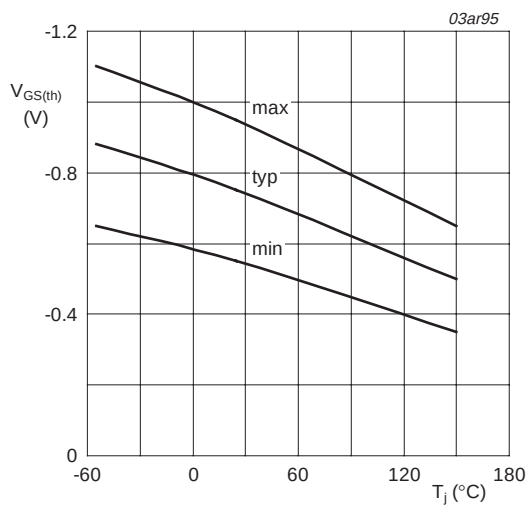
T_j = 25 °C and 150 °C; V_{DS} > I_D × R_{DSon}

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



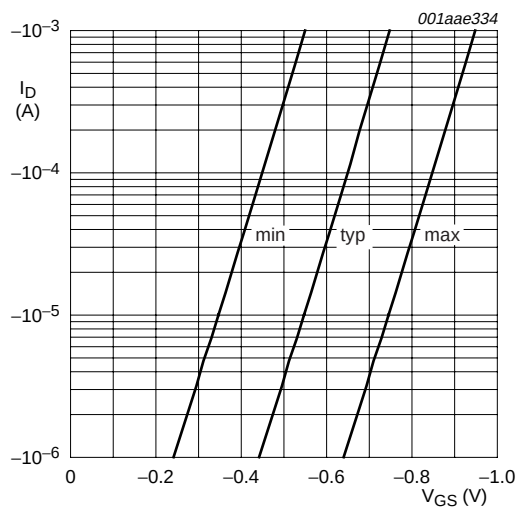
$$a = \frac{R_{DSon}}{R_{DSon(25\text{ °C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



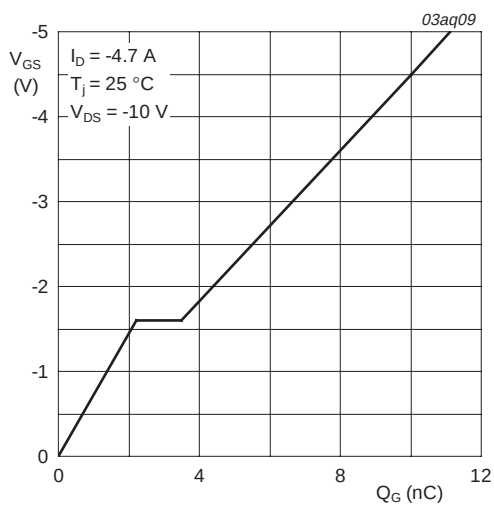
$I_D = -0.25$ mA; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



$T_J = 25$ °C; $V_{DS} = -5$ V

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$I_D = -4.7$ A; $V_{DS} = -10$ V

Fig 11. Gate-source voltage as a function of gate charge; typical values

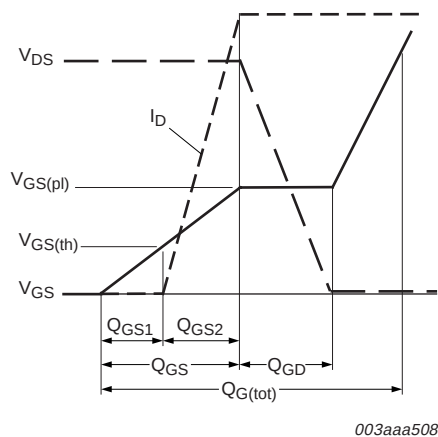
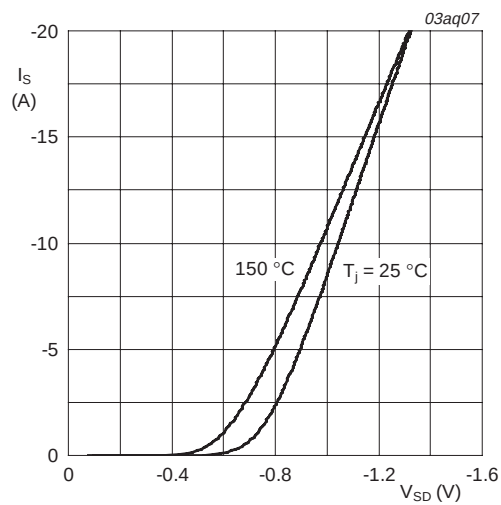
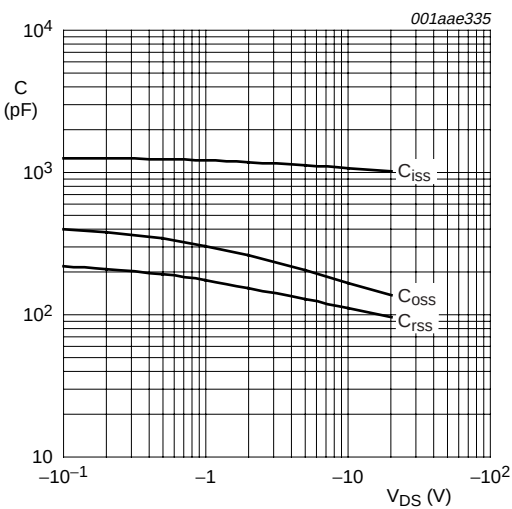


Fig 12. Gate charge waveform definitions



$T_j = 25\text{ °C}$ and 150 °C ; $V_{GS} = 0\text{ V}$

Fig 13. Source current as a function of source-drain voltage; typical values



$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

7. Package outline

Plastic surface mounted package (TSOP6); 6 leads

SOT457

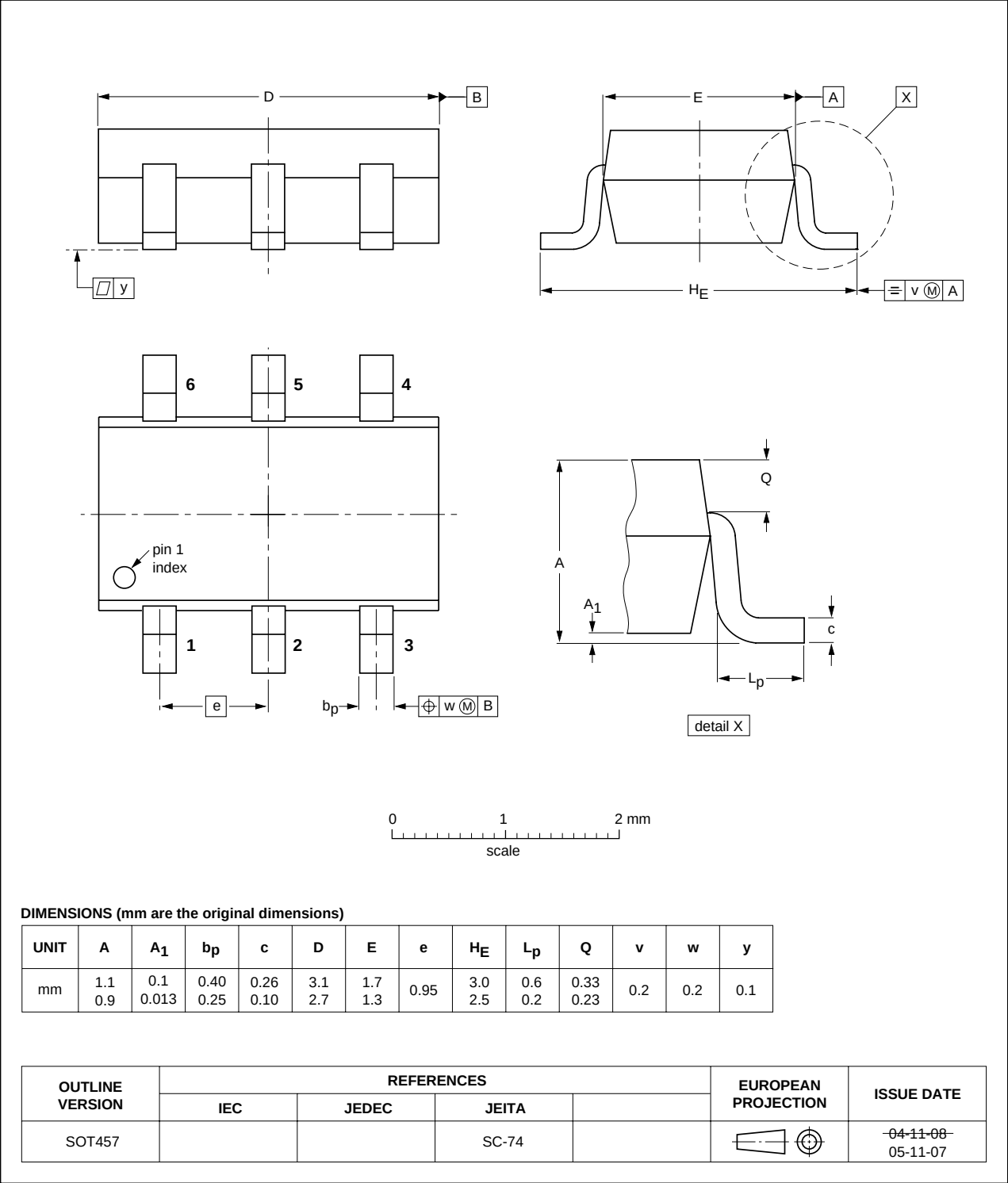


Fig 15. Package outline SOT457 (TSOP6)

8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PMN50XP_1	20060123	Product data sheet	-	-	-

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Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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14. Contents

1 **Product profile** 1

1.1 General description..... 1

1.2 Features 1

1.3 Applications 1

1.4 Quick reference data..... 1

2 **Pinning information**..... 1

3 **Ordering information**..... 2

4 **Limiting values**..... 2

5 **Thermal characteristics**..... 4

6 **Characteristics**..... 5

7 **Package outline** 9

8 **Revision history**..... 10

9 **Data sheet status** 11

10 **Definitions** 11

11 **Disclaimers**..... 11

12 **Trademarks**..... 11

13 **Contact information** 11



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Date of release: 23 January 2006
Document number: PMN50XP_1

Published in The Netherlands