Document Title

256Mb (16Mb x 16) SDRAM Datasheet

Revision History

Revision	Date	Page	Notes
0.1	March, 2010	—	Original

Features

- Clock frequency: 166, 133 MHz
- Fully synchronous; all signals referenced to a positive clock edge
- Four banks operation
- Single 3.3V power supply
- LVTTL interface
- Programmable burst length 1, 2, 4, 8, full page
- Programmable burst sequence: Sequential/Interleave
- 8192 refresh cycles /64ms
- Random column address every clock cycle
- Programmable /CAS latency (2, 3 clocks)
- Burst read/write and burst read/single write operations capability
- Burst termination by burst stop and precharge command
- Byte controlled by LDQM and UDQM

General Description

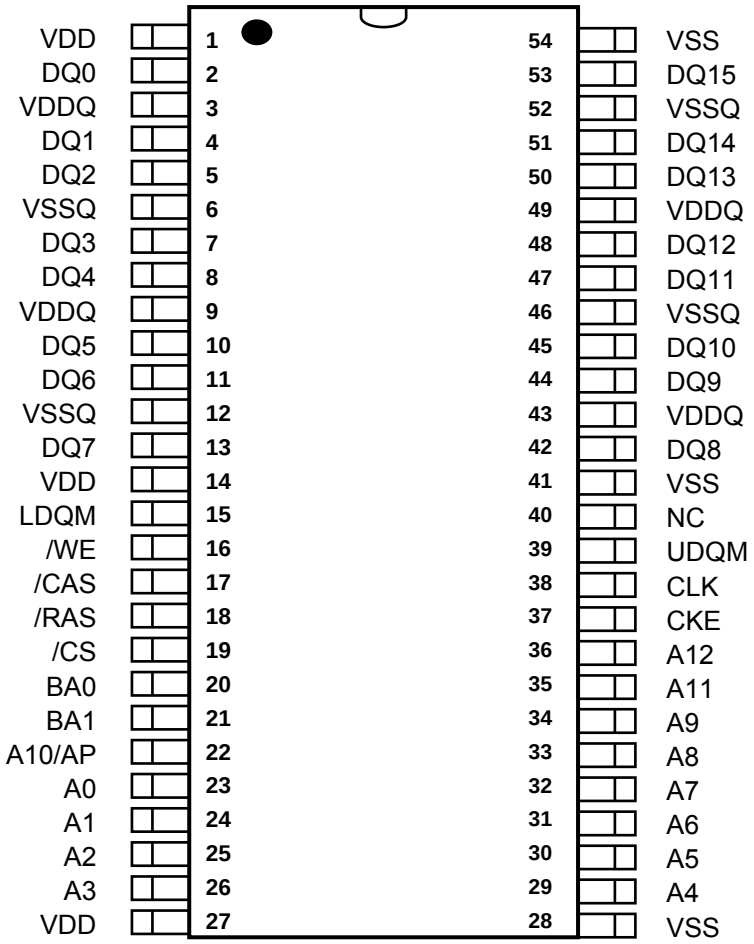
The PMS308416B is a high-speed CMOS synchronous DRAM. It is organized as 4 banks of 4,194,304 Words x 16 Bits DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Ordering Information

Commercial Temperature Range: 0°C to 70°C

Frequency	tCK	Part No.	Package
166MHz	6ns	PMS308416BTR-6CN	400-mil TSOP II Lead-free
133MHz	7.5ns	PMS308416BTR-75CN	

Pin Configuration



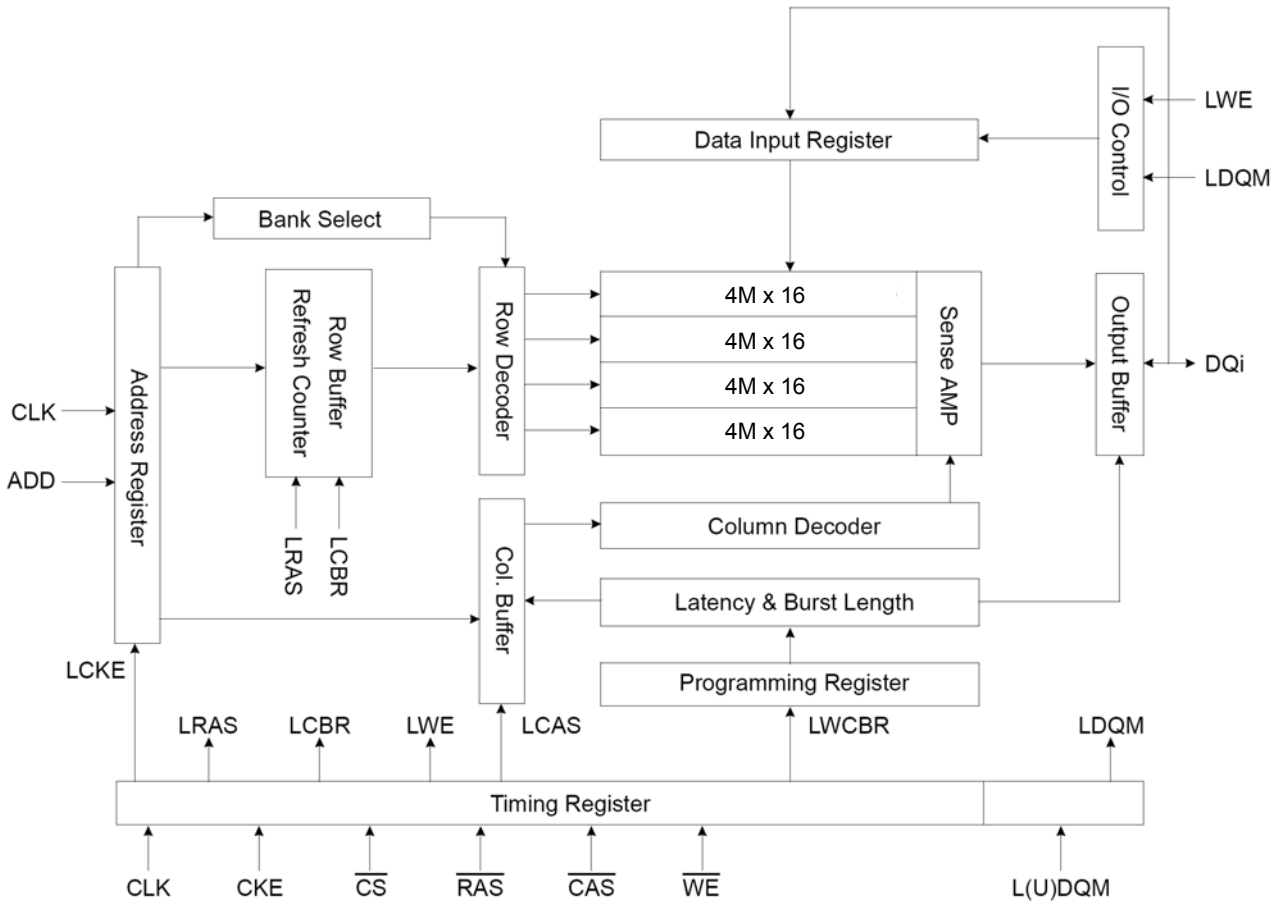
Pin Descriptions

A0-A12	Address Input	/CAS	Column Address Strobe Command
A0-A12	Row Address Input	/WE	Write Enable
BA0, BA1	Bank Select Address	LDQM	Lower Byte, Input/Output Mask
A0-A8	Column Address Input	UDQM	Lower Byte, Input/Output Mask
DQ0-DQ15	Data DQ	VDD	Power
CLK	System Clock Input	VSS	Ground
CKE	Clock Enable	VDDQ	Power Supply for DQ Pin
/CS	Chip Select	VSSQ	Ground for DQ Pin
/RAS	Row Address Strobe Command	NC	No Connection

Pin Functions

Symbol	Type	Function
A0-A12	Input	**Address Inputs:** A0-A12 are used as row address inputs during active command input and A0-A8 as column address inputs during read or write command input. A10 is also used to determine the precharge mode during other commands. If A10 is LOW during precharge command, the bank selected by BA0-BA1 is precharged, but if A10 is HIGH, both banks will be precharged. When A10 is HIGH in read or write command cycle, the precharge starts automatically after the burst access.
BA1, BA0	Input	**Bank Select:** Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
CLK	Input	**Clock:** Active on the positive going edge to sample all inputs.
CKE	Input	**Clock Enable:** The CKE input determines whether the CLK input is enables within the device. When CKE is HIGH, the next rising edge of the CLK signal will be valid, and when LOW, invalid. When CKE is LOW< the device will be in either the power-down mode, the clock suspend mode, or the self refresh mode. The CKE is an asynchronous input.
/CS	Input	**Chip Select:** /CS enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when /CS is sampled HIGH. /CS provides for external bank selection on systems with multiple banks. It is considered part of the command code.
/RAS	Input	**Row Address Strobe:** /RAS in conjunction with /CAS and /WE, forms the device command. See the “Command Truth Table” item for details on device commands.
/CAS	Input	**Column Address Strobe:** /CAS in conjunction with /RAS and /WE, forms the device command. See the “Command Truth Table” item for details on device commands.
/WE	Input	**Write Enable:** /WE in conjunction with /RAS and /CAS, forms the device command. See the “Command Truth Table” item for details on device commands.
LDQM, UDQM	Input	**Data Input/Output Mask:** LDQM and UDQM control the lower the upper bytes of the DQ buffers. In read mode, LDQM and UDQM control the output buffer. When LDQM or UDQM is LOW, the corresponding buffer byte is enables, and when HIGH, disables. The outputs go to the HIGH impedance state when LDQM/UDQM is HIGH. In write mode, LDQM and UDQM control the input buffer. When LDQM or UDQM is LOW the corresponding buffer byte is enables, and data can be written to the device. When LDQM or UDQM is HIGH, input data is masked and cannot be written to the device.
DQ0-DQ15	I/O	**Data I/O:** DQ0-15 are data input/output pins. DQ through these pins can be controlled in byte units using the LDQM and UDQM pins.
NC	-	**No Connect:** These pins should be left unconnected.
VDDQ	Supply	**DQ Power:** VDDQ is the output buffer power supply.
VDD	Supply	**Power Supply:** VDD is the device internal power supply.
VSS	Supply	**Ground:** VSS is the device internal ground.
VSSQ	Supply	**DQ Ground:** VSSQ is the output buffer ground

Block Diagram



Absolute Maximum Rating

Symbol	Parameters	Rating	Unit
V_{IN}, V_{OUT}	Input, Output Voltage	-0.3 ~ V_{DD} + 0.3	V
V_{DD}, V_{DDQ}	Power Supply Voltage	-0.3 ~ +4.6	V
T_A	Operating Temperature	0 ~ 70	°C
T_{STG}	Storage Temperature	- 55 ~ +125	°C
P_D	Power Dissipation	1	W
I_{OS}	Short Circuit Output Current	50	mA

Note: Permanent device damage may occur if Absolute Maximum Rating are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

Recommended DC Operating Conditions (T_A = 0~70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V_{DD}, V_{DDQ}	Power Supply Voltage,	3.0	3.3	3.6	V	
V_{IH}	Input High Voltage	2.0	–	V_{DD} +0.3	V	1
V_{IL}	Input Low Voltage	-0.3	0	0.8	V	2
V_{OH}	Output High Voltage	2.4	–	–	V	IOH = -2mA
V_{OL}	Output Low Voltage	–	–	0.4	V	IOL = +2mA
I_{IL}	Input Leakage Voltage	-10	–	10	μA	3
I_{OL}	Output Leakage Voltage	-10	–	10	μA	4

Note:

1. $V_{IH(max)}$ = V_{DD} + 1.2V for pulse width ≤ 5ns.
2. $V_{IL(min)}$ = V_{SS} - 1.2V for pulse width ≤ 5ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DD}, all other pins are not under test = 0V.
4. V_{OUT} is disabled, 0V ≤ V_{OUT} ≤ V_{DD}

Capacitance (V_{DD} = 3.3V, f = 1MHz, T_A = 25°C)

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Clock	2.5	3.5	pF
C_{IN2}	CKE, /CS, /RAS, /CAS, /WE, LDQM, UDQM	2.5	3.8	pF
C_{IN3}	Address	2.5	3.8	pF
$C_{I/O}$	DQ0~DQ15	4.0	6.5	pF

Note: These parameters are periodically sampled and are not 100% tested.

DC Characteristics (V_{DD} = 3.3V ± 0.3V, T_A = 0~70°C)

Parameter/Test condition	Symbol	Max.		Unit
		-6	-75	
Operating Current $t_{RC} \geq t_{RC}$(min), I_O = 0 mA, Burst Length = 2	I_{DD1}	150	140	mA
Precharge Standby Current in power down mode t_{CK} = 10ns, CKE ≤ V_{IL}(max)	I_{DD2P}	2		
Precharge Standby Current in power down mode t_{CK} = ∞, CKE ≤ V_{IL}(max)	I_{DD2PS}	2		
Precharge Standby Current in non-power down mode t_{CK} = 10ns, /CS ≥ V_{IH}(min), CKE ≥ V_{IH} Input signals are changed once every 20ns	I_{DD2N}	40		
Precharge Standby Current in non-power down mode t_{CK} = ∞, CLK ≤ V_{IL}(max), CKE ≥ V_{IH}	I_{DD2NS}	30		
Active Standby Current in power down mode t_{CK} = 10ns, CKE ≤ V_{IL}(max)	I_{DD3P}	35		
Active Standby Current in power down mode t_{CK} = ∞, CKE ≤ V_{IL}(max)	I_{DD3PS}	20		
Active Standby Current in non-power down mode t_{CK} = 10ns, CKE ≥ V_{IH}(min), /CS ≥ V_{IH}(min) Input signals are changed once every 20ns	I_{DD3N}	65		
Active Standby Current in non-power down mode CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CK} = ∞	I_{DD3NS}	45		
Operating Current (Burst mode) All banks activated, I_O = 0 mA, t_{CCD} = 2CLKs	I_{DD4}	165	155	
Refresh Current $t_{RFC} \geq t_{RFC}$(min)	I_{DD5}	200	175	
Self Refresh Current CKE ≤ 0.2V	I_{DD6}	3		

Note:

1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noted, input swing level is CMOS(VIH /VIL=VDDQ/VSSQ)

AC Characteristics (V_{DD} = 3.3V ± 0.3V, T_A = 0~70°C)[1,2,3]

Parameter		Symbol	-6		-75		Unit	Note
			Min.	Max.	Min.	Max.		
Clock Cycle Time	CL* = 3	t_{CK3}	6	–	7.5	–	ns	4
	CL* = 2	t_{CK2}	10	–	10	–		4
Clock High Time		t_{CH}	2.5	–	2.5	–		6
Clock Low Time		t_{CL}	2.5	–	2.5	–		6
Access Time from CLK (positive edge)	CL* = 3	t_{AC3}	–	5	–	5.4		4, 5
	CL* = 2	t_{AC2}	–	6	–	6		4, 5
Data Output Hold Time	CL* = 3	t_{OH3}	2.5	–	2.5	–		5
	CL* = 2	t_{OH2}	2.5	–	2.5	–		5
Data Output Low Impedance		t_{LZ}	0	–	0	–		
Data Output High Impedance	CL* = 3	t_{HZ3}	–	5	–	5.4		
	CL* = 2	t_{HZ2}	–	6	–	6		
Data/Address/Control Input Setup Time		t_{IS}	1.5	–	1.5	–		6
Data/Address/Control Input Hold Time		t_{IH}	1	–	1	–		6
Command Period (ACT to ACT)		t_{RC}	60	–	65	–		1
Command Period (ACT to PRE)		t_{RAS}	42	100K	45	100K		1
Command period (PRE to ACT)		t_{RP}	18	–	20	–		1
RAS to CAS Delay Time		t_{RCD}	18	–	20	–		1
Command Period (ACT[0] to ACT[1])		t_{RRD}	12	–	15	–		1
Last Data in to row precharge		t_{RDL}	2	–	2	–	CLK	2, 3
Last Data in to New Col. Address Delay		t_{CCD}	1	–	1	–		
Last Data In to Active Latency		t_{DAL}	5	–	5	–		
Last Data In to New Col. Address Delay		t_{CDL}	1	–	1	–		2
Last data In to Burst Stop		t_{BDL}	1	–	1	–		2
Mode Register Set Cycle Time		t_{MRD}	2	–	2	–		
Auto Refresh Cycle Time		t_{RFC}	60	–	70	–	ns	
Transition Time of Clock		t_T	0.3	1.5	0.3	1.5		
Refresh Cycle Time		t_{REF}	–	64	–	64	ms	

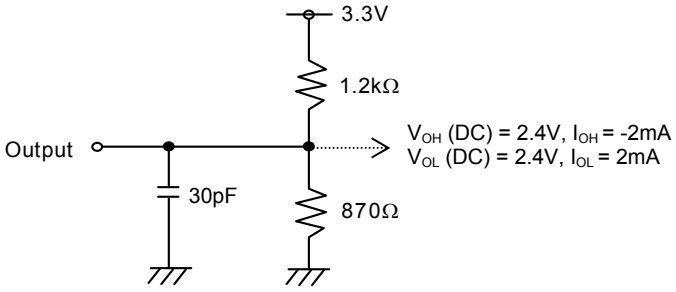
* CL is CAS# Latency.

Note:

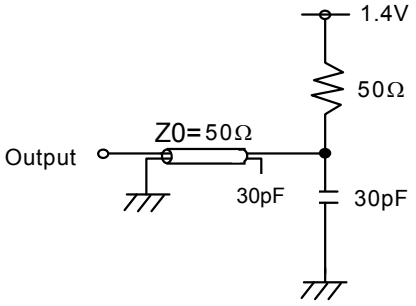
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. tRDL = tWR.
4. Parameters depend on programmed CAS latency.
5. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
6. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered.
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

AC Operating Test Conditions (V_{DD} = 3.3V ± 0.3V, T_A = 0~70°C)

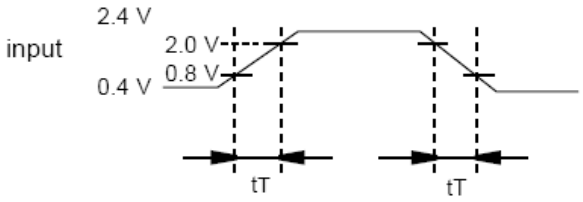
Parameter	Value
Input Signal Levels (Vih/Vil)	2.4V / 0.4V
Reference Level of Output Signals	1.4V
Output Load	Reference to the Under Output Load (B)
Transition Time (Rise and Fall) of Input Signals	1ns
Reference Level of Input Signals	1.4V



LVTTL D.C. Test Load (A)



LVTTL A.C. Test Load (B)



Input Waveform

Commands

Mode Register Set Command

(/CS, /RAS, /CAS, /WE = LOW)

The mode register stores the data for controlling the various operating modes of SDRAM. It programs the CAS latency, burst type, burst length, test mode and various vendor specific options to make SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore, the mode register must be written after power up to operate the SDRAM. The mode register is written by asserting LOW on /CS, /RAS, /CAS, and /WE (The SDRAM should be in active mode should be in active mode with CKE already high prior to writing the mode register). The state of address pins A0-A12 and BA0–BA1 in the same cycle as/CA, /RAS, /CAS, and /WE going LOW is the data written in the mode register. Two clock cycles are required to complete the write in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields into depending on functionality. The burst length field use A0-A2, Burst type uses A3, /CAS latency (read latency from column address) use A4-A6. The write burst length is programmed using A9. A7-A8, A10/AP-A12, and BA0–BA1 must be set to low for normal SDRAM operation. Refer to the table for specific codes for various burst length, burst type and /CAS latency.

Active Command

(/CS, /RAS = LOW, /CAS, /WE = HIGH)

This SDRAM includes four banks of 8,192 rows each. This command address BA0–BA1 selects one of the fours banks according and activates the row selected by the pins A0 to A12. This command corresponds to the fall of the /RAS signal from HIGH to LOW in conventional DRAMs.

Precharge Command

(/CS, /RAS, /WE = LOW, /CAS = HIGH)

This command begins precharge operation of the bank selected by pins A10/AP and BA0–BA1. When A10 is HIGH, all banks are precharged at the same time. When A10 is LOW, the bank selected by BA0–BA1 is precharged. After executing this command, the next command for the selected bank(s) is executed after passage of the period t_{RP}, which is the period required for bank precharging. This Command corresponds to the /RAS signal from LOW to HIGH in conventional DRAMs.

Read Command

(/CS, /CAS = LOW, /RAS, /WE = HIGH)

This command selects the bank specified by the BA0-BA1 pins and begins a burst read operation at the start address specified by pin A0 to A12. Data is output following /CAS latency. The selected bank must be activated before executing this command. This Command corresponds to the /RAS signal from LOW to HIGH in conventional DRAMs. When the A10/AP pin is HIGH, this command functions as a read with Auto Precharge command. After the burst read completes, the bank selected by pin BA0-BA1 is precharged. When A10/AP pin is LOW, the bank selected by the BA0-BA1 pins remains in the activated state after the burst read completes.

Write Command

(/CS, /CAS, /WE = LOW, /RAS = HIGH)

When burst write mode has been selected with the mode register set command, this command selects the bank specified by the BA0–BA1 pins pin and begins a burst write operation at the start address specified by pins A0 to A12. This first data must be input to the DQ pins in the cycle with this command. The selected bank must be activated before executing this command. When A10/AP pin is HIGH, this command functions as a write with Auto Precharge command. After the burst write completes, the bank selected by pin BA0-BA1 is precharged. When the A10/AP pin is LOW, the bank selected by the BA0-BA1 pins remains in the activated state after the burst write completes.

Auto Refresh Command

(/CS, /RAS, /CAS = LOW, /WE, CKE = HIGH)

This command executes the Auto Refresh operation. The row address and bank to be refreshed are automatically generated during this operation. All banks must be placed in the idle state before executing this command. The stipulated period (t_{RC}) is required for a single refresh operation, and no other commands can be executed during this period. The SDRAM goes to the idle state after the internal refresh operation completes. This command must be executed at least 8192 times every 64ms. This command corresponds to CBR Auto Refresh in conventional DRAMs.

Self Refresh Command

(/CS, /RAS, /CAS, CKE = LOW, /WE = HIGH)

This command executes the Self Refresh operation. The row address, the bank, and the refresh interval to be refreshed are automatically generated internally during this operation. The Self Refresh operation is started by dropping the CKE pin from HIGH to LOW. The Self Refresh operation continues as long as the CKE pin remains LOW and there is no need for external control of any other pins. The Self Refresh operation is terminated by raising the CKE pin from LOW to HIGH. The next command cannot be executed until the SDRAM internal recovery period (t_{RC}) has elapsed. After the Self Refresh, since it is impossible to determine the address of the last row to be refreshed, an Auto Refresh should immediately be performed for all addresses (8,192 cycles).

Burst Stop Command

(/CS, /WE = LOW, /RAS, /CAS = HIGH)

This command forcibly terminates burst read and write operations. When this command is executed during a burst read operation, data output stops after the /CAS latency period has elapsed.

No Operation

(/CS = LOW, /RAS, /CAS, /WE = HIGH)

This command has no effect on the SDRAM.

Device Deselect Command

(/CS = HIGH)

This command does not select the SDRAM for an object of operation. In other words, it performs no operation with respect to the SDRAM.

Power Down Command

(CKE = LOW)

When both banks are in the idle state, or when at least one of the banks is not in the idle state, this command can be used to suppress device power dissipation by reducing device internal operations to the absolute minimum. Power Down mode is started by dropping the CKE pin from HIGH to LOW. Power Down mode continues as long as the CKE pin is held LOW. All pins other than CEK pins are invalid and none of the other commands can be executed in this mode. The Power Down operation is terminated by raising the CKE pin from LOW to HIGH. The next command cannot be executed until the recovery period (t_{CKA}) has elapsed. Since this command differs from the Self Refresh command described above in that the refresh operation is not performed automatically internally, the refresh operation must be performed within the refresh period (t_{REF}). Thus the maximum time that Power Down mode can be held is just under the refresh cycle time.

Clock Suspend

(CKE = LOW)

This command can be used to stop the SDRAM internal clock temporarily during a read or write cycle. Clock Suspend mode is started by dropping the CKE pin from HIGH to LOW. Clock suspend mode continues as long as the CKE pin is held LOW. All input pins other than the CKE pin are invalid and none of the other commands can be executed in this mode. Also note that the SDRAM internal state is maintained. Clock Suspend mode is terminated by rising the CKE pin from LOW to HIGH, at which point SDRAM operation restarts, the next command cannot be executed until the recovery period (t_{CKA}) has elapsed. Since this command differs from the Self Refresh command described above in that the refresh operation is not performed automatically internally, the refresh operation must be performed within the refresh period (t_{REF}). Thus the maximum time that Clock Suspend mode can be held is just under the refresh cycle time.

Command Truth Table(1,2)

Command	Symbol	CKE_{n-1}	CKE_n	/CS	/RAS	/CAS	/WE	DQM	BA0–BA1	A10	A0-A12	DQ
Mode Register Set(3,4)	MRS	H	X	L	L	L	L	X	OP CODE			X
Auto Refresh(5)	REF	H	H	L	L	L	H	X	X	X	X	High-Z
Self Refresh(5,6)	SREF	H	L	L	L	L	H	X	X	X	X	High-Z
Precharge Selected Bank	PRE	H	X	L	L	H	L	X	V	L	X	X
Precharge All Banks	PALL	H	X	L	L	H	L	X	X	H	X	X
Bank Activate(7)	ACT	H	X	L	L	H	H	X	V	Row address		X
Write	WRIT	H	X	L	H	L	L	X	V	L	Column address(18)	X
Write and Auto Precharge(8)	WRITA	H	X	L	H	L	L	X	V	H		X
Read(8)	READ	H	X	L	H	L	H	X	V	L	Column address(18)	X
Read and Auto precharge(8)	READA	H	X	L	H	L	H	X	V	H		X
Burst Stop(9)	BST	H	X	L	H	H	L	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X	X	X
Device Deselect	DESL	H	X	H	X	X	X	X	X	X	X	X
Clock Suspend Mode	SBY	L	X	X	X	X	X	X	X	X	X	X
Data Write/Output Enable	ENB	H	X	X	X	X	X	L	X	X	X	Active
Data Mask/Output Disable	MASK	H	X	X	X	X	X	H	X	X	X	High-Z

DQM Truth Table(1,2)

Command	Symbol	CKE_{n-1}	CKE_n	UDQM	LDQM
Data Write/Output Enable	ENB	H	X	L	L
Data Mask/Output Disable	MASK	H	X	H	H
Upper Byte Data Write/Output Enable	ENBU	H	X	L	X
Lower Byte Data Write/Output Enable	ENBL	H	X	X	L
Upper Byte Data Mask/Output Disable	MASKU	H	X	H	X
Lower Byte Data Mask/Output Disable	MASKL	H	X	X	H

CKE Truth Table(1,2)

Command	Symbol	Current State	CKE_{n-1}	CKE_n	/CS	/RAS	/CAS	/WE	BA0-BA1	A10	A0-A12
Start Clock Suspend Mode	SPND	Active	H	L	X	X	X	X	X	X	X
Clock Suspend	—	Other States	L	L	X	X	X	X	X	X	X
Terminate Clock Suspend Mode	—	Clock Suspend	L	H	X	X	X	X	X	X	X
Auto Refresh	REF	Idle	H	H	L	L	L	H	X	X	X
Start Self Refresh Mode	SELF	Idle	H	L	L	L	L	H	X	X	X
Terminate Self Refresh Mode	SELFX	Self Refresh	L	H	L	H	H	H	X	X	X
			L	H	H	X	X	X	X	X	X
Start Power Down Mode	PDWN	Idle	H	L	L	H	H	H	X	X	X
			H	L	H	X	X	X	X	X	X
Terminate Power Down Mode	—	Power Down	L	H	X	X	X	X	X	X	X

Operation Command Table(1,2)

Current State	Command	Operation	/CS	/RAS	/CAS	/WE	BA0-BA1	A10	A0-A12
Idle	DESL	No Operation or Power Down(12)	H	X	X	X	X	X	X
	NOP	No Operation or Power Down(12)	L	H	H	H	X	X	X
	BST	Illegal	L	H	H	L	X	X	X
	READ/READA	Illegal	L	H	L	H	V	V	V(18)
	WRIT/WRITA	Illegal	L	H	L	L	V	V	V(18)
	ACT	Row Active	L	L	H	H	V	V	V(18)
	PRE/PALL	No Operation	L	L	H	L	V	V	X
	REF/SELF	Auto Refresh or Self Refresh	L	L	L	H	X	X	X
	MRS	Mode Register Set	L	L	L	L	OP CODE		
Row Active	DESL	No Operation	H	X	X	X	X	X	X
	NOP	No Operation	L	H	H	H	X	X	X
	BST	Illegal	L	H	H	L	X	X	X
	READ/READA	Read Start(17)	L	H	L	H	V	V	V(18)
	WRIT/WRITA	Write Start(17)	L	H	L	L	V	V	V(18)
	ACT	Illegal(10)	L	L	H	H	V	V	V(18)
	PRE/PALL	Precharge(15)	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OP CODE		
Read	DESL	Burst Read Continues, Row Active When Done	H	X	X	X	X	X	X
	NOP	Burst Read Continues, Row Active When Done	L	H	H	H	X	X	X
	BST	Burst Interrupted, Row Active After Interrupt	L	H	H	L	X	X	X
	READ/READA	Burst Read Continues to /CAS latency, New Read(16)	L	H	L	H	V	V	V(18)
	WRIT/WRITA	Burst Interrupted, Write Start After Interrupt(11,16)	L	H	L	L	V	V	V(18)
	ACT	Illegal(10)	L	L	H	H	V	V	V(18)
	PRE/PALL	Burst Read Interrupted, Precharge After Interrupt	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OP CODE		

Operation Command Table(1,2) (Cont.)

Current State	Command	Operation	/CS	/RAS	/CAS	/WE	BA0-BA1	A10	A0-A12
Write	DESL	Burst Write Continues, Write Recovery When Done	H	X	X	X	X	X	X
	NOP	Burst Write Continues, Write Recovery When Done	L	H	H	H	X	X	X
	BST	Burst Write Interrupted, Row Active After Interrupt	L	H	H	L	X	X	X
	READ/READA	Burst Write Interrupted, Read Restart After Interrupt(16)	L	H	L	H	V	V	V(18)
	WRIT/WRITA	Burst Write Interrupted, Write Restart After Interrupt(11,16)	L	H	L	L	V	V	V(18)
	ACT	Illegal(10)	L	L	H	H	V	V	V(18)
	PRE/PALL	Burst Write Interrupted, Precharge After Interrupt	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OP CODE		
Read With Auto Precharge	DESL	Burst Read Continues, Precharge When Done	H	X	X	X	X	X	X
	NOP	Burst Read Continues, Precharge When Done	L	H	H	H	X	X	X
	BST	Illegal	L	H	H	L	X	X	X
	READ/READA	Illegal(10)	L	H	L	H	V	V	V(18)
	WRIT/WRITA	Illegal(10)	L	H	L	L	V	V	V(18)
	ACT	Illegal(10)	L	L	H	H	V	V	V(18)
	PRE/PALL	Illegal(10)	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OP CODE		
Write With Auto Precharge	DESL	Burst Write Continues, Write Recovery and Precharge When Done	H	X	X	X	X	X	X
	NOP	Burst Write Continues, Write Recovery and Precharge When Done	L	H	H	H	X	X	X
	BST	Illegal	L	H	H	L	X	X	X
	READ/READA	Illegal(10)	L	H	L	H	V	V	V(18)
	WRIT/WRITA	Illegal(10)	L	H	L	L	V	V	V(18)
	ACT	Illegal(10)	L	L	H	H	V	V	V(18)
	PRE/PALL	Illegal(10)	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OP CODE		

Operation Command Table(1,2) (Cont.)

Current State	Command	Operation	/CS	/RAS	/CAS	/WE	BA0-BA1	A10	A0-A12
Row Precharge	DESL	No Operation, Idle State After t_{RP} Has Elapsed	H	X	X	X	X	X	X
	NOP	No Operation, Idle State After t_{RP} Has Elapsed	L	H	H	H	X	X	X
	BST	Illegal	L	H	H	L	X	X	X
	READ/READA	Illegal(10)	L	H	L	H	V	V	V(18)
	WRIT/WRITA	Illegal(10)	L	H	L	L	V	V	V(18)
	ACT	Illegal(10)	L	L	H	H	V	V	V(18)
	PRE/PALL	No Operation	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OP CODE		
Immediately Following Row Active	DESL	No Operation, Row Active After t_{RCD} Has Elapsed	H	X	X	X	X	X	X
	NOP	No Operation, Row Active After t_{RCD} Has Elapsed	L	H	H	H	X	X	X
	BST	Illegal	L	H	H	L	X	X	X
	READ/READA	Illegal(10)	L	H	L	H	V	V	V(18)
	WRIT/WRITA	Illegal(10)	L	H	L	L	V	V	V(18)
	ACT	Illegal(10,14)	L	L	H	H	V	V	V(18)
	PRE/PALL	Illegal(10)	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OP CODE		
Write Recovery	DESL	No Operation, Row Active After t_{DLP} Has Elapsed	H	X	X	X	X	X	X
	NOP	No Operation, Row Active After t_{DLP} Has Elapsed	L	H	H	H	X	X	X
	BST	No Operation, Row Active After t_{DLP} Has Elapsed	L	H	H	L	X	X	X
	READ/READA	Read Start	L	H	L	H	V	V	V(18)
	WRIT/WRITA	Write Start	L	H	L	L	V	V	V(18)
	ACT	Illegal(10)	L	L	H	H	V	V	V(18)
	PRE/PALL	Illegal(10)	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OP CODE		

Operation Command Table(1,2) (Cont.)

Current State	Command	Operation	/CS	/RAS	/CAS	/WE	BA0-BA1	A10	A0-A12
Write Recovery With Auto Precharge	DESL	No Operation, Idle State After t_{DAL} Has Elapsed	H	X	X	X	X	X	X
	NOP	No Operation, Row Active After t_{DLP} Has Elapsed	L	H	H	H	X	X	X
	BST	No Operation, Row Active After t_{DLP} Has Elapsed	L	H	H	L	X	X	X
	READ/READA	Illegal(10)	L	H	L	H	V	V	V(18)
	WRIT/WRITA	Illegal(10)	L	H	L	L	V	V	V(18)
	ACT	Illegal(10)	L	L	H	H	V	V	V(18)
	PRE/PALL	Illegal(10)	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OP CODE		
Refresh	DESL	No Operation, Idle State After t_{RC} Has Elapsed	H	X	X	X	X	X	X
	NOP	No Operation, Idle State After t_{RC} Has Elapsed	L	H	H	H	X	X	X
	BST	Illegal	L	H	H	L	X	X	X
	READ/READA	Illegal	L	H	L	H	V	V	V(18)
	WRIT/WRITA	Illegal	L	H	L	L	V	V	V(18)
	ACT	Illegal	L	L	H	H	V	V	V(18)
	PRE/PALL	Illegal	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OP CODE		
Mode Register Set	DESL	No Operation	H	X	X	X	X	X	X
	NOP	No Operation	L	H	H	H	X	X	X
	BST	Illegal	L	H	H	L	X	X	X
	READ/READA	Illegal	L	H	L	H	V	V	V(18)
	WRIT/WRITA	Illegal	L	H	L	L	V	V	V(18)
	ACT	Band and Row Active	L	L	H	H	V	V	V(18)
	PRE/PALL	No Operation	L	L	H	L	V	V	X
	REF/SELF	Refresh	L	L	L	H	X	X	X
	MRS	Most Register Set	L	L	L	L	OP CODE		

Note for Command Rule Table, DQM Truth Table, CKE Truth Table, Operation Command Table:

1. H: HIGH level input, L: LOW level input, X: HIGH or LOW level input, V: Valid data input.
2. All input signals are latched on the rising edge of the CLK signal.
3. Both banks must be placed in the idle state in advance.
4. The states of the A0 to A12 pins are loaded into the mode register as an OP CODE.
5. The row address is generated automatically internally at this time. The DQ pin and the address pin data are ignored.

6. During a self refresh operation, all pin data (states) other than CKE is ignored.
7. The selected bank must be placed in the idle state in advance.
8. The selected bank must be placed in the active state in advance.
9. This command is valid only when the burst length set to full page.
10. This is possible depending on the state of the bank selected by the BA0, BA1 pins.
11. Time to switch internal busses is required.
12. The device can be switched to power down mode by dropping the CKE pin LOW when both banks in the idle state. Input pins other than CKE are ignored at this time.
13. The device can be switched to self refresh mode by dropping the CKE pin LOW when both banks in the idle state. Input pins other than CKE are ignored at this time.
14. Possible if t_{RRD} is satisfied.
15. Illegal if t_{RAS} is not satisfied.
16. The conditions for burst interruption must be observed. Also note that the device will enter the precharged state immediately after the burst operation completes if auto precharge is selected.
17. Command input becomes possible after the period t_{RCD} has elapsed. Also note that the device will enter the precharge state immediately after the burst operation completes if auto precharge is selected.
18. A8, A9 = don't care.

CKE Command Truth Table(1)

Current State	Operation	CKE_{n-1}	CKE_n	/CS	/RAS	/CAS	/WE	BA0-BA1	A10	A0-A12
Self Refresh	Undefined	H	X	X	X	X	X	X	X	X
	Self Refresh Recovery(2)	L	H	H	X	X	X	X	X	X
	Self Refresh Recovery(2)	L	H	L	H	H	X	X	X	X
	Illegal(2)	L	H	L	H	L	X	X	X	X
	Illegal(2)	L	H	L	L	X	X	X	X	X
	Self Refresh	L	L	X	X	X	X	X	X	X
Self Refresh Recovery	Idle State After t_{RC} Has Elapsed	H	H	H	X	X	X	X	X	X
	Idle State After t_{RC} Has Elapsed	H	H	L	H	H	X	X	X	X
	Illegal	H	H	L	H	L	X	X	X	X
	Illegal	H	H	L	L	X	X	X	X	X
	Illegal	H	L	H	X	X	X	X	X	X
	Illegal	H	L	L	H	H	X	X	X	X
	Illegal	H	L	L	H	L	X	X	X	X
	Illegal	H	L	L	L	X	X	X	X	X

CKE Command Truth Table(1) (Cont.)

Current State	Operation	CKE_{n-1}	CKE_n	/CS	/RAS	/CAS	/WE	BA0-BA1	A10	A0-A12
Power Down	Invalid, CLK(n-1) would exit power down	H	X	X	X	X	X	X	X	X
	Exit Power Down	L	H	H	X	X	X	X	X	X
	Exit Power Down	L	H	L	H	H	H	X	X	X
	Power Down Mode	L	L	X	X	X	X	X	X	X
All Banks Idle	See Operation Command Table	H	H	H	X	X	X	X	X	X
	See Operation Command Table	H	H	L	H	X	X	X	X	X
	See Operation Command Table	H	H	L	L	H	X	X	X	X
	Auto Refresh	H	H	L	L	L	H	X	X	X
	See Operation Command Table	H	H	L	L	L	L	OP CODE		
	Begin Power Down Next Cycle	H	L	H	X	X	X	X	X	X
	See Operation Command Table	H	L	L	H	X	X	X	X	X
	See Operation Command Table	H	L	L	L	H	X	X	X	X
	Self Refresh(3)	H	L	L	L	L	H	X	X	X
	See Operation Command Table	H	L	L	L	L	L	OP CODE		
	Exit Power Down Next Cycle	L	H	X	X	X	X	X	X	X
	Power Down Mode(3)	L	L	X	X	X	X	X	X	X
Row Active	See Operation Command Table	H	X	X	X	X	X	X	X	X
	Clock Suspend	L	X	X	X	X	X	X	X	X
Other States	See Operation Command Table	H	H	X	X	X	X	X	X	X
	Clock Suspend On Next Cycle(4)	H	L	X	X	X	X	X	X	X
	Clock Suspend Termination On Next Cycle	L	H	X	X	X	X	X	X	X
	Maintain Clock Suspend	L	L	X	X	X	X	X	X	X

Note:

1. H: HIGH level input, L: LOW level input, X: HIGH or LOW level input.
2. The CLK pin and the other input are reactivated asynchronously by the transition of the CKE level from LOW to HIGH. The minimum setup time (t_{CKA}) required before all commands other than mode termination must be satisfied.
3. All banks must be set to the idle state in advance to switch to power down mode or self refresh mode.
4. The input must be command defined in the Operation Command Table.

Bank Selection and Precharge Address Allocation

Bank active at read/write are controlled by BA0-BA1.

BA0	BA1	Active & Read/Write
0	0	Bank 0
1	0	Bank 1
0	1	Bank 2
1	1	Bank 3

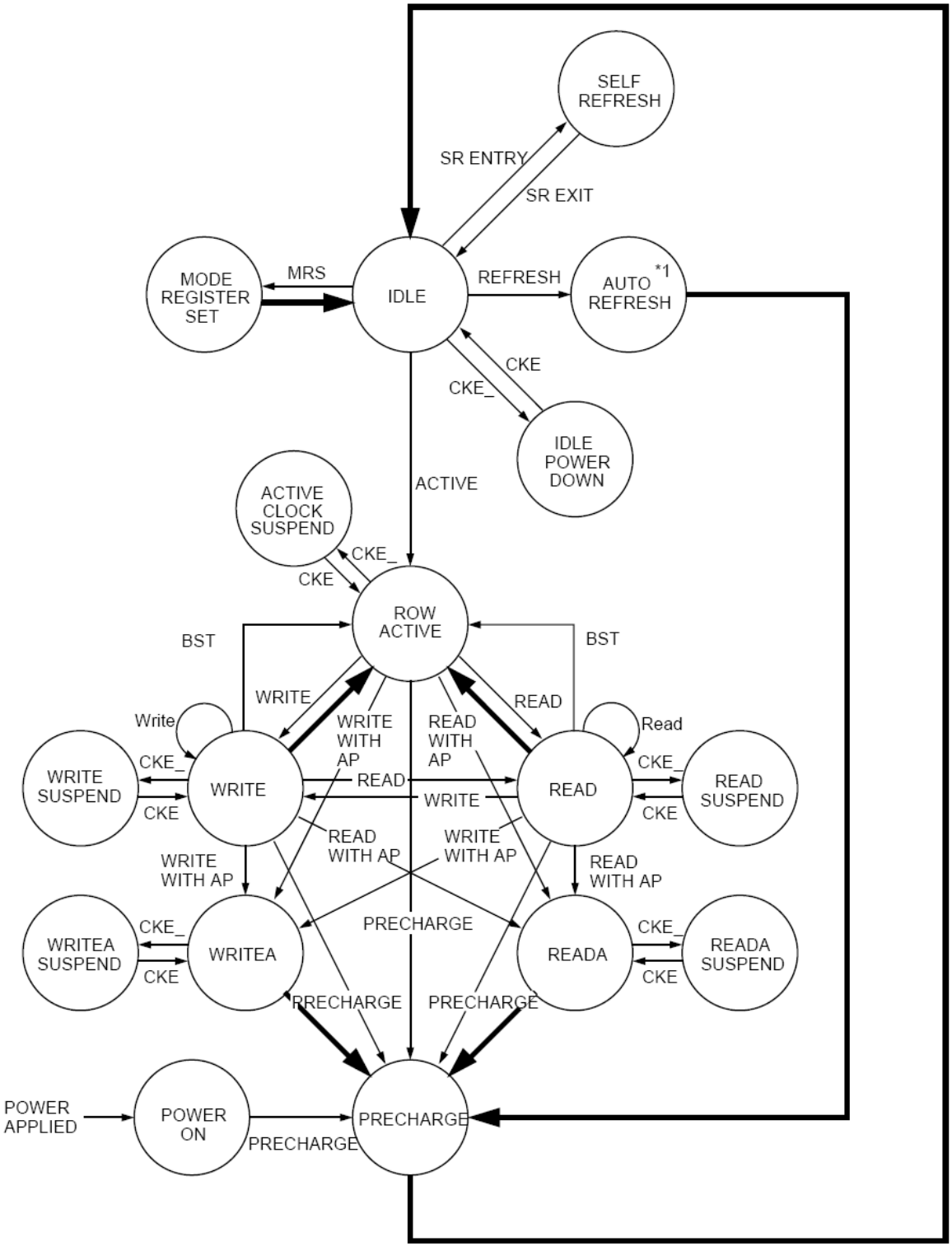
Enable and disable Auto Precharge function are controlled by A10/AP and BA0-BA1 in read/write command

A10/AP	BA0	BA1	Operation
0	0	0	Disable Auto Precharge, leave Bank 0 active at end of burst
	1	0	Disable Auto Precharge, leave Bank 1 active at end of burs
	0	1	Disable Auto Precharge, leave Bank 2 active at end of burs
	1	1	Disable Auto Precharge, leave Bank 3 active at end of burs
1	0	0	Enable Auto Precharge, precharge Bank 0 at end of burst
	1	0	Enable Auto Precharge, precharge Bank 1 at end of burst
	0	1	Enable Auto Precharge, precharge Bank 2 at end of burst
	1	1	Enable Auto Precharge, precharge Bank 3 at end of burst

A10/AP and BA0-BA1 control bank precharge when precharge is asserted

A10/AP	BA0	BA1	Precharge
0	0	0	Bank 0
0	1	0	Bank 1
0	0	1	Bank 2
0	1	1	Bank 3
1	X	X	All Banks

Simplified State Diagram



→ Automatic transition after completion of command.

→ Transition resulting from command input.

Note: After the Auto Refresh operation, Precharge operation is performed automatically and enter the IDLE state.

Function Descriptions

Power Up Sequence

Power Up Sequence

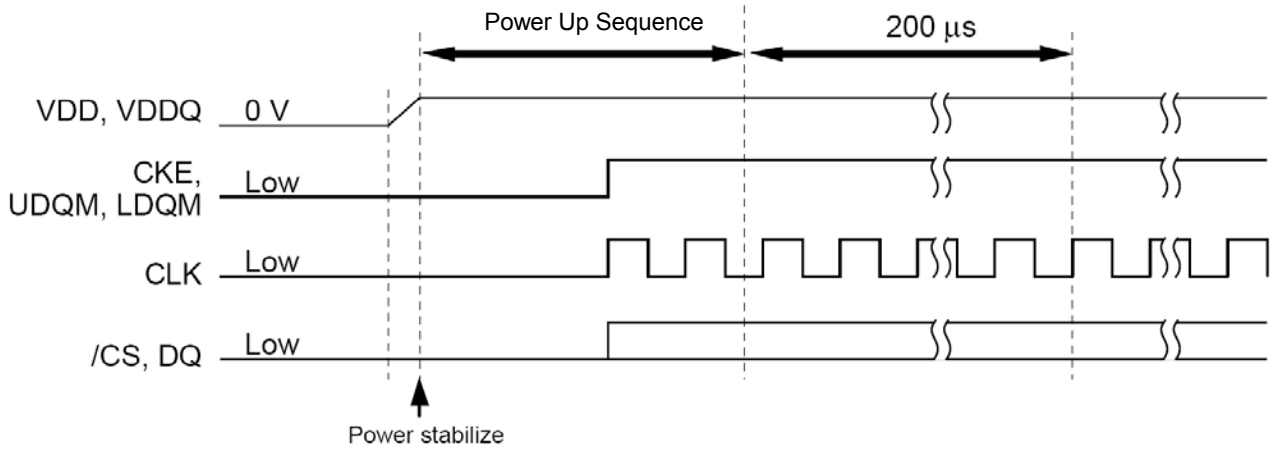
1. Apply VDD and VDDQ at the same time. Keep CKE low during power up.
2. Wait for stable power.
3. Start clock and drive CKE high.

Note : Voltage on any input pin must not exceed VDD+0.3V during power up.

Initialization Sequence

4. After stable power and stable clock, wait 200us.
5. Issue precharge all command (PALL).
6. After tRP delay, set 2 or more auto refresh commands (REF).
7. Set the mode register set command (MRS) to initialize the mode register.

Note : To keep DQM and CKE high during initialization sequence to prevent data contention on the DQ bus is recommended.



Power Up Sequence and Initialization Sequence

Mode Register Settings

The mode register set command sets the mode register. When this command is executed, A9, A6-A0 function as data input pins for setting the register, and this data becomes the device internal OP CODE. This OP CODE has fields as listed in the table below.

Input Pin	Field
A9	Write Burst Mode
A6, A5, A4	/CAS Latency
A3	Burst Type
A2, A1, A0	Burst Length

Note that the mode register set command can be executed only when all banks are in the idle state. Wait at least two cycles after executing a mode register set command before executing the next command.

/CAS Latency

During a read operation, between the execution of the read command and data output is stipulated as the /CAS latency. This period can be set using the mode register set command. The optimal /CAS latency is determined by the clock frequency and device speed grade. See the table of Operating Frequency / Latency Relationships for details on the relation ship between the clock frequency and the /CAS latency. See the table of the Mode Register for details.

Burst Length

When writing or ready, data can be input or output data continuously. In these operations, an address is input only once and that address is taken as the starting address internally by the SDRAM. The SDRAM then automatically generates the following address. The burst length field in the mode register stipulates the number of data items input or output in sequence. In the SDRAM, a burst length of 1, 2, 4, 8, or full page can be specified. See the table of the Mode Register for details.

Burst Type

The burst data order during a read or write operation is stipulated by the burst type, which can be set by the mode register set command. The SDRAM supports sequential mode and interleaved mode burst type settings. See the table of the Mode Register for details. Also see the table of Burst Length and Column Address Sequence for details on DQ data orders in these modes.

Mode Register

Address	BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	0	0	0	0	0	WB	0	0	CAS Latency			BT	Burst Length		

	A2	A1	A0	Sequential	Interleaved
Burst Length	0	0	0	1	1
	0	0	1	2	2
	0	1	0	4	4
	0	1	1	8	8
	1	0	0	Reserved	Reserved
	1	0	1	Reserved	Reserved
	1	1	0	Reserved	Reserved
	1	1	1	Full Page	Reserved

	A3	Type
Burst Type	0	Sequential
	1	Interleaved

	A6	A5	A4	/CAS Latency
CAS Latency	0	0	0	Reserved
	0	0	1	Reserved
	0	1	0	2
	0	1	1	3
	1	X	X	Reserved

A9	Write Burst Mode
0	Burst Read & Burst Write
1	Burst Read & Single Write

Note: Other values for these bits are reserved.

Burst Length And Column Address Sequence

Burst Length	Column Address			Address Sequence	
	A2	A1	A0	Sequential	Interleaved
2	X	X	0	0-1	0-1
	X	X	1	1-0	1-0
4	X	0	0	0-1-2-3	0-1-2-3
	X	0	1	1-2-3-0	1-0-3-2
	X	1	0	2-3-0-1	2-3-0-1
	X	1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (256)	n	n	n	C_n, C_{n+1}, C_{n+2}, C_{n+3}, C_{n+4},…… C_{n-1}(C_{n+511}), …. C_n(C_{n+512})……	None

Note: The burst length in full page mode is 512.

Operation of the SDRAM

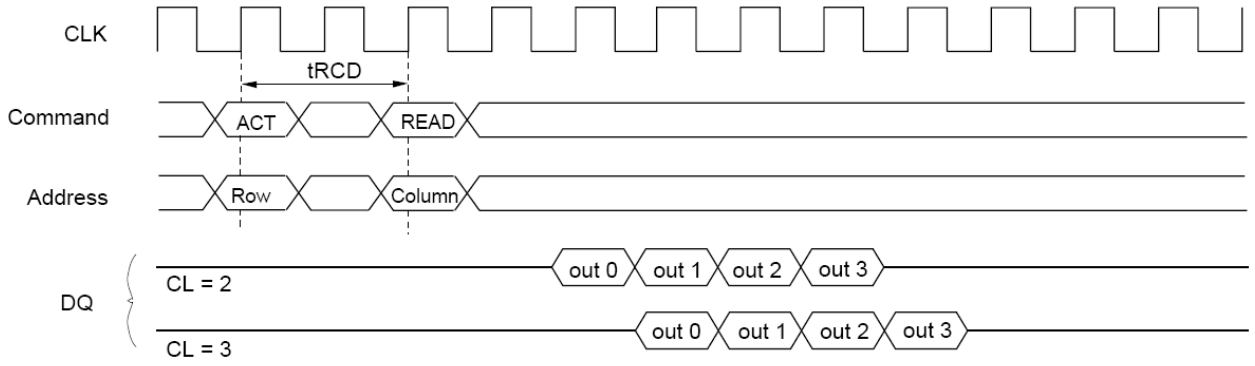
Read/Write Operations

Bank Active

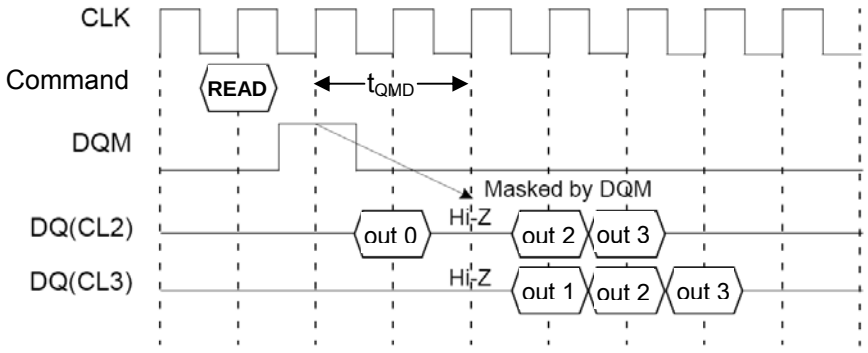
Before executing a read or write operation, the corresponding bank and the row address must be activated by the bank active (ACT) command. An interval of t_{RCD} is required between the bank active command input and the following read/write command input.

Burst Read

The Read cycle is started by executing the read command. The address provided during read command execution is used as the starting address. First, the data corresponding to this address is output in synchronization with the clock signal after /CAS latency period. Next, data corresponding to an address generated automatically by the device is output in synchronization with the clock signal. The output buffers go to the LOW impedance state /CAS latency minus one cycle after the read command, and go to the HIGH impedance state automatically after the last data is output. However, the case where the burst length is a full page is an exception. In this case output buffers must be set to the high impedance state by executing a burst stop command. Note that upper byte and lower byte output data can be masked in dependently under control of the signals applied to the U/LQM pins. The delay period (t_{QMD}) is fixed at two, regardless of the /CAS latency setting, when this function is used. The selected bank must be set to the active state before executing this command.



Burst Read Operation (Burst Length = 4, /CAS Latency = 2, 3)

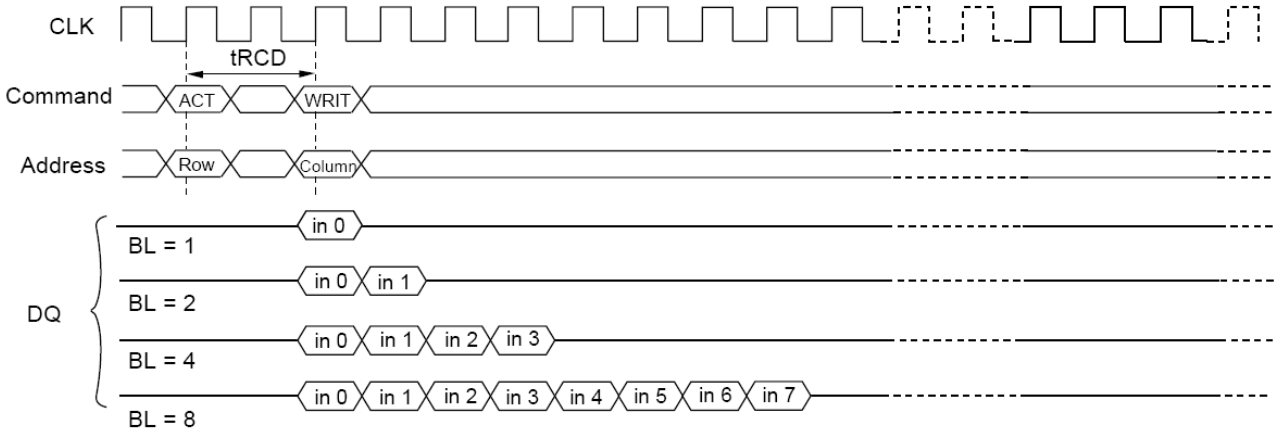


Burst Read masked by DQM Operation (Burst Length = 4, /CAS Latency = 2, 3)

Burst Write

The Write cycle is started by executing the command. The address provided during write command execution is used as the starting address, at the same time, data for this address is input in synchronization

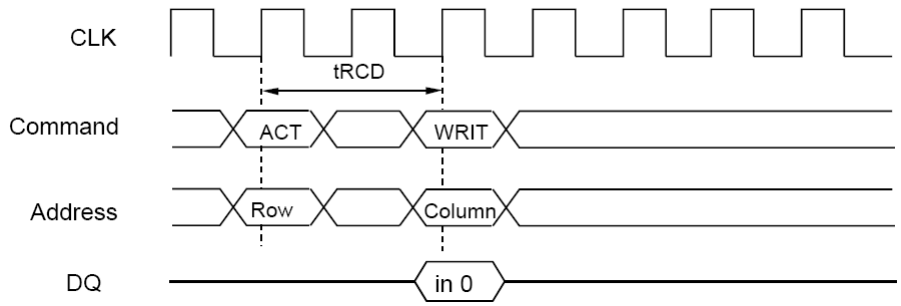
with the clock signal. Next, data is input in other in synchronization with the clock signal. During this operation, data is written to address generated automatically by the device. This cycle terminates automatically after a number of clock cycles determined by the stipulated burst length. However, the case where the burst length is a full page is an exception. In this case the write cycle must be terminated by executing a burst stop command. The latency for DQ pin data input is zero, regardless of the /CAS latency setting. However, a wait period (write recovery: tDPL) after the last data input is required for the device to complete the write operation. Note that the upper byte and lower byte input data ca be masked independently under control of the signal applied to the U/LQM pins. The delay period (t_{DMD}) is fixed at zero, regardless of the /CAS latency setting, when this function is used. The selected bank must be set to the active state before executing this command.



Burst Write Operation (Burst Length = 1, 2, 4, 8, /CAS Latency = 2, 3)

Single Write

The single write operation is enabled by setting OP CODE (A9) to (1). In a single write operation, data is only written to the column address and the bank select address specified by the write command set cycle without regard to the burst length. (The latency of data input is 0 clock).



Auto Precharge Operations

Read With Auto-Precharge

In this operation, since precharge is automatically performed after completing a read operation, a precharge command does not need to be executed after each read operation. The command executed for the same

bank after the execution of this command must be the bank active (ACT) command. The next ACT command can be issued at the later time of either tRP after internal precharge or tRC after the previous ACT.

Write With Auto-Precharge

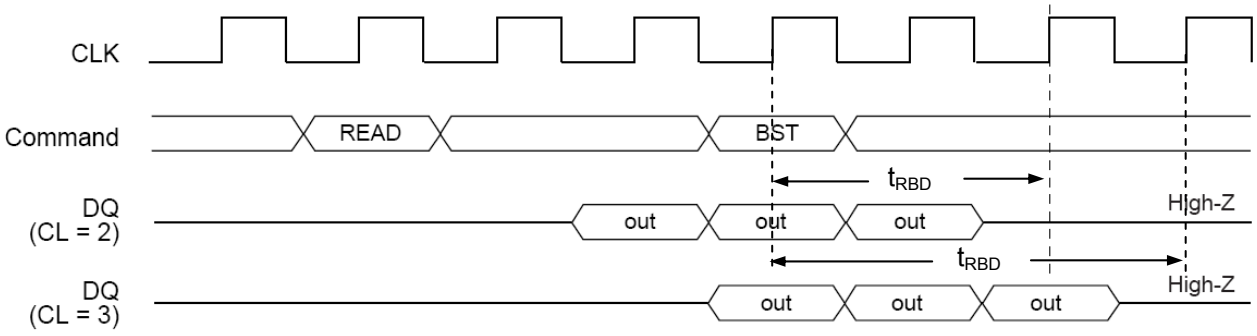
In this operation, since precharge is automatically performed after completing a burst write or single write operation, a precharge command does not need to be executed after each write operation. The command executed for the same bank after the execution of this command must be the bank active (ACT) command. The next ACT command can be issued at the later time of either tDAL from the last input data cycle or tRC after the previous ACT.

Burst Stop Operations

Burst Stop At Read

The SDRAM can output data continuously from the burst start address (a) to location a + 255 during a read cycle in which the burst length is set to full page. The SDRAM repeats the operation starting at the 256th cycle with the data output returning to location (a) and continuing with a+1, a+2, a+3, etc. A burst stop command must be executed to terminate this cycle. A precharge command must be executed within the ACT to PRE command period (tRAS max.) following the burst stop command. After the period (t_{RBD}) required for burst data output to stop following the execution of the burst stop command has elapsed, the outputs go to the HIGH impedance state. This period t_{RBD} is two clock cycles when the /CAS latency is two and three clock cycle when the /CAS latency is three.

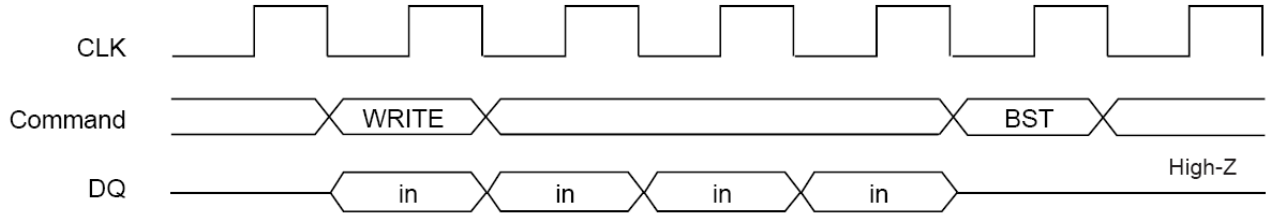
/CAS Latency	3	2
t_{RBD}	3	2



Burst Stop At Read Operation (Burst Length = Full, /CAS Latency = 2, 3)

Burst Stop At Write

The SDRAM can input data continuously from the burst start address (a) to location a + 255 during a write cycle in which the burst length is set to full page. The SDRAM repeats the operation starting at the 256th cycle with the data input returning to location (a) and continuing with a+1, a+2, a+3, etc. A burst stop command must be executed to terminate this cycle. A precharge command must be executed within the ACT to PRE command period (tRAS max.) following the burst stop command. After the period (t_{WBD}) required for burst data input to stop following the execution of the burst stop command has elapsed, the write cycle terminates. This period t_{WBD} is zero clock cycle, regardless of the /CAS latency.

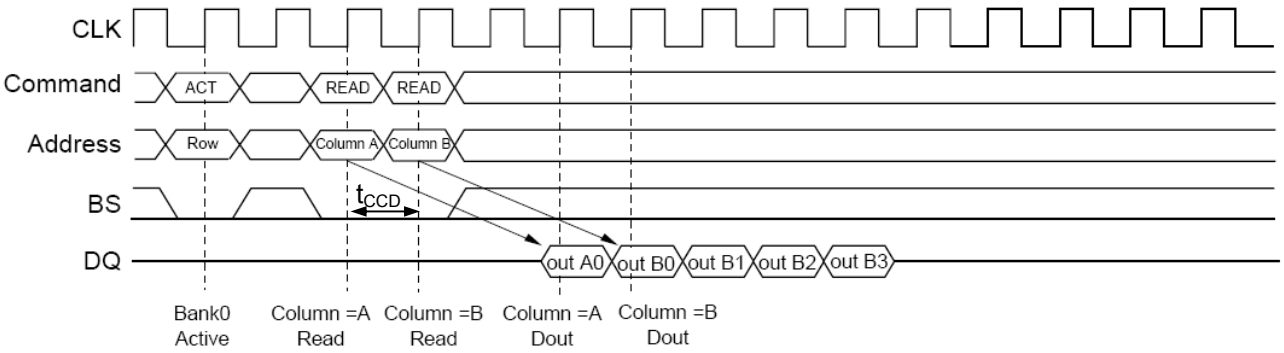


Burst Stop At Write Operation (Burst Length = Full, /CAS Latency = 2, 3)

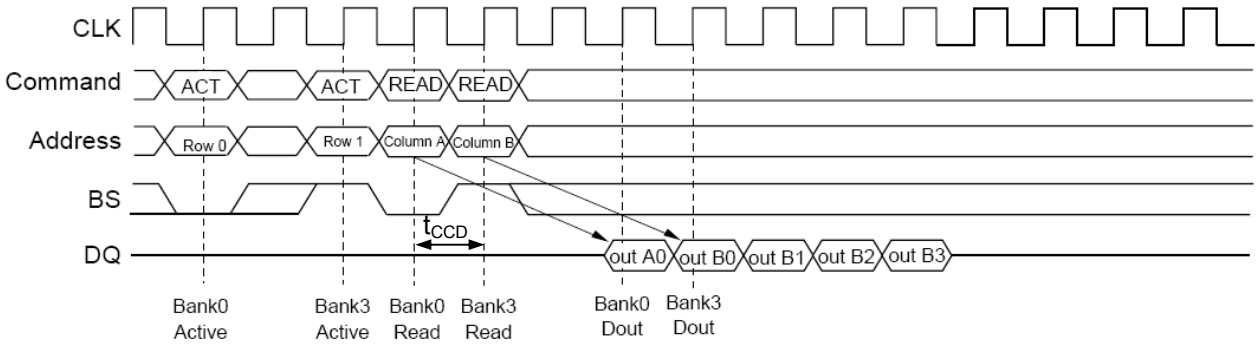
Command Intervals

Read To Read Interval

A new command can be executed while a read cycle is in progress, i.e. before that cycle completes. When the second read command is executed, after the /CAS latency has elapsed, data corresponding to the new read command is output in place of the data due to the previous read command. The interval between two read commands (t_{CCD}) must be at least one clock cycle. The selected bank must be set to the active state before executing this command.



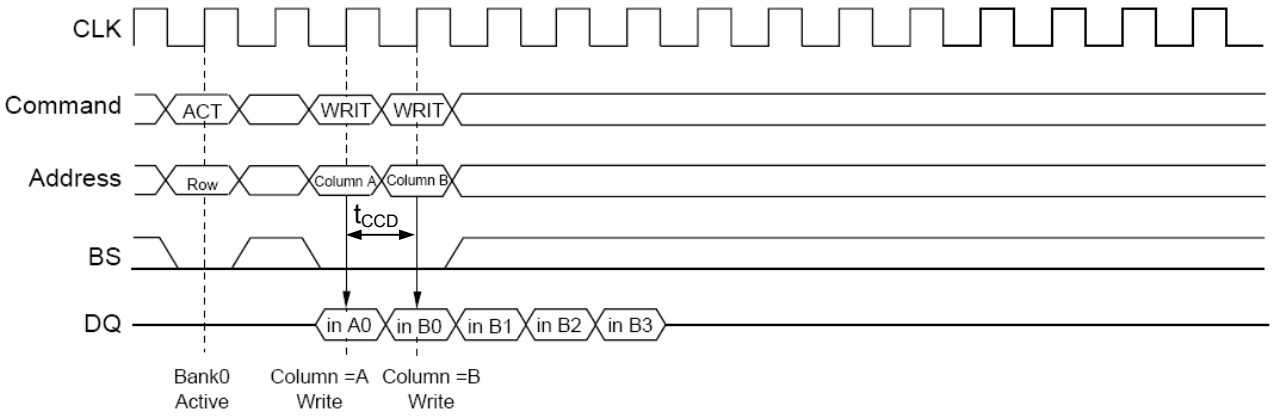
Read To Read Command Interval, Same ROW address in same bank (Burst Length = 4, /CAS Latency = 3)



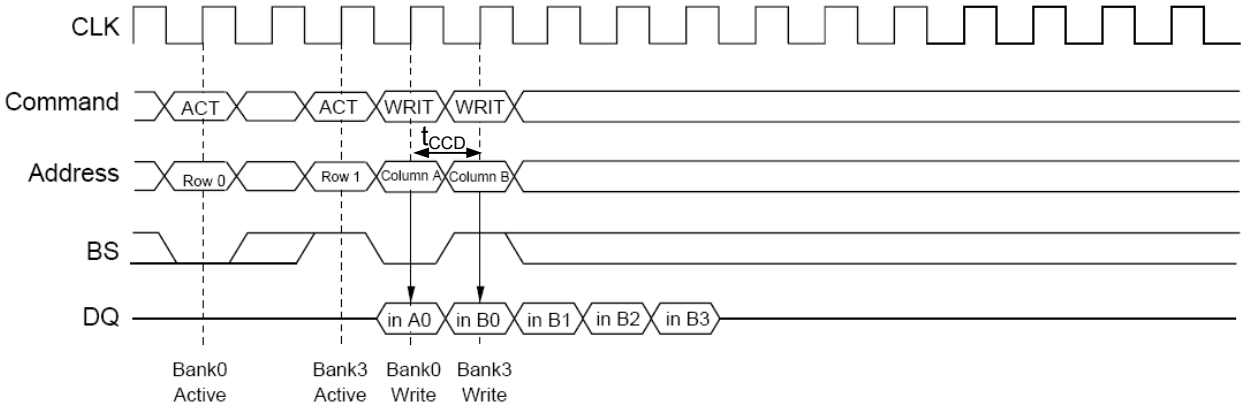
Read To Read Command Interval, different bank (Burst Length = 4, /CAS Latency = 3)

Write To Write Interval

A new command can be executed while a write cycle is in progress, i.e. before that cycle completes. When the second read command is executed, data corresponding to the new write command can be input in place of the data due for the previous write command. The interval between two write commands (t_{CCD}) must be at least one clock cycle. The selected bank must be set to the active state before executing this command.



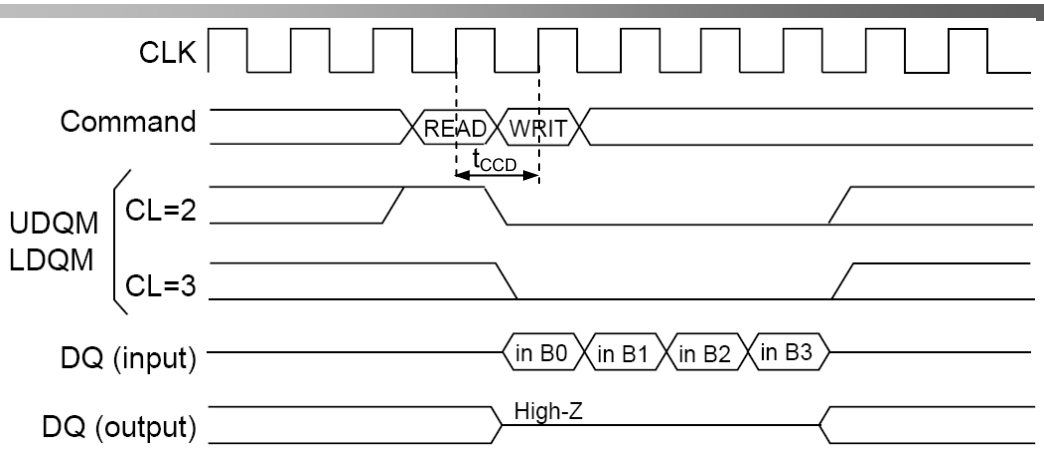
Write To Write Command Interval, Same ROW address in same bank (Burst Length = 4, /CAS Latency = 2, 3)



Write To Write Command Interval, different bank (Burst Length = 4, /CAS Latency = 2, 3)

Read To Write Interval

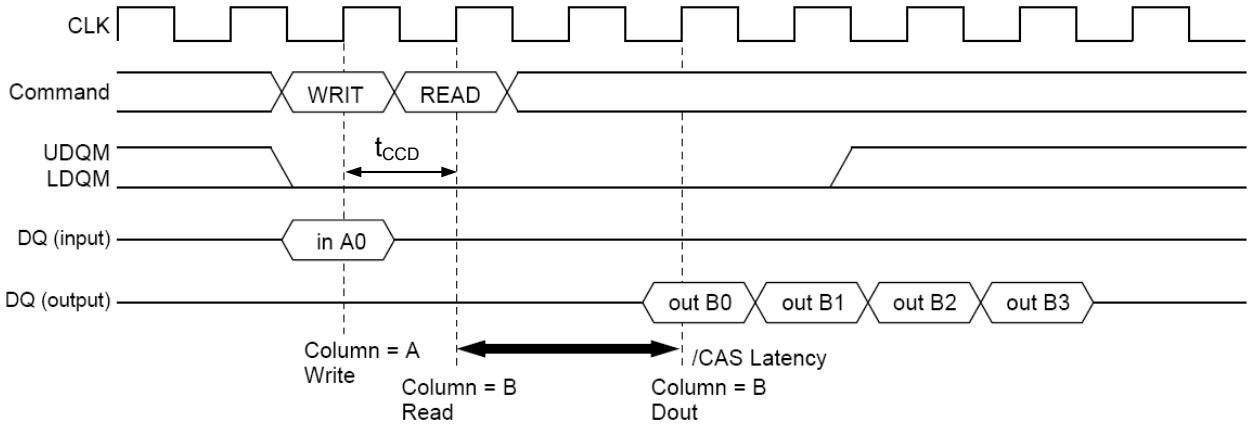
A read command can be interrupted and a new write command executed while the read cycle is in progress, i.e. before that cycle completes. Data corresponding to the new write command can be input at the point new write command is executed. To prevent collision between input and output data at the DQn pins during this operation, the output data must be masked using the U/LDQM pins. The interval (t_{CCD}) between these commands must be at least on clock cycle. The selected bank must be set to the active state before executing this command.



Read To Write Command Interval (Burst Length = 4, /CAS Latency = 2)

Write To Read Interval

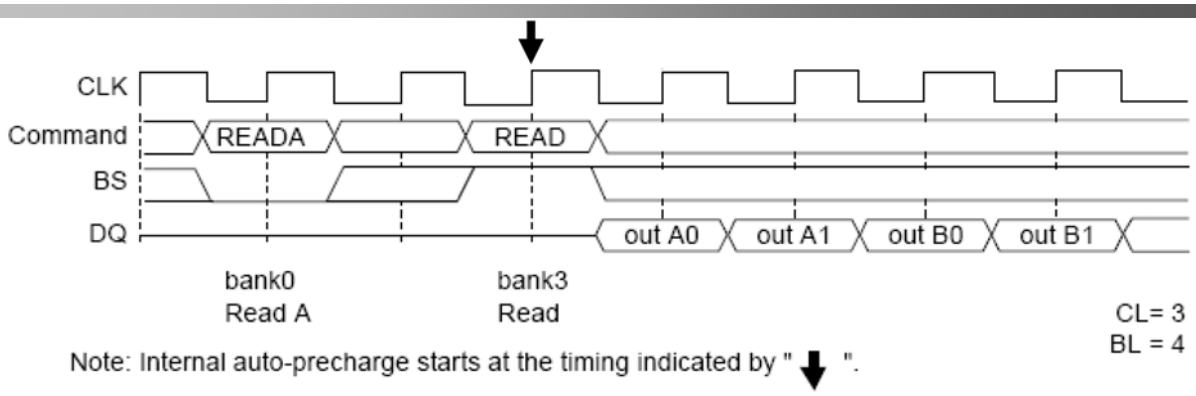
A new command can be executed while the read a write cycle is in progress, i.e. before that cycle completes. Data corresponding to the new read command is output after the /CAS latency has elapsed from the point the new read command was executed. The I/On pins must be placed in the HIGH impedance state at least one cycle before data is output during this operation. The interval (t_{CCD}) between these commands must be at least on clock cycle. The selected bank must be set to the active state before executing this command.



Write To Read Command Interval (Burst Length = 4, /CAS Latency = 2)

Read with auto precharge to Read command interval (concurrent auto-precharge)

1. Different bank: When some banks are in the active state, the second read command (another bank) is executed. Even when the first read with auto-precharge is a burst read that is not yet finished, the data read by the second command is valid. The internal auto-precharge of one bank starts at the clock of the second command.

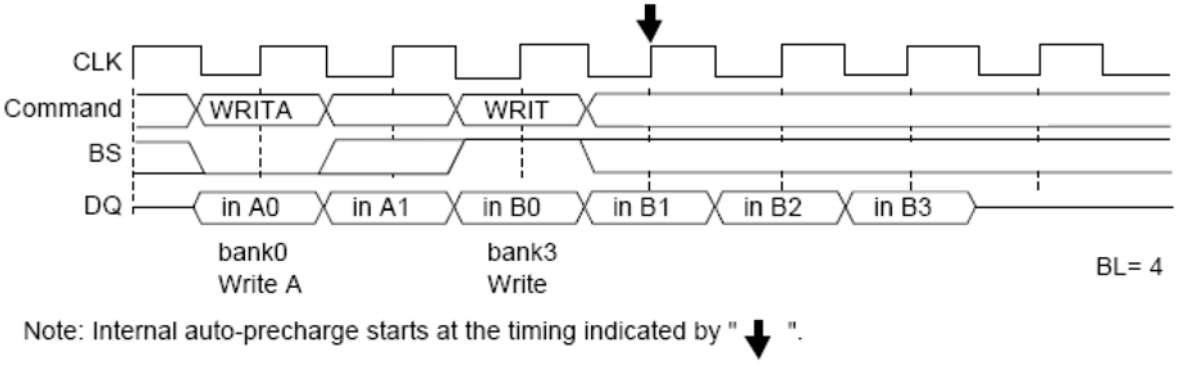


Read with Auto Precharge to Read Command Interval (Different bank)

2. Same bank: The consecutive read command (the same bank) is illegal.

Write with auto precharge to Write command interval (concurrent auto-precharge)

1. Different bank: When some banks are in the active state, the second write command (another bank) is executed. In the case of burst writes, the second write command has priority. The internal auto-precharge of one bank starts at the next clock of the second command.

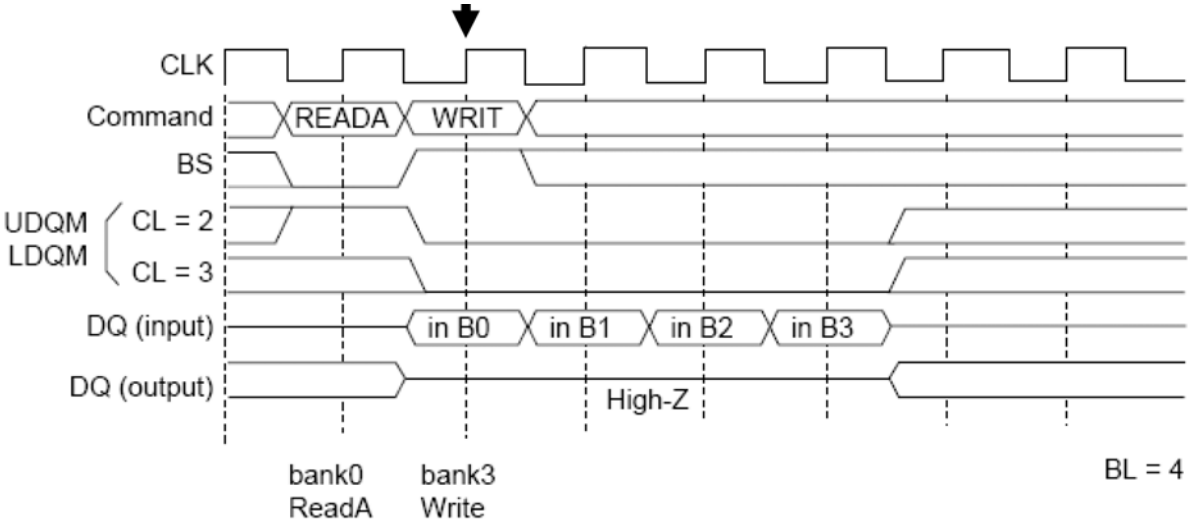


Write with Auto Precharge to Write Command Interval (Different bank)

2. Same bank: The consecutive write command (the same bank) is illegal.

Read with auto precharge to Write command interval (concurrent auto-precharge)

1. Different bank: When some banks are in the active state, the second write command (another bank) is executed. However, DQMU and DQML must be set High so that the output buffer becomes High-Z before data input. The internal auto-precharge of one bank starts at the clock of the second command.



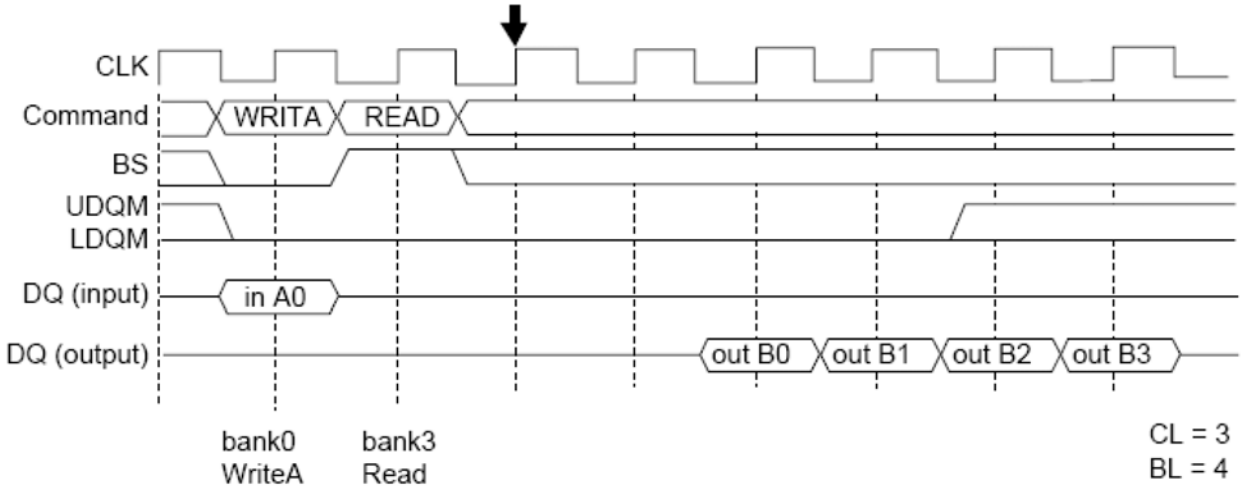
Note: Internal auto-precharge starts at the timing indicated by " ↓ ".

Read with Auto Precharge to Write Command Interval (Different bank)

2. Same bank: The consecutive write command from read with auto precharge (the same bank) is illegal. It is necessary to separate the two commands with a bank active command.

Write with auto precharge to Read command interval (concurrent auto-precharge)

1. Different bank: When some banks are in the active state, the second read command (another bank) is executed. However, in case of a burst write, data will continue to be written until one clock before the read command is executed. The internal auto-precharge of one bank starts at the next clock of the second command.



Note: Internal auto-precharge starts at the timing indicated by " ↓ ".

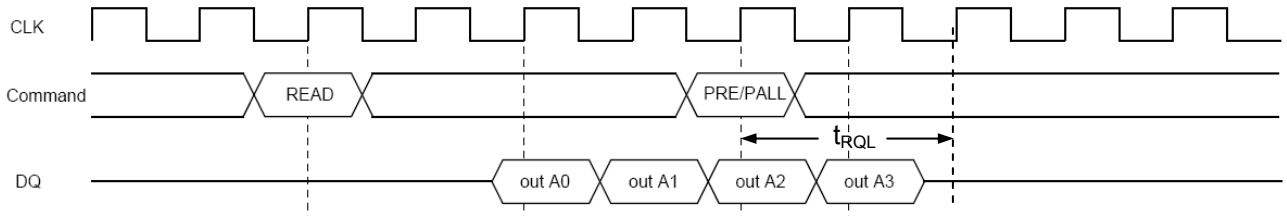
Write with Auto Precharge to Read Command Interval (Different bank)

2. Same bank: The consecutive read command from write with auto precharge (the same bank) is illegal. It is necessary to separate the two commands with a bank active command.

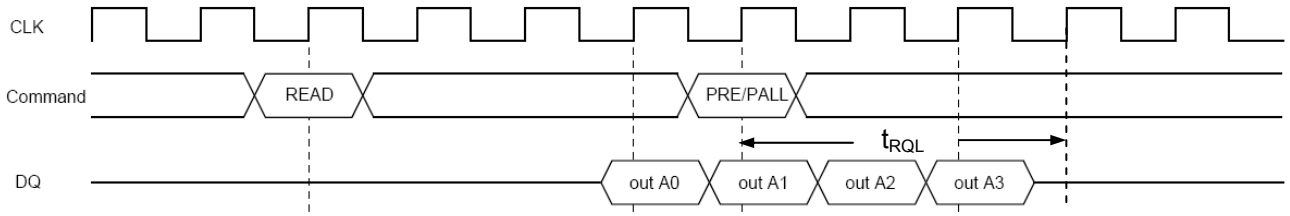
Read To Precharge Interval

A read cycle can be interrupted by the execution of the precharge command before that cycle completes. The delay time (t_{RQL}) from the execution of the precharge command to the completion of the burst output is the clock cycle /CAS latency.

/CAS Latency	3	2
t_{RQL}	3	2



Read To Precharge Command Interval (Burst Length = 4, /CAS Latency = 2)

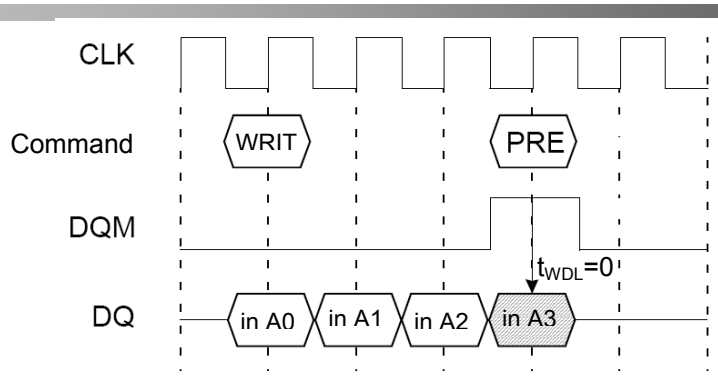


Read To Precharge Command Interval (Burst Length = 4, /CAS Latency = 3)

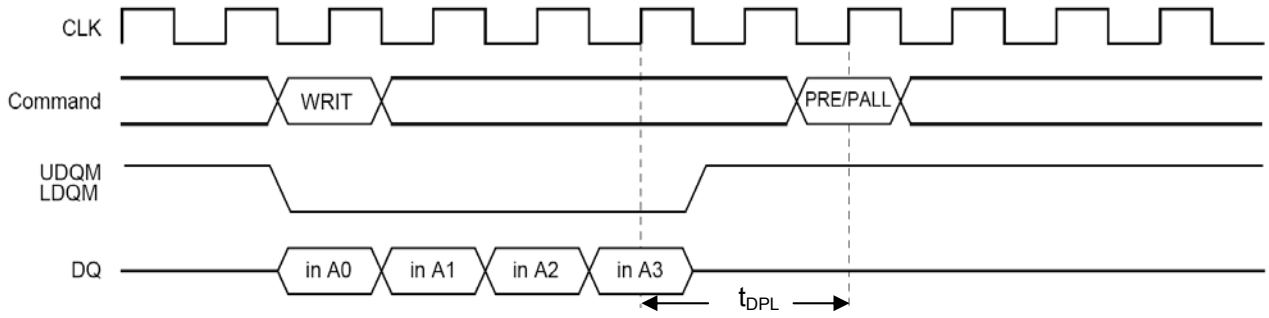
Write To Precharge Interval

A write cycle can be interrupted by the execution of the precharge command before that cycle completes. The delay time (t_{WDL}) from the precharge command to the point where burst input is invalid, i.e. the point where input data is no longer written to device internal memory is zero clock cycle regardless of the /CAS latency. To inhibit invalid write, the DQM signal must be asserted HIGH with the precharge command. This precharge command and burst write command must be of the same bank, otherwise it is not precharge interrupt but only another bank precharge of dual bank operation. Inversely, to write all the burst data to the device, the precharge command must be executed after the write data recovery period (t_{DPL}) has elapsed. Therefore, the precharge command must be executed on one clock cycle that follows the input of the last burst data item.

/CAS Latency	3	2
t_{WDL}	0	0
t_{DPL}	2	2



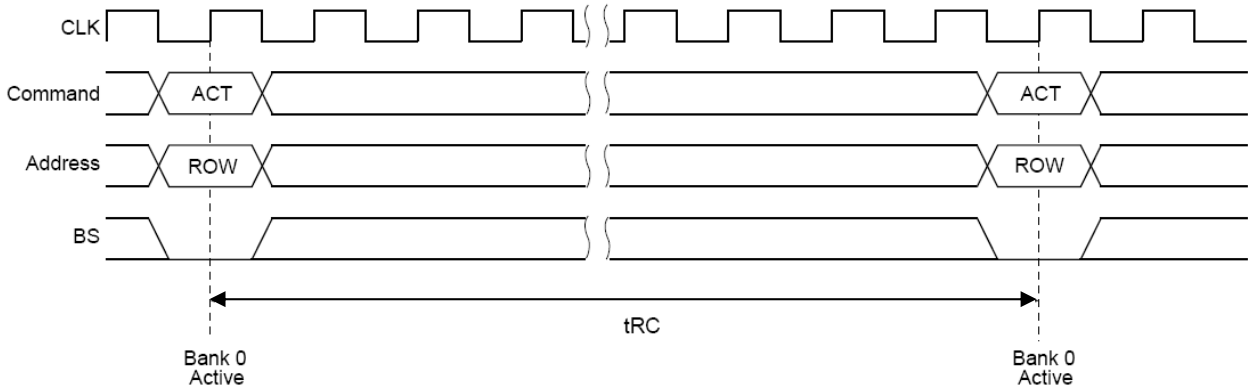
Write To Precharge Command Interval masked by DQM (Burst Length = 4, /CAS Latency = 2)



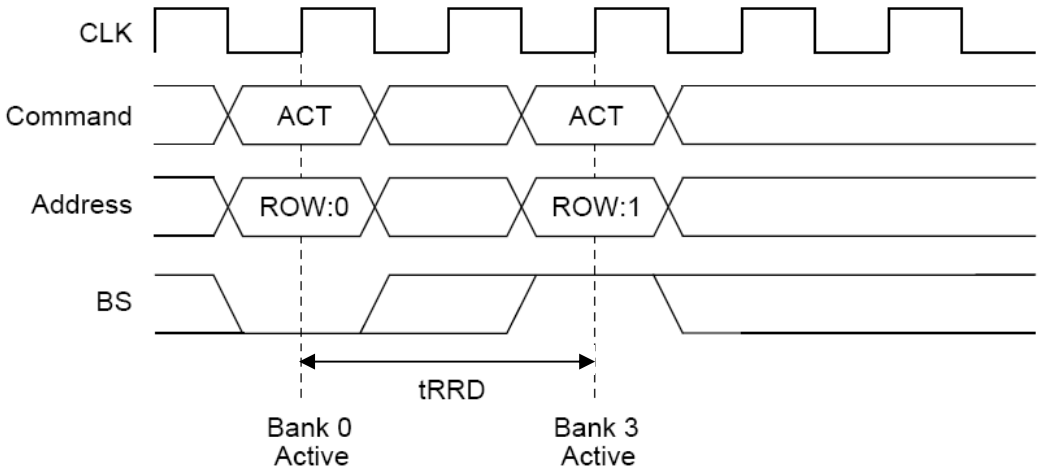
Write To Precharge Command Interval (Burst Length = 4, /CAS Latency = 3)

Bank Active Command Interval

The interval between the two bank active commands must be no less than t_{RC}. In the case of different bank active commands, the interval between the two bank active commands must be no less than t_{RRD}.



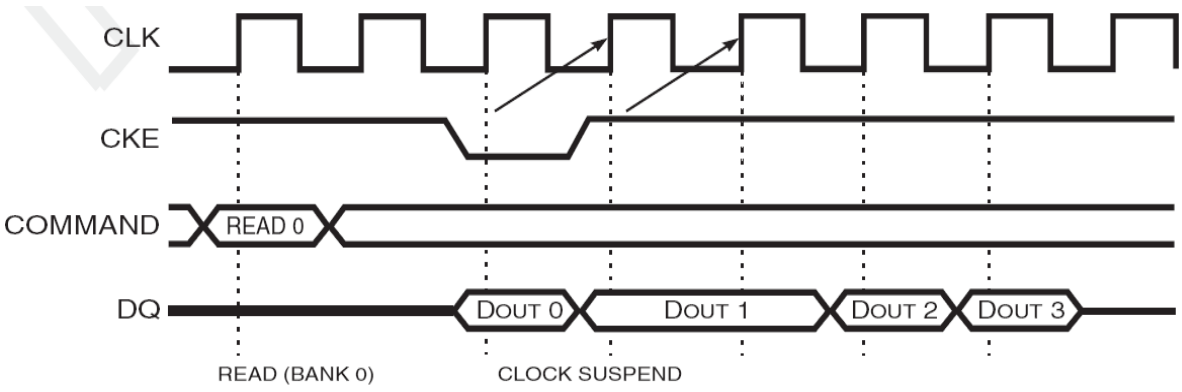
Bank Active to Bank Active for the same bank



Bank Active to Bank Active for the different bank

Clock Suspend

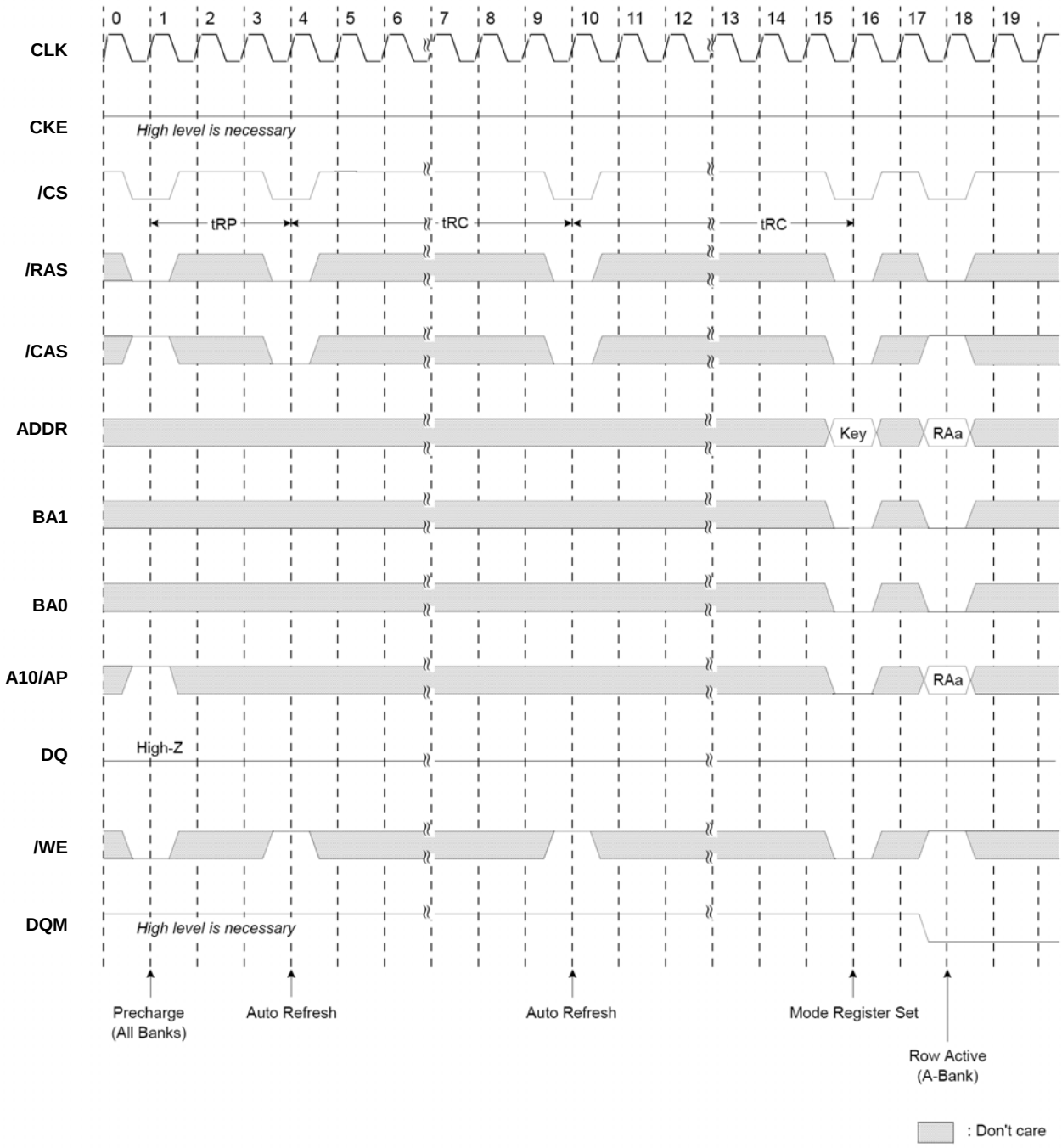
When the CKE pin is dropped from HIGH to LOW during a read or write cycle, the SDRAM enters clock suspend mode on the next CLK rising edge. This command reduced the device power dissipated by stopping the device internal clock. Clock suspend mode continues as long as the CKE pin remains low. In this state, all inputs other than CKE pin are invalid and no other commands can be executed. Also, the device internal states are maintained. When the CKE pin goes from LOW to HIGH clock suspend mode is terminated on the next CLK rising edge and device operation resumes. The next command cannot be executed until the recovery period (t_{CKA}) has elapsed. Since this command differs from Self Refresh command described previously in that the refresh operation is no performed automatically internally, the refresh operation must be performed within in the refresh period (t_{REF}). Thus the maximum time that clock suspend mode can be held is just under the refresh cycle time.



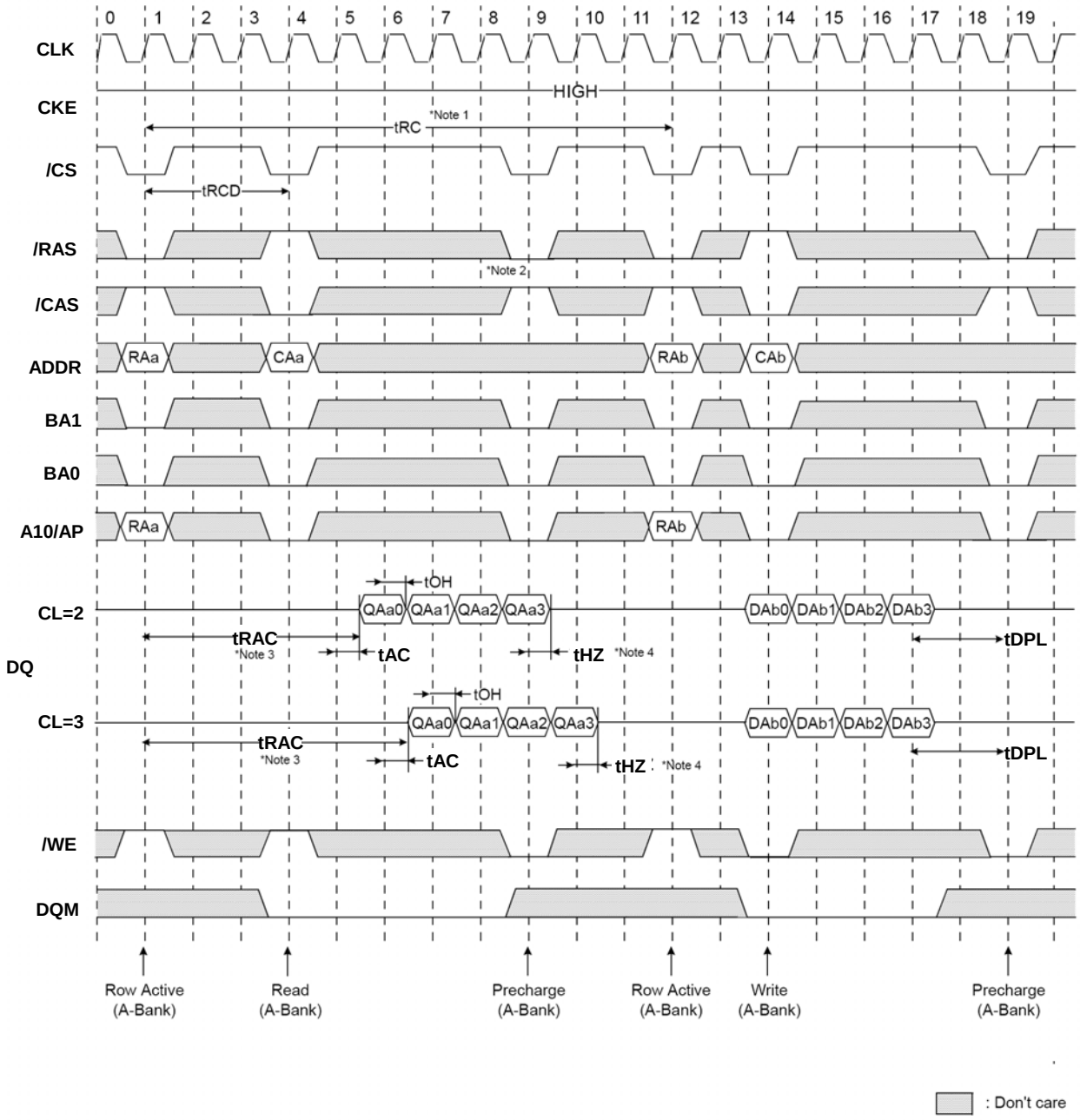
Clock Suspend (Burst Length = 4, /CAS Latency = 2)

Timing Waveforms

Power Up Sequence



Read & Write Cycle at Same Bank @ Burst Length = 4

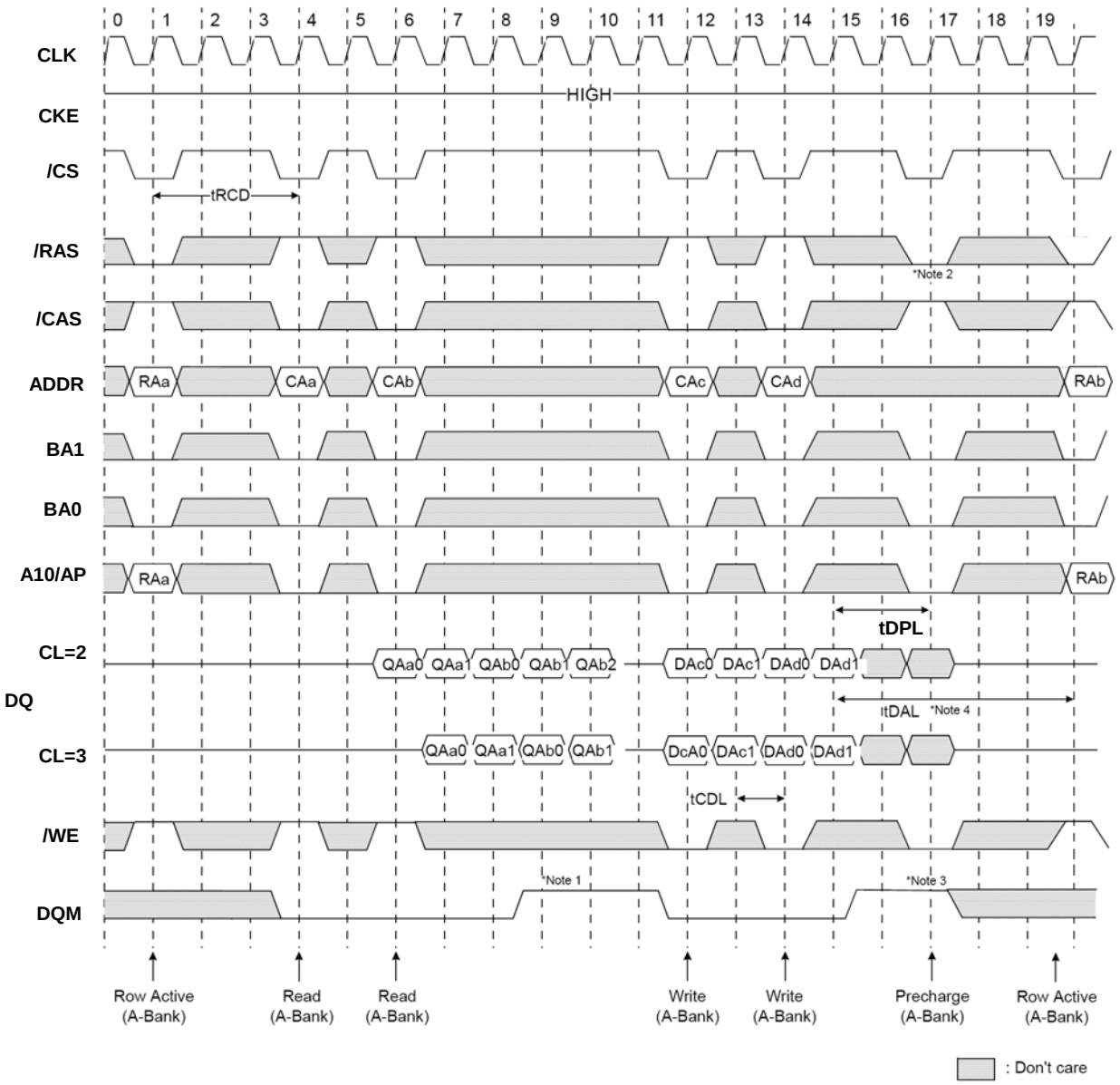


Note:

1. Minimum row cycle time is required to complete internal DRAM operation.
2. Row precharge can interrupt burst on any cycle. [CAS Latency -1] number of valid output data is available after row precharge. Last valid output will be HIGH Z (t_{HZ}) after the clock.
3. Access time from row active command $t_{RAC} = t_{RCD}$ + /CAS latency -1) + t_{AC}.
4. Output will be HIGH Z after the end of burst (1, 2, 4, 8, & Full Page burst).

A10/AP

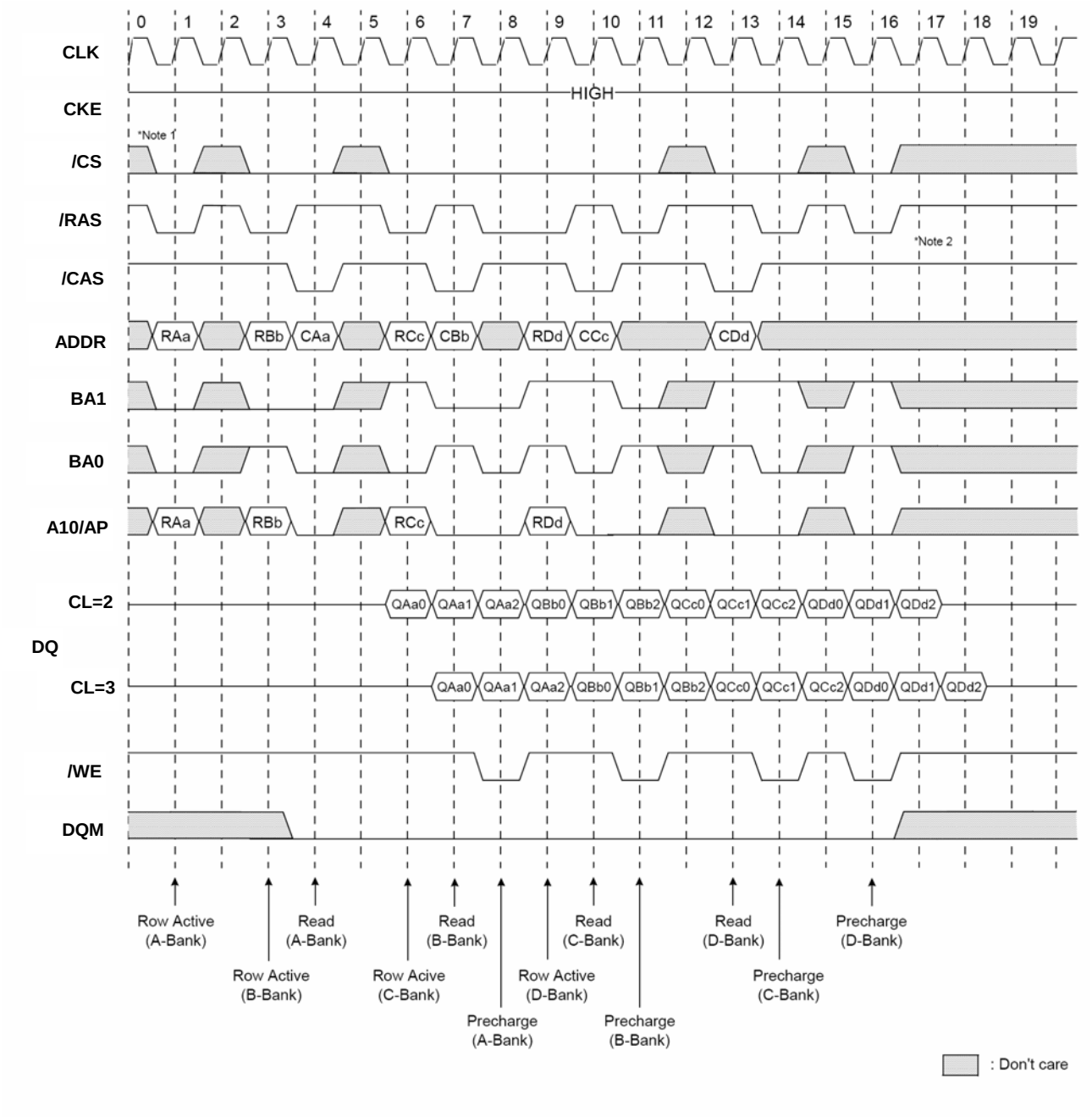
Page Read & Write Cycle at Same Bank @ Burst Length = 4



Note:

1. To write data before burst read ends, DQM should be asserted three cycle prior to write command to avoid bus contention.
2. Row precharge will interrupt writing. Last data input, t_{DPL} before row precharge, will be written.
3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after row precharge cycle will be masked internally.
4. t_{DAL}, last data in to active delay, is 2CLK + t_{RP}.

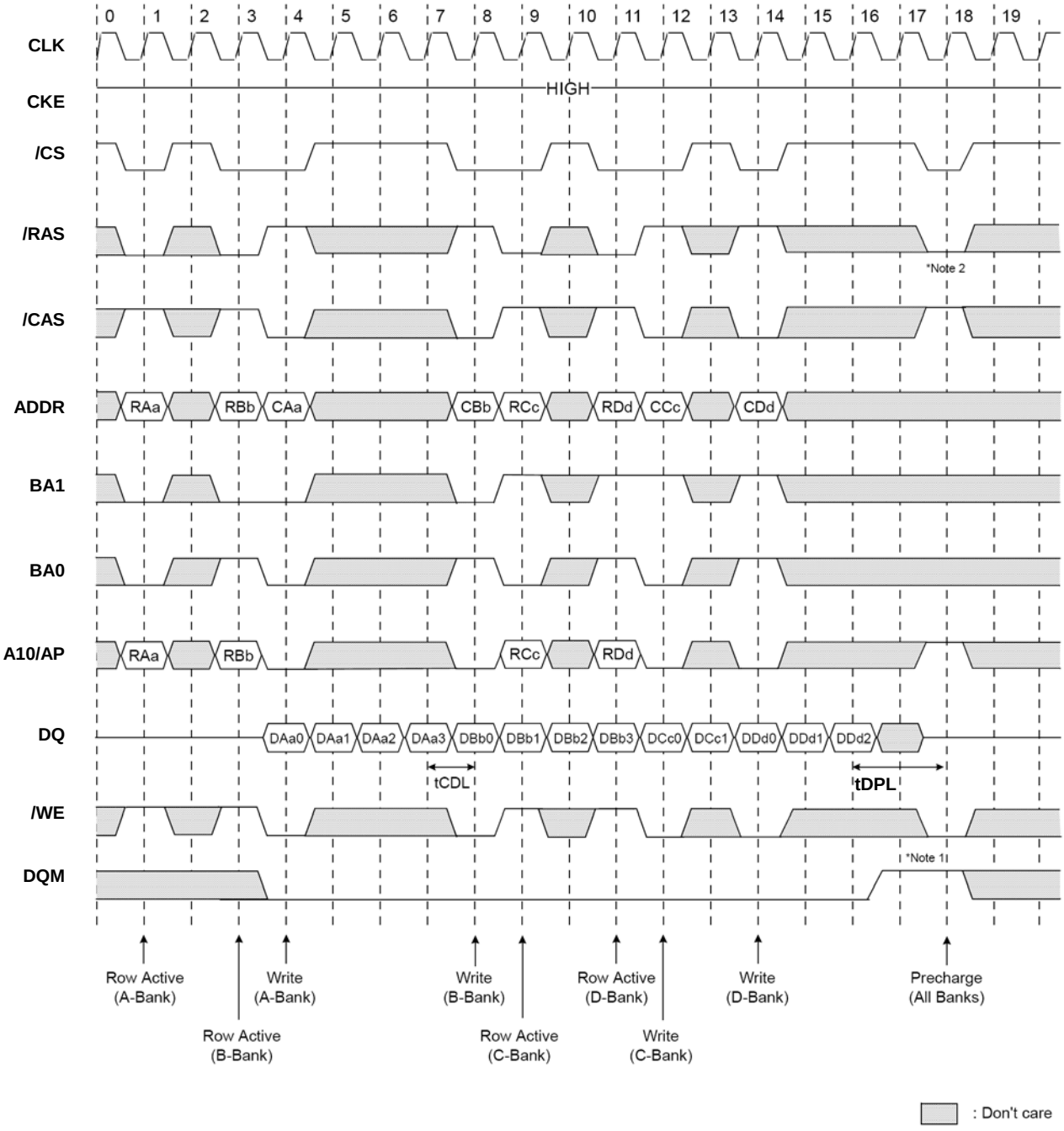
Page Read Cycle at Different Bank @ Burst Length = 4



Note:

1. /CS can be Don't Care when /RAS, /CAS, and /WE are HIGH at the clock going edge.
2. To interrupt a burst read by row precharge, both the read and the precharge banks must be the same.

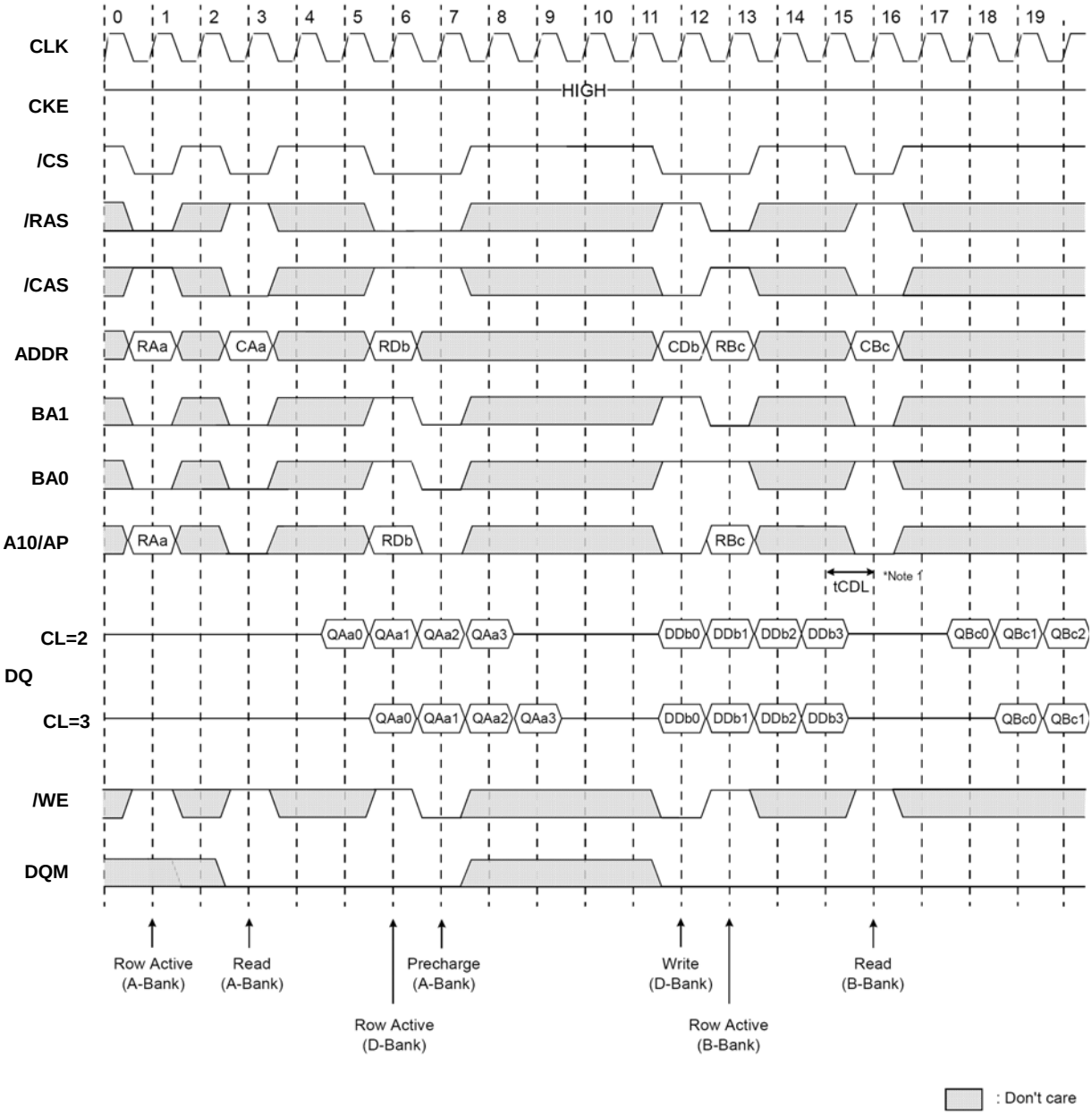
Page Write Cycle at Different Bank @ Burst Length = 4



Note:

1. To interrupt a burst write by row precharge, DQM should be asserted to mask invalid input data.
2. To interrupt a burst write by row precharge, both the write and the precharge banks must be the same.

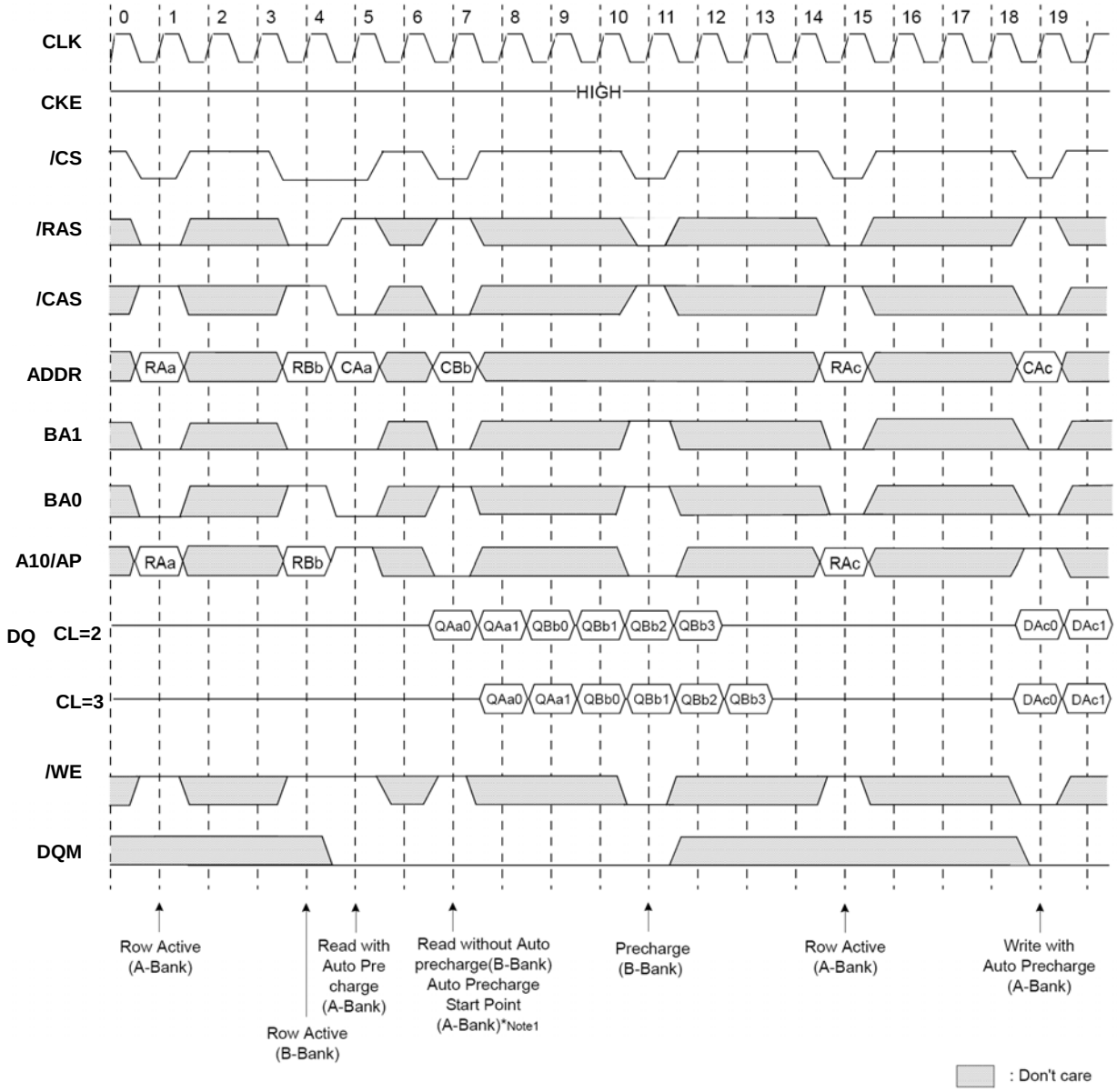
Read & Write Cycle at Different Bank @ Burst Length = 4



Note:

1. t_{CDL} should be met to complete write.

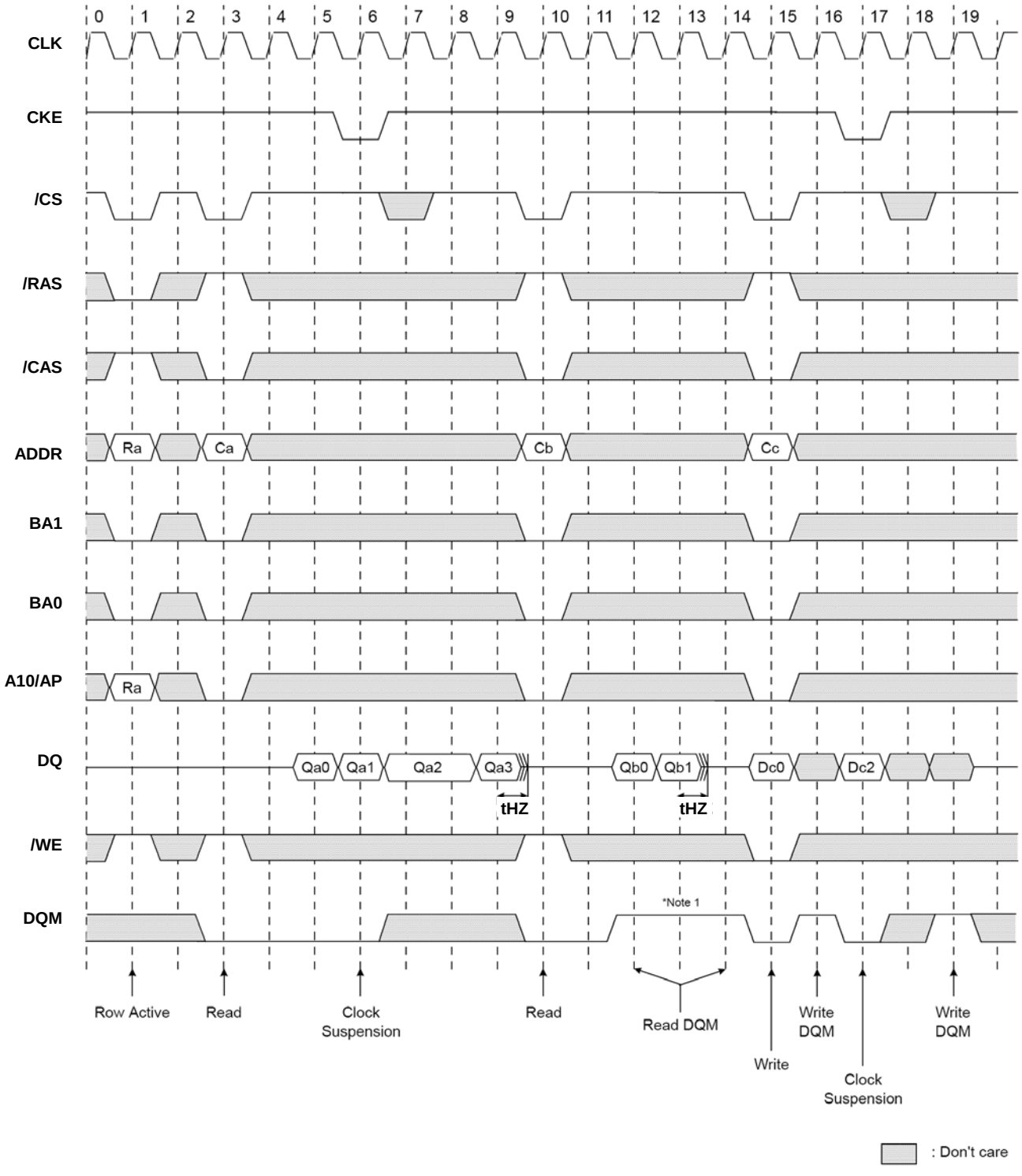
Read & Write Cycle with Auto Precharge @ Burst Length = 4



Note:

1. t_{CDL} should be controlled to meet minimum t_{RAS} before internal precharge start. (In the case of burst length = 1 & 2)

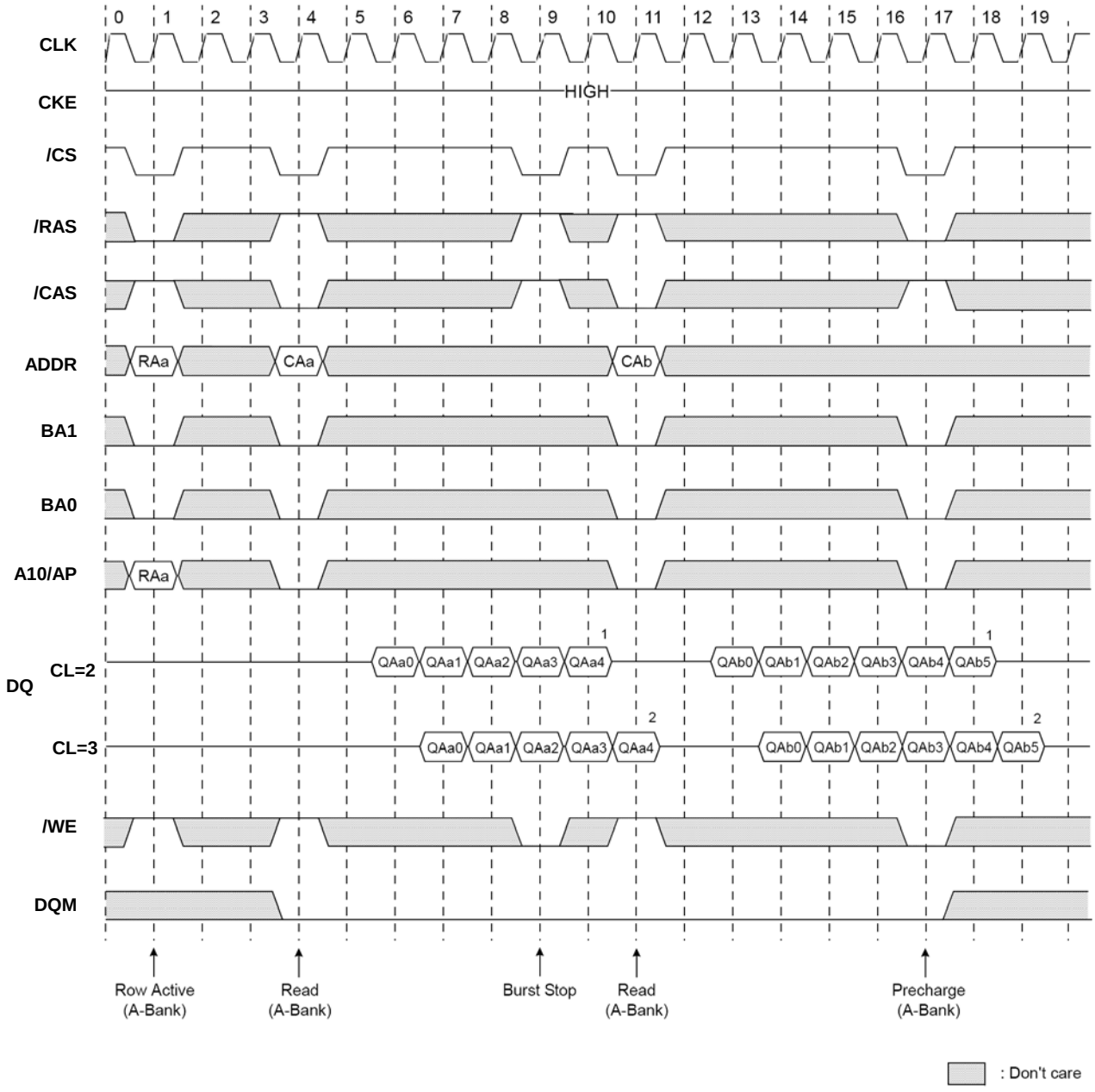
Clock Suspend & DQM Operation Cycle @ /CAS Latency = 2, Burst Length = 4



Note:

1. DQM is needed to prevent bus contention.

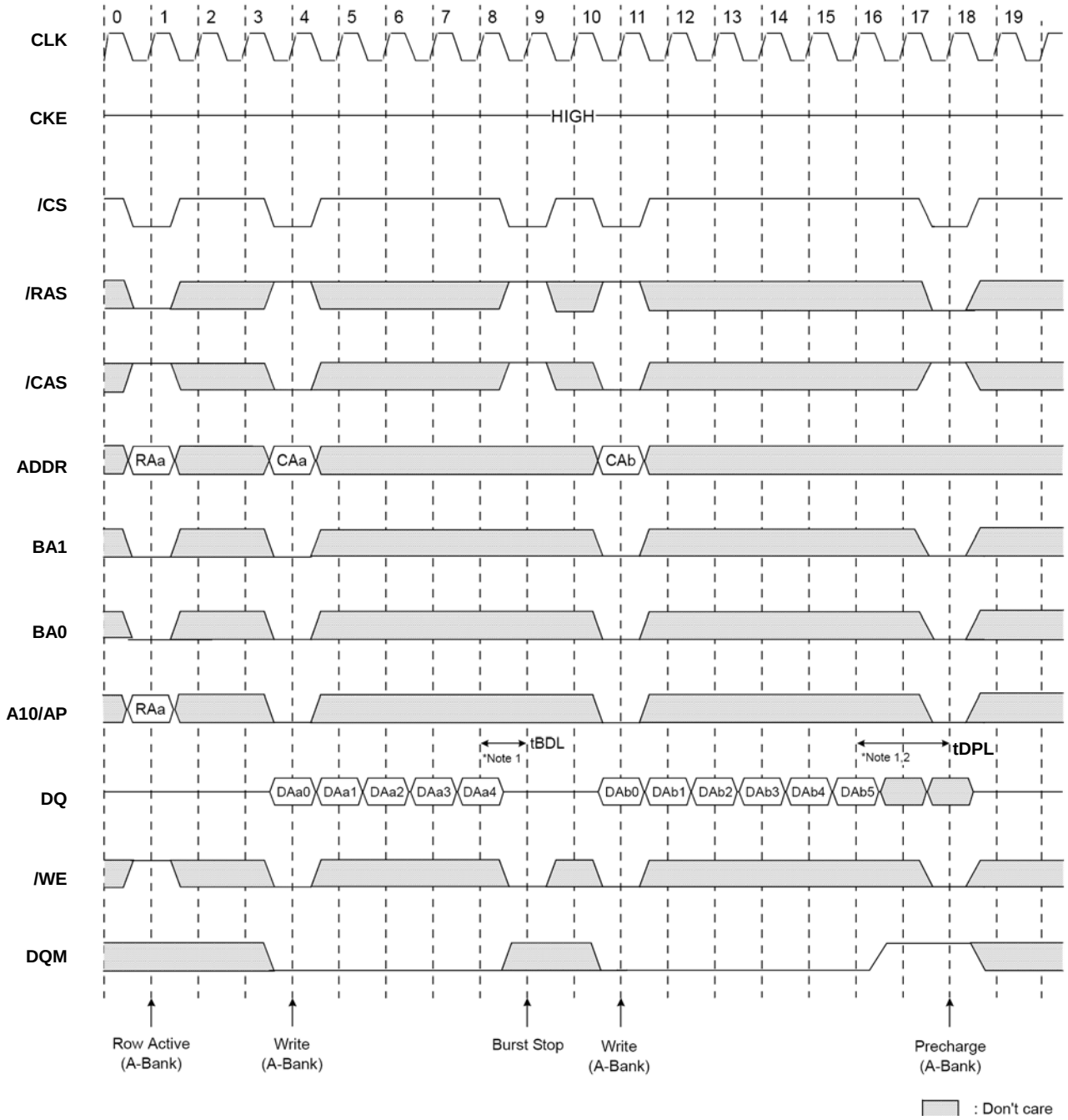
Read Interrupted by Precharge Command & Read Burst Stop Cycle @ Full Page Burst



Note:

1. At full page mode, burst is finished by burst stop or precharge.
2. About the valid DQs after burst stop, it is same as the case of /RAS interrupt.
   Both cases are illustrated above timing diagram. See the label 1, 2, on them.
   But at burst write, burst stop and /RAS interrupt should be compared carefully.
   Refer to the timing diagram of “Full Page Write Burst Stop Cycle”.
3. Burst stop is valid at every burst length.

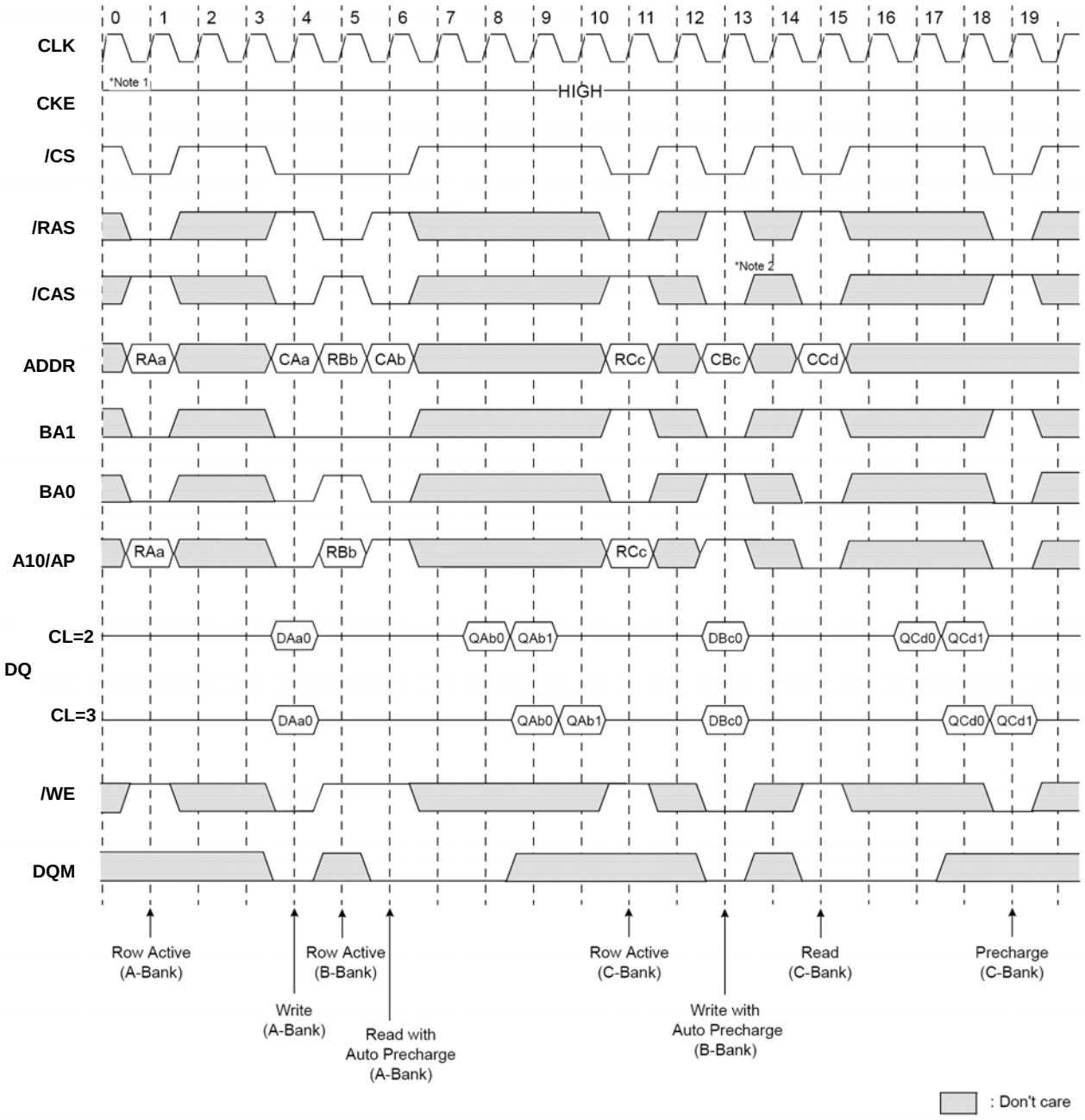
Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Full Page Burst



Note:

1. At full page mode, burst is finished by burst stop or precharge.
2. Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell. It is defined by AC parameter of t_{DPL}. DQM at write interrupted by precharge command is needed to prevent invalid write. DQM should mask invalid data on precharge command cycle when asserting precharge before end of burst. Input data after row precharge cycle will be masked internally.
3. Burst stop is valid at every burst length.

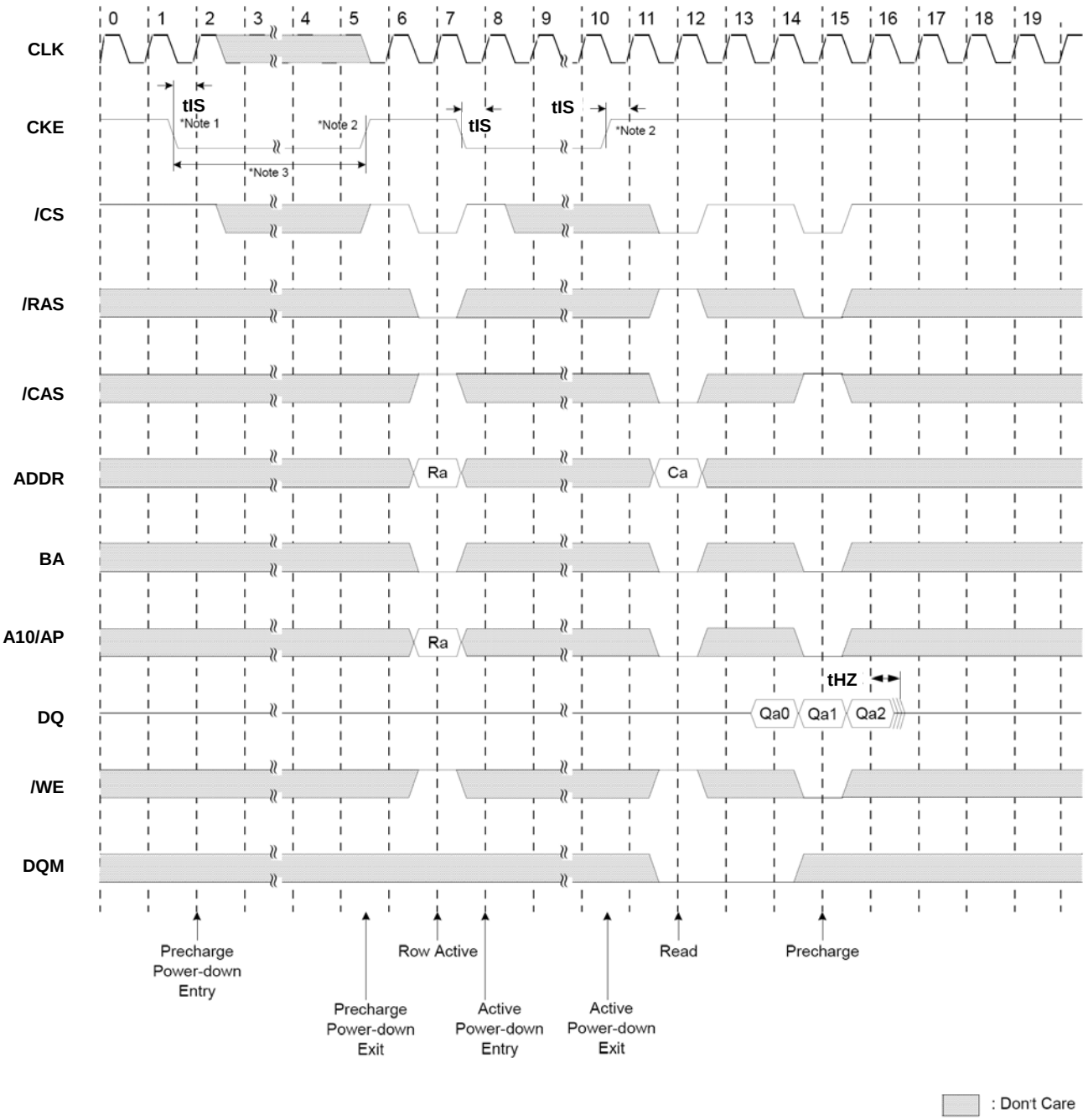
Burst Read Single Bit Write Cycle @ Burst Length = 2



Note:

1. BRSW modes is enabled by setting A9 HIGH at MRS (Mode Register Set). At the BRSE Mode, the burst length at write is fixed to "1" regardless of programmed burst length.
2. When BRSW write command with Auto Precharge is executed, keep it in mind that t_{RAS} should not be violated. Auto Precharge is executed at the burst end cycle, so in the case of BRSW write commend, the next cycle starts the precharge.

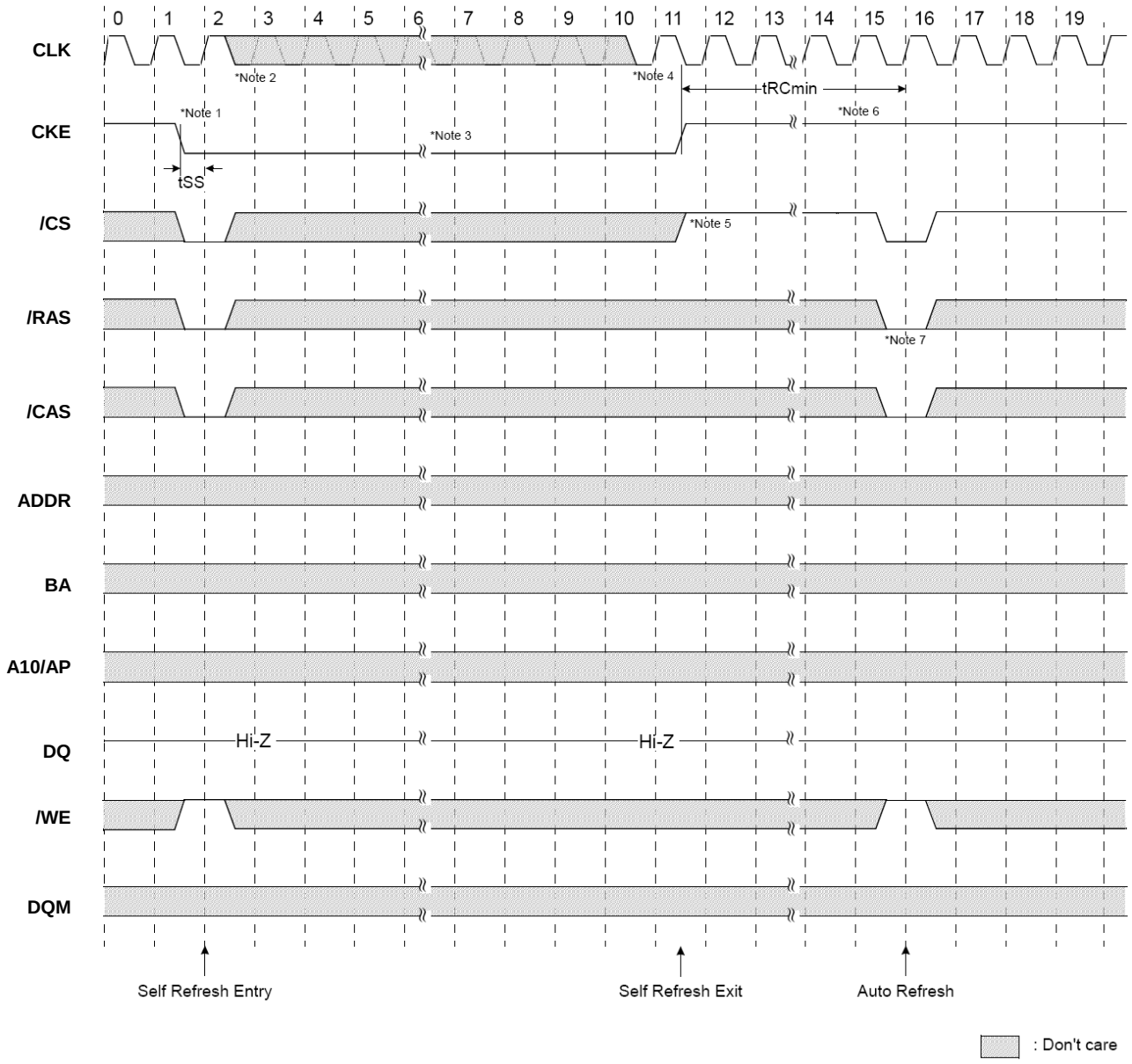
Active/Precharge Power Down Mode @ /CAS Latency = 2, Burst Length = 4



Note:

1. All banks should be in idle state prior to entering precharge power down mode.
2. CKE should be set high at least 1CLK + t_{IS} prior to row active command.
3. Can not violate minimum refresh specification (64ms).

Self Refresh Entry and Exit Cycle



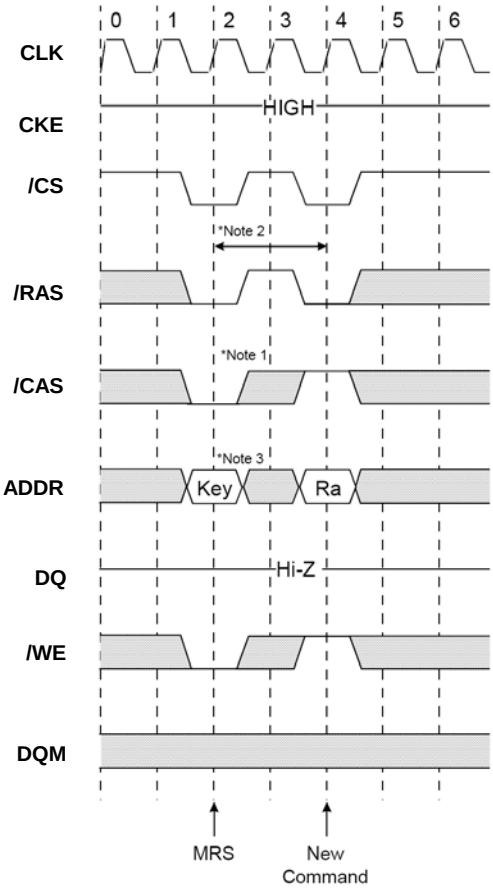
Note: To Enter Self Refresh Mode

1. /CA, /RAS, /CAS with CKE should be LOW at the same clock cycle.
2. After 1 clock cycle, all of the inputs including the system clock can be “Don’t Care” except for CKE.
3. The SDRAM remains in Self Refresh mode as long as CKE stays LOW. Once the device enters Self Refresh mode, minimum tRAS is required before exit from Self Refresh.

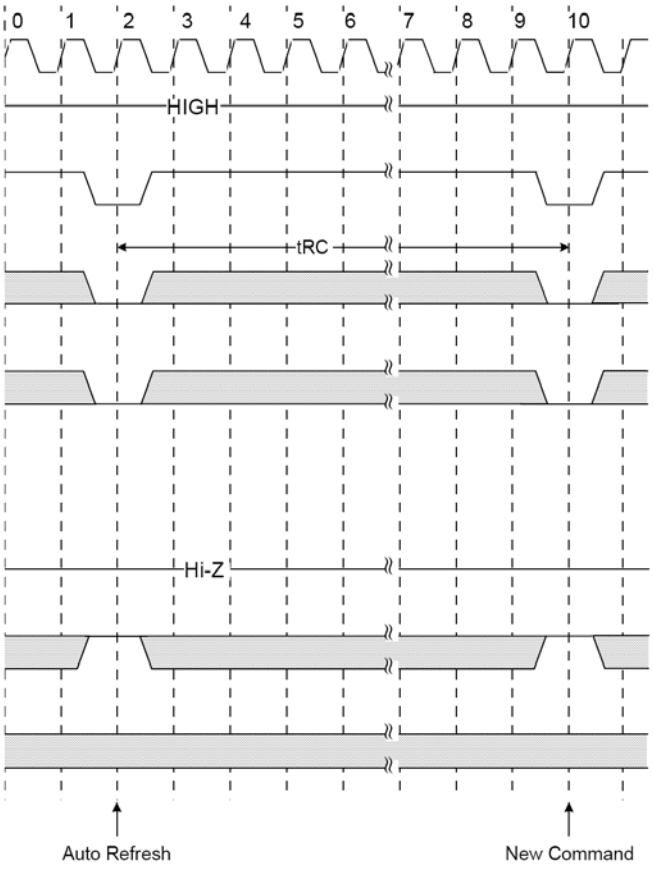
Note: To Exit Self Refresh Mode

4. System clock restart and be stable before returning CKE HIGH.
5. /CAS starts from HIGH.
6. Minimum tRC is required after CKE going HIGH to complete Self Refresh exit.
7. 8K cycles of burst auto refresh is required before Self Refresh entry and after Self Refresh exit if the system uses burst refresh

Mode Register Set Cycle



Auto Refresh Cycle



: Don't care

Note:

1. All banks precharge should be completed before Mode Register Set cycle and Auto Refresh cycle.
2. Mode Register Set cycle
   (a) /CAS, /RAS, /CAS, & /WE activation at the same clock cycle with address key will set internal mode register.
   (b) Minimum 2 clock cycles should be met before new /RAS activation.
   (c) Please refer to Mode Register table.

Package Dimensions

(400mil; 54 lead; Thin Small Outline Package)