Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a small SOT23 (TO-236AB) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Low on-state resistance
- Trench MOSFET technology
- Enhanced power dissipation capability of 1096 mW

3. Applications

- Relay driver
- High-speed line driver
- High-side loadswitch
- Switching circuits

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{DS}	drain-source voltage	T _j = 25 °C		-	-	-20	V
V _{GS}	gate-source voltage			-12	-	12	V
I _D	drain current	$V_{GS} = -4.5 \text{ V}; T_{amb} = 25 \text{ °C}; t \le 5 \text{ s}$	[1]	-	-	-4.4	Α
Static charac	Static characteristics						
R _{DSon}	drain-source on-state resistance	V_{GS} = -4.5 V; I_D = -3.6 A; T_j = 25 °C		-	48	60	mΩ

^[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².



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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	3	D
2	S	source		
3	D	drain	1 2	G S S 017aaa257
			TO-236AB (SOT23)	

6. Ordering information

Table 3. Ordering information

Type number	Package	ackage					
	Name	Description	Version				
PMV50XP	TO-236AB	plastic surface-mounted package; 3 leads	SOT23				

7. Marking

Table 4. Marking codes

Table II III III II II II II II II II II II	
Type number	Marking code
	[1]
PMV50XP	%2M

[1] % = placeholder for manufacturing site code

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-20	V
V _{GS}	gate-source voltage			-12	12	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	-4.4	Α
		V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-3.6	Α
		V _{GS} = -4.5 V; T _{amb} = 100 °C	[1]	-	-2.3	Α
I _{DM}	peak drain current	T_{amb} = 25 °C; single pulse; $t_p \le 10$ μs		-	-14.5	Α
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	490	mW
			[1]	-	1096	mW
		T _{sp} = 25 °C		-	4630	mW
Tj	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain o	liode					J.
Is	source current	T _{sp} = 25 °C	[1]	-	-1	Α

- Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

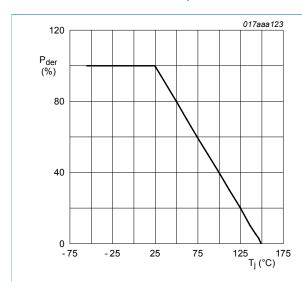


Fig. 1. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

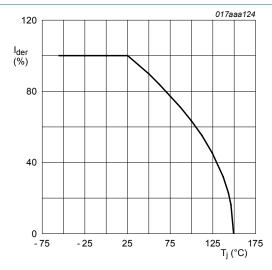


Fig. 2. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100 \%$$

PMV50XP

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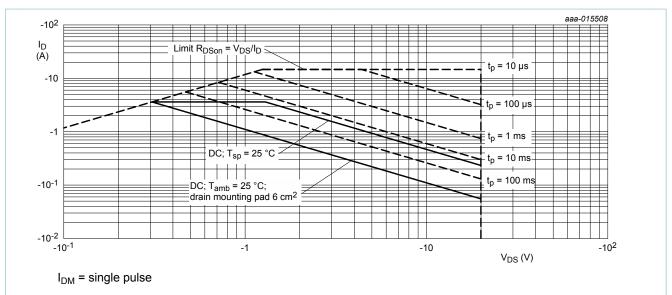


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	_	[1]	-	217	255	K/W
			<u>[2]</u>	-	97	114	K/W
		in free air; t ≤ 5 s	<u>[2]</u>	-	65	76	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	23	27	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

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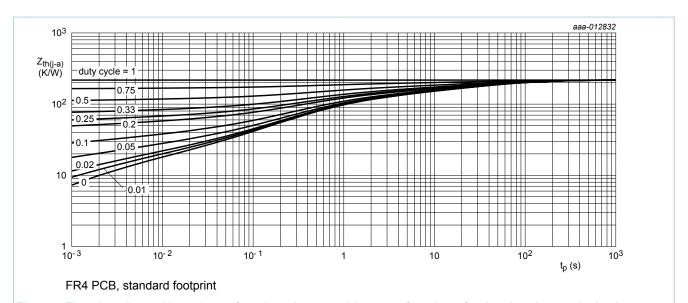


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

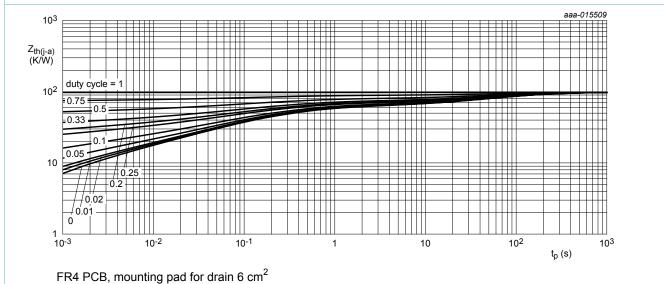


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

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10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = -250 μ A; V_{GS} = 0 V; T_j = 25 °C	-20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \ \mu A; \ V_{DS} = V_{GS}; \ T_j = 25 \ ^{\circ}C$	-0.47	-0.65	-0.9	V
I _{DSS}	drain leakage current	V _{DS} = -20 V; V _{GS} = 0 V; T _j = 25 °C	-	-	-1	μA
I _{GSS}	gate leakage current	V _{GS} = -12 V; V _{DS} = 0 V; T _j = 25 °C	-	-	-100	nA
		V _{GS} = 12 V; V _{DS} = 0 V; T _j = 25 °C	-	-	100	nA
R _{DSon}	drain-source on-state	V_{GS} = -4.5 V; I_D = -3.6 A; T_j = 25 °C	-	48	60	mΩ
	resistance	V _{GS} = -4.5 V; I _D = -3.6 A; T _j = 150 °C	-	68	86	mΩ
		V_{GS} = -2.5 V; I_D = -3.1 A; T_j = 25 °C	-	60	80	mΩ
		V _{GS} = -1.8 V; I _D = -0.8 A; T _j = 25 °C	-	82	121	mΩ
		V _{GS} = -1.5 V; I _D = -0.1 A; T _j = 25 °C	-	116	250	mΩ
9 _{fs}	forward transconductance	V_{DS} = -10 V; I_{D} = -2 A; T_{j} = 25 °C	-	9	-	S
Dynamic ch	naracteristics					
Q _{G(tot)}	total gate charge	V_{DS} = -6 V; I_{D} = -2.8 A; V_{GS} = -4.5 V;	-	7.7	12	nC
Q_{GS}	gate-source charge	T _j = 25 °C	-	1	-	nC
Q_{GD}	gate-drain charge		-	1.65	-	nC
C _{iss}	input capacitance	V _{DS} = -20 V; f = 1 MHz; V _{GS} = 0 V;	-	744	-	pF
C _{oss}	output capacitance	T _j = 25 °C	-	65	-	pF
C _{rss}	reverse transfer capacitance		-	53	-	pF
t _{d(on)}	turn-on delay time	V_{DS} = -6 V; V_{GS} = -4.5 V; $R_{G(ext)}$ = 6 Ω ;	-	7	-	ns
t _r	rise time	T _j = 25 °C; I _D = -1 A	-	18	-	ns
t _{d(off)}	turn-off delay time		-	135	-	ns
t _f	fall time		-	68	-	ns
Source-dra	in diode		l l	1	1	
V _{SD}	source-drain voltage	I _S = -1 A; V _{GS} = 0 V; T _i = 25 °C	-	-0.74	-1.2	V

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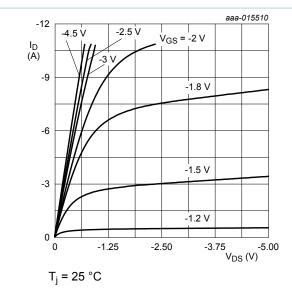


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

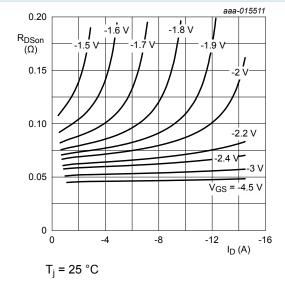


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

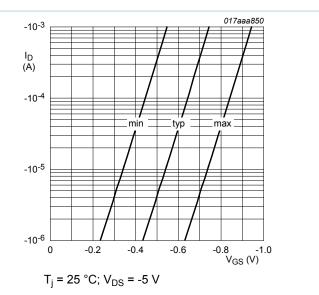


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

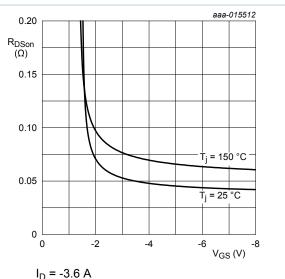


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

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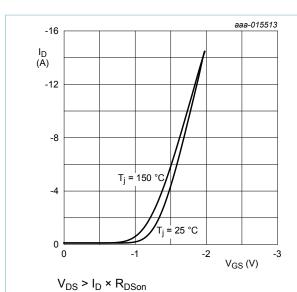


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

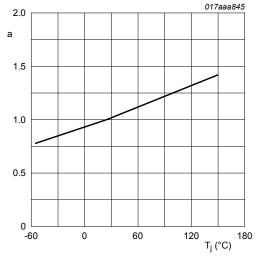


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

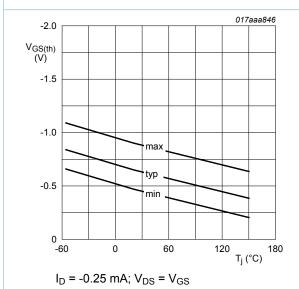


Fig. 12. Gate-source threshold voltage as a function of junction temperature

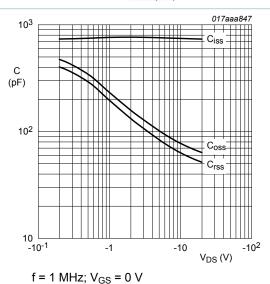


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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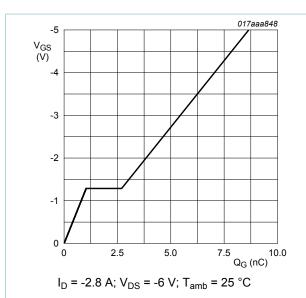


Fig. 14. Gate-source voltage as a function of gate charge; typical values

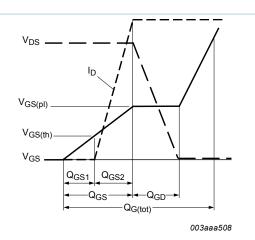
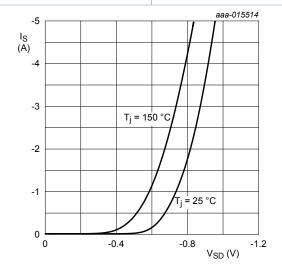


Fig. 15. MOSFET transistor: Gate charge waveform definitions



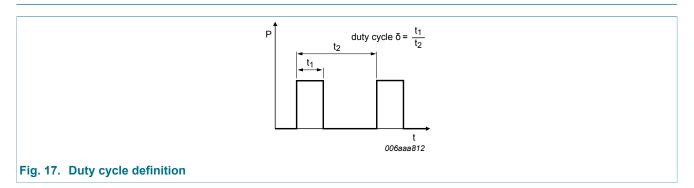
 $V_{GS} = 0 V$ (1) $T_i = 150 \, ^{\circ}C$ (2) $T_i = 25 \, ^{\circ}C$

Fig. 16. Source current as a function of source-drain voltage; typical values

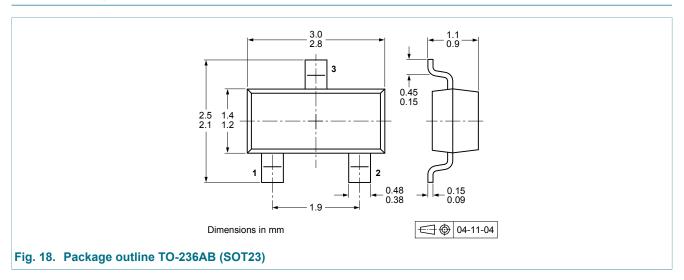
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11. Test information

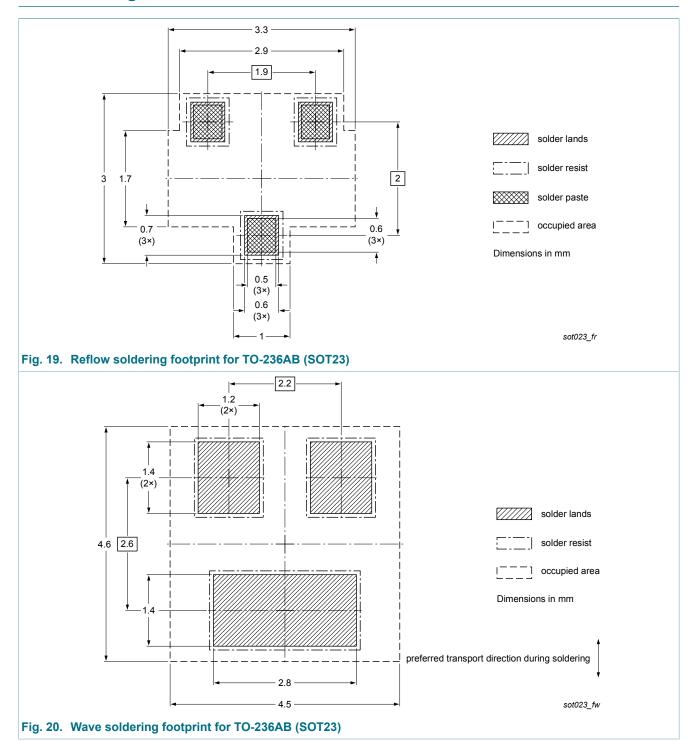


12. Package outline



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13. Soldering



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14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes					
PMV50XP v.2	20141119	Product data sheet	-	PMV50XP v.1					
Modifications:	Table 7: R _{DSon} unit corre	Table 7: R _{DSon} unit corrected							
PMV50XP v.1	20141111	Product data sheet	-	-					

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Document status [1][2]	Product status [3]	Definition
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