



# PMV65UNEA

20 V, N-channel Trench MOSFET

17 March 2017

Product data sheet

## 1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a small SOT23 (TO-236AB) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Trench MOSFET technology
- Low threshold voltage
- Enhanced power dissipation capability of 940 mW
- ElectroStatic Discharge (ESD) protection > 2KV HBM
- AEC-Q101 qualified

## 3. Applications

- LED driver
- Power management
- Low-side loadswitch
- Switching circuits

## 4. Quick reference data

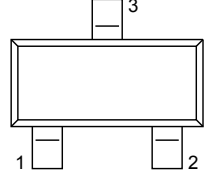
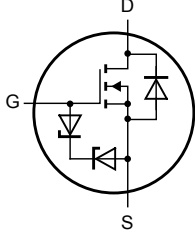
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ }^\circ\text{C}$	-	-	20	V
$V_{GS}$	gate-source voltage	$T_j = 25\text{ }^\circ\text{C}; T_{amb} = 25\text{ }^\circ\text{C}$	-8	-	8	V
$I_D$	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ }^\circ\text{C}$	[1]	-	2.8	A
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 2.8\text{ A}; T_j = 25\text{ }^\circ\text{C}$	-	63	73	m $\Omega$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>TO-236AB (SOT23)</p>	 <p>017aaa255</p>
2	S	source		
3	D	drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMV65UNEA	TO-236AB	plastic surface-mounted package; 3 leads	SOT23

## 7. Marking

Table 4. Marking codes

Type number	Marking code <sup>[1]</sup>
PMV65UNEA	EM%

[1] % = placeholder for manufacturing site code

## 8. Limiting values

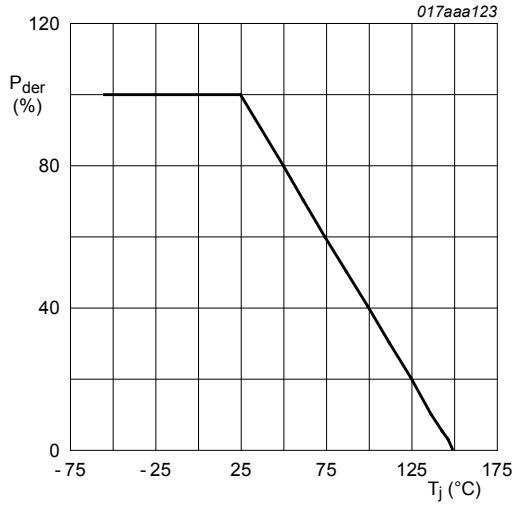
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$		-	20	V
$V_{GS}$	gate-source voltage	$T_j = 25\text{ °C}; T_{amb} = 25\text{ °C}$		-8	8	V
$I_D$	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	2.8	A
		$V_{GS} = 4.5\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	1.8	A
$I_{DM}$	peak drain current	$T_{amb} = 25\text{ °C};$ single pulse; $t_p \leq 10\text{ }\mu\text{s}$		-	11	A
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$T_{j(\text{init})} = 25\text{ °C}; I_D = 0.3\text{ A};$ DUT in avalanche (unclamped)		-	5.6	mJ
$P_{tot}$	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	490	mW
			[1]	-	940	mW
		$T_{sp} = 25\text{ °C}$		-	6.25	W
$T_j$	junction temperature			-55	150	°C
$T_{amb}$	ambient temperature			-55	150	°C
$T_{stg}$	storage temperature			-65	150	°C
<b>Source-drain diode</b>						
$I_S$	source current	$T_{amb} = 25\text{ °C}$	[1]	-	0.9	A
<b>ESD Maximum rating</b>						
$V_{ESD}$	electrostatic discharge voltage	HBM		-	2000	V

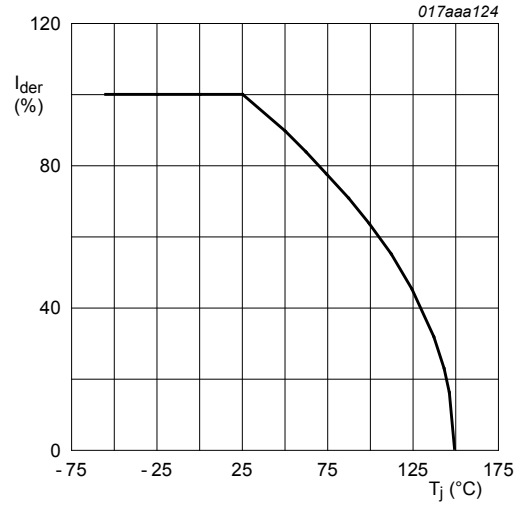
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



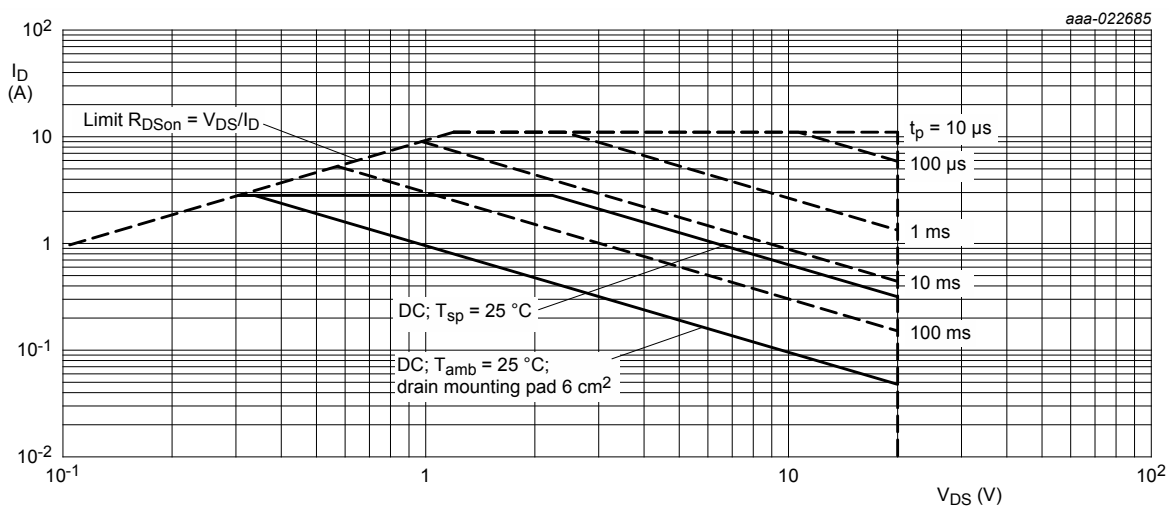
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100 \%$$

Fig. 1. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100 \%$$

Fig. 2. Normalized continuous drain current as a function of junction temperature



$I_{DM}$  = single pulse

Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	221	254	K/W
			[2]	-	116	133	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	17	20	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.

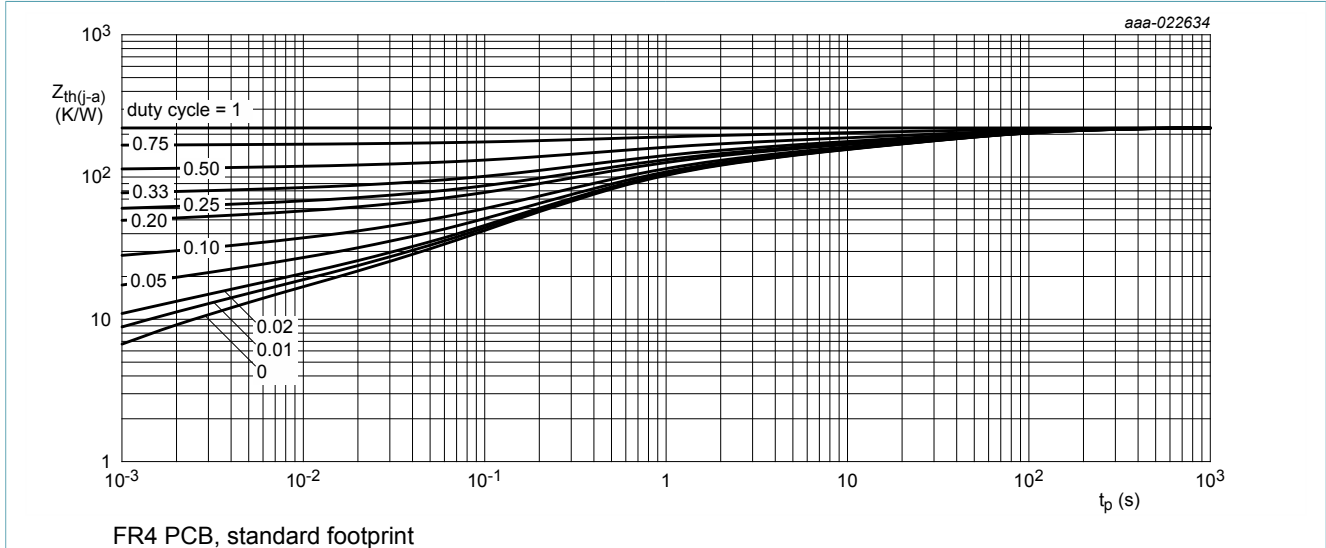


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

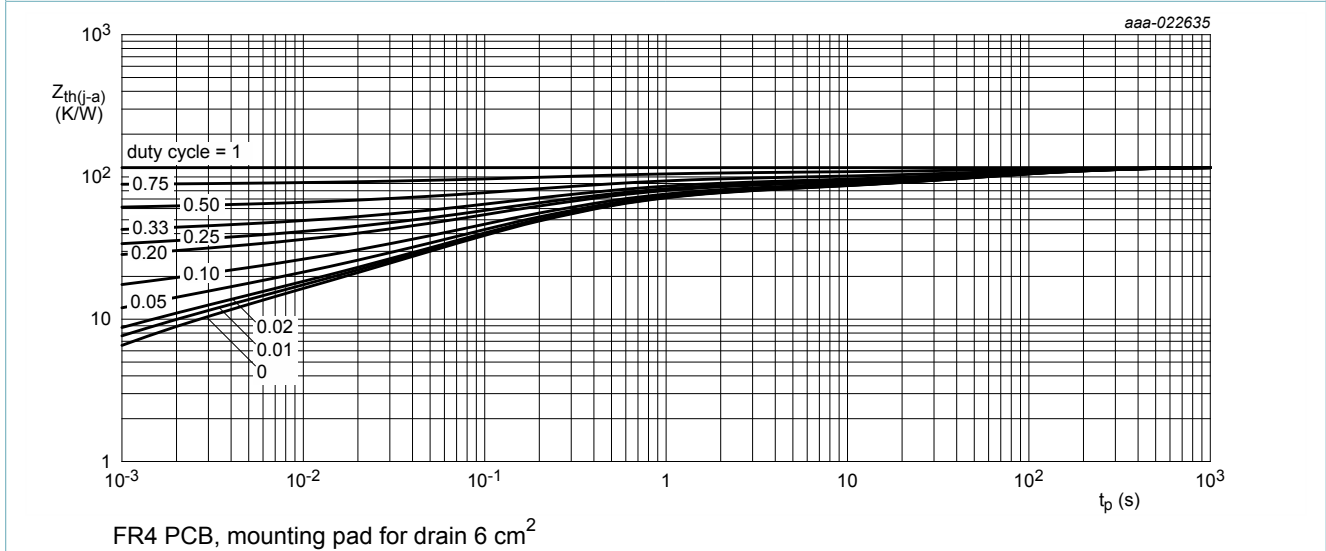
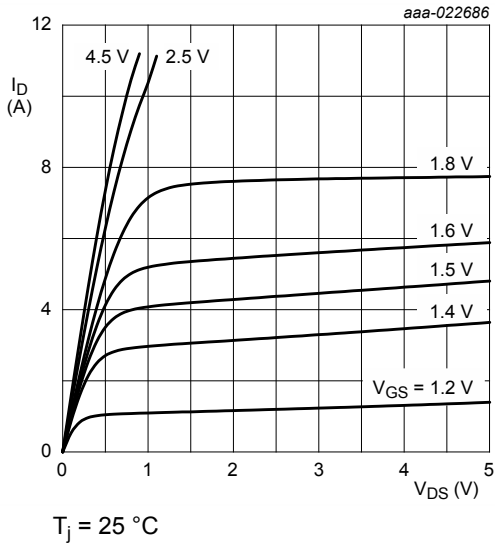


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

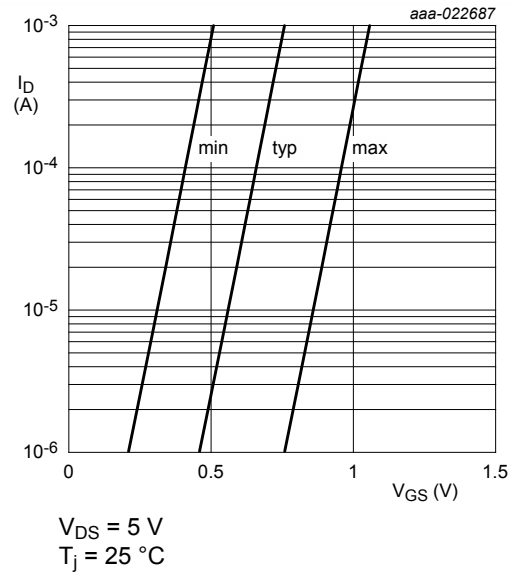
## 10. Characteristics

Table 7. Characteristics

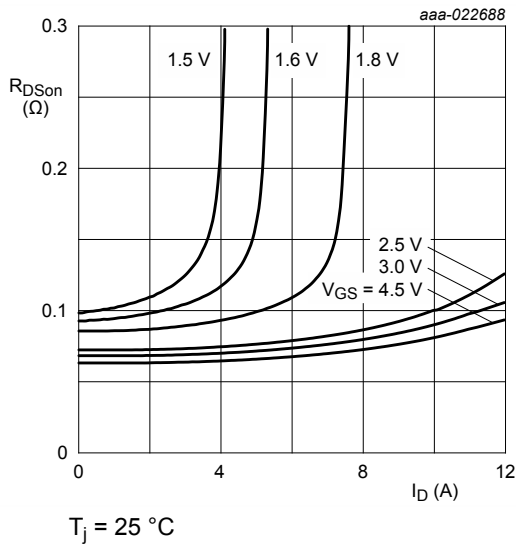
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	20	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 250 \mu A$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ C$	0.45	0.7	1	V
$I_{DSS}$	drain leakage current	$V_{DS} = 20 V$ ; $V_{GS} = 0 V$	-	-	1	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 8 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	10	$\mu A$
		$V_{GS} = -8 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	-10	$\mu A$
		$V_{GS} = 4.5 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	5	$\mu A$
		$V_{GS} = -4.5 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	-5	$\mu A$
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5 V$ ; $I_D = 2.8 A$ ; $T_j = 25 \text{ }^\circ C$	-	63	73	m $\Omega$
		$V_{GS} = 4.5 V$ ; $I_D = 2.8 A$ ; $T_j = 150 \text{ }^\circ C$	-	93	108	m $\Omega$
		$V_{GS} = 2.5 V$ ; $I_D = 2.4 A$ ; $T_j = 25 \text{ }^\circ C$	-	71	83	m $\Omega$
		$V_{GS} = 1.8 V$ ; $I_D = 0.8 A$ ; $T_j = 25 \text{ }^\circ C$	-	83	94	m $\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = 10 V$ ; $I_D = 3 A$ ; $T_j = 25 \text{ }^\circ C$	-	11	-	S
$R_G$	gate resistance	$T_j = 25 \text{ }^\circ C$ ; $f = 1 \text{ MHz}$	-	1.8	-	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 10 V$ ; $I_D = 2.8 A$ ; $V_{GS} = 4.5 V$ ; $T_j = 25 \text{ }^\circ C$	-	3.8	6	nC
$Q_{GS}$	gate-source charge		-	0.3	-	nC
$Q_{GD}$	gate-drain charge		-	0.9	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 10 V$ ; $f = 1 \text{ MHz}$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	291	-	pF
$C_{oss}$	output capacitance		-	52	-	pF
$C_{rss}$	reverse transfer capacitance		-	43	-	pF
$t_{d(on)}$	turn-on delay time		$V_{DS} = 10 V$ ; $I_D = 2.8 A$ ; $V_{GS} = 4.5 V$ ; $R_{G(ext)} = 6 \Omega$ ; $T_j = 25 \text{ }^\circ C$	-	8	-
$t_r$	rise time	-		23	-	ns
$t_{d(off)}$	turn-off delay time	-		35	-	ns
$t_f$	fall time	-		12	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 0.9 A$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	0.7	1.2	V



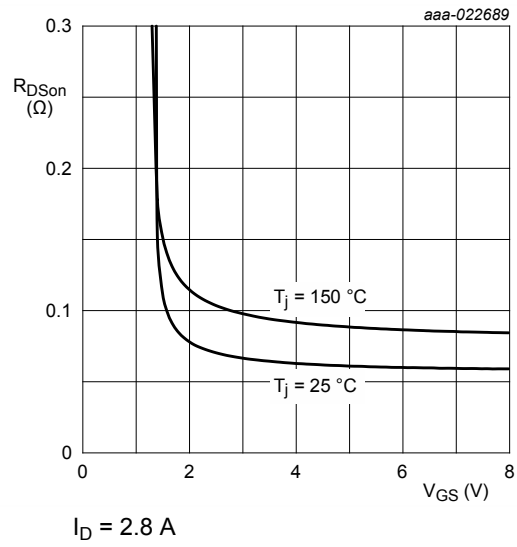
**Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values**



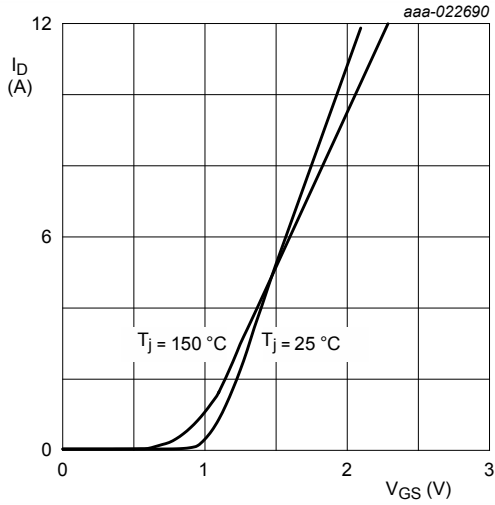
**Fig. 7. Sub-threshold drain current as a function of gate-source voltage**



**Fig. 8. Drain-source on-state resistance as a function of drain current; typical values**

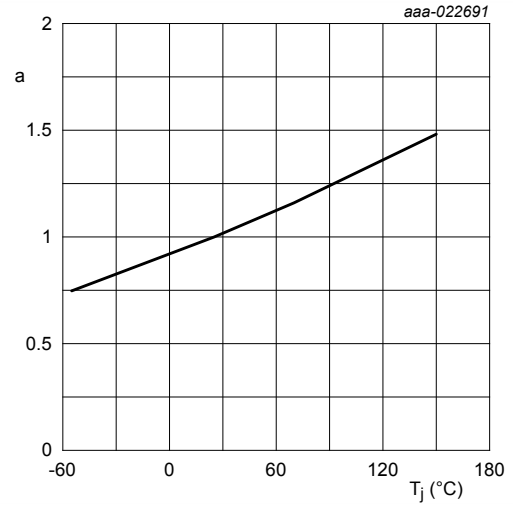


**Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values**



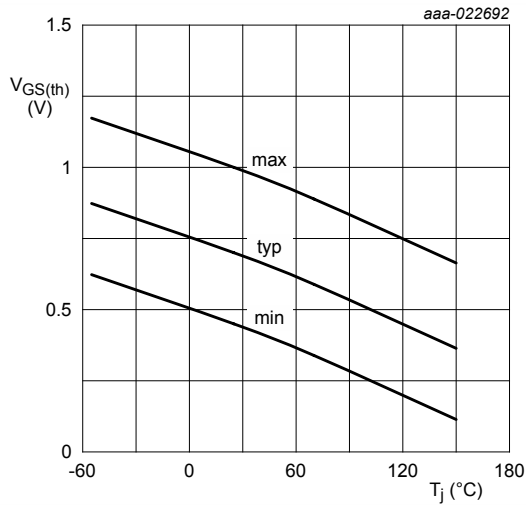
$$V_{DS} > I_D \times R_{DSon}$$

**Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



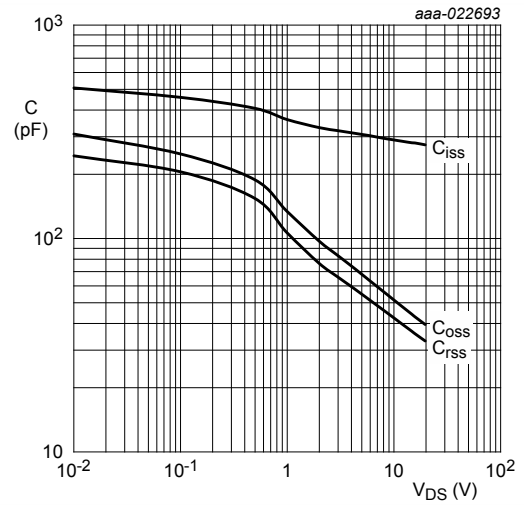
$$a = \frac{R_{DSon}}{R_{DSon}(25\text{ }^\circ\text{C})}$$

**Fig. 11. Normalized drain-source on-state resistance as a function of ambient temperature; typical values**



$$I_D = 250\ \mu\text{A}; V_{DS} = V_{GS}$$

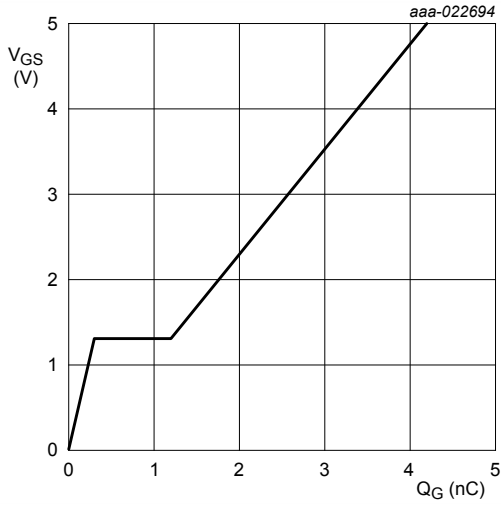
**Fig. 12. Gate-source threshold voltage as a function of ambient temperature**



$$f = 1\ \text{MHz}; V_{GS} = 0\ \text{V}$$

**Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**





$V_{DS} = 10\text{ V}; I_D = 2.8\text{ A}$

Fig. 14. Gate-source voltage as a function of gate charge; typical values

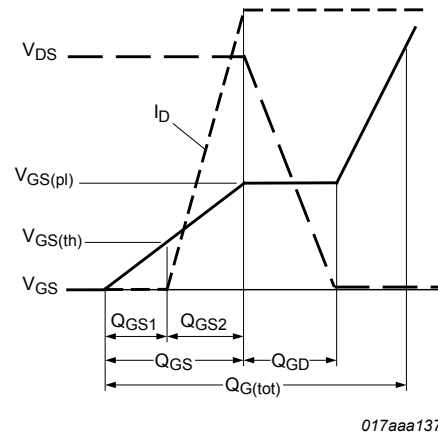
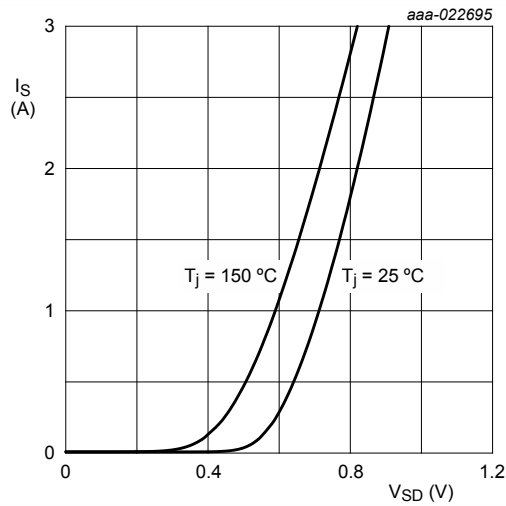


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0\text{ V}$

Fig. 16. Source current as a function of source-drain voltage; typical values

## 11. Test information

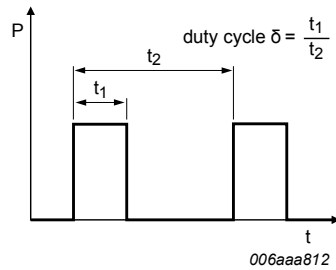


Fig. 17. Duty cycle definition

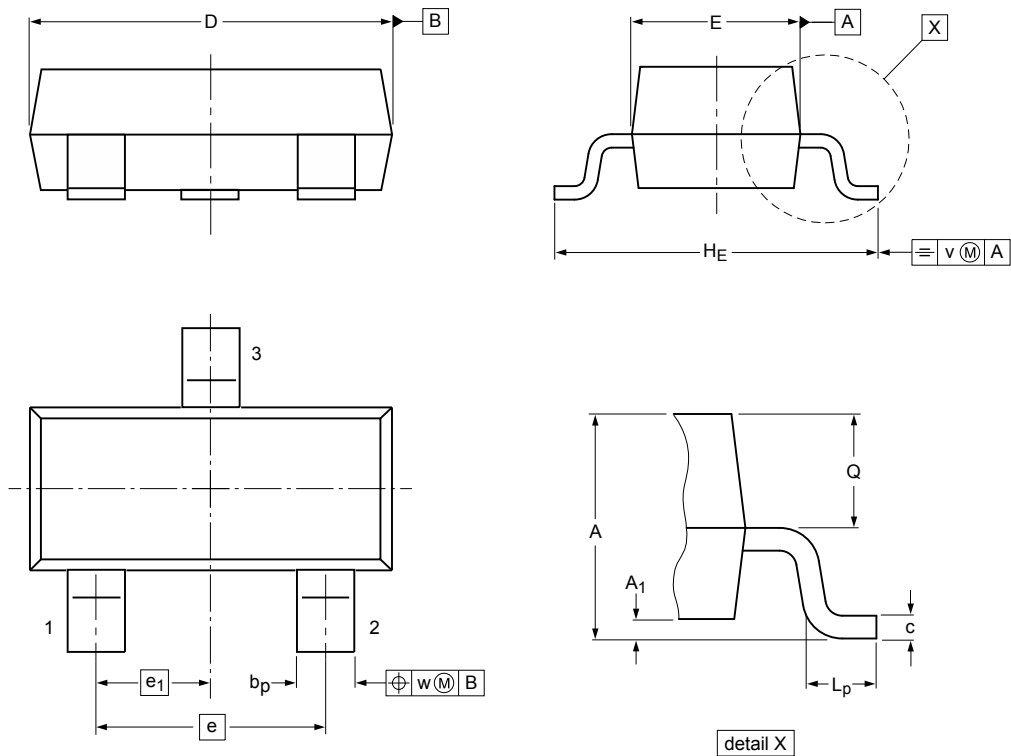
### Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

## 12. Package outline

Plastic surface-mounted package; 3 leads

SOT23



Dimensions (mm are the original dimensions)

Unit	A	A <sub>1</sub>	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w
max	1.1	0.1	0.48	0.15	3.0	1.4			2.5	0.45	0.55		
nom							1.9	0.95				0.2	0.1
min	0.9		0.38	0.09	2.8	1.2			2.1	0.15	0.45		

sot023\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT23		TO-236AB			-14-06-19 14-09-22

Fig. 18. Package outline TO-236AB (SOT23)

### 13. Soldering

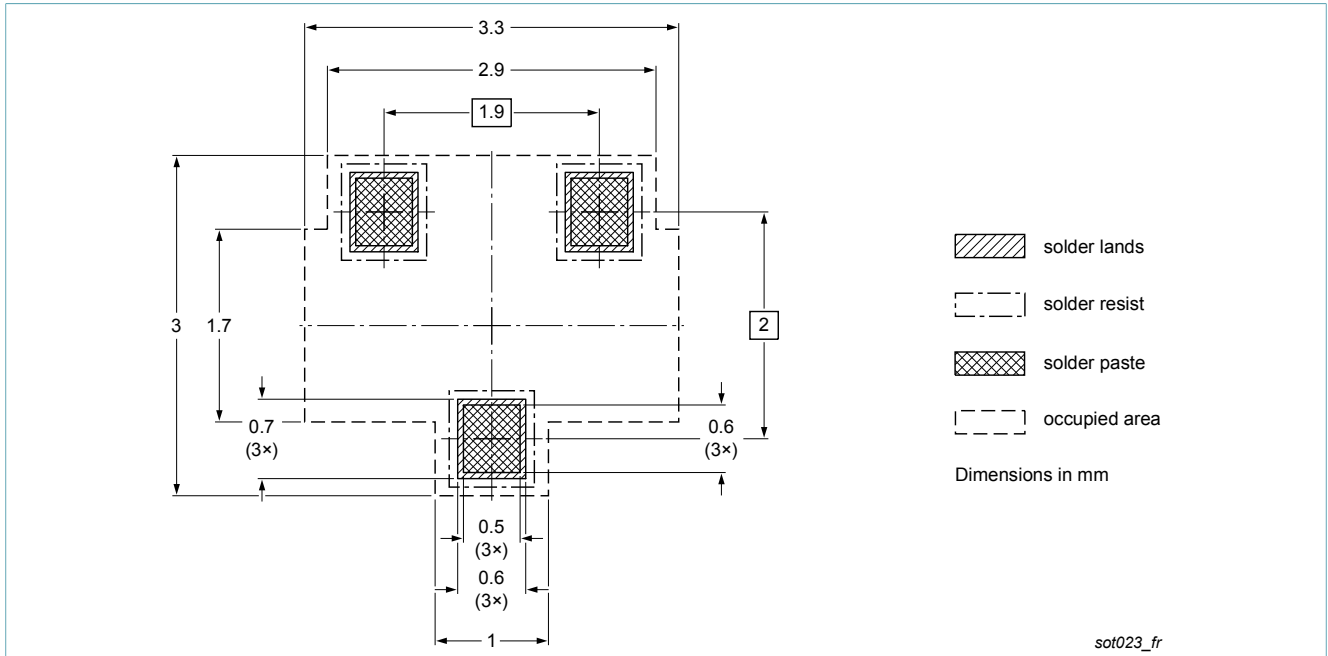


Fig. 19. Reflow soldering footprint for TO-236AB (SOT23)

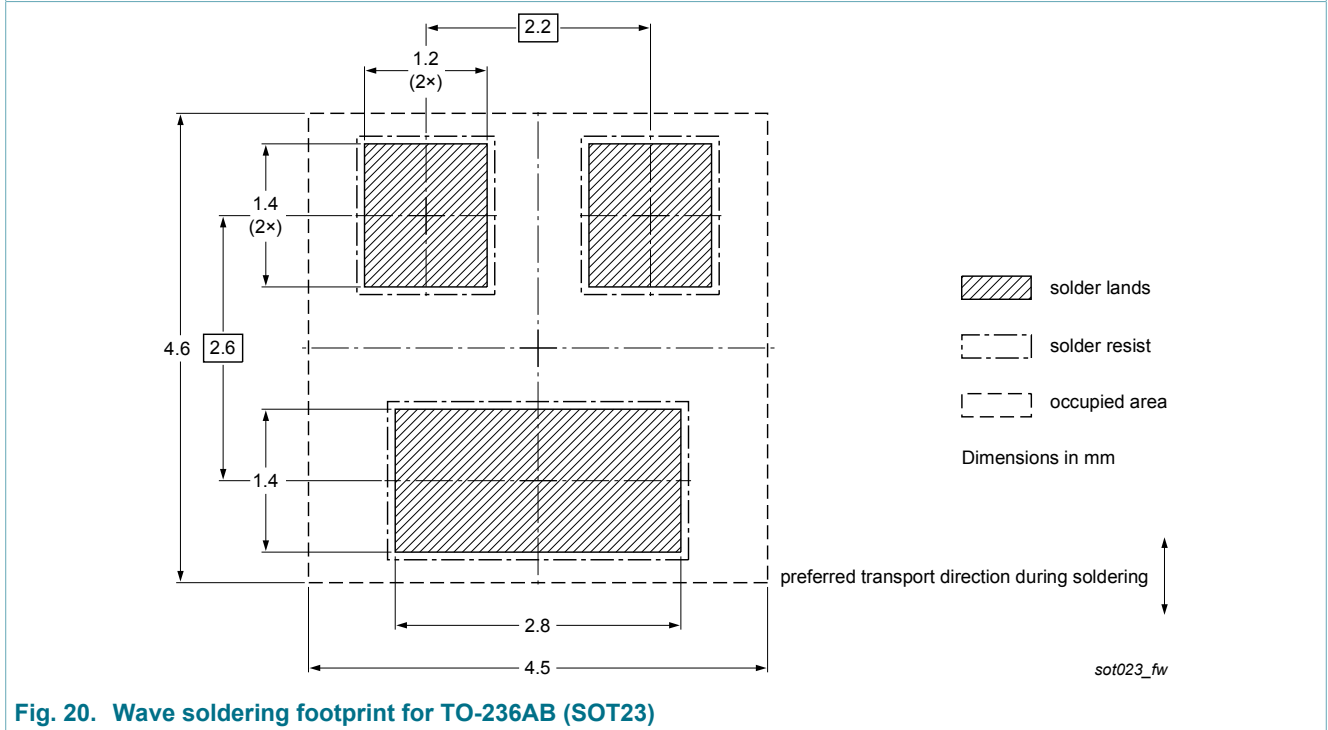


Fig. 20. Wave soldering footprint for TO-236AB (SOT23)

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMV65UNEA v.1	20170317	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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