PixArt Imaging Inc.

PMW3310DH-AWQT

Low Power LED Gaming Mouse Sensor

Data Sheet

Lead (Pb) Free
RoHS 6 fully
compliant

Description

PMW3310DH-AWQT low power gaming sensor is a new addition to PixArt Imaging's gaming sensor family. The tracking system comprises of navigation IC, HSDL-4261 IR LED and lens. It provides enhanced features such as variable frame rate, programmable resolution, angle tunability, X-Y axis independent resolution, programmable angle snap plus configurable sleep and wake up time to suit various gamers' preferences.

This gaming sensor is in a 20-pin staggered dual in- line package (DIP). It is designed to be used with ADNS-2120-001 trim lens to achieve optimum performance featured in this document.

Theory of Operation

The sensor measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement. It contains an Image Acquisition System (IAS), a Digital Signal Processor (DSP), and a four wire serial port. The IAS acquires microscopic surface images via the lens and illumination system. These images are processed by the DSP to determine the direction and distance of motion. The DSP calculates the Δx and Δy relative displacement values. An external microcontroller reads the Δx and Δy information from the sensor serial port. The microcontroller then translates the data into PS2, USB, or RF signals before sending them to the host PC or game console.

Features

- 20-pin DIP package
- Operating Voltage: 2.7V – 3.3V
- VDDIO range: 1.65V – 3.3V
- 16-bits motion data registers
- High speed motion detection of 130ips and acceleration up to 30g
- Variable Frame Rate for optimum power performance
- Motion detect pin output
- Internal oscillator – no external clock input needed
- Enhanced Programmability
  - Frame rate up to 6,500fps
  - Resolution up to 5000cpi with step of ~50cpi
  - X and Y axis independent resolution setting
  - Programmable Rest Modes
  - Programmable Angle Snap
  - Angle Tunabilty

Applications

- Corded and cordless gaming mice
- Motion input devices

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Device Pinout

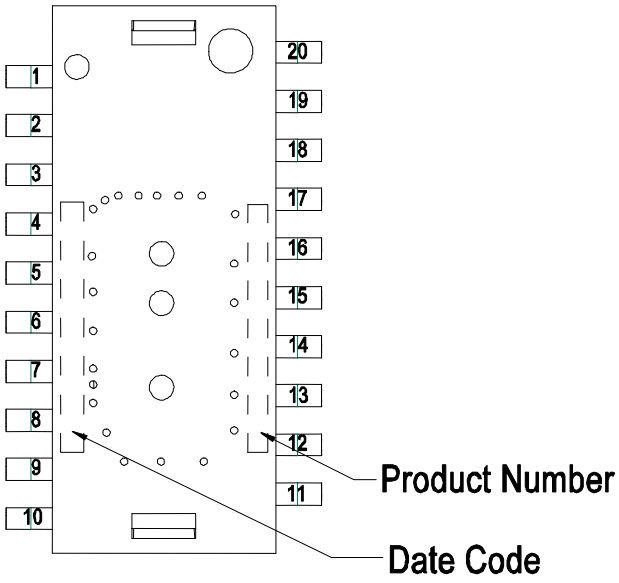

Figure 1. Device Pinout of PMW3310DH-AWQT

Product Number: PMW3310DH-AWQT
Date Code: $CYW_kW_kW_fW_fR$ (C = CM Code, Y = Year Code, W_kW_k = Week Code, W_fW_f = Wafer Code, R = Remark (mark E for engineering lot))

Pin No	Pin Name	Input / Output/ Power	Description
1 – 2	NC	-	-
3	NCS	IN	Chip Select (Active Low Input)
4	SCLK	IN	Serial Clock Input
5	MOSI	IN	Serial Data Input (Master Out/Slave In)
6	MOTION	OUT	Motion Detect (Active Low Output)
7	VDDIO	PWR	IO Voltage
8	XYLED	OUT	LED Illumination Control
9	GND	PWR	Ground
10 – 11	VDD	PWR	3V Supply
12	NC	-	-
13	REF	PWR	Internal regulator output pin (To connect to external bypass cap)
14	GND	PWR	Ground
15	NC	-	-
16	MISO	OUT	Serial Data Output (Master In/Slave Out)
17 – 18	NC	-	-
19	GND	PWR	Ground
20	NC	-	-

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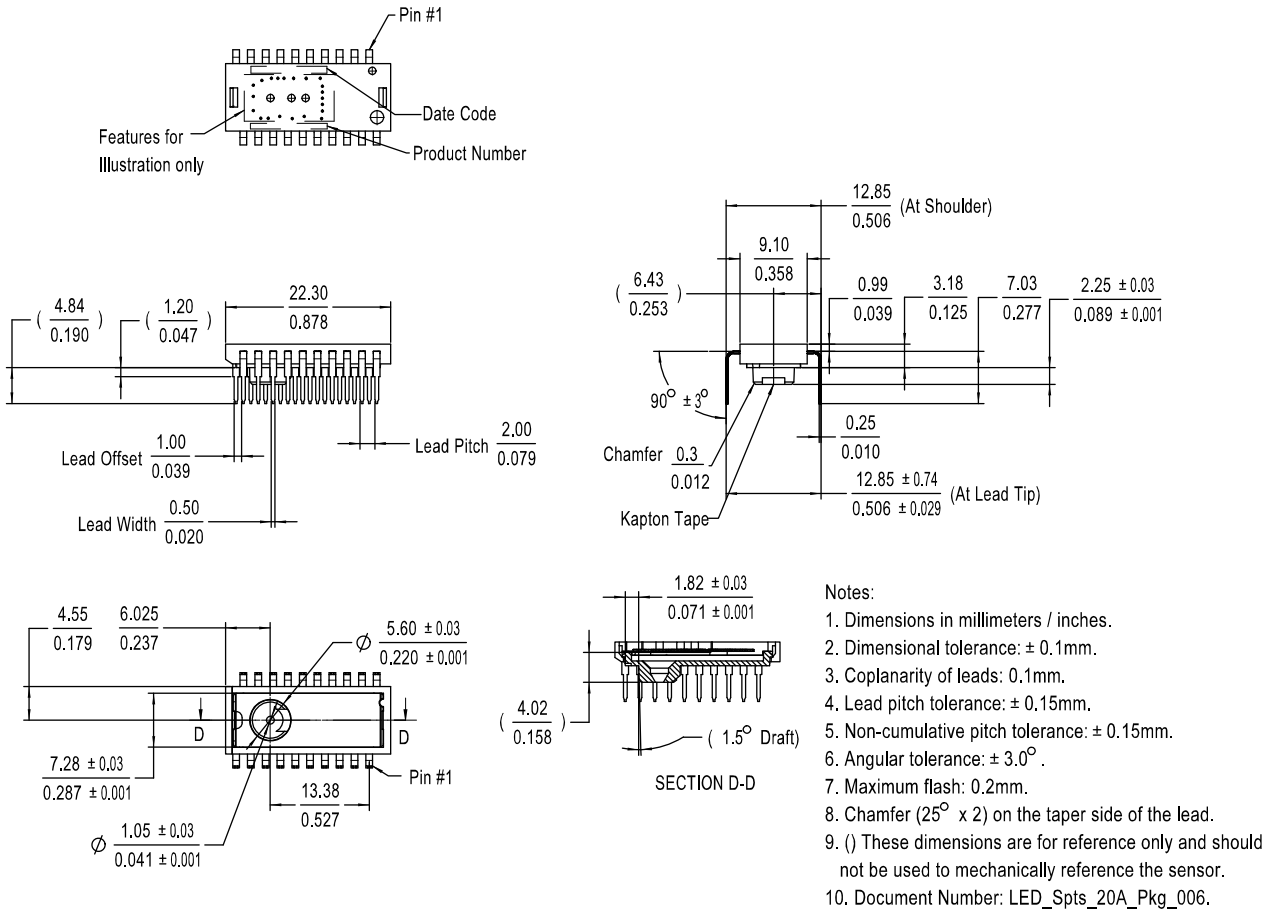

Figure 2. Package Outline Drawing

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD

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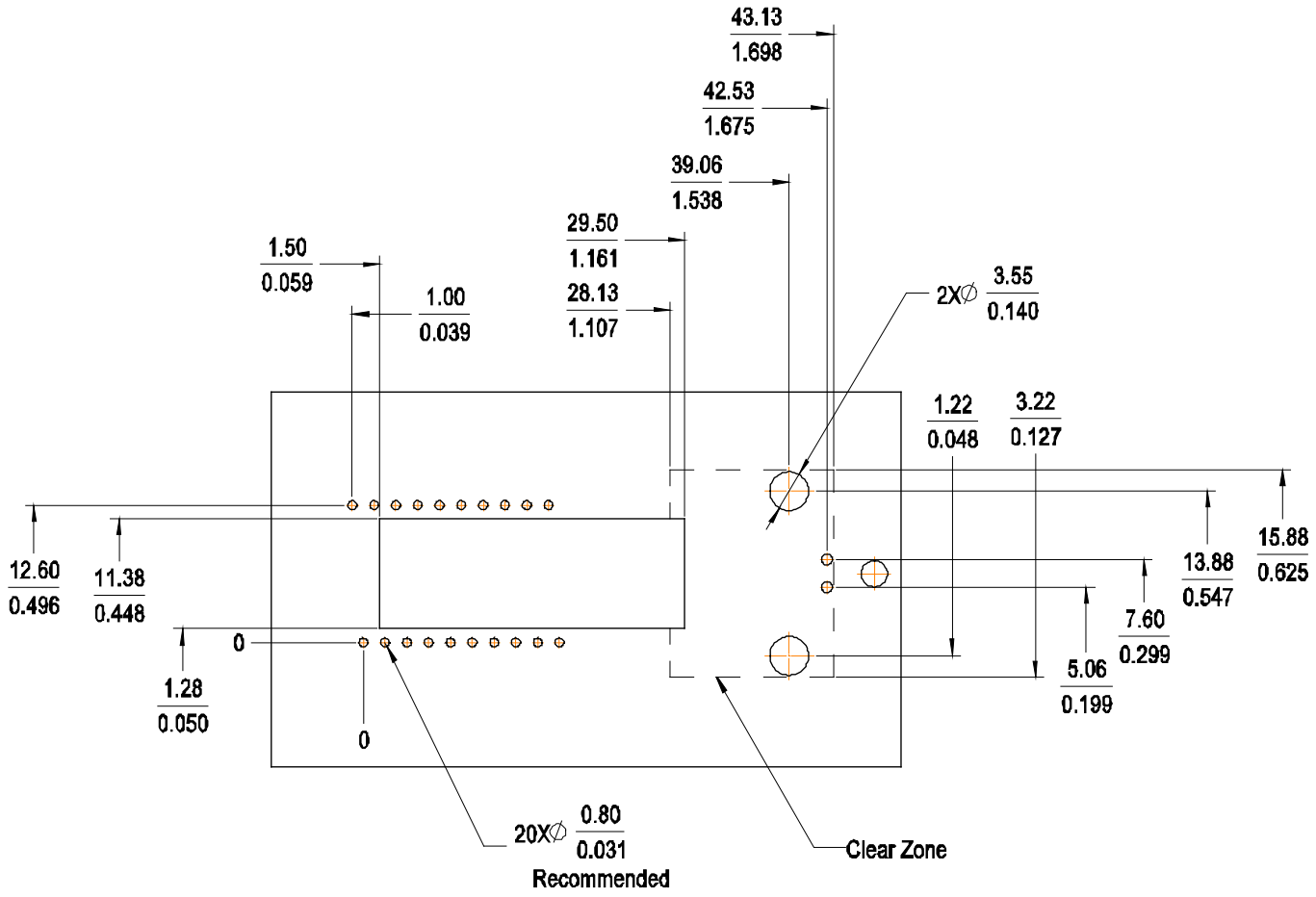

Figure 3. Recommended PCB Mechanical Cutouts and Spacing (Top View)

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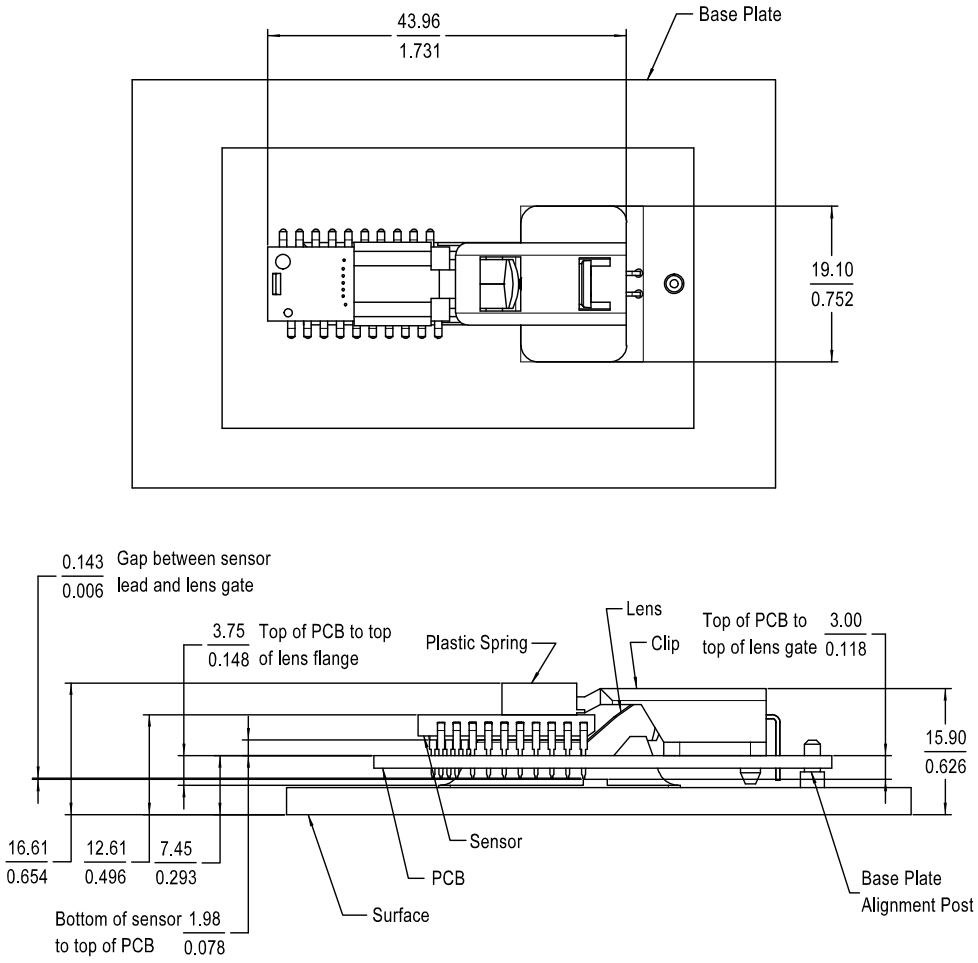

Figure 4. Cross Section Top and Side View

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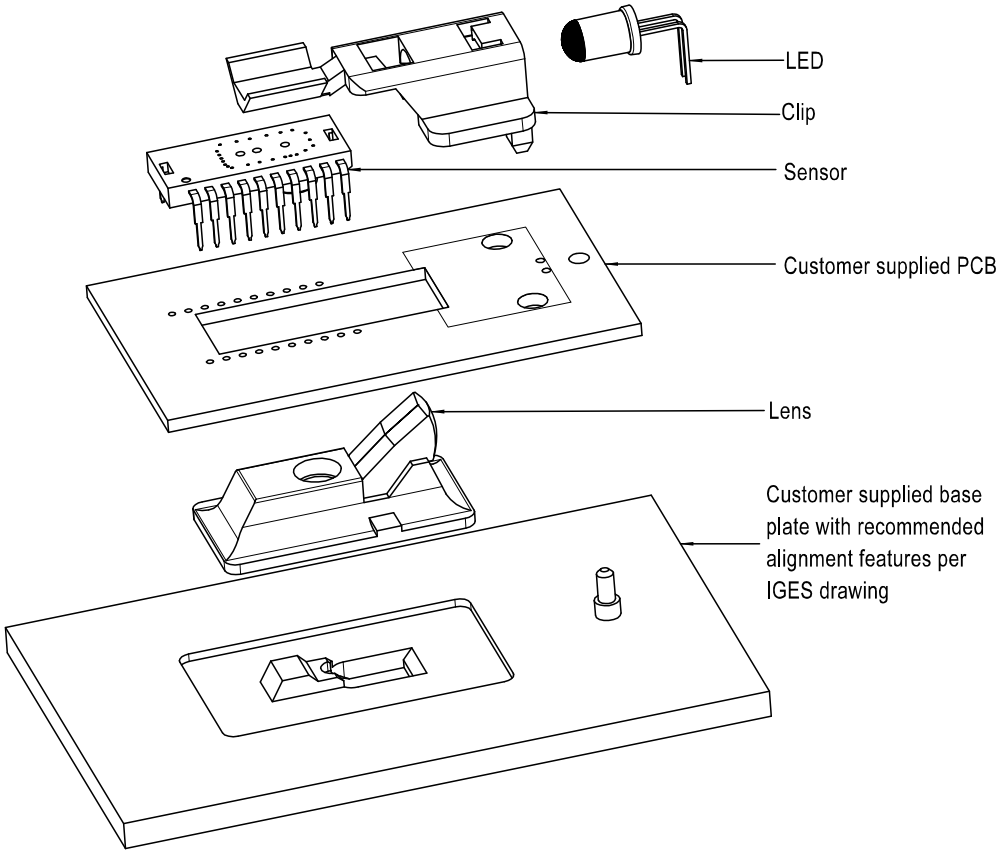

Figure 5. Exploded View of Assembly

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PCB Assembly Considerations

1. Insert the sensor and all other electrical components into PCB.
2. Insert the LED into the assembly clip and bend the leads 90 degrees.
3. Insert the LED clip assembly into PCB.
4. Wave-solder the entire assembly in a no-wash solder process utilizing solder-fixture. The solder-fixture is needed to protect the sensor from flux spray during the solder process. It also sets the correct sensor-to-PCB distance as the lead shoulders do not normally rest on the PCB surface. The fixture should be designed to expose only the sensor leads to solder while shielding the optical aperture from direct solder contact.
5. Place the lens onto the base plate.
6. Remove the protective kapton tape from optical aperture of the sensor. Care must be taken to keep contaminants from entering the aperture. Do not place the PCB with the sensor facing up during the entire mouse assembly process. Hold the PCB vertically when removing kapton tape.
7. Insert PCB assembly over the lens onto the base plate aligning post to retain PCB assembly.
8. The optical position reference for the PCB is set by the base plate and lens. Note that the PCB motion due to button presses must be minimized to maintain optical alignment.
9. Install mouse top case. There must be a feature in the top case to press down onto the PCB assembly to ensure all components are interlocked to the correct vertical height.

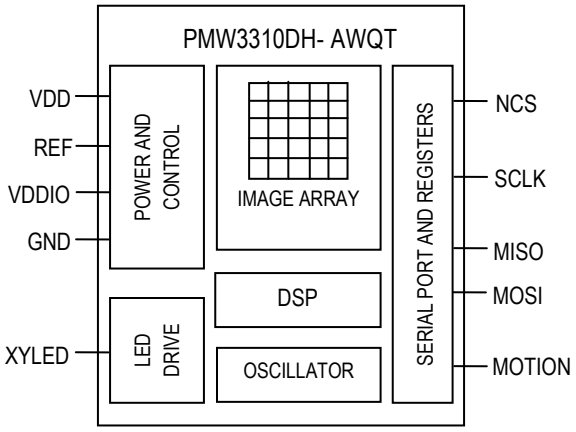

Figure 6. Block diagram of PMW3310DH-AWQT

All data and information is provided to and as a reference in the application of PixArt Imaging's product, but the responsibility for proper design of printed circuit SMT process design still lies with the SMT assembly company. PixArt Imaging has no liability for customer's design.

Regulatory Requirements

- Passes FCC B and worldwide analogous emission limits when assembled into a mouse with shielded cable and following PixArt recommendations.
- Passes IEC-1000-4-3 radiated susceptibility level when assembled into a mouse with shielded cable and following PixArt recommendations.
- Passes EN-61000-4-4/IEC-801-4 EFT tests when assembled into a mouse with shielded cable and following PixArt recommendations. Passes IEC-6100-4-2 Electrostatic Discharge Immunity (ESD) and provides sufficient ESD creepage/clearance distance to withstand discharge up to 15kV when assembled into a mouse according to usage instructions above.

Application Circuits

1. The supply and ground paths should be laid out using a star methodology.
2. Level shifting is required to interface a 5V micro-controller to PMW3310DH-AWQT.
3. All caps MUST be as close as possible to VDD, VDDIO & REF sensor pins with trace length less than 5mm.
4. Ceramic non-polarity caps and tantalum polarity caps are recommended.
5. Caps should have less than 5nH of self inductance and less than 0.2Ω ESR.

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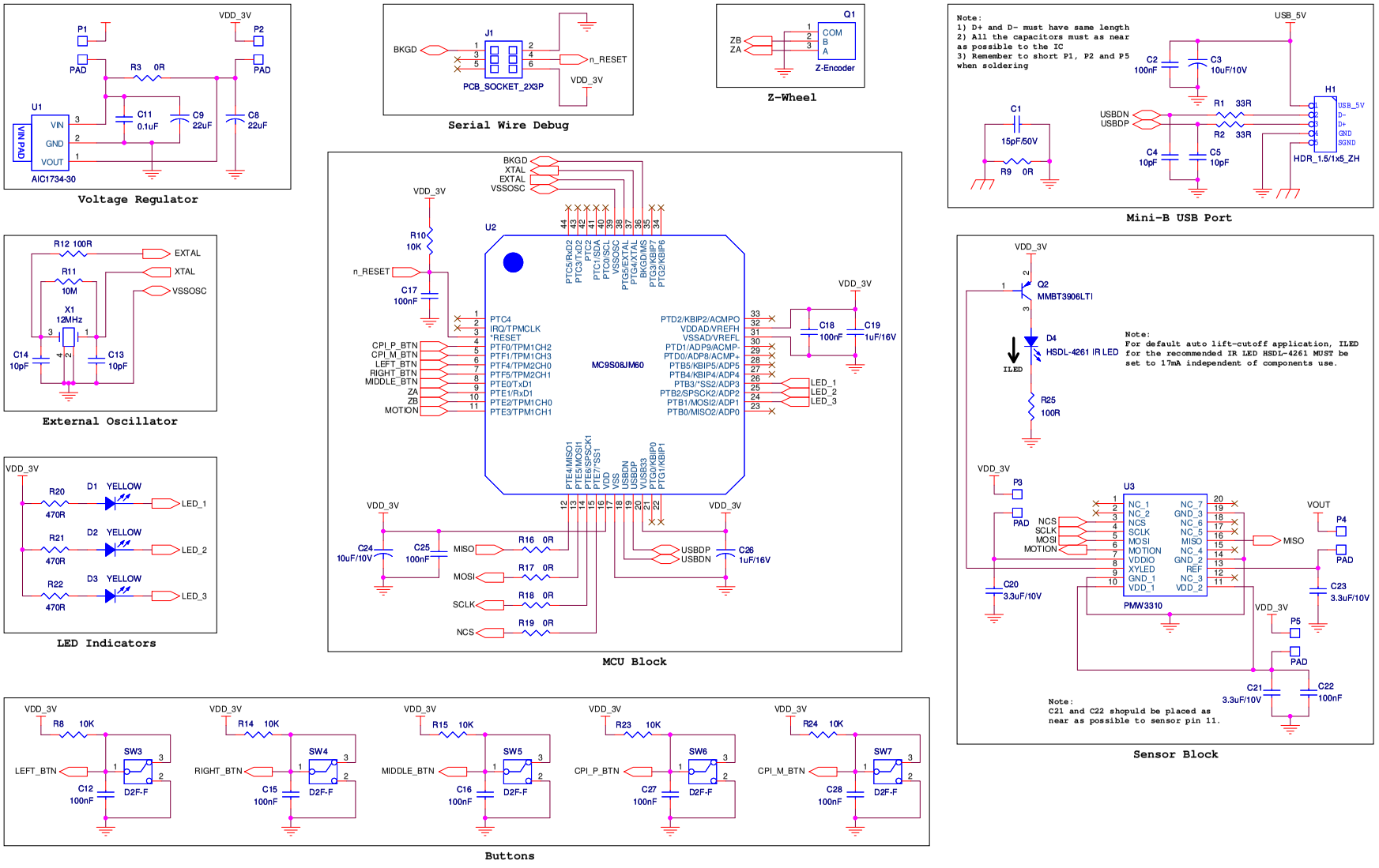

Figure 7. Schematic Diagram for 5-Button Scroll Wheel Corded Mouse

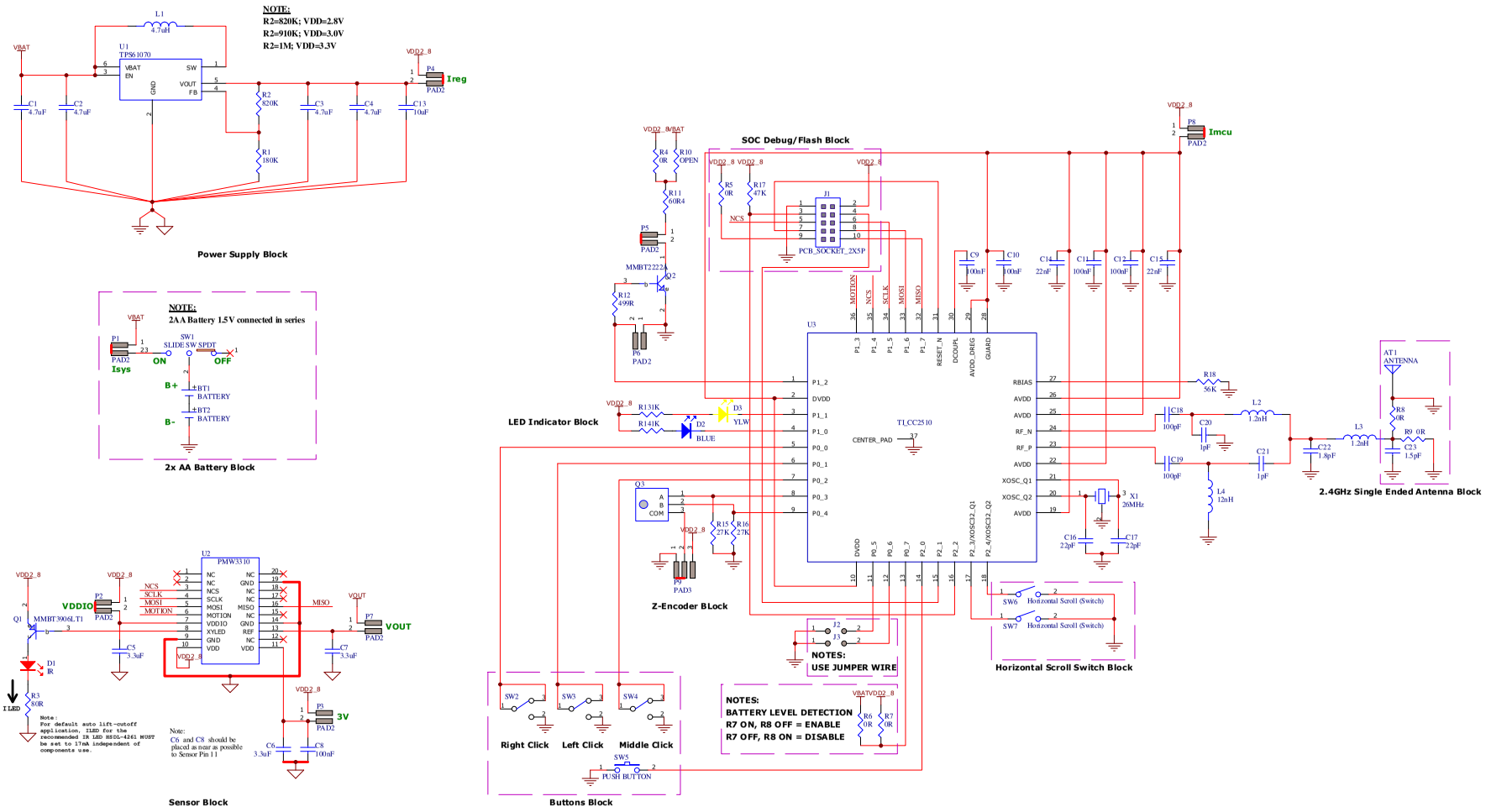

Figure 8. Schematic Diagram for 5-Button Scroll Wheel Cordless Mouse

Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_S	-40	85	℃	
Lead-Free Solder Temp			260	℃	
Supply Voltage	V_{DD}	-0.5	3.4	V	
	V_{DD_LED}	-0.5	3.4	V	
	V_{DDIO}	-0.5	3.4	V	
ESD (Human body model)			2	kV	All Pins
Input Voltage	V_{IN}	-0.5	3.4	V	All I/O Pins

Comments:

1. *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are the stress ratings only and functional operation of the device at these or any other condition beyond those indicated for extended period of time may affect device reliability.*
2. *The inherent design of this component causes it to be sensitive to electrostatic discharge. The ESD threshold is listed above. To prevent ESD-induced damage, take adequate ESD precautions when handling this product.*

Recommended Operating Conditions

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Units*	*Notes*
Operating Temperature	T_A	0		40	°C	
Power supply voltage	V_{DD}	2.7	2.8	3.3	Volts	Including noise.
	V_{DD-LED}	2.7	2.8	3.3	Volts	Including noise.
	V_{DDIO}	1.65		3.3	Volts	Including noise.
Power supply rise time	V_{RT3}	1		100	ms	0 to 2.8V
Supply noise (Sinusoidal)	V_{NA}			100	mV_{p-p}	10kHz-50MHz
Serial Port Clock Frequency	f_{SCLK}			2	MHz	Active drive, 50% duty cycle
Distance from lens reference plane to surface (Z)	Z	2.2	2.4	2.6	mm	Results in +/- 0.2 mm minimum DOF.
Speed	S		130		ips	
Lift Cutoff	L		3		mm	
Acceleration	A		30		g	
Load Capacitance	C_{out}			100	pF	MOTION, MISO

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AC Electrical Specifications

Electrical Characteristics over recommended operating conditions. (Typical values at 25 °C, VDD = 2.8V)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Motion delay after reset	$t_{MOT-RST}$	30			ms	From SW_RESET register write to valid motion, assuming motion is present
Shutdown	t_{STDWN}			500	µs	From Shutdown mode active to low current
Wake Up from Shutdown	t_{WAKEUP}	30			ms	From Shutdown mode inactive to valid motion. Notes: A RESET must be asserted after a shutdown. Refer to section "Notes on Shutdown and Forced Rest", also note $t_{MOT-RST}$
Forced Rest enable	$t_{REST-EN}$			1	s	From RESTEN bits set to low current
Wake Up from Forced Rest	$t_{REST-DIS}$			1	s	From RESTEN bits cleared to valid motion
MISO rise time	t_{r-MISO}		50	200	ns	C_L = 100pF
MISO fall time	t_{f-MISO}		50	200	ns	C_L = 100pF
MISO delay after SCLK	$t_{DLY-MISO}$			120	ns	From SCLK falling edge to MISO data valid, no load conditions
MISO hold time	$t_{hold-MISO}$	200			ns	Data held until next falling SCLK edge
MOSI hold time	$t_{hold-MOSI}$	200			ns	Amount of time data is valid after SCLK rising edge
MOSI setup time	$t_{setup-MOSI}$	120			ns	From data valid to SCLK rising edge
SPI time between write commands	t_{SWW}	120			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second data byte.
SPI time between write and read commands	t_{SWR}	120			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second address byte.
SPI time between read and subsequent commands	t_{SRW} t_{SRR}	20			µs	From rising SCLK for last bit of the first data byte, to falling SCLK for the first bit of the address byte of the next command.
SPI read address-data delay	t_{SRAD}	150			µs	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read.
NCS inactive after motion burst	t_{BEXIT}	500			ns	Minimum NCS inactive time after motion burst before next SPI usage
NCS to SCLK active	$t_{NCS-SCLK}$	120			ns	From last NCS falling edge to first SCLK rising edge
SCLK to NCS inactive (for read operation)	$t_{SCLK-NCS}$	120			ns	From last SCLK rising edge to NCS rising edge, for valid MISO data transfer
SCLK to NCS inactive (for write operation)	$t_{SCLK-NCS}$	20			us	From last SCLK rising edge to NCS rising edge, for valid MOSI data transfer
NCS to MISO High-Z	$t_{NCS-MISO}$			500	ns	From NCS rising edge to MISO high-Z state
MOTION rise time	$t_{r-MOTION}$		50	200	ns	C_L = 100pF
MOTION fall time	$t_{f-MOTION}$		50	200	ns	C_L = 100pF
Transient Supply Current	I_{DDT}			65	mA	Max supply current during a V_{DD} ramp from 0 to 2.8V

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DC Electrical Specifications

Electrical Characteristics over recommended operating conditions. (Typical values at 25 °C, VDD = 2.8 V, VDDIO = 2.8V)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
DC Supply Current	I_{DD_RUN1}		11		mA	Average current, inclusive of LED current. No load on MISO, MOTION. RUN1 = Run mode at less than 6 ips RUN2 = Run mode at between 6 ips and 25 ips RUN3 = Run mode at more than 25 ips
	I_{DD_RUN2}		18		mA	
	I_{DD_RUN3}		27		mA	
	I_{DD_REST1}		0.30		mA	
	I_{DD_REST2}		0.15		mA	
	I_{DD_REST3}		0.05		mA	
Peak Supply Current	I_{DDPP}			65	mA	
Shutdown Supply Current	$I_{DDSTDWN}$		65		µA	NCS, SCLK, MOSI = VDDIO MISO = GND
Input Low Voltage	V_{IL}			0.3 * V_{DDIO}	V	SCLK, MOSI, NCS
Input High Voltage	V_{IH}	0.7 * V_{DDIO}			V	SCLK, MOSI, NCS
Input Hysteresis	V_{I_HYS}		100		mV	SCLK, MOSI, NCS
Input Leakage Current	I_{leak}		±1	±10	µA	Vin = 0.7*VDDIO , SCLK, MOSI, NCS
Output Low Voltage, MISO, MOTION	V_{OL}			0.3 * V_{DDIO}	V	Iout = 1mA, MISO, MOTION
Output High Voltage, MISO, MOTION	V_{OH}	0.7 * V_{DDIO}			V	Iout = -1mA, MISO, MOTION
Input Capacitance	C_{in}			10	pF	MOSI, NCS, SCLK

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Sensor's Typical Performance Characteristics

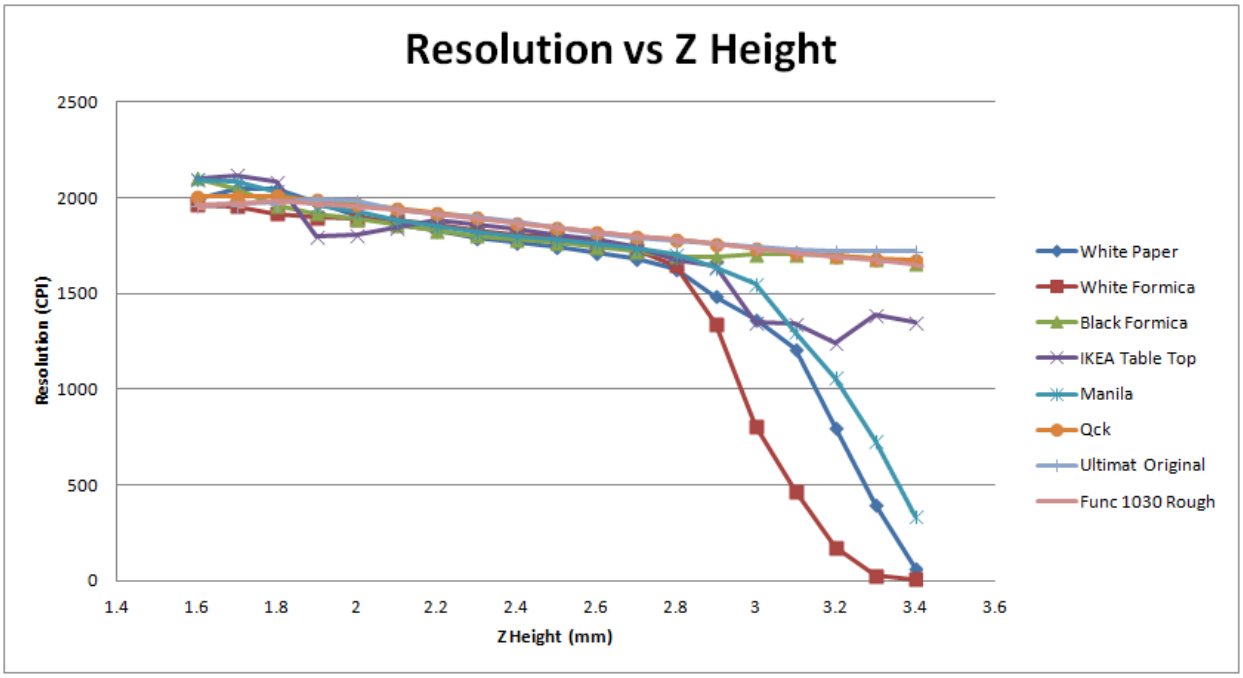

Figure 9. Mean Resolution vs. Z Height at Resolution of 1800cpi

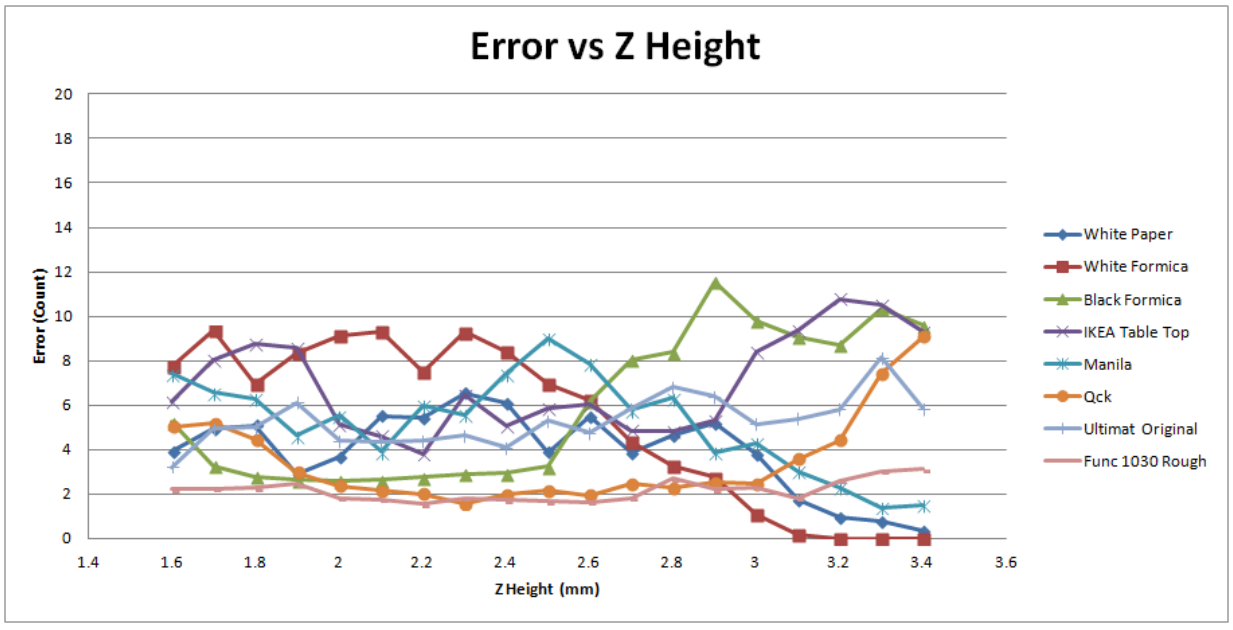

Figure 10. Error Count vs. Z Height at Resolution of 1800cpi

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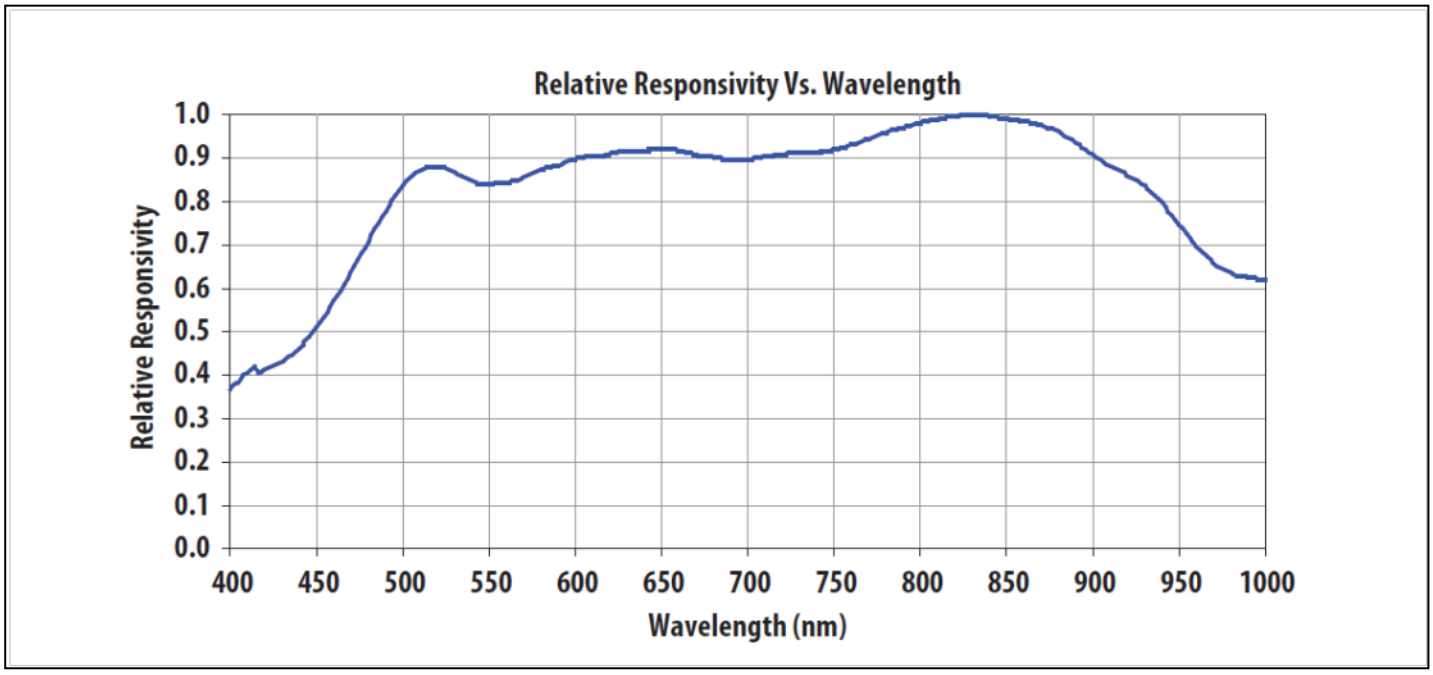

Figure 11. Wavelength Responsivity

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Synchronous Serial Port

The synchronous serial port is used to set and read parameters in PMW3310DH-AWQT sensor, and to read out the motion information. The serial port is also used to load SROM data into PMW3310DH-AWQT sensor.

The port is a four wire port. The host micro-controller always initiates communication; PMW3310DH-AWQT sensor never initiates data transfers. SCLK, MOSI, and NCS may be driven directly by a micro-controller. The port pins may be shared with other SPI slave devices. When the NCS pin is high, the inputs are ignored and the output is tri-stated.

The lines that comprise the SPI port are:

- SCLK: Clock input, generated by the master (microcontroller).
- MOSI: Input data. (Master Out/Slave In)
- MISO: Output data. (Master In/Slave Out)
- NCS: Chip select input (active low). NCS needs to be low to activate the serial port; otherwise, MISO will be high Z, and MOSI & SCLK will be ignored. NCS can also be used to reset the serial port in case of an error.

Motion Pin Timing

The motion pin is an active low output that signals the micro-controller when motion has occurred. The motion pin is lowered whenever the motion bit is set; in other words, whenever there is data in the Delta_X_L, Delta_X_H, Delta_Y_L or Delta_Y_H registers. Clearing the motion bit (by reading Delta_X_L, Delta_X_H, Delta_Y_L or Delta_Y_H registers, or writing to the Motion register) will put the motion pin high.

Chip Select Operation

The serial port is activated after NCS goes low. If NCS is raised during a transaction, the entire transaction is aborted and the serial port will be reset. This is true for all transactions including SROM download. After a transaction is aborted, the normal address-to-data or transaction-to-transaction delay is still required before beginning the next transaction. To improve communication reliability, all serial transactions should be framed by NCS. In other words, the port should not remain enabled during periods of non-use because ESD and EFT/B events could be interpreted as serial communication and put the chip into an unknown state. In addition, NCS must be raised after each burst-mode transaction is complete to terminate burst-mode. The port is not available for further use until burst-mode is terminated.

Write Operation

Write operation, defined as data going from the micro-controller to PMW3310DH-AWQT sensor, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address (seven bits) and has a “1” as its MSB to indicate data direction. The second byte contains the data. PMW3310DH-AWQT sensor reads MOSI on rising edges of SCLK.

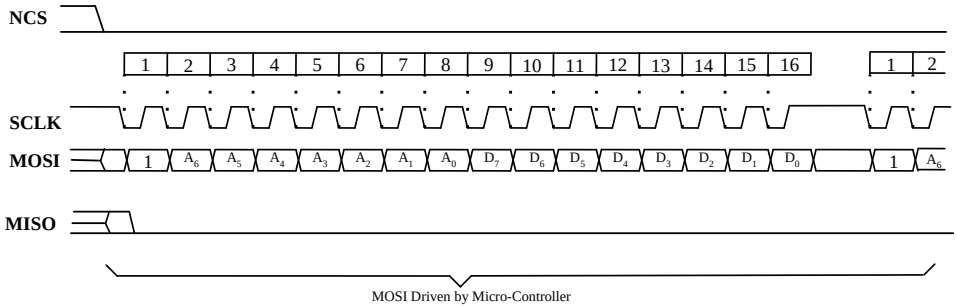

Figure 12. Write Operation

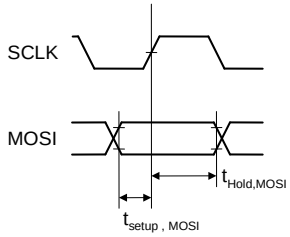

Figure 13. MOSI Setup and Hold Time

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Read Operation

A read operation, defined as data going from PMW3310DH-AWQT sensor to the micro-controller, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address, is sent by the micro-controller over MOSI, and has a "0" as its MSB to indicate data direction. The second byte contains the data and is driven by PMW3310DH-AWQT sensor over MISO. The sensor outputs MISO bits on falling edges of SCLK and samples MOSI bits on every rising edge of SCLK.

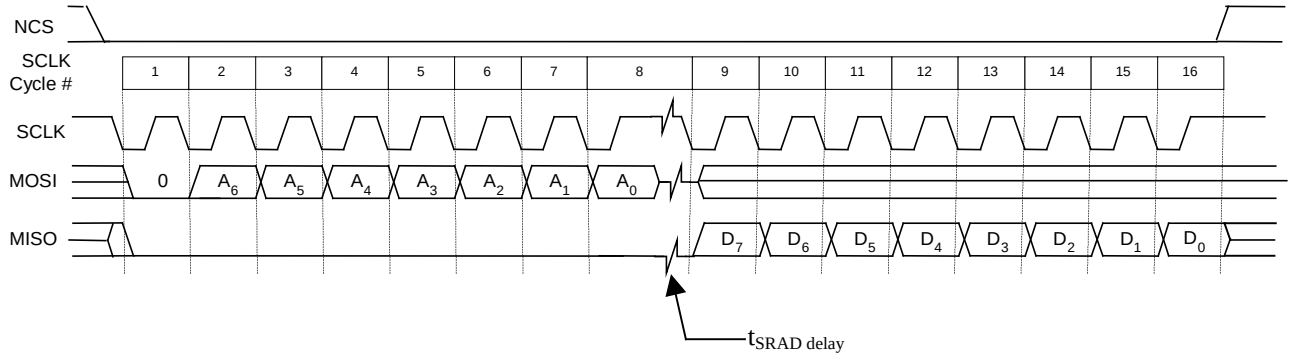

Figure 14. Read Operation

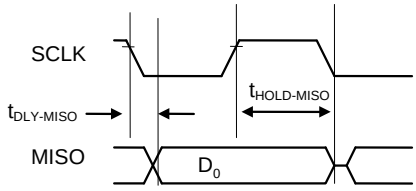

Figure 15. MISO Delay and Hold Time

Note: The minimum high state of SCLK is also the minimum MISO data hold time of PMW3310DH-AWQT sensor. Since the falling edge of SCLK is actually the start of the next read or write command, PMW3310DH-AWQT sensor will hold the state of data on MISO until the falling edge of SCLK.

Required timing between Read and Write Commands (t_{SXX})

There are minimum timing requirements between read and write commands on the serial port.

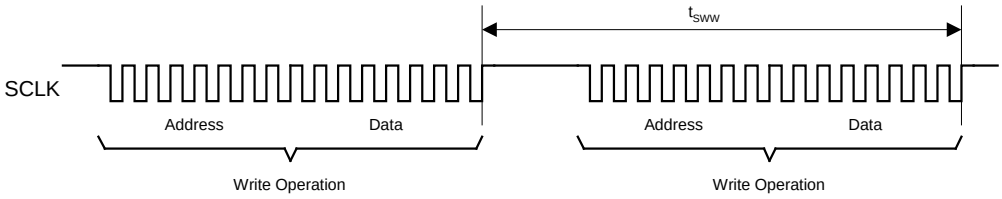

Figure 16. Timing between two write commands

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If the rising edge of the SCLK for the last data bit of the second write command occurs before the t_{sww} delay, then the first write command may not complete correctly.

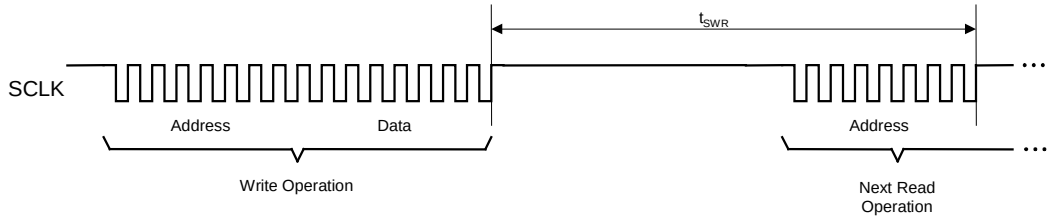

Figure 17. Timing between write and read commands

If the rising edge of SCLK for the last address bit of the read command occurs before the t_{swr} required delay, the write command may not complete correctly.

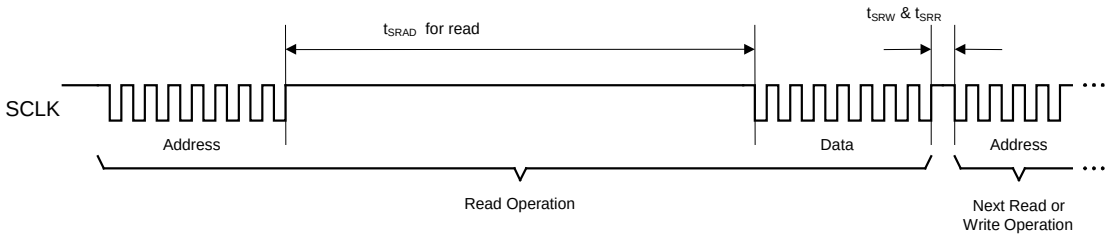

Figure 18. Timing between read and either write or subsequent read commands

During a read operation SCLK should be delayed at least t_{SRAD} after the last address data bit to ensure that the Sensor has time to prepare the requested data.

The falling edge of SCLK for the first address bit of either the read or write command must be at least t_{SRR} or t_{SRW} after the last SCLK rising edge of the last data bit of the previous read operation. In addition, during a read operation SCLK should be delayed after the last address data bit to ensure that PMW3310DH-AWQT sensor has time to prepare the requested data.

Burst Mode Operation

Burst mode is a special serial port operation mode which may be used to reduce the serial transaction time for three predefined operations: motion read and SROM download and frame capture. The speed improvement is achieved by continuous data clocking to or from multiple registers without the need to specify the register address, and by not requiring the normal delay period between data bytes.

Motion Read

Reading the Motion_Burst register activates this mode. PMW3310DH-AWQT sensor will respond with the contents of the Motion, Observation, Delta_X_L, Delta_X_H, Delta_Y_L, Delta_Y_H, Pixel Statistic and Shutter registers in that order. After sending the register address, the micro-controller must wait one frame, and then begin reading data. All data bits can be read with no delay between bytes by driving SCLK at the normal rate. The data are latched into the output buffer after the last address bit is received. After the burst transmission is complete, the micro-controller must raise the NCS line for at least t_{BEXIT} to terminate burst mode. The serial port is not available for use until it is reset with NCS, even for a second burst transmission.

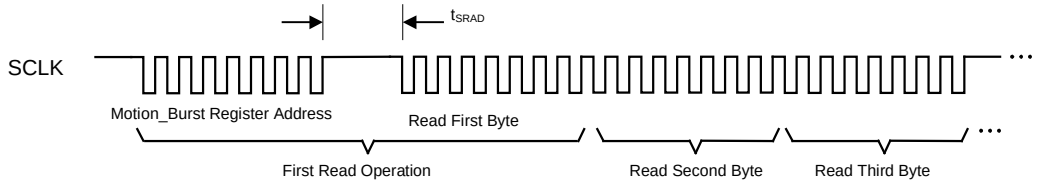

Figure 19. Motion Read Timing

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Procedure to start motion burst,

1. Lower NCS
2. Send 0x50 to Motion_Burst register.
3. Wait for one frame. (This is applicable in Run mode for wake up but not require for rest mode)
4. Start reading SPI Data continuously up to 14bytes. Motion burst may be terminated by pulling NCS high for at least t_{BEXIT}.
5. To read new motion burst data, repeating from step 1.

Information detail for motion burst report:

BYTE[00] = Motion
BYTE[01] = Observation
BYTE[02] = Delta_X_L
BYTE[03] = Delta_X_H
BYTE[04] = Delta_Y_L
BYTE[05] = Delta_Y_H
BYTE[06] = SQUAL
BYTE[07] = Pixel_Sum
BYTE[08] = Maximum_Pixel
BYTE[09] = Minimum_Pixel
BYTE[10] = Shutter_Upper
BYTE[11] = Shutter_Lower

Note: In rest mode, motion burst data is always available or in other words, motion burst data can be read from Motion_Burst register even in rest modes.

SROM Download

This function is used to load the PixArt supplied firmware file contents into PMW3310DH-AWQT after sensor power up sequence. The firmware file is an ASCII text file. In the current version of PMW3310DH-AWQT sensor, 3K bytes of SROM will be used.

SROM download procedure:

1. Write 0x1d to SROM_Enable register for initializing
2. Wait for one frame
3. Write 0x18 to SROM_Enable register again to start SROM Download
4. Write SROM file into SROM_Load_Burst register, 1st data must start with SROM_Load_Burst address. All the SROM data must be downloaded before SROM start running.

The SROM download success may be verified in two ways. Once execution from SROM space begins, the SROM_ID register will report the firmware version. At any time, a self-test may be executed which performs a CRC on the SROM contents and reports the results in a register. The test is initiated by writing 0x15 to the SROM_Enable register; the result is placed in the Data_Out_Lower and Data_Out_Upper registers. See those register description for more details.

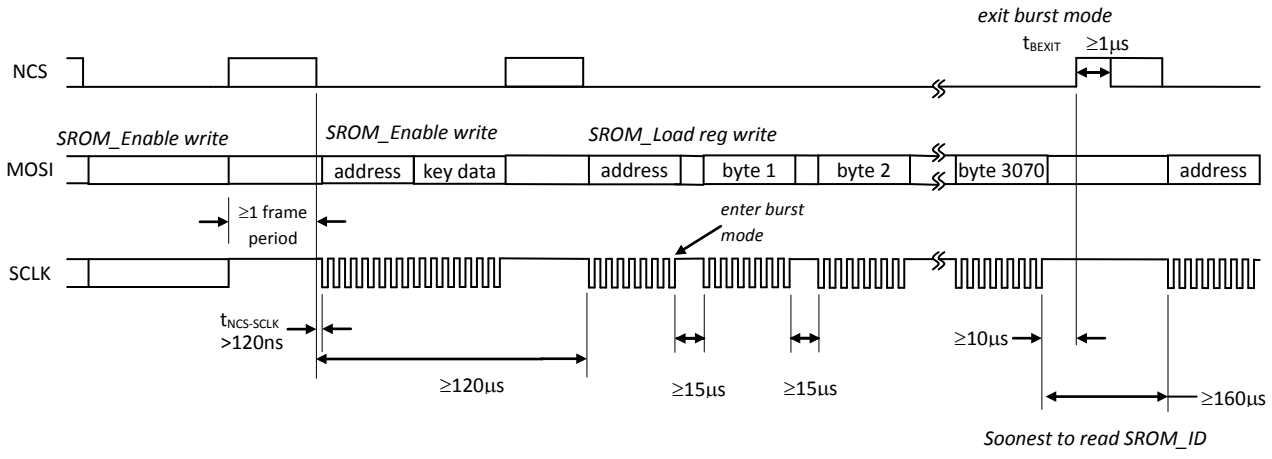

Figure 20. SROM Download Burst Mode

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Frame Capture

This is a fast way to download a full array of pixel values from a single frame. This mode disables navigation and overwrites any downloaded firmware. A hardware reset is required to restore navigation, and the firmware must be reloaded.

To trigger the capture, write to the Frame_Capture register. The next available complete 1 frame image will be stored to memory. The data are retrieved by reading the Pixel_Burst register once using the normal read method, after which the remaining bytes are clocked out by driving SCLK at the normal rate. If the Pixel_Burst register is read before the data is ready, it will return all zeros.

Procedure of Frame Capture:

1. Reset the chip by writing 0x5a to Power_Up_Reset register (address 0x3a).
2. Write 0x93 to Frame_Capture register.
3. Write 0xc5 to Frame_Capture register.
4. Wait for two frames.
5. Check for first pixel by reading bit zero of Motion register. If =1, first pixel is available.
6. Continue read from Pixel_Burst register until all 900 pixels are transferred. Refer to Pixel Map in Figure 22.
7. Continue step 1~5 to capture another frame.

Note: Manual reset and SROM download are needed after frame capture to restore navigation.

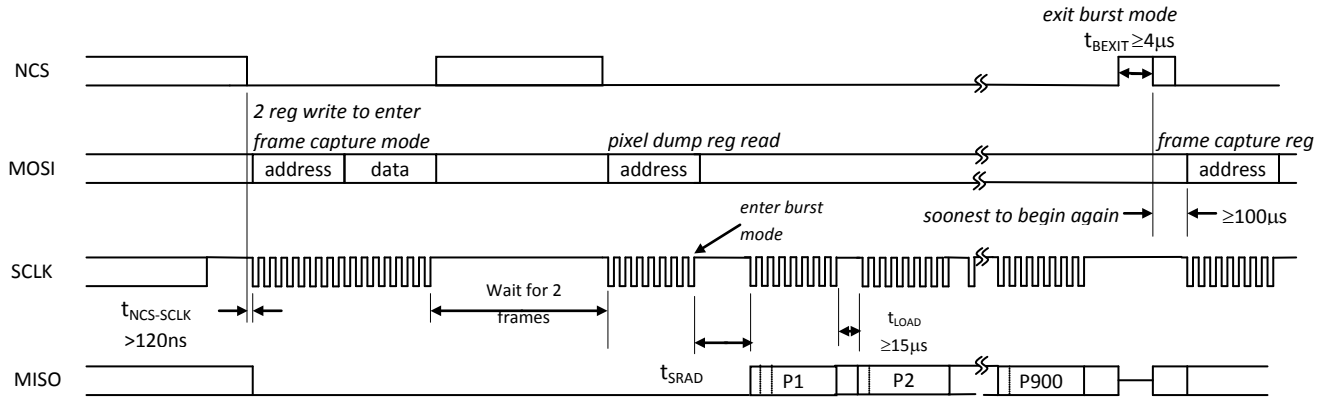

Figure 21. Frame Capture Burst Mode

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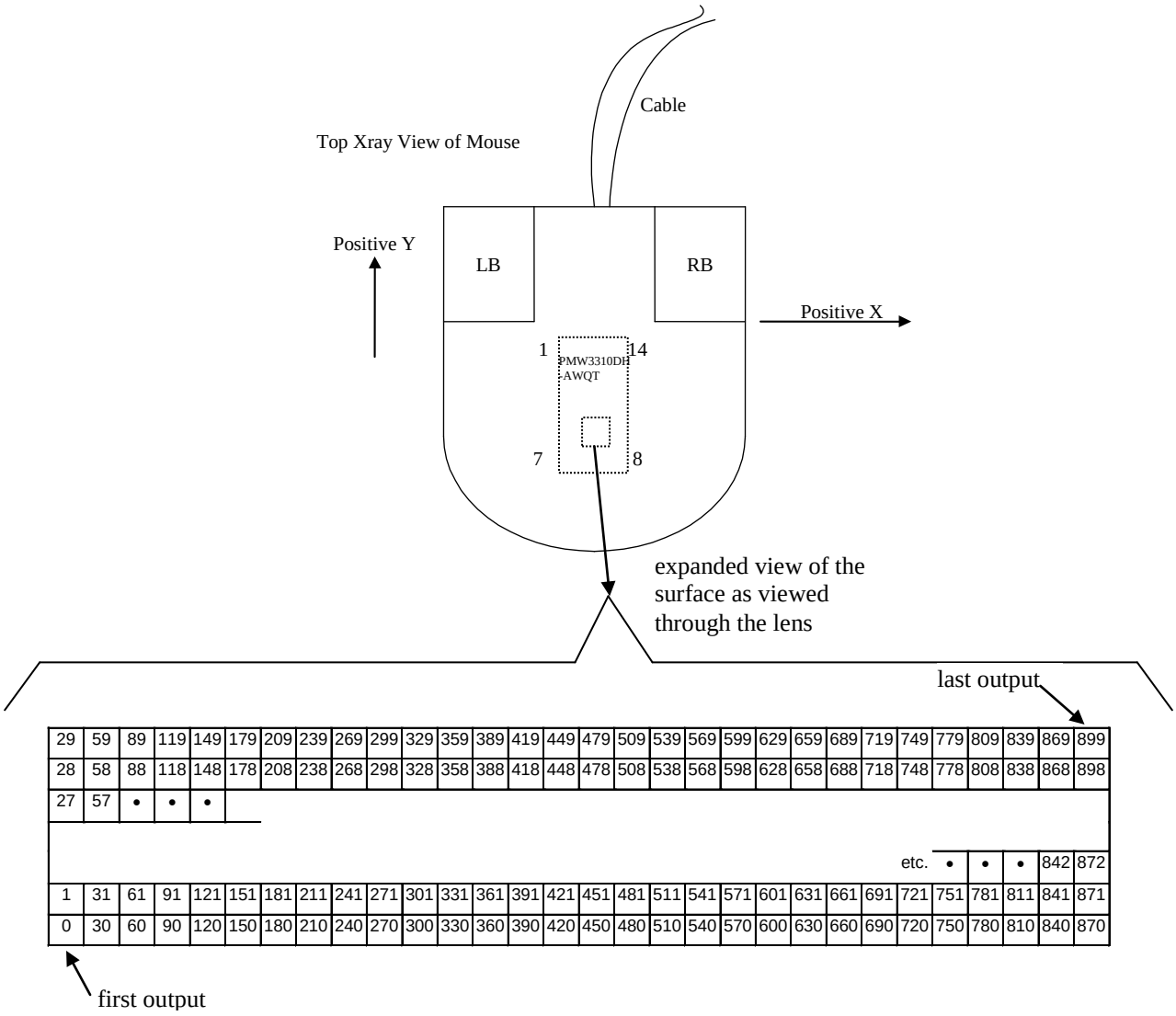

Figure 22. Pixel Map (Surface referenced)

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Power Up

PMW3310DH-AWQT sensor does not perform an internal power up self-reset; the Power_Up_Reset register must be written every time power is applied. The appropriate sequence is as follows:

1. Apply power to VDD and VDDIO in any order.
2. Drive NCS high, and then low to reset the SPI port.
3. Write 0x5a to Power_Up_Reset register (address 0x3a).
4. Wait for at least 50ms.
5. Read from registers 0x02, 0x03, 0x04, 0x05 and 0x06 (or read these same 5 bytes from burst motion register) one time regardless of the motion pin state.
6. SROM download.

During power-up there will be a period of time after the power supply is high but before normal operation. The table below shows the state of the various pins during power-up and reset.

State of Signal Pins After VDD is Valid				
Pin	On Power-Up	NCS High before Reset	NCS Low before Reset	After Reset
NCS	Functional	Hi	Low	Functional
MISO	Undefined	Undefined	Functional	Depends on NCS
SCLK	Ignored	Ignored	Functional	Depends on NCS
MOSI	Ignored	Ignored	Functional	Depends on NCS
MOTION	Undefined	Undefined	Undefined	Functional

Shutdown

PMW3310DH-AWQT can be set in Shutdown mode by writing 0xb6 to register 0x3b. The SPI port should not be accessed when Shutdown mode is asserted, except the power-up command (writing 0x5a to register 0x3a). Other ICs on the same SPI bus can be accessed, as long as the sensor's NCS pin is not asserted. The SROM download is required when wake up from Shutdown mode. To de-assert Shutdown mode:

1. Maintain VDD and VDDIO supplies to the sensor.
2. Drive NCS high, then low to reset the SPI port.
3. Write 0x5a to Power_Up_Reset register (address 0x3a).
4. Wait for at least 50ms.
5. Clear observation register.
6. Wait at least one frame and check observation register, Bit[5:0] must be set.
7. Read from registers 0x02, 0x03, 0x04, 0x05 and 0x06 (or read these same 5 bytes from burst motion register) one time regardless of the motion pin state.
8. SROM download.
9. Any register setting must then be reloaded.

The table below shows the state of various pins during shutdown.

Pin	Status when Shutdown Mode
NCS	Functional *1
MISO	Undefined *2
SCLK	Ignore if NCS = 1 *3
MOSI	Ignore if NCS = 1 *4
MOTION	Undefined *2

*1. NCS pin must be held to 1 (high) if SPI bus is shared with other devices. It is recommended to hold to 1 (high) during Power Down unless powering up the Sensor. It must be held to 0 (low) if the sensor is to be re-powered up from shutdown (writing 0x5a to register 0x3a).

*2. Depends on last state. MISO should be configured to drive LOW during shutdown to meet the low current consumption as specified in the datasheet. This can be achieved by reading Inverse_Product_ID register (address 0x3f) since the return value (0xc0) on MISO line ends in a 0 (low state).

*3. SCLK is ignored if NCS is 1 (high). It is functional if NCS is 0 (low).

*4. MOSI is ignored if NCS is 1 (high). If NCS is 0 (low), any command present on the MOSI pin will be ignored except power-up command (writing 0x5a to register 0x3a).

Note:

i. Do not turn off VDD and leave VDDIO on or vice-versa at anytime as it will introduce high leakage current path. As an alternative, both VDD and VDDIO can be turned off together in shutdown mode.

ii. There is long wakeup time from shutdown and Forced Rest. These features should not be used for power management during normal operation.

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Registers

PMW3310DH-AWQT registers are accessible via the serial port. The registers are used to read motion data and status as well as to set the device configuration.

Address	Register	Read/Write	Default Value
0x00	Product_ID	R	0x3f
0x01	Revision_ID	R	0x01
0x02	Motion	R	0x20
0x03	Delta_X_L	R	0x00
0x04	Delta_X_H	R	0x00
0x05	Delta_Y_L	R	0x00
0x06	Delta_Y_H	R	0x00
0x07	SQUAL	R	0x00
0x08	Pixel_Sum	R	0x00
0x09	Maximum_Pixel	R	0x00
0x0a	Minimum_Pixel	R	0x00
0x0b	Shutter_Lower	R	0x7a
0x0c	Shutter_Upper	R	0x31
0x0d-0x0e	Reserved		
0x0f	Configuration_A	R/W	0x24
0x10	Configuration_B	R/W	0x00
0x11	Configuration_C	R/W	0x00
0x12	Frame_Capture	R/W	0x00
0x13	SROM_Enable	W	0x00
0x14	Run_Downshift	R/W	0x32
0x15	Rest1_Rate	R/W	0x01
0x16	Rest1_Downshift	R/W	0x1f
0x17	Rest2_Rate	R/W	0x09
0x18	Rest2_Downshift	R/W	0xbc
0x19	Rest3_Rate	R/W	0x31
0x1a	FrameDuration_MaxLimit_Lower	R/W	0x60
0x1b	FrameDuration_MaxLimit_Upper	R/W	0x6d
0x1c	FrameDuration_MinLimit_Lower	R/W	0x0c
0x1d	FrameDuration_MinLimit_Upper	R/W	0x1e
0x1e	Shutter_MaxLimit_Lower	R	0xb8
0x1f	Shutter_MaxLimit_Upper	R	0x0b
0x24	Observation	R/W	0x00
0x25	Data_Out_Lower	R	Undefined
0x26	Data_Out_Upper	R	Undefined
0x27-0x28	Reserved		
0x29	Pixel_Grab	R/W	0x00
0x2a	SROM_ID	R	0x00
0x2b-0x2e	Reserved		
0x2f	Configuration_D	R/W	0x00
0x30-0x38	Reserved		

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Address	Register	Read/Write	Default Value
0x39	Configuration_E	R/W	0x00
0x3a	Power_Up_Reset	W	NA
0x3b	Shutdown	W	NA
0x3c-0x3e	Reserved		
0x3f	Inverse_Product_ID	R	0xc0
0x40-0x41	Reserved		
0x42	Snap_Angle	R/W	0x06
0x43-0x46	Reserved		
0x47	Sensor_Mode	R/W	0x01
0x48-0x4f	Reserved		
0x50	Motion_Burst	R/W	0x00
0x51-0x61	Reserved		
0x62	SROM_Load_Burst	W	NA
0x63	Reserved		
0x64	Pixel_Burst	R	0x00

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Product_ID
Access: Read Only

Address: 0x00
Reset Value: 0x3f

Bit	7	6	5	4	3	2	1	0
Field	PID_7	PID_6	PID_5	PID_4	PID_3	PID_2	PID_1	PID_0

Data Type: 8-bit unsigned integer
USAGE: This value is a unique identification assigned to this model only. The value in this register does not change; it can be used to verify that the serial communications link is functional.

Revision_ID
Access: Read Only

Address: 0x01
Reset Value: 0x01

Bit	7	6	5	4	3	2	1	0
Field	RID_7	RID_6	RID_5	RID_4	RID_3	RID_2	RID_1	RID_0

Data Type: 8-bit unsigned integer
USAGE: This register contains the current IC revision, the revision of the permanent internal firmware. It is subject to change when new IC versions are released.

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Motion Address: 0x02
Access: Read Only Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	MOT	Reserved	Lift_Off	Pix_First	Reserved	OP_Mode_1	OP_Mode_0	Frame_First

Data Type: Bit field

USAGE: Register 0x02 allows the user to determine if motion has occurred since the last time it was read. If the MOT bit is set, Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H registers should be read in sequence to get the accumulated motion. Read this register before reading the Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H registers as reading this register freezes the Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H register values. If Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H registers are not read before the motion register is read for the second time, the data in Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H will be lost. Writing anything to this register clears the MOT bit, Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H registers. The written data byte is not saved.

Field Name	Description
MOT	Motion since last report or PD 0 = No motion 1 = Motion occurred, data ready for reading in Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H registers
Lift_Off	Lift mode 0 = sensor not lifted and normal operation 1 = sensor is lifted and motion being cut off
Pix_First	This bit is set when the Pixel_Grab (address 0x29) register is written to or when a complete pixel array has been read, initiating an increment to pixel 0,0. 0 = Pixel_Grab data not from pixel 0,0 1 = Pixel_Grab data is from pixel 0,0
OP_Mode[1:0]	Operating mode of the sensor 00 = Run 01 = Rest 1 10 = Rest 2 11 = Rest 3
Frame_First	This bit is set when the Frame_Capture (address 0x12) register is written to, initiating an increment to pixel 0,0. 0 = Frame_Capture data not from pixel 0,0 1 = Frame_Capture data is from pixel 0,0

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Delta_X_L
Access: Read Only

Address: 0x03
Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0

Data Type: 16-bit 2's complement number. Lower 8 bits of Delta_X.
USAGE: X movement is counts since last report. Absolute value is determined by resolution. Reading it clears the register.

Delta_X_H
Access: Read Only

Address: 0x04
Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	X_{15}	X_{14}	X_{13}	X_{12}	X_{11}	X_{10}	X_9	X_8

Data Type: 16-bit 2's complement number. Upper 8 bits of Delta_X.
USAGE: Delta_X_H must be read after Delta_X_L to have the full motion data. Reading it clears the register.

Delta_Y_L
Access: Read Only

Address: 0x05
Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0

Data Type: 16-bit 2's complement number. Lower 8 bits of Delta_Y.
USAGE: Y movement is counts since last report. Absolute value is determined by resolution. Reading it clears the register.

Delta_Y_H
Access: Read Only

Address: 0x06
Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8

Data Type: 16-bit 2's complement number. Upper 8 bits of Delta_Y.
USAGE: Delta_Y_H must be read after Delta_Y_L to have the full motion data. Reading it clears the register.

Note: PixArt RECOMMENDS that register 0x02, 0x03, 0x04, 0x05 and 0x06 to be read sequentially.

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SQUAL
Access: Read Only

Address: 0x07
Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	SQ_7	SQ_6	SQ_5	SQ_4	SQ_3	SQ_2	SQ_1	SQ_0

Data Type: Upper 8-bits of a 10-bit unsigned integer.
USAGE: The SQUAL (Surface quality) register is a measure of the number of valid features visible by the sensor in the current frame. Use the following formula to find the total number of valid features.

Internal Squal = SQUAL * 4

The maximum SQUAL register value is 169. Since small changes in the current frame can result in changes in SQUAL, variations in SQUAL when looking at a surface are expected. The graph below shows 800 sequentially acquired SQUAL values, while a sensor was moved slowly over white paper. SQUAL is nearly equal to zero if there is no surface below the sensor. SQUAL remains fairly high throughout the Z-height range which allows illumination of most pixels in the sensor.

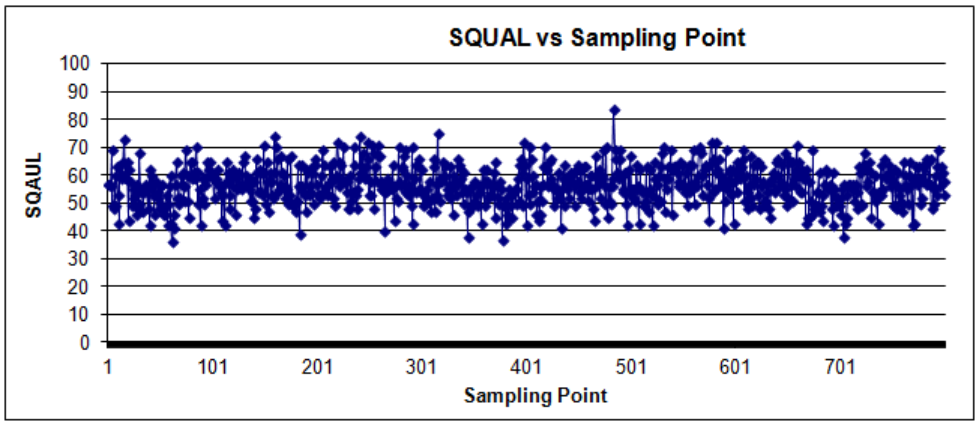

Figure 23. SQUAL Values at 1800cpi (White Paper)

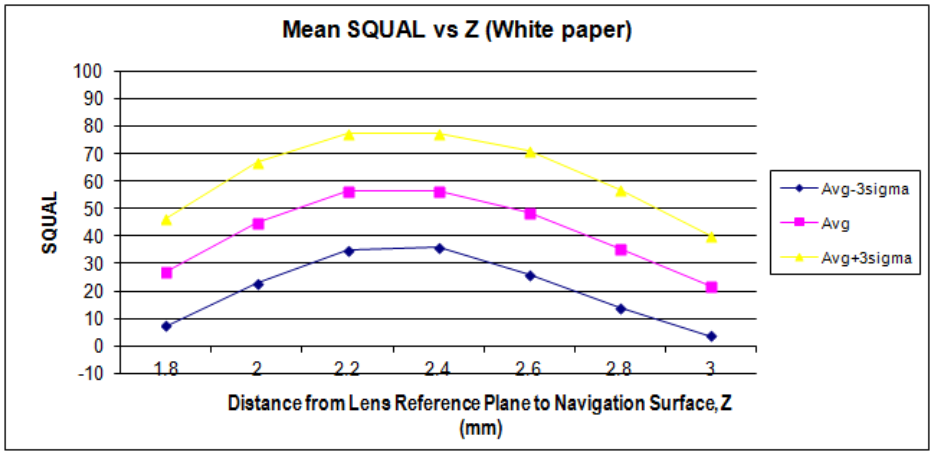

Figure 24. Mean SQUAL vs. Z (White Paper)

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Pixel_Sum
Access: Read Only

Address: 0x08
Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	AP_7	AP_6	AP_5	AP_4	AP_3	AP_2	AP_1	AP_0

Data Type: High 8-bits of an unsigned 17-bit integer.
USAGE: This register is used to find the average pixel value. It reports the upper byte of a 17-bit counter which sums all 900 pixels in the current frame. It may be described as the full sum divided by 512. To find the average pixel value follows the formula below.

Average Pixel = Register Value * 512 / 900 ≅ Register Value / 1.76

The maximum register value is 223 (127 * 900 / 512 truncated to an integer). The minimum register value is 0. The pixel sum value can change every frame.

Maximum_Pixel
Access: Read Only

Address: 0x09
Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	MP_7	MP_6	MP_5	MP_4	MP_3	MP_2	MP_1	MP_0

Data Type: 7-bit integer.
USAGE: Maximum Pixel value in current frame. Minimum value = 0, maximum value = 127. The maximum pixel value can be adjusted every frame.

Minimum_Pixel
Access: Read Only

Address: 0x0A
Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	$MinP_7$	$MinP_6$	$MinP_5$	$MinP_4$	$MinP_3$	$MinP_2$	$MinP_1$	$MinP_0$

Data Type: 7-bit integer.
USAGE: Minimum Pixel value in current frame. Minimum value = 0, maximum value = 127. The maximum pixel value can be adjusted every frame.

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Shutter_Lower
Access: Read Only

Address: 0x0B
Reset Value: 0x7a

Bit	7	6	5	4	3	2	1	0
Field	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

Shutter_Upper
Access: Read Only

Address: 0x0C
Reset Value: 0x31

Bit	7	6	5	4	3	2	1	0
Field	S_{15}	S_{14}	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8

Data Type: 16-bit unsigned integer.

USAGE: Units are clock cycles of the internal oscillator (nominally 50MHz). Read Shutter_Upper first, then Shutter_Lower. They should be read consecutively. The shutter is adjusted to keep the average pixel values within normal operating ranges. The shutter value is checked and automatically adjusted to a new value if needed on every frame when operating in default mode. The shutter value can be set manually by disabling the AGC using the Configuration_B register and writing to the Shutter_Maximum_Bound registers. Because the automatic frame rate feature is related to shutter value it may also be appropriate to enable the fixed frame rate mode using the Configuration_B register. The maximum value of the shutter is dependent upon the setting in the Shutter_Maximum_Bound registers.

Shown below is a graph of 800 sequentially acquired shutter values, while the sensor was moved slowly over white paper.

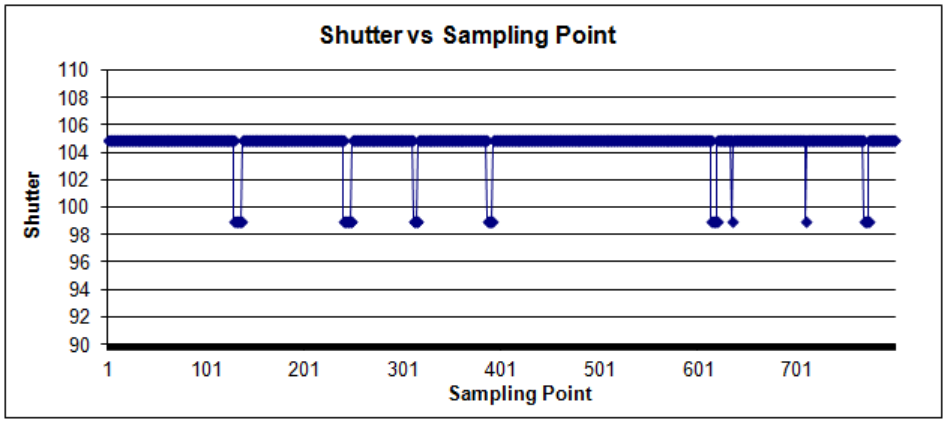

Figure 25. Shutter Values at 1800cpi (White Paper)

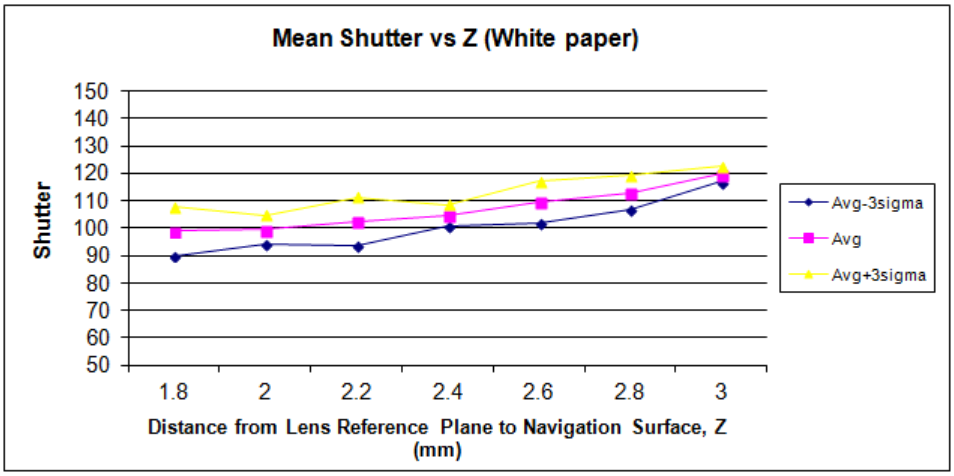

Figure 26. Mean Shutter vs. Z (White Paper)

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Configuration_A
Access: R/W

Address: 0x0F
Reset Value: 0x24

Bit	7	6	5	4	3	2	1	0
Field	RES_7	RES_6	RES_5	RES_4	RES_3	RES_2	RES_1	RES_0

Data Type: Bit field

USAGE: This register sets the resolution on XY axes or X axis only. The approximate resolution value for each register setting can be calculated using the following formula. Each bit change is ~50cpi. The maximum write value is 0x64 which the resolution setting is approximately 5000cpi.

Resolution value (counts per inch, cpi) = RES [7:0] x 50

For example:

Configuration_A Register Value	Approximate Resolution (cpi)	Description
0x01	50	Minimum
0x24	1800	Default
0x40	3200	
0x64	5000	Maximum

Note: Rpt_Mod bit in Configuration_B register is used to select CPI reporting mode either X and Y axis resolution setting in sync or independent setting for X-axis and Y-axis respectively. Refer to Configuration_D register for Y-axis resolution setting.

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Configuration_B
Access: R/W

Address: 0x10
Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	F_Rest$_1$	F_Rest$_0$	Rest_En	NAGC	Fixed_FR	Rpt_Mod	0	0

Data Type: Bit field
USAGE: This register is used to change configuration of sensor.

When the sensor is put into Force Rest function via F_Rest[1:0], the operation mode of sensor will change from current mode to the next desired Rest mode and stay at the desired Rest mode until the Force Rest mode is released. Once Force Rest mode is released, the sensor will resume to normal operation from the desired Rest mode and auto downshift to the next level of Rest modes if no motion or recover to Run mode if motion is detected.

For example:

Current mode	Next desired mode	Force Rest mode action	After Force Rest mode is released (F_Rest[1:0] = 00)
Run	Rest1	Force Rest1 F_Rest[1:0] = 01	Resume to normal operation from REST1, auto downshift to Rest2, then Rest3 in sequence if no motion or back to Run mode if motion detected.
Run	Rest2	Force Rest2 F_Rest[1:0] = 10	Resume to normal operation from REST2, auto downshift to Rest3 if no motion or back to Run mode if motion detected.
Run	Rest3	Force Rest3 F_Rest[1:0] = 11	Resume to normal operation from REST3, stay in Rest3 if no motion or back to Run mode if motion detected.

Field Name	Description
F_Rest[1:0]	Puts chip into Rest mode 00 = Normal operation 01 = Force Rest1 10 = Force Rest2 11 = Force Rest3
Rest_En	Enable Rest mode 0 = Normal operation without REST modes 1 = REST modes enabled
NAGC	Disable AGC. Shutter value will be set to the value in the Shutter_Maximum_Bound registers. 0 = no, AGC is active 1 = yes, AGC is disabled
Fixed_FR	Fixed frame rate (disable automatic frame rate control). When this bit is set the frame rate will be set by the value in the FrameDuration_MaxLimit registers. 0 = automatic frame rate 1 = fixed frame rate
Rpt_Mod	Select CPI reporting mode. 0 = XY axes CPI setting in sync 1 = CPI setting independently for X-axis and Y-axis. Configuration_A register sets X-axis resolution, while Configuration_D register sets Y-axis resolution.
BIT[1:0]	Must be set to 00

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Configuration_C
Access: R/W

Address: 0x11
Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	A_Tune_7	A_Tune_6	A_Tune_5	A_Tune_4	A_Tune_3	A_Tune_2	A_Tune_1	A_Tune_0

Data Type: Bit field

USAGE: This register can set the angle tunability feature in the sensor. The angle tune ranges from -30° to +30° with step of 1°. Any values outside the range will be ignored. The motion data output by the sensor will be rotated from the actual angle of mouse motion by the value set by A_Tune[7:0].

Field Name	Description
ANGLE[4:0]	Angle tune settings, example: 0xE2 = -30° 0xF6 = -10° 0x00 = 0° 0x0F = +15° 0x1E = +30°

Frame_Capture
Access: R/W

Address: 0x12
Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	FC_7	FC_6	FC_5	FC_4	FC_3	FC_2	FC_1	FC_0

Data Type: Bit field

USAGE: Used to capture the next available complete 1 frame of pixel values to be stored to RAM. Writing to this register will cause any firmware loaded to be overwritten and stops navigation. A hardware reset and SROM download are required to restore normal operation for motion reading. Refer to Frame Capture section for use details. The data pointer is automatically incremented after each read so all 900 pixel values may be obtained by reading this register 900 times in a row.

SROM_Enable
Access: Write only

Address: 0x13
Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	SE_7	SE_6	SE_5	SE_4	SE_3	SE_2	SE_1	SE_0

Data Type: 8-bit integer

USAGE: Write to this register to start either SROM download or SROM CRC test. See SROM Download section for details SROM download procedure.

SROM CRC test can be performed to check for the successful of SROM downloading procedure. SROM CRC test is only valid after SROM downloaded. Navigation is halted and the SPI port should not be used during this SROM CRC test. PixArt recommends reading the

SROM CRC test procedure is as below:

1. Write 0x15 to SROM_Enable register to start SROM CRC test.
2. Wait for at least 10ms.
3. Read the CRC value from Data_Lower and Data_Upper registers.

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Run_Downshift
Access: R/W

Address: 0x14
Reset Value: 0x32

Bit	7	6	5	4	3	2	1	0
Field	RD_7	RD_6	RD_5	RD_4	RD_3	RD_2	RD_1	RD_0

Data Type: 8-bit integer
USAGE: This register sets the Run to Rest 1 downshift time. Default value is 500ms. Use the formula below for calculation.

Run Downshift time (ms) = RD[7:0] x 10
Default = 50 x 10 = 500ms

All the above values are calculated based on system clock, which is expected to have 20% tolerance.

Rest1_Rate
Access: R/W

Address: 0x15
Reset Value: 0x01

Bit	7	6	5	4	3	2	1	0
Field	$R1R_7$	$R1R_6$	$R1R_5$	$R1R_4$	$R1R_3$	$R1R_2$	$R1R_1$	$R1R_0$

Data Type: 8-bit integer
USAGE: This register sets the Rest 1 frame rate duration. Default value is 20ms. Use the formula below for calculation.

Rest1 frame rate duration = (R1R[7:0] + 1) x 10ms.
Default = (1 + 1) x 10 = 20ms

All the above values are calculated based on 100Hz Hibernate clock, which is expected to have 40% tolerance.

Rest1_Downshift
Access: R/W

Address: 0x16
Reset Value: 0x1f

Bit	7	6	5	4	3	2	1	0
Field	$R1D_7$	$R1D_6$	$R1D_5$	$R1D_4$	$R1D_3$	$R1D_2$	$R1D_1$	$R1D_0$

Data Type: 8-bit integer
USAGE: This register sets the Rest 1 to Rest 2 downshift time. Default value is 9920ms. Use the formula below for calculation.

Rest1 Downshift time = R1D[7:0] x 16 x Rest1_Rate.
Default = 31 x 16 x 20 = 9920ms

All the above values are calculated based on 100Hz Hibernate clock, which is expected to have 40% tolerance.

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Rest2_Rate
Access: R/W

Address: 0x17
Reset Value: 0x09

Bit	7	6	5	4	3	2	1	0
Field	$R2R_7$	$R2R_6$	$R2R_5$	$R2R_4$	$R2R_3$	$R2R_2$	$R2R_1$	$R2R_0$

Data Type: 8-bit integer
USAGE: This register sets the Rest 2 frame rate duration. Default value is 100ms. Use the formula below for calculation.

Rest2 frame rate duration = (R2R[7:0] + 1) x 10ms.
Default = (9 + 1) x 10 = 100ms

All the above values are calculated based on 100Hz Hibernate clock, which is expected to have 40% tolerance.

Rest2_Downshift
Access: R/W

Address: 0x18
Reset Value: 0xbc

Bit	7	6	5	4	3	2	1	0
Field	$R2D_7$	$R2D_6$	$R2D_5$	$R2D_4$	$R2D_3$	$R2D_2$	$R2D_1$	$R2D_0$

Data Type: 8-bit integer
USAGE: This register sets the Rest 2 to Rest 3 downshift time. Default value is 10mins. Use the formula below for calculation.

Rest2 Downshift time = R2D[7:0] x 32 x Rest2_Rate.
Default = 188 x 32 x 100 = 601.6s = 10mins

All the above values are calculated based on 100Hz Hibernate clock, which is expected to have 40% tolerance.

Rest3_Rate
Access: R/W

Address: 0x19
Reset Value: 0x31

Bit	7	6	5	4	3	2	1	0
Field	$R3R_7$	$R3R_6$	$R3R_5$	$R3R_4$	$R3R_3$	$R3R_2$	$R3R_1$	$R3R_0$

Data Type: 8-bit integer
USAGE: This register sets the Rest 3 frame rate duration. Default value is 500ms. Use the formula below for calculation.

Rest3 frame rate duration = (R3R[7:0] + 1) x 10ms.
Default = (49 + 1) x 10 = 500ms

All the above values are calculated based on 100Hz Hibernate clock, which is expected to have 40% tolerance.

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FrameDuration_MaxLimit_Lower Address: 0x1A
Access: R/W Reset Value: 0x60

Bit	7	6	5	4	3	2	1	0
Field	FLM_7	FLM_6	FLM_5	FLM_4	FLM_3	FLM_2	FLM_1	FLM_0

FrameDuration_MaxLimit_Upper Address: 0x1B
Access: R/W Reset Value: 0x6d

Bit	7	6	5	4	3	2	1	0
Field	FLM_{15}	FLM_{14}	FLM_{13}	FLM_{12}	FLM_{11}	FLM_{10}	FLM_9	FLM_8

Data Type: 16-bit unsigned integer

USAGE: This value sets the maximum frame duration in automatic frame rate control mode or actual frame duration in manual mode. To read back the registers value, read the Upper (0x1B) register first then follow by Lower (0x1A) register. To write into the registers, write Lower register first, then follow by Upper register. Units are in clock cycles of internal oscillator (nominally 50MHz). The formula is:

Frame Rate (fps) = Internal Oscillator Clock Frequency (MHz) / Register Value

To set the frame rate manually, disable automatic frame rate mode via the Configuration_B register and write the desired count value to these registers. Writing to the FrameDuration_MaxLimit_Upper and Lower registers also activate any new values in the following registers:

- FrameDuration_MinLimit_Upper and Lower
- Shutter_MaxLimit_Upper and Lower

Any data written to the other two sets of registers will be saved but will not take effect until the write to the FrameDuration_MaxLimit_Upper and Lower is completed. After writing to this register, two complete frame times are required to implement the new settings. Writing to any of the above registers before the implementation is completed may put the chip into an undefined state which requires reset.

The three limit registers must also follow this rule when set to non-default values. There is no protection against illegal register settings, which will impact the navigation.

FrameDuration_MaxLimit ≥ *FrameDuration_MinLimit* + *Shutter_MaxLimit.*

The following table lists some Frame Duration example values with a 50MHz clock.

Frame Rate	Frame Duration		FrameDuration Register Value	
	Decimal	Hex	Upper	Lower
1,800	27,777	6c81	6c	81
2,000	25,000	61a8	61	a8
3,200	15,625	3d09	3d	09
5,000	10,000	2710	27	10
6,500	7692	1e0c	1e	0c

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FrameDuration_MinLimit_Lower
Access: R/W

Address: 0x1C
Reset Value: 0x0c

Bit	7	6	5	4	3	2	1	0
Field	FLN_7	FLN_6	FLN_5	FLN_4	FLN_3	FLN_2	FLN_1	FLN_0

FrameDuration_MinLimit_Upper
Access: R/W

Address: 0x1D
Reset Value: 0x1e

Bit	7	6	5	4	3	2	1	0
Field	FLN_{15}	FLN_{14}	FLN_{13}	FLN_{12}	FLN_{11}	FLN_{10}	FLN_9	FLN_8

Data Type: 16-bit unsigned integer

USAGE: This value sets the minimum frame duration in automatic frame rate control mode or actual frame duration in manual mode. To read back the registers value, read the Upper (0x1D) register first then follow by Lower (0x1C) register. To write into the registers, write Lower register first, then follow by Upper register, then write anything to the FrameDuration_MaxLimit Lower and Upper registers to activate the new settings, wait at least two frame times before writing to FrameDuration_MinLimit_Upper or Lower again. A good practice is to read the content of the FrameDuration_MaxLimit registers and write it back, please refer to FrameDuration_MaxLimit register USAGE for details. Units are in clock cycles of internal oscillator (nominally 50MHz). The formula is:

Frame Rate (fps) = Internal Oscillator Clock Frequency / Register Value

In addition, the three limit registers must also follow this rule when set to non-default values:

FrameDuration_MaxLimit ≥ *FrameDuration_MinLimit* + *Shutter_MaxLimit.*

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Shutter_MaxLimit_Lower
Access: Read Only

Address: 0x1E
Reset Value: 0xb8

Bit	7	6	5	4	3	2	1	0
Field	SB_7	SB_6	SB_5	SB_4	SB_3	SB_2	SB_1	SB_0

Shutter_MaxLimit_Upper
Access: Read Only

Address: 0x1F
Reset Value: 0x0b

Bit	7	6	5	4	3	2	1	0
Field	SB_{15}	SB_{14}	SB_{13}	SB_{12}	SB_{11}	SB_{10}	SB_9	SB_8

Data Type: 16-bit unsigned integer

USAGE: This value sets the maximum allowable shutter value when operating in automatic mode. Units are clock cycles of internal oscillator (nominally 50MHz). Since the automatic frame rate function is based on shutter value, the value in these registers can limit the range of the frame rate control.

To read back the registers value, read the Upper (0x1F) register first then follow by Lower (0x1E) register. To write into the registers, write Lower register first, then follow by Upper register, then write anything to the FrameDuration_MaxLimit Lower and Upper registers to activate the new settings, wait at least two frame times before writing to FrameDuration_MinLimit_Upper or Lower again. A good practice is to read the content of the FrameDuration_MaxLimit registers and write it back, please refer to FrameDuration_MaxLimit register USAGE for details. To set the shutter manually, disable the AGC via the Configuration_B register and write the desired value to these registers.

In addition, the three limit registers must also follow this rule when set to non-default values:

$$FrameDuration\_MaxLimit \geq FrameDuration\_MinLimit + Shutter\_MaxLimit$$

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Observation — Address: 0x24
Access: R/W — Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	OB_7	OB_6	OB_5	OB_4	OB_3	OB_2	OB_1	OB_0

Data Type: Bit field
USAGE: The user must clear the register by writing 0x00, delay for one frame, and read the register. The active processes will set their corresponding bit indicating the sensor is functioning. This register may be used as part of a recovery scheme to detect a problem caused by EFT/B or ESD by monitoring the OB[5:0] status.

Field Name	Description
OB_6	0 = chip is not running SROM code 1 = chip is running SROM code
OB[5:0]	Navigation flag. Set once per frame

Data_Out_Lower — Address: 0x25
Access: Read Only — Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
Field	DO_7	DO_6	DO_5	DO_4	DO_3	DO_2	DO_1	DO_0

Data_Out_Upper — Address: 0x26
Access: Read Only — Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
Field	DO_{15}	DO_{14}	DO_{13}	DO_{12}	DO_{11}	DO_{10}	DO_9	DO_8

Data Type: 16-bit word
USAGE: Data in these registers come from the SROM CRC test. The data can be read out in either order.

CRC Result	Data_Out_Upper	Data_Out_Lower
SROM CRC test	BE	EF

SROM CRC Test: Performs a CRC test on the SROM contents. The test is initiated by writing 0x15 to SROM_Enable register.

Pixel_Grab — Address: 0x29
Access: R/W — Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	Valid	Pix_D_6	Pix_D_5	Pix_D_4	Pix_D_3	Pix_D_2	Pix_D_1	Pix_D_0

Data Type: 8-bit unsigned integer
USAGE: Write any value to this register to initialize the pixel dump. Read motion register to check if first pixel is ready, and then read data from this register for the pixel data.

If Rest mode enable, make sure force awake before do pixel dump, procedure as below,
1) Write 0 to bit 5 of register 0x10 (Configuration_B) to force the sensor awake
2) Read pixel dump data section for more details
3) Write 1 to bit 5 to register 0x10 (Configuration_B) to enable rest mode again

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SROM_ID
Access: Read only

Address: 0x2A
Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	SR_7	SR_6	SR_5	SR_4	SR_3	SR_2	SR_1	SR_0

Data Type: 8-bit unsigned integer
USAGE: Contains the revision of the downloaded SROM firmware. If the firmware has been successfully downloaded and the chip is operating out of SROM, this register will contain the SROM firmware revision; otherwise it will contain 0x00.

Configuration_D
Access: R/W

Address: 0x2F
Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	$ResY_7$	$ResY_6$	$ResY_5$	$ResY_4$	$ResY_3$	$ResY_2$	$ResY_1$	$ResY_0$

Data Type: Bit field
USAGE: This register allows the user to change the Y-axis resolution when the sensor is configured to have independent X-axis and Y-axis resolution reporting mode via Rpt_Mod = 1 (Configuration_B register, bit-2). The setting in this register will be inactive if Rpt_Mod = 0. The approximate resolution value for each register setting can be calculated using the following formula. Each bit change is~50cpi. The minimum write value is 0x01 and maximum is 0x64.

Resolution value (counts per inch, cpi) = RES [7:0] x 50

Configuration_E
Access: R/W

Address: 0x39
Reset Value: 0x02

Bit	7	6	5	4	3	2	1	0
Field	Reserve	Reserve	Reserve	Reserve	Reserve	Reserve	Reserve	Res_Ang_Pr

Data Type: Bit field
USAGE: The order of resolution scaling and angle tune rotation functions can be selected via Res_Ang_Pr bit. When Res_Ang_Pr = 0, the sensor will perform the resolution scaling as per setting in Configuration_A register, followed by the angle tune rotation set in Configuration_C register and vise versa for the setting Res_Ang_Pr = 1.

Field Name	Description
Res_Ang_Pr	= 0: Resolution Scaling first then Angle Tune Rotation. = 1: Angle Tune Rotation first then Resolution Scaling

Power_Up_Reset
Access: Write Only

Address: 0x3A
Reset Value: NA

Bit	7	6	5	4	3	2	1	0
Field	PUR_7	PUR_6	PUR_5	PUR_4	PUR_3	PUR_2	PUR_1	PUR_0

Data Type: 8-bit integer
USAGE: Write 0x5a to this register to reset the chip. All settings will revert to default values. Reset is required after recovering from shutdown mode and restore normal operation after Frame Capture.

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Shutdown
Access: Write Only

Address: 0x3B
Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
Field	SD_7	SD_6	SD_5	SD_4	SD_3	SD_2	SD_1	SD_0

Data Type: 8-bit integer
USAGE: Write 0xb6 to set the chip to shutdown mode and use Power_Up_Reset register to wake up the chip from shutdown. Refer to Shutdown section for more details.

Inverse_Product_ID
Access: R

Address: 0x3F
Reset Value: 0xc0

Bit	7	6	5	4	3	2	1	0
Field	PID_7	PID_6	PID_5	PID_4	PID_3	PID_2	PID_1	PID_0

Data Type: 8-bit unsigned integer
USAGE: This value is the inverse of the Product_ID, located at the inverse address. It is used to test the SPI port hardware.

Snap_Angle
Access: R/W

Address: 0x42
Reset Value: 0x06

Bit	7	6	5	4	3	2	1	0
Field	Snap_En	Reserve	Reserve	Reserve	$Snap\_Thr_3$	$Snap\_Thr_2$	$Snap\_Thr_1$	$Snap\_Thr_0$

Data Type: Bit field
USAGE: The snap angle register is used to enable or disable the Angle Snapping function. When it is enabled, actual movement ranges from ±5degrees from X or Y-axis will be output as either X or Y-axis only motion data. For example, if the sensor is moved at a+ 2degree from X-axis, the motion data output will be single X-axis at 0degree.

Field Name	Description
Snap_En	Angle Snapping function = 0 : Disable = 1 : Enable
Snap_Thr[3:0]	Snap angle threshold, rough calculation as below, Tan^{-1} ((Snap_Thr[3:0] – 1) / 32). For example: if set to 0x83 Tan-1 (2/32) = 3.57degree

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Sensor_Mode
Access: R/W

Address: 0x47
Reset Value: 0x01

Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	VFR_ON

Data Type: Bit field
USAGE: The register is used to enable or disable variable frame rate for power saving purpose.

Field Name	Description
VFR_ON	Frame Rate = 0 : Fixed Frame Rate = 1 : Enable Variable Frame Rate

Motion_Burst
Access: R/W

Address: 0x50
Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	MB_7	MB_6	MB_5	MB_4	MB_3	MB_2	MB_1	MB_0

Data Type: 8-bit unsigned integer
USAGE: The Motion_Burst register is used for high-speed access to the Motion, Delta_X_L, Delta_X_H, Delta_Y_L, Delta_Y_H, SQUAL, Pixel_Sum, Maximum_Pixel, Minimum_Pixel, Shutter_Upper and Shutter_Lower registers. See Burst Mode-Motion Read section for use details. Write any value to this register will clear all motion burst data.

SROM_Load_Burst
Access: Write Only

Address: 0x62
Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
Field	SL_7	SL_6	SL_5	SL_4	SL_3	SL_2	SL_1	SL_0

Data Type: Bit field
USAGE: The SROM_Load_Burst register is used for high-speed programming SROM from an external memory or micro-controller. See SROM Download section for use details.

Pixel_Burst
Access: Read Only

Address: 0x64
Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	PB_7	PB_6	PB_5	PB_4	PB_3	PB_2	PB_1	PB_0

Data Type: 8-bit unsigned integer
USAGE: The Pixel_Burst register is used for high-speed access to all the pixel values for one complete frame capture, without writing to the register address to obtain each pixel data. The data pointer is automatically incremented after each read so all 900 pixel values may be obtained by reading this register 900 times. See Frame Capture section for use details.

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