PixArt Imaging Inc.

PMW3610DM-SUDU
Low Power Laser Mouse Sensor

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

Description

The PMW3610DM-SUDU integrated molded lead-frame DIP laser sensor comprises of sensor and VCSEL in a single package. PMW3610DM-SUDU provides enhanced features such as programmable resolution, configurable sleep and wake up time to suit various wireless optical navigation applications.

The advanced class of VCSEL was engineered by Pixart to provide a laser diode with a single longitudinal and a single transverse mode.

This laser sensor is in 16-pin integrated molded lead-frame (DIP) package. It is designed to be used with LM18-LSI lens to achieve the optimum performance featured in this document. These parts provide a complete and compact navigation system without moving parts. Laser calibration process is NOT required in the complete system; it was pre-calibrated at sensor level which helps to facilitate high volume assembly.

Theory of Operation

The sensor is based on Pixart Laser Technology, which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determines the direction and magnitude of movement. It contains an Image Acquisition System (IAS), a Digital Signal Processor (DSP), and a three wire serial port. The IAS acquires microscopic surface images via the lens and illumination system. These images are processed by the DSP to determine the direction and distance of motion. The DSP calculates the Δx and Δy relative displacement values. An external microcontroller reads the Δx and Δy information from the sensor serial port. The microcontroller then translates the data into USB or RF signals before sending them to the host PC or game console.

Features

- Small form factor molded lead frame 16-pin DIP package
- Single low operating voltage: 1.7 – 2.1V
- 12-bits motion data registers
- High speed motion detection up to 30ips and acceleration up to 10g
- Advanced technology 832-865nm wavelength VCSEL (single mode)
- Pre-calibrated laser power
- Compliance to IEC/EN 60825-1 Eye Safety
  - Class 1 laser power output level
  - On-chip laser fault detection circuitry
- Motion detect pin output
- Internal oscillator – no clock input needed
- Built-in laser control MOSFET
- 3-wire SPI communication with NRESET
- Improved dust robustness
- Enhanced Programmability
  - Resolution up to 3200 cpi with 200 cpi step
  - Downshift and wake up time
  - Sensor orientation

Applications

- Laser mice
- Optical trackballs
- Motion input devices

Pin out of PMW3610DM-SUDU Optical Mouse Sensor

Pin	Name	IN/OUT /PWR	Description
1	+VCSEL	IN	Positive terminal of VCSEL
2	SDIO	IN/OUT	Serial data input/output
3	SCLK	IN	Serial clock input
4	NC	-	-
5	NCS	IN	Chip select
6	VDDIO	IN	IO voltage input
7	NRESET	IN	Reset (Active low)
8	MOTION	OUT	Motion detect (Active low)
9	VCP	PWR	Internal PMOSFET source
10	PASS_T	PWR	Internal PMOSFET drain (to connect to +ve VCSEL)
11	GND	IN	Ground
12	CP	PWR	Charge pump capacitor +ve terminal
13	CN	PWR	Charge pump capacitor -ve terminal
14	VDD	IN	1.8V supply input
15	XYLASER	IN	XYLASER (Connect to -ve VCSEL)
16	-VCSEL	IN	Negative terminal of VCSEL

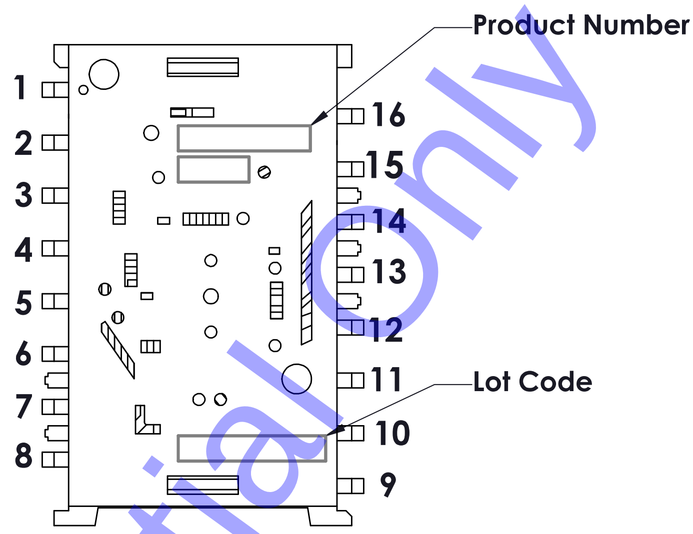
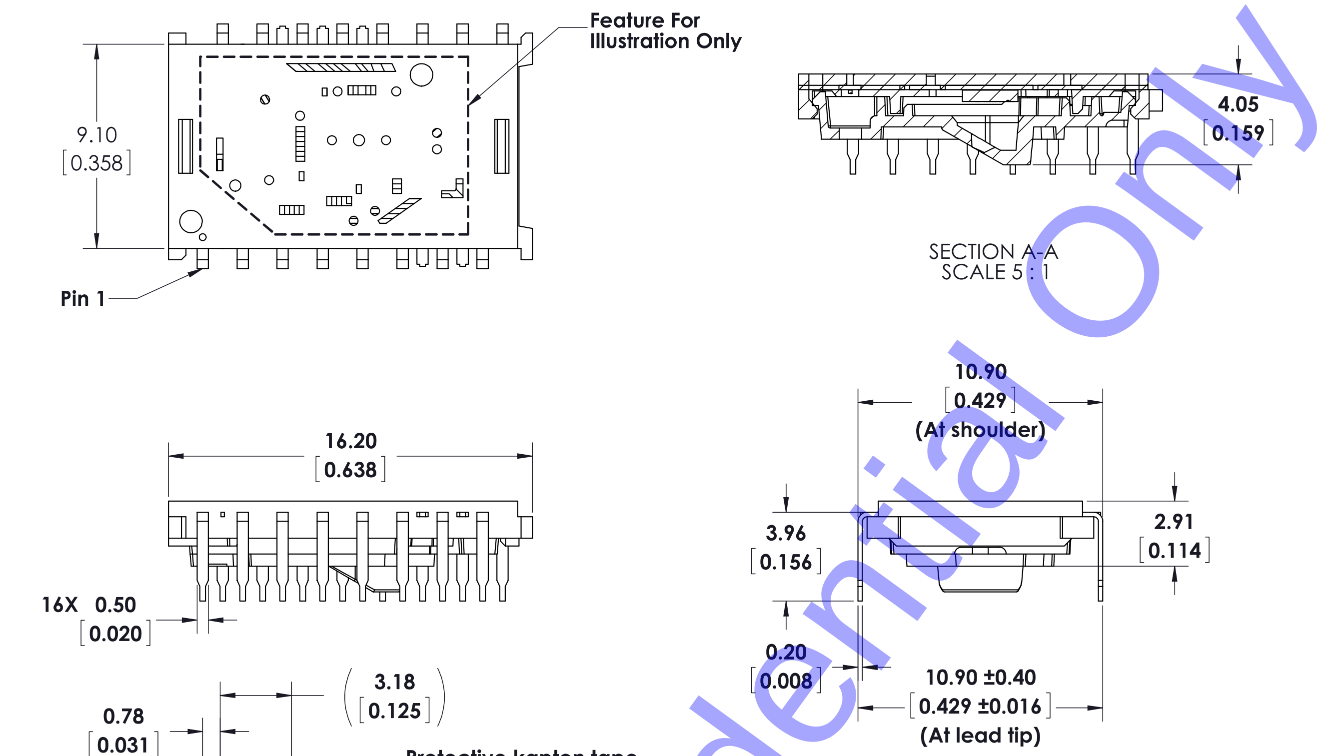
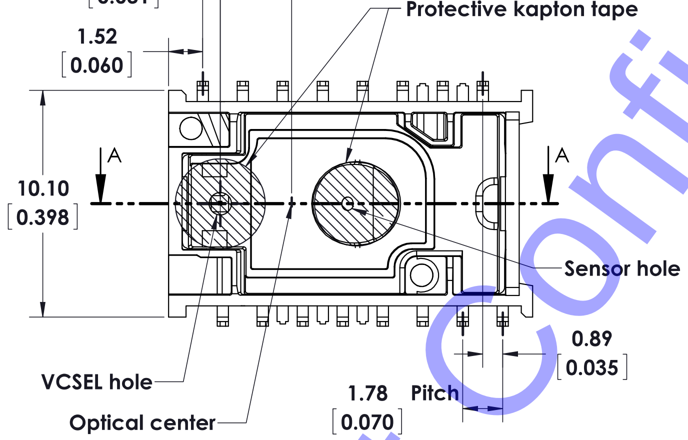


Figure 1. Package Pin out

Item	Marking	Remark
Part Number	PMW3610DM- SUDU	
Lot Code	AYWWXXXXX	A – Assy house
		Y – Year
		WW – Week
		XXXXX – PixArt reference





Notes:

1. Dimensions in milimeter [inches].
2. Dimensional tolerance: ±0.1mm.
3. Coplanarity of lead: 0.1mm.
4. Lead pitch tolerance: ±0.15mm.
5. Non-cumulative pitch tolerance: ±0.15mm.
6. Maximum flash: 0.2mm.
7. Angular tolerance: ±3°.
8. Chamfer (25°x2) on the taper side of the lead.
9. Dimension in brackets () indicate reference dimension.
10. Document Number: LSR_INT_16A_Pkg_005.

Figure 2 . Package outline drawing

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

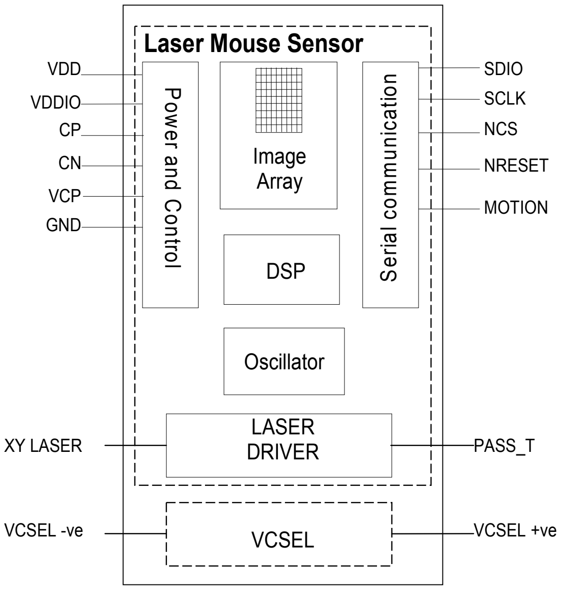


Figure 3. Block diagram of PMW3610DM-SUDU

Regulatory Requirements

- Passes FCC B and worldwide analogous emission limits when assembled into a mouse with shielded cable and following Pixart recommendations.
- Passes IEC-1000-4-3 radiated susceptibility level when assembled into a mouse with shielded cable and following Pixart recommendations.
- Passes IEC-61000-4-2 Electrostatic Discharge Immunity Test (ESD) and provides sufficient ESD creepage/ clearance distance to withstand discharge up to 15KV when assembled into a mouse according to usage instructions above.
- Passes IEC/EN 60825-1 Eye Safety Class 1 when operating with the laser output power pre-calibrated by Pixart without external hardware and software control of laser current.

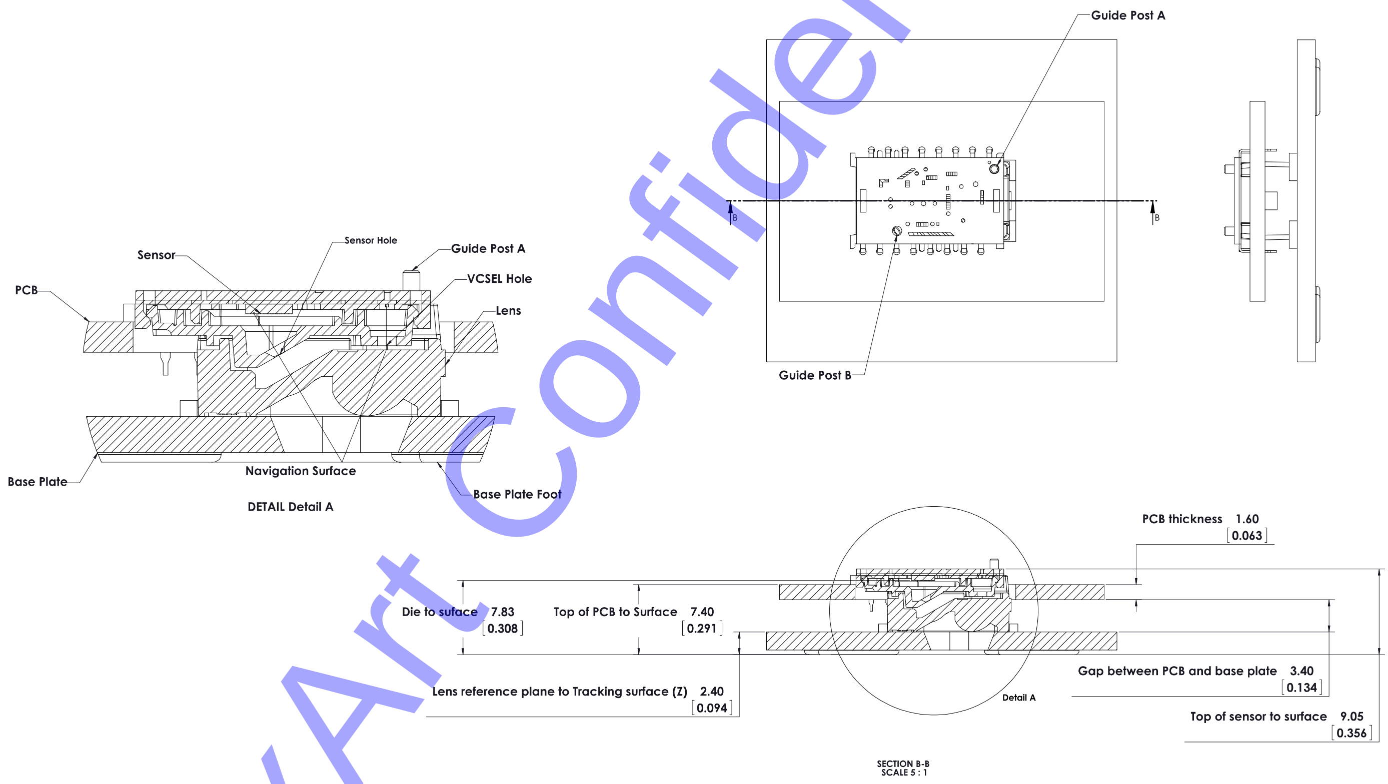


Figure 4. 2D Assembly drawing of PMW3610DM-SUDU sensor and LM18-LSI lens coupled with PCB and base plate(top and cross-sectional view)

Assembly Recommendation

1. Insert the integrated molded lead-frame DIP sensor and all other electrical components into the application PCB.

2. This sensor package is only qualified for wave solder process.

3. Wave-solder the entire assembly in a no-wash soldering process utilizing a solder fixture. The solder fixture is needed to provide protection to the sensor body from flux spraying and wave solder process. Avoid getting any flux onto sensor body as there is potential for flux fumes to seep into the sensor package. The fixture should be designed to expose only the sensor leads to flux/ solder while shielding the entire body of the sensor from direct contact with flux/ solder.

4. Place the lens onto the base plate. Care must be taken to avoid contamination on the optical surfaces.

5. Remove the protective kapton tapes from the optical aperture of the sensor and VCSEL respectively. Care must be taken to keep contaminants from entering the aperture.

6. Insert the PCB assembly over the lens onto the base plate. The sensor package should self-align to the lens. The optical position reference for the PCB is set by the base plate and lens. The alignment guide post of the lens locks the lens and integrated molded lead-frame DIP sensor together. Note that the PCB motion due to button presses must be minimized to maintain optical alignment.

7. Recommended: The lens can be permanently locked to the sensor package by melting the lens' guide posts over the sensor with heat staking process.

8. Install the mouse top case. There must be a feature in the top case (or other area) to press down onto the sensor to ensure the sensor and lenses are interlocked to the correct vertical height.

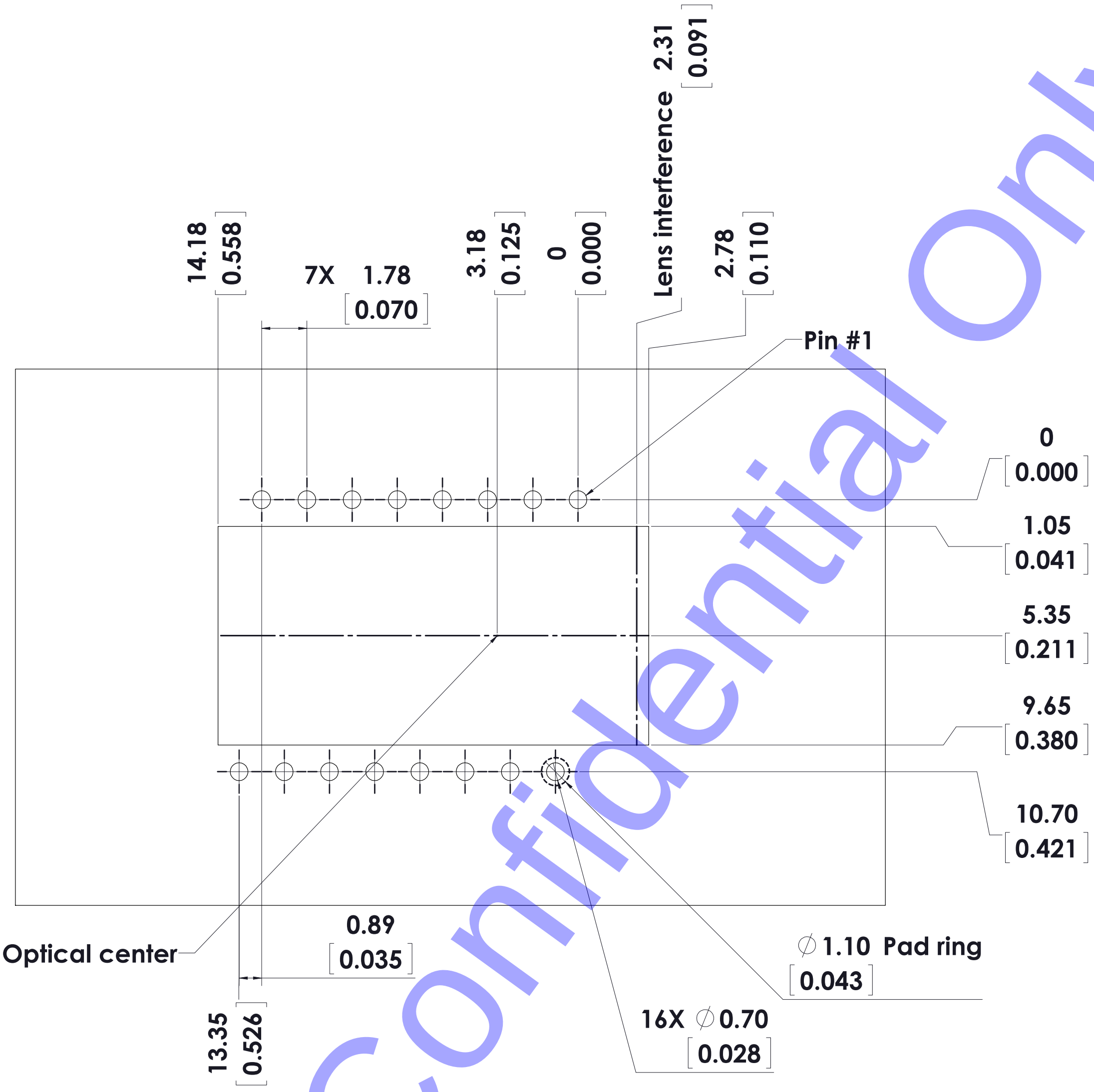


Figure 5. Recommended PCB mechanical cutouts and spacing

Application circuits

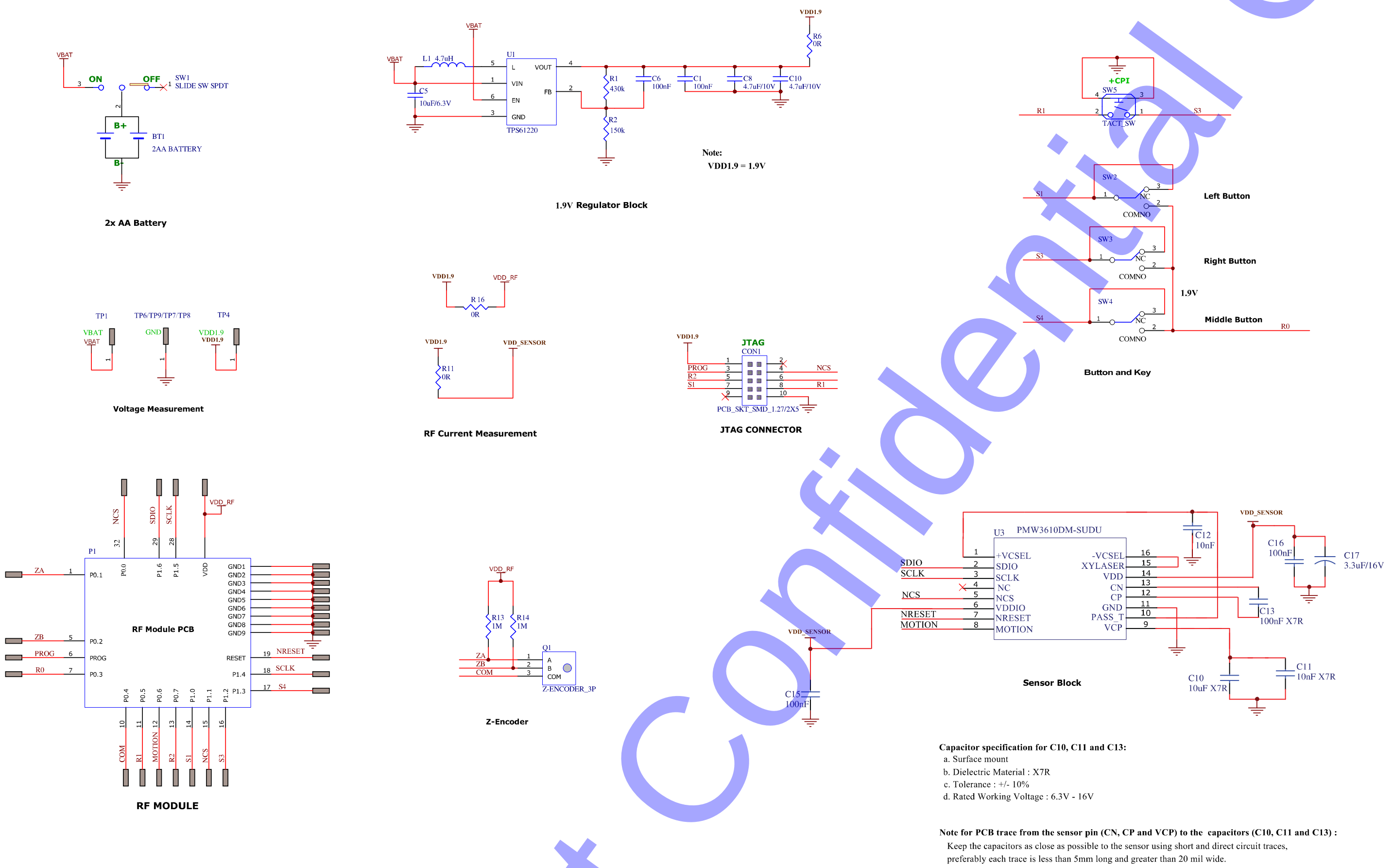


Figure 6. Schematic Diagram

Eye Safety

The PMW3610DM-SUDU sensor and the associated components in the schematic of Figure 6 are intended to comply with Class 1 Eye Safety Requirements of IEC 60825-1. Pixart calibrates the sensor's laser output power (LOP) to Class 1 eye safety level and store the registers values that control the LOP prior shipping out, thus no LOP calibration is required in complete mouse system at manufacturer site.

PMW3610DM-SUDU sensor is designed to maintain the laser output power using LM18-LSI lens within Class 1 Eye Safety requirements over components manufacturing tolerances under the recommended operating conditions and application circuits of Figure 6 as specified in this document. Under normal operating condition, the sensor generates the drive current for the VCSEL. Increasing the LOP by other means on hardware and software can result in a violation of the Class 1 eye safety limit of 716W.

Single Fault Detection

PMW3610DM-SUDU is able to detect a short circuit or fault condition at the XYLASER pin, which could lead to excessive laser power output. A path to ground on this pin will trigger the fault detection circuit, which will turn off the laser drive current source.

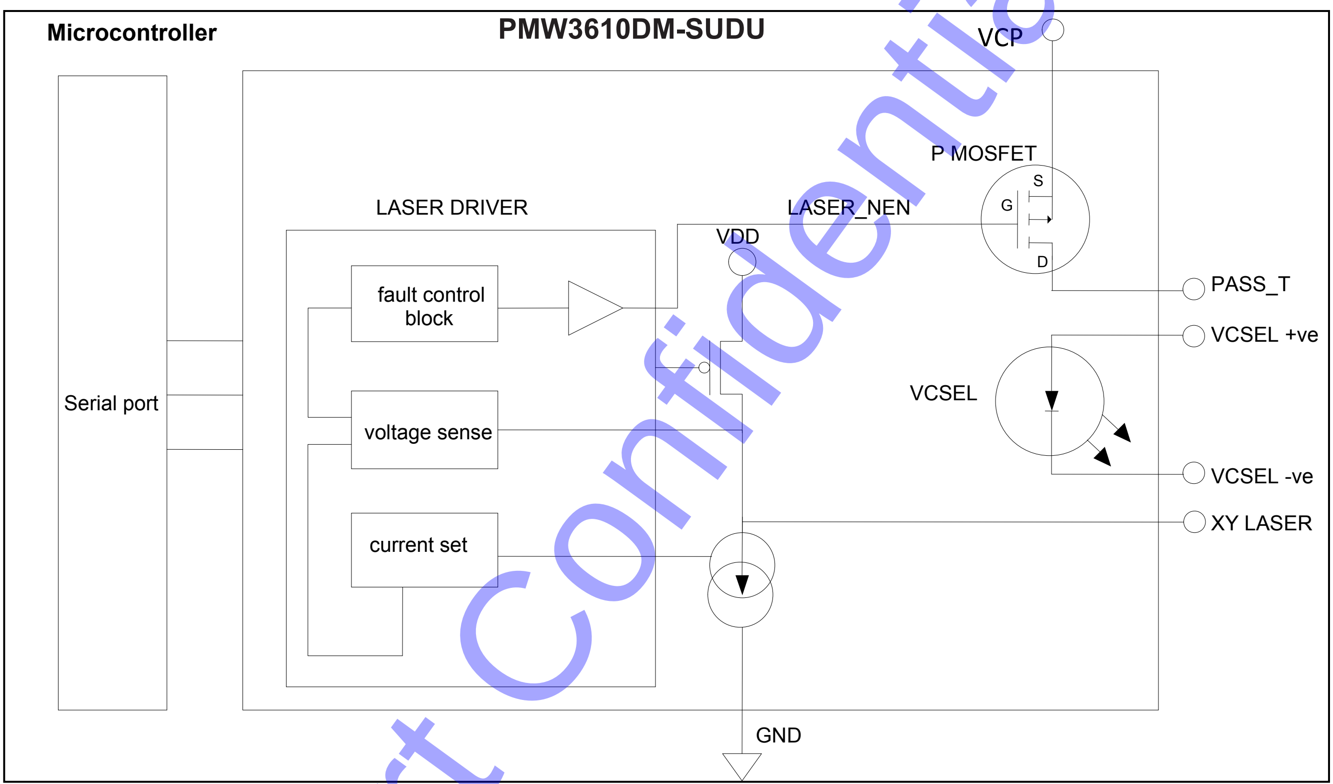


Figure 7. Single Fault Detection and Eye-safety Feature Block Diagram

Table 1. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-40	85	C	
Lead-Free Solder Temperature			260	C	For 7 seconds, 1.8mm below seating plane. Refer to wave soldering profile in PCB Assembly & Soldering Considerations Application Note AN-5023.
Power Supply Voltage	V_{DD}	-0.5	2.2	Volts	
	V_{DDIO}	-0.5	3.4	Volts	
ESD (Human Body Model)	ESD		2	kV	All Pins
Input Voltage	V_{IN}	-0.5	V_{DDIO} +0.5	Volts	All I/O Pins
Laser Output Power	LOP_{MAX}		716	µW	Class 1 Eye Safety AEL limit
VCSEL forward current	I_f		3.3	mA	

Notes:

1. ***Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are the stress ratings only and functional operation of the device at these or any other condition beyond those indicated for extended period of time may affect device reliability.***
2. ***The maximum ratings do not reflect eye-safe operation.***
3. ***The inherent design of this component causes it to be sensitive to electrostatic discharge. The ESD threshold is listed above. To prevent ESD induced damage, take adequate ESD precautions when handling this product***

Table 2. Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Operating Temperature	T_A	0		40	ºC	
Power supply voltage	V_{DD}	1.7	1.8	2.1	Volts	Including V_{NA} of $100mV_{pp}$
	V_{DDIO}	1.7	1.8	3.3		Including V_{NA} of $100mV_{pp}$
Power supply rise time	t_{RT}	1			ms	0 to VDD
Supply noise (Sinusoidal)	V_{NA}			100	mV_{p-p}	10kHz-50MHz
Serial Port Clock Frequency	f_{SCLK}			2	MHz	Active drive, 50% duty cycle
Distance from lens reference plane to surface	Z	2.2	2.4	2.6	mm	Results in +/- 0.2 mm minimum DOF.
Speed	S		24	30	in/ sec	30 ips with certain surface
Acceleration	A		10		g	
Load Capacitance	C_{out}			100	pF	SDIO and MOTION
Peak Wavelength	λ	832		865	nm	

AC Electrical Specifications

Table 3. Electrical Characteristics over recommended operating conditions. Typical values at 25 °C, VDD=1.8V

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Motion delay after reset	$t_{MOT-RST}$	3.5			ms	From SW_RESET register write to valid motion, assuming motion is present
Shutdown	t_{STDWN}			50	ms	From Shutdown mode active to low current
Wake from shutdown	t_{WAKEUP}	16	23		ms	From Shutdown mode inactive to valid motion. Notes: A RESET must be asserted after a shutdown. Refer to section "Notes on shutdown also not $t_{MOT-RST}$"
SDIO Output Rise Time	$t_{r\text{-}SDIO\ output}$		40	200	ns	C_L = 100 pF
SDIO Output Fall Time	$t_{f\text{-}SDIO\ output}$		40	200	ns	C_L = 100 pF
SDIO Output Delay after SCLK	$t_{DLY\text{-}SDIO\ output}$			120	ns	From SCLK falling edge to SDIO output data valid, no load conditions
SDIO output hold time	$t_{hold\text{-}SDIO\ output}$	250			ns	Data held until next falling SCLK edge
SDIO input hold time	$t_{hold\text{-}SDIO\ input}$	200			ns	Amount of time data is valid after SCLK rising edge
SDIO input setup time	$t_{setup\text{-}SDIO\ input}$	120			ns	From data valid to SCLK rising edge
SPI time between write command	t_{SWW}	30			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second data byte
SPI time between write and read commands	t_{SWR}	20			us	From rising SCLK for last bit of the 1st data byte, to rising SCLK for last bit of the second address byte
SPI time between read and subsequent commands	t_{SRW} t_{SRR}	250			ns	From rising SCLK for last bit of the 1st data byte , to falling SCLK for the 1st bit of data being read.
SPI read address-data delay	t_{SRAD}	4			us	From rising SCLK for last bit of the address byte, to falling SCLK for the 1st bit of data being read.
NCS inactive after motion burst	t_{BEXIT}	250			ns	Minimum NCS inactive time after motion burst before next SPI usage
NCS to SCLK active	$t_{NCS\text{-}SCLK}$	120			ns	From last NCS falling edge to 1st SCK rising edge.
SCLK to NCS inactive for SDIO write	$t_{SCLK\text{-}NCS\ write}$	10			us	From last SCLK falling edge to NCS rising edge, for valid SDIO data transfer
SCLK to NCS inactive for SDIO read	$t_{SCLK\text{-}NCS\ read}$	120			ns	From last SCLK falling edge to NCS rising edge, for valid SDIO data transfer
NCS to SDIO high-Z	$t_{NCS\text{-}SDIO}$			250	ns	From NCS rising edge to SDIO high-Z state
MOTION rise time	$t_{r\text{-}MOTION}$		40	200	ns	CL = 100pF
MOTION fall time	$t_{f\text{-}MOTION}$		40	200	ns	CL = 100pF
Transient Supply Current	IDDT			60	mA	Max supply current during a VDD ramp from 0 to 1.8

DC Electrical Specifications

Table 4. Electrical Characteristics over recommended operating conditions. Typical values at 25 °C, VDD= 1.8V.

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
DC supply Current in various modes	I_{DD_RUN}		0.60		mA	Average current, including LASER current. No load on SDIO
	I_{DD_Rest1}		36		uA	
	I_{DD_Rest2}		16		uA	
	I_{DD_Rest3}		7		uA	
Shutdown Supply Current			3		µA	
Input Low Voltage	V_{IL}			0.2*VDDIO	V	SCLK, SDIO
Input High Voltage	V_{IH}	0.8*VDDIO			V	SCLK, SDIO
Input Hysteresis	V_{I_HYS}		100		mV	SCLK, SDIO
Input Leakage Current	I_{leak}		±1	±10	µA	Vin = 0.7*VDDIO, SCLK, SDIO
Laser Current (fault mode)	I_{LAS_FAULT}			300	uA	XY_LASER $R_{leakage}$ < 75kOhms to Gnd
Output Low Voltage, SDIO, MOTION	V_{OL}			0.2*VDDIO	V	Iout= 1mA, SDIO, MOTION
Output Low Voltage, SDIO, MOTION	V_{OH}	0.8*VDDIO			V	Iout= -1mA, SDIO, MOTION
Input Capacitance	C_{in}			10	pF	SCLK, SDIO

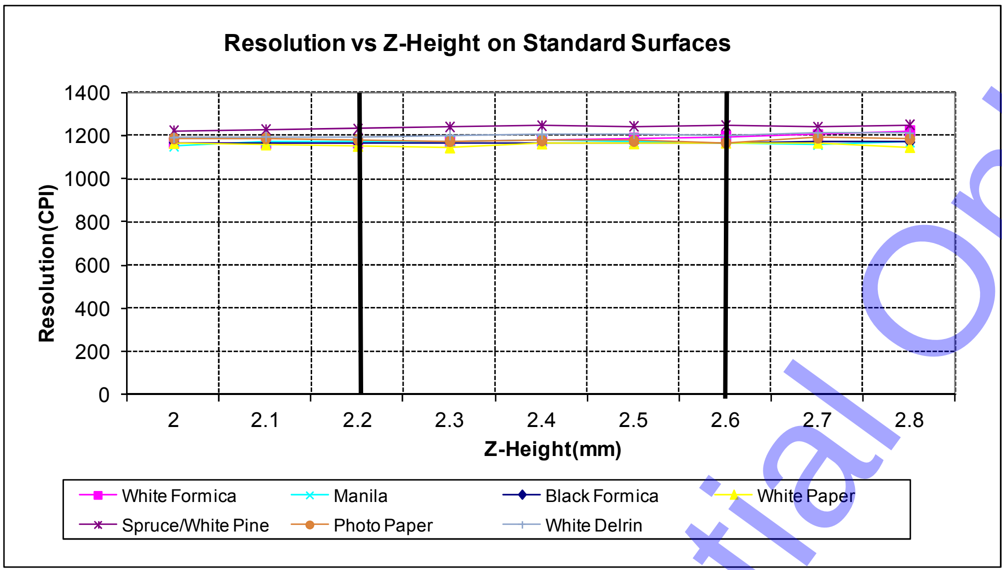


Figure 8. Mean Resolution vs. Z at default resolution at 1200cpi

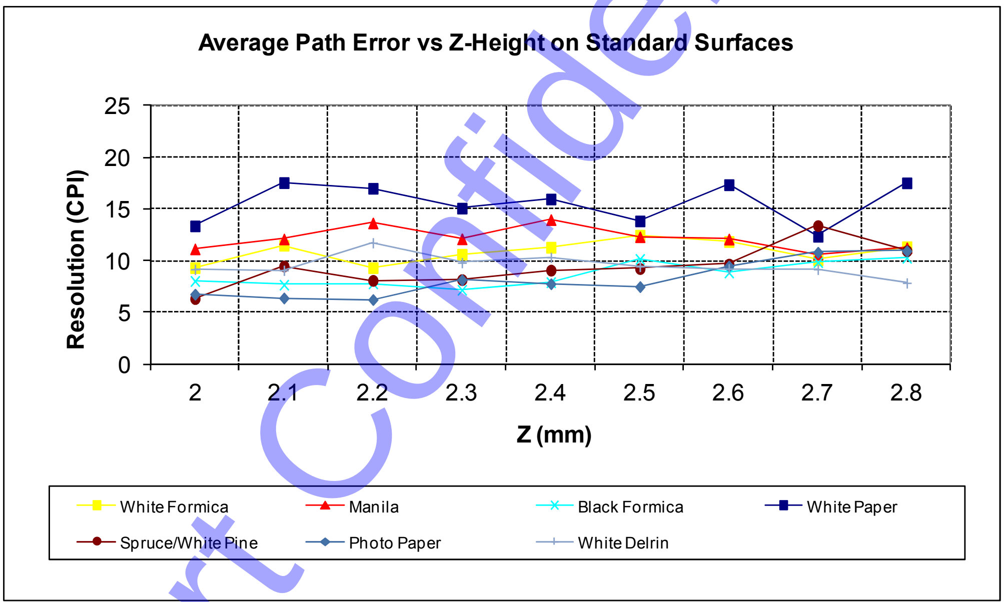


Figure 9. Average Error vs. Distance at 1200cpi (mm)

Motion Pin Timing

The motion pin is an active low output that signals the micro-controller when motion has occurred. The motion pin is lowered whenever the motion bit is set; in other words, the 12-bit motion data register are DELTA_X, DELTA_Y and DELTA_XY_HIGH.

Synchronous Serial Port

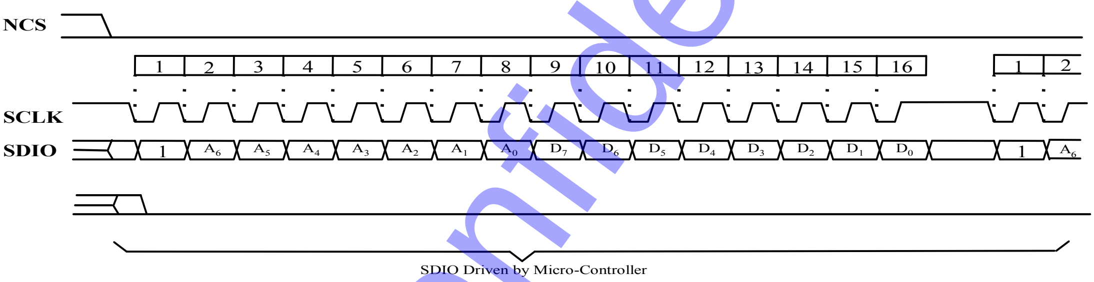
The synchronous serial port is used to set and read parameters in the PMW3610DM-SUDU, and to read out the motion information. The port is a three wire serial port. The host micro-controller always initiates communication; the PMW3610DM-SUDU never initiates data transfers. SCLK and SDIO may be driven directly by a micro-controller.

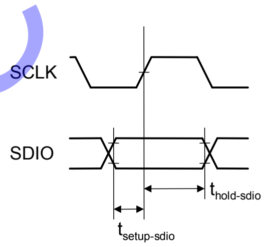
The lines that comprise the SPI port:

SCLK: Clock input. It is always generated by the master
(the micro-controller).
SDIO: Input/output data.
NCS: Chip Select

Write Operation

Write operation, defined as data going from the micro-controller to the PMW3610DM-SUDU, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate write sequence. The second byte contains the data. The PMW3610DM-SUDU reads SDIO on rising edges of SCLK. Before any write operation, write 0xBA to address 0x41 to turn on spi clock and wait for 300us. After write operation(s), write 0xB5 to address 0x41 to turn off spi clock for power saving purpose.

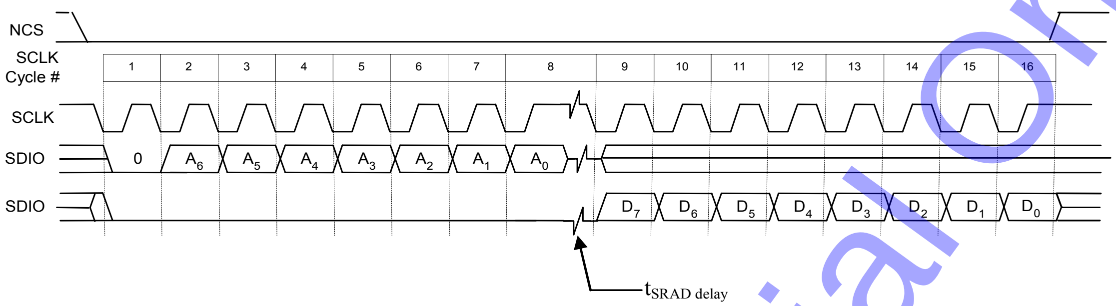


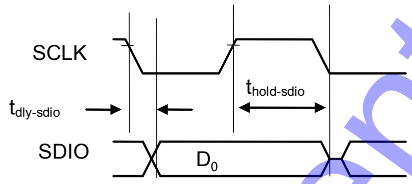


SDIO setup and hold time during write operation

Read Operation

A read operation, defined as data going from the PMW3610DM-SUDU to the microcontroller, is always initiated by the microcontroller and consists of two bytes. The first byte contains the address, is sent by the microcontroller over SDIO, and has a “0” as its MSB to indicate data direction. The sensor outputs SDIO bits on falling edges of SCLK and samples SDIO bits on every rising edge of SCLK. In the diagram below, two SDIO lines are illustrated for the sake for clarity, but there are actually one and the same in reality.





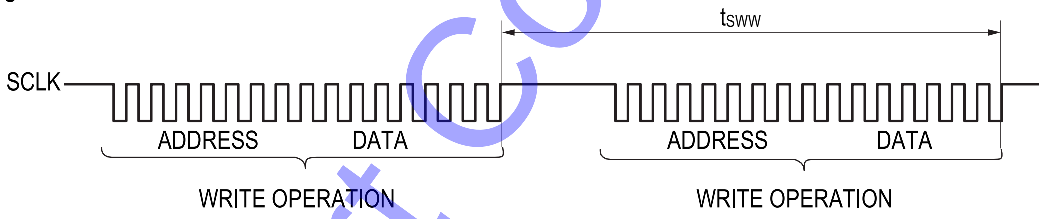
SDIO delay and hold time during read operation

NOTE: The 250 ns minimum high state of SCLK is also the minimum SDIO data hold time of the PMW3610DM-SUDU. Since the falling edge of SCLK is actually the start of the next read or write command, the PMW3610DM-SUDU will hold the state of data on SDIO until the falling edge of SCLK.

Required timing between Read and Write Commands (tsxx)
There are minimum timing requirements between read and write commands on the serial port.

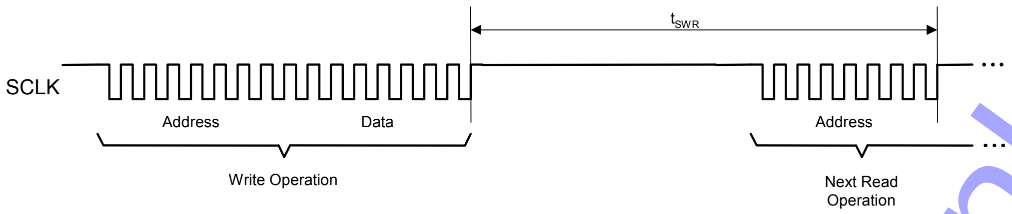
Required Timing between Read and Write Commands

Timing between Two Write Commands



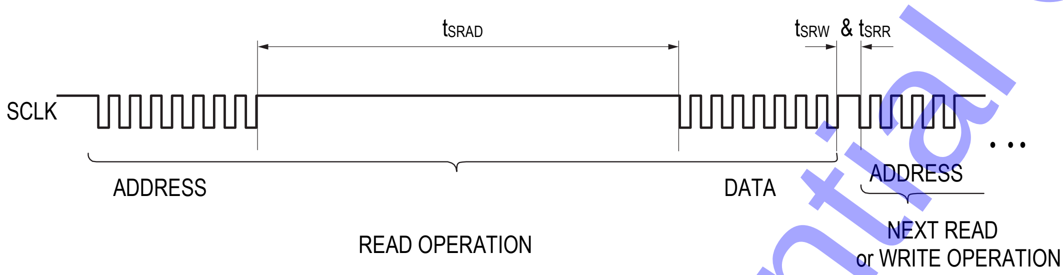
Timing between Two Write Commands

If the rising edge of the SCLK for the last data bit of the second write command occurs before the required delay (tSWW), then the first write command may not complete correctly.



Timing between Write and Read Commands

If the rising edge of SCLK for the last address bit of the read command occurs before the required delay (t_{SWR}), the write command may not complete correctly.



Timing between Read and Subsequent Write or Read Commands

The falling edge of SCLK for the first address bit of either the read or write command must be at least 250 ns after the last SCLK rising edge of the last data bit of the previous read operation. In addition, during a read operation SCLK should be delayed after the last address data bit to ensure that the sensor has time to prepare the requested data.

Burst Mode Operation

Burst mode is a special serial port operation mode which may be used to reduce the serial transaction time for a predefined registers. The speed improvement is achieved by continuous data clocking to or from multiple registers without the need to specify the register address

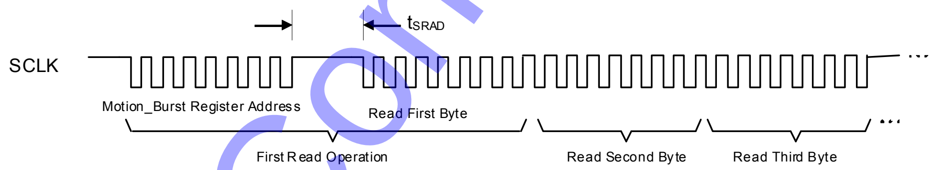


Figure 10. Motion Burst Timing

Motion Burst Read

This mode is activated by reading register BURST_READ (0x12). At this time, burst mode is activated and the first data is from address indicated in REGA_BURST_START_ADDRESS. By default, this register point to REGA_MOTION. So when default, the first data will be from REGA_MOTION, followed by DELTA_X_L, DELTA_Y_L, DELTA_XY_H, SQUAL, SHUT_HI, SHUT_LO, PIX_MAX, PIX_AVG, and PIX_MIN. Not all registers must be read.

Reporting format:-
BYTE [00] = Motion
BYTE [01] = Delta_X_L
BYTE [02] = Delta_Y_L
BYTE [03] = Delta_XY_H
BYTE [04] = Squal
BYTE [05] = Shutter_Hi
BYTE [06] = Shutter_Lo
BYTE [07] = Maximum_Pixel
BYTE [08] = Average_Pixel
BYTE [09] = Minimum_Pixel

Procedure to start motion burst as below.

1. Lower NCS
2. Read Motion_Burst register (address 0x12).
3. Wait for t_{SRAD}. (This only applicable in Run mode for wakeup but not require for rest mode)
4. Start reading SPI Data continuously up to 10 bytes.
   Motion burst may be terminated by pulling NCS high for at least t_{BEXIT}.
5. To read new motion burst data, repeating from step 1.
6. Write any value to Motion register (address 0x02) to clear any residual motion.

Burst must be terminated by the micro-controller by raising the NCS line for at least tBEXIT. The serial port is not available for use until it is reset with NCS, even for a second burst transmission.

Note: In rest mode, motion burst data is always available or in other words, motion burst data can be read from Motion_Burst register even in rest modes.

Frame Capture

This is a fast way to download a full array of pixel values from a single frame. Once frame grab is enabled, the next complete frame image will be stored to memory. To stream out the pixels values, burst read is used. Procedure to start frame capture burst mode as below:

1. Write 0xF1 to register PERFORMANCE (0x11) to disable rest mode.
2. Write 0xBA to register SPI_CLK_ON_REQ (register 0x41) and wait for 300us to enable spi clock.
3. Write 0x10 to register 0x32 to turn on the test clock.
4. Write 0x80 to FRAME_GRAB (register 0x36) to enable frame grab where the next single image will be stored in memory.
5. Wait for 10 ms.
6. Read from register BURST_READ (register 0x12) to get the first pixel.
7. Continue clocking out the pixel by driving SCLK at normal burst rate.

After the full image is read, the micro-controller must raise the NCS line for at least t_{BEXIT} to terminate burst mode. A full reset is required to resume navigation. Refer to the following diagram for timing details.

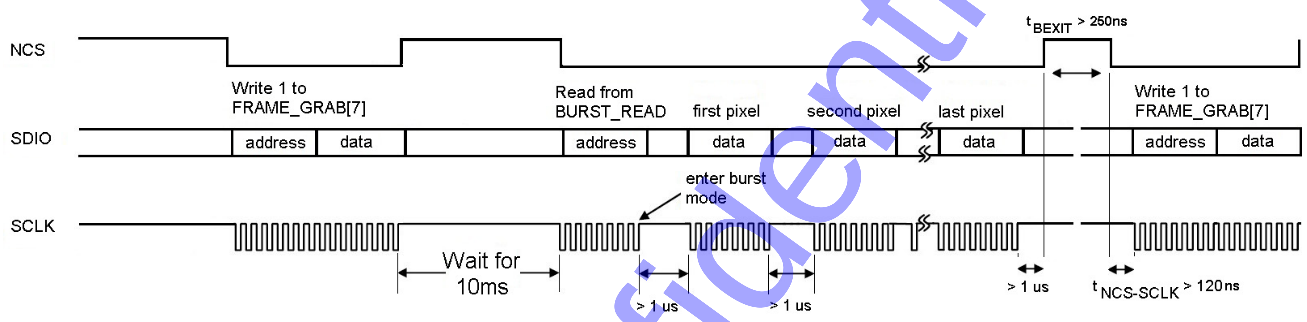


Figure 11. Frame Capture Burst Mode timing

Notes on Power-up

The PMW3610DM-SUDU performs an internal power up self-reset. The appropriate sequence is as follows:

I. Apply power to VDD and VDDIO in any order, with the delay of no more than 100us in between each supply. Ensure all supplies are stable.
II. Drive NCS high, and then low to reset the SPI port.
III. Wait for at least one frame (150us).
IV. Write register 0x2d with value 0x00 (clear observation1 register for sensor self test check).
V. Wait for 10ms, after that read register 0x2d again. Make sure all the bit $_{[3-0]}$ must be set to 1.
VI. Read from registers 0x02, 0x03, 0x04 and 0x05 one time regardless of the motion pin state.

VII. Write register 0x11 with value 0x0d, required setting to configure.
VIII. Write register 0x1b with value 0x04, required setting to configure.
IX. Write register 0x1c with value 0x04, required setting to configure.
X. Write register 0x1d with value 0x0f, required setting to configure.

During power-up there will be a period of time after the power supply is high but before any clocks are available.
The table below shows the state of the various pins during power-up and reset.

State of Signal Pins After VDD is Valid

Pin	After sensor ready
NCS	Functional
SCLK	Depends on NCS
SDIO	Depends on NCS
XYLASER	Functional
MOTION	Functional

Notes on Shutdown and Forced Rest

The PMW3610DM-SUDU can be set in Rest mode through the Performance register (0x11), and also can be set in Shutdown mode by writing register 0x3b with value 0xe7. This is to allow for further power savings in applications where the sensor does not need to operate all the time. The SPI port should not be accessed when Shutdown mode is asserted, except the power-up command (writing register 0x3a with value 0x96). (Other ICs on the same SPI bus can be accessed, as long as the sensor's NCS pin is not asserted.) The table below shows the state of various pins during shutdown.

To deassert Shutdown mode:-
Write register 0x3a with value 0x96 to wake up from shutdown which remains all register values that configured during power up.

State of Signal Pins when shutdown Mode

Pin	During Power Down
NCS	Functional *1
SCLK	Ignore if NCS = 1 *2
SDIO	Ignore if NCS = 1
XYLASER	High Z
MOTION	Undefined

Notes:

*1 NCS pin must be held to 1 (high) if SPI bus is shared with other devices. It is recommended to held to 1 (high) during Power Down unless powering up the Sensor. It should be held to 0 (low) if the sensor is to be re-powered up from shutdown (writing 0x96 to register 0x3a).

*2 SCLK and SDIO is ignore if NCS is 1 (high). It is functional if NCS is 0 (low).

Note: There are long wakeup times from shutdown and forced Rest. These features should not be used for power management during normal mouse motion.

Mouse level algorithm to enhance surface coverage

In order to further extend sensor tracking across a wider range of surfaces such as granites and tiles, a new algorithm is introduced. The new algorithm requires mouse MCU level implementation. The algorithm implementation should be placed right after the motion burst read as its operation is dependent on sensor shutter values.

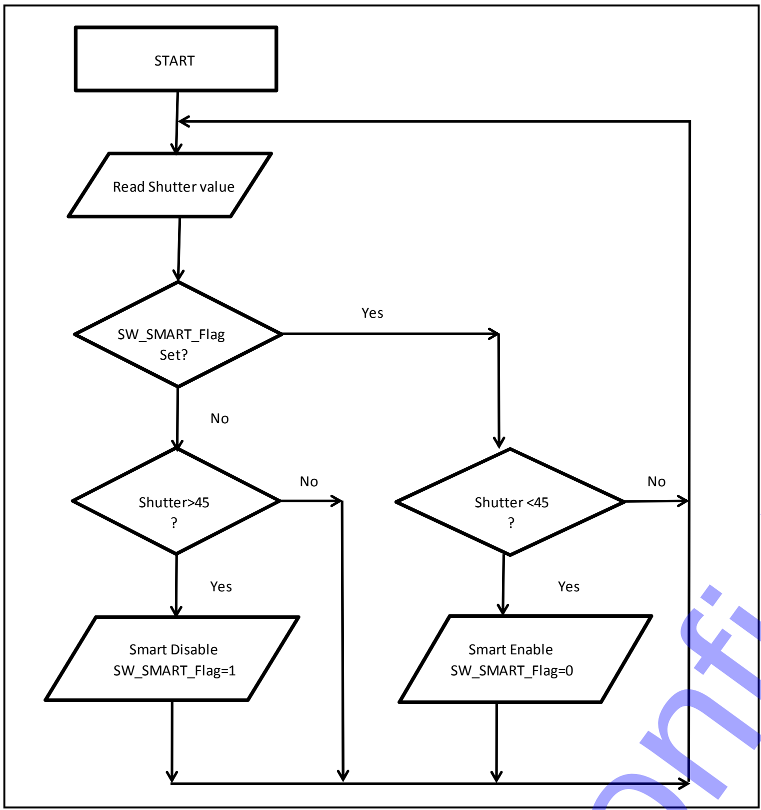


Figure 12. Algorithm flowchart

Example of pseudo code in C language:

```
if (Sw_SMART_En)
{
        if (SW_SMART_Flag && shutter6.b[0]==0 && shutter6.b[1]< 45)
        {
                write_sensor(0x41,0xba);
                write_sensor(0x32,0x00);        //Smart enable
                write_sensor(0x41,0xb5);
                SW_SMART_Flag = 0;
        }
        if (!SW_SMART_Flag && shutter6.b[0]==0 && shutter6.b[1]> 45)
        {
                write_sensor(0x41,0xba);
                write_sensor(0x32,0x80);        // Smart disable
                write_sensor(0x41,0xb5);
                SW_SMART_Flag = 1;
        }
}
```

Note:-

- Sw_SMART_En , this is a switch control to enable or disable the algorithm
- SW_SMART_Flag, this is either a boolean or unsigned integer declaration
- shutter6.b[0] is upper shutter high value and shutter6.b[1] is shutter low value
- write_sensor(register address, value to be written)

Registers

The PMW3610DM-SUDU registers are accessible via the serial port. The registers are used to read motion data and status as well as to set the device configuration.

Address	Register	Read/Write	Default Value
0x00	PROD_ID	R	0x3e
0x01	REV_ID	R	0x01
0x02	MOTION	R/W	0x09
0x03	DELTA_X_L	R	0x00
0x04	DELTA_Y_L	R	0x00
0x05	DELTA_XY_H	R	0x00
0x06	SQUAL	R	0x00
0x07	SHUTTER_HIGHER	R/W	0x00
0x08	SHUTTER_LOWER	R/W	0x22
0x09	PIX_MAX	R	0x60
0x0a	PIX_AVG	R	0x4f
0x0b	PIX_MIN	R	0x7f
0x0c	CRC0	R	0x00
0x0d	CRC1	R	0x00
0x0e	CRC2	R	0x00
0x0f	CRC3	R	0x00
0x10	SELF_TEST	W	0x00
0x11	PERFORMANCE	R/W	0x01
0x12	BURST_READ	R/W	0x0b
0x13 - 0x1a	RESERVED		
0x1b	RUN_DOWNSHIFT	R/W	0x04
0x1c	REST1_RATE	R/W	0x04
0x1d	REST1_ DOWNSHIFT	R/W	0x1f
0x1e	REST2_RATE	R/W	0x0a
0x1f	REST2_ DOWNSHIFT	R/W	0x2f
0x20	REST3_RATE	R/W	0x32
0x21 – 0x2c	RESERVED		
0x2d	OBSERVATION1	R/W	0x00
0x2e – 0x34	RESERVED		
0x35	PIXEL_GRAB	R/W	0x00
0x36	FRAME_GRAB	R/W	0x00
0x37 – 0x39	RESERVED		
0x3a	POWER_UP_RESET	W	NA
0x3b	SHUTDOWN	W	NA
0x3c – 0x3d	RESERVED		
0x3e	NOT_REV_ID	R	0xfe
0x3f	NOT_PROD_ID	R	0xc1
0x40	RESERVED		
0x41	SPI_CLK_ON_REQ	W	NA
0x42 – 0x46	RESERVED		
0x47	PRBS_TEST_CTL	RW	0x00
0x48 – 0x7e	RESERVED		
0x7f	SPI_PAGE0	RW	0x00
0x80-0x84	RESERVED		
0x85	RES_STEP	RW	0x06
0x86 – 0x9d	RESERVED		
0x9e	VCSEL_CTL	R/W	0x00
0x9f	LSR_CONTROL	R/W	0x00
0xa0 – 0xfe	RESERVED		
0xff	SPI_PAGE1	RW	0x00

PROD_ID **Address: 0x00**
Access: Read Reset Value: 0x3e

Bit	7	6	5	4	3	2	1	0
Field	PID_7	PID_6	PID_5	PID_4	PID_3	PID_2	PID_1	PID_0

Data Type : 8-Bit unsigned integer

USAGE : This register contains a unique identification assigned to the PMW3610DM-SUDU. The value in this register does not change; it can be used to verify that the serial communications link is functional.

REV_ID **Address: 0x01**
Access: Read Reset Value: 0x01

Bit	7	6	5	4	3	2	1	0
Field	RID_7	RID_6	RID_5	RID_4	RID_3	RID_2	RID_1	RID_0

Data Type : 8-Bit unsigned integer

USAGE : This register contains the IC revision. It is subject to change when new IC versions are released.

MOTION **Address: 0x02**
Access: Read/Write Reset Value: 0x09

Bit	7	6	5	4	3	2	1	0
Field	MOT	Reserved	Reserved	OVF	LP_VALID	LSR_FAULT	Reserved	RST_FLAG

Data Type : Bit field.

USAGE : Register 0x02 allows the user to determine if motion has occurred since the last time it was read. If the MOT bit is set, then the user can read registers 0x03, 0x04 and 0x05 to get the accumulated motion.

Writing anything to this register clears the MOT and OVF bits, Delta_X_L, Delta_Y_L and Delta_XY_H registers. The written data byte is not saved.

If one of the 12 bits motion registers overflows, then absolute path data is lost and the OVF bit is set. Once OVF bit set, Sensor will stop accumulating motion data. Motion registers and OVF bit will be clear after data been read out.

Field Name	Description
MOT	Motion since last report **0 = No motion** 1 = Motion occurred, data ready for reading in Delta_X_L, Delta_Y_L and Delta_XY_H registers
OVF	Motion overflow, ΔY and/or ΔX buffer has overflowed since last report **0 = no overflow** 1 = Overflow has occurred
LP_VALID	Laser Power Settings **0 = laser power invalid** 1 = laser power is valid
LSR_FAULT	Indicates that –VCSEL is shorted to GND or VDD **0 = no fault detected** 1 = fault detected.
RST_FLAG	Indicates that power up reset has been triggered 0 = reset not been triggered **1 = reset has been triggered**

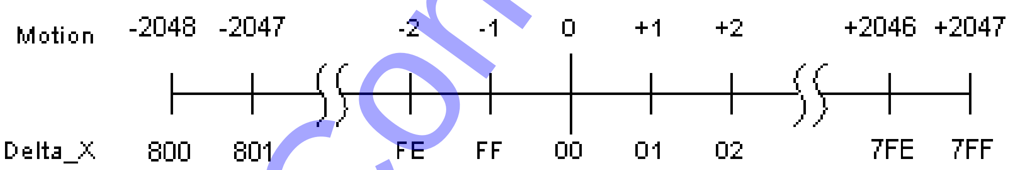
NOTE: Pixart recommends that registers 0x02, 0x03, 0x04and 0x05 be read sequentially.

DELTA_X_L Address: 0x03
Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0

Data Type : Eight bit 2's complement number.

USAGE : X movement is counts since last report. Absolute value is determined by resolution. Reading clears the register.



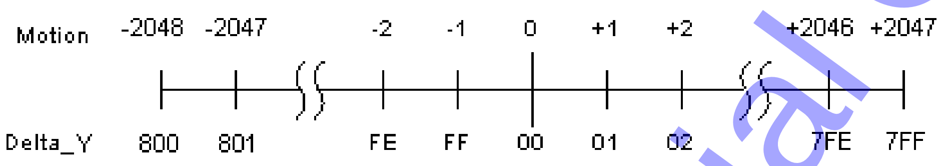
NOTE: Pixart recommends that registers 0x02, 0x03, 0x04 and 0x05 be read sequentially.

DELTA_Y_L **Address: 0x04**
Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0

Data Type : Eight bit 2's complement number.

USAGE : Y movement is counts since last report. Absolute value is determined by resolution. Reading clears the register.



NOTE: Pixart recommends that registers 0x02, 0x03, 0x04 and 0x05 be read sequentially.

DELTA_XY_H **Address: 0x05**
Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	X_{11}	X_{10}	X_9	X_8	Y_{11}	Y_{10}	Y_9	Y_8

Data Type : 2's complement number, upper 4 bits of Delta_X and Delta_Y.

USAGE : Delta_XY_H must be read after Delta_X_L and Delta_Y_L to have the full motion data. Reading clears the register.

NOTE: Pixart recommends that registers 0x02, 0x03, 0x04 and 0x05 be read sequentially.

SQUAL **Address: 0x06**
Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	SQ_7	SQ_6	SQ_5	SQ_4	SQ_3	SQ_2	SQ_1	SQ_0

Data Type : Upper 8 bits of a 9-bit unsigned integer.

USAGE : SQUAL (Surface Quality) is a measure of the number of valid features visible by the sensor in the current frame.

SQUAL (Surface Quality) is a measure of the number of valid features visible by the sensor in the current frame. The maximum SQUAL register value is 361. Since small changes in the current frame can result in changes in SQUAL, variations in SQUAL when looking at a surface are expected. The graph below shows 800 sequentially acquired SQUAL values, while a sensor was moved slowly over white paper. SQUAL is nearly equal to zero, if there is no surface below the sensor. SQUAL is typically maximized when the navigation surface is at the optimum distance from the imaging lens (the nominal Z-height).

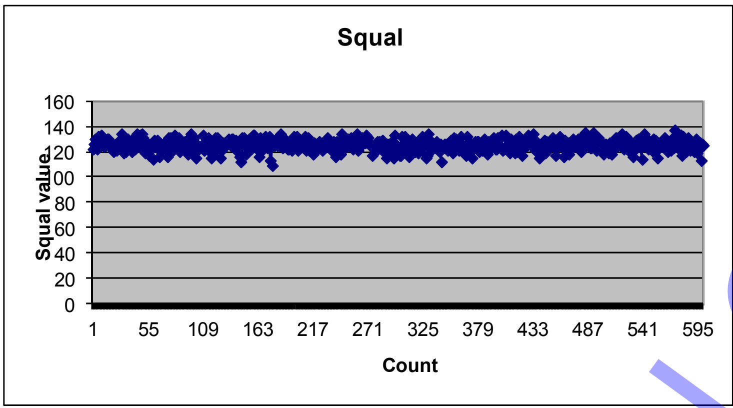


Figure 13. SQUAL Values at 1200cpi (White Paper)

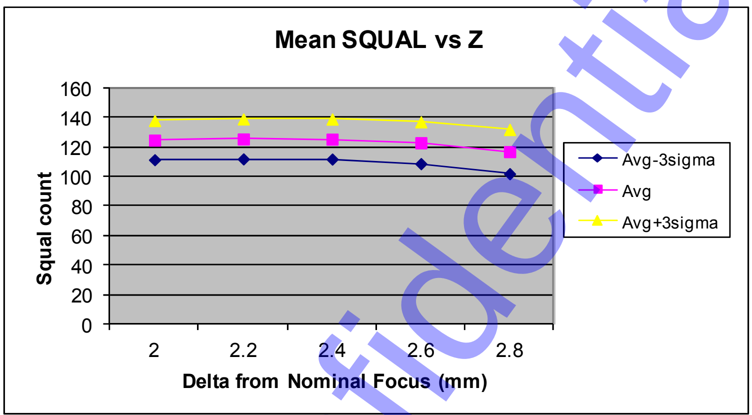


Figure 14. Mean SQUAL vs. Z (White Paper)

SHUTTER_HIGHER | **Address: 0x07**

Access: Read | Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	S_8

Data Type : Eight-bit number.

USAGE : Units are clock cycles. The shutter is adjusted to keep the average and maximum pixel values within normal operating ranges. The shutter value is automatically adjusted.

Field Name	Description
S_8	Shutter open time, higher 1-bit

SHUTTER_LOWER Access: Read

Address: 0x08 Reset Value: 0x22

Bit	7	6	5	4	3	2	1	0
Field	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

Data Type : Eight-bit number.

USAGE : Units are clock cycles. The shutter is adjusted to keep the average and maximum pixel values within normal operating ranges. The shutter value is automatically adjusted.

Field Name	Description
S_{7-0}	Shutter open time, lower-8bit

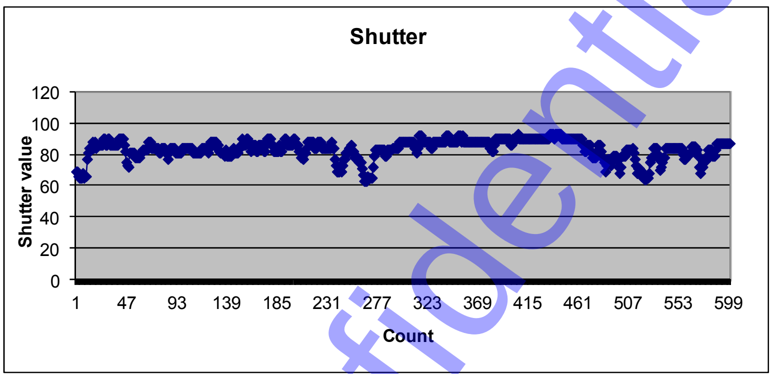


Figure 15. Shutter Values at 1200cpi (White Paper)

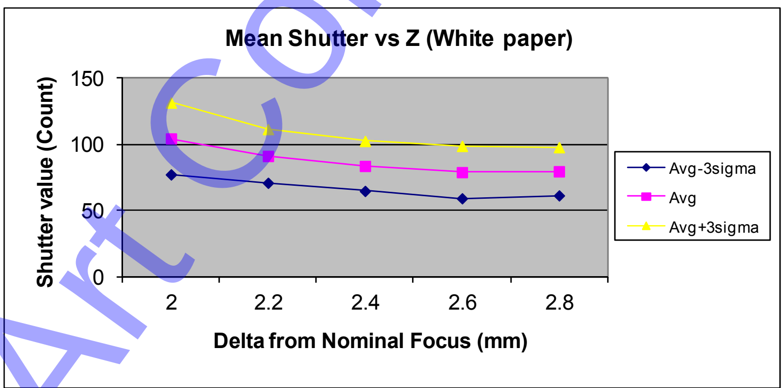


Figure 16. Mean Shutter vs. Z (White Paper)

PIX_MAX **Address: 0x09**
Access: Read Reset Value: 0x60

Bit	7	6	5	4	3	2	1	0
Field	$PMAX_7$	$PMAX_6$	$PMAX_5$	$PMAX_4$	$PMAX_3$	$PMAX_2$	$PMAX_1$	$PMAX_0$

Data Type : Eight-bit number.

USAGE : Maximum Pixel value in current frame. Minimum value = 0, maximum value = 254. The maximum pixel value can vary with every frame.

PIX_AVG **Address: 0x0a**
Access: Read Reset Value: 0x4f

Bit	7	6	5	4	3	2	1	0
Field	PA_7	PA_6	PA_5	PA_4	PA_3	PA_2	PA_1	PA_0

Data Type : High 8 bits of an unsigned 18-bit integer.

USAGE : This register is used to find the average pixel value. It reports the upper eight bits of a 18-bit counter, which sums all pixels in the current frame. It may be described as the full sum divided by 1024. To find the average pixel value, use the following formula:

Average Pixel = Register Value * 1024/676 = Register Value * 1.515

The maximum register value is 167. The minimum is 0. The pixel sum value can change on every frame.

PIX_MIN **Address: 0x0b**
Access: Read Reset Value: 0x7f

Bit	7	6	5	4	3	2	1	0
Field	$PMIN_7$	$PMIN_6$	$PMIN_5$	$PMIN_4$	$PMIN_3$	$PMIN_2$	$PMIN_1$	$PMIN_0$

Data Type : Eight-bit number.

USAGE : Minimum Pixel value in current frame. Minimum value = 0, maximum value = 254. The minimum pixel value can vary with every frame.

CRC0 **Address: 0x0c**
Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	$CRC0_7$	$CRC0_6$	$CRC0_5$	$CRC0_4$	$CRC0_3$	$CRC0_2$	$CRC0_1$	$CRC0_0$

Data Type : Eight-bit number

USAGE : Register 0x0c reports the first byte of the system self test results. Value = 0x73.

CRC1 **Address: 0x0d**
Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	$CRC1_7$	$CRC1_6$	$CRC1_5$	$CRC1_4$	$CRC1_3$	$CRC1_2$	$CRC1_1$	$CRC1_0$

Data Type : Eight bit number

USAGE : Register 0x0d reports the second byte of the system self test results. Value = 0xc4.

CRC2 **Address: 0x0e**
Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	$CRC2_7$	$CRC2_6$	$CRC2_5$	$CRC2_4$	$CRC2_3$	$CRC2_2$	$CRC2_1$	$CRC2_0$

Data Type : Eight-bit number

USAGE : Register 0x0e reports the third byte of the system self test results. Value = 0xc1.

CRC3 **Address: 0x0f**
Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	$CRC3_7$	$CRC3_6$	$CRC3_5$	$CRC3_4$	$CRC3_3$	$CRC3_2$	$CRC3_1$	$CRC3_0$

Data Type : Eight-bit number

USAGE : Register 0x0f reports the fourth byte of the system self test results. Value =0xea.

SELF_TEST Access: Write

Address: 0x10 Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	TESTEN

Data Type : Bit field

USAGE : Self test is allow user to do a self verification check to ensure all major components in the sensor is workings normally.
Procedure for self test:-

1) Write value 0x5a to register 0x3a for a reset
2) Write value 0xba to register SPI_CLK_ON_REQ (register 0x41)
3) Wait for 300us
4) Write value 0x10 to register 0x32
5) Write value 0x01 to Self_Test (register 0x10)
6) Wait for 64 frames
7) Read $CRC_{0\text{-}3}$ registers.
   Expected results after self test procedure completed,
   CRC0 = 0x73
   CRC1 = 0xc4
   CRC2 = 0xc1
   CRC3 = 0xea

   After self-test, reset the chip again to start normal operation.

Field Name	Description
TESTEN	Enable System Self Test 0= Disabled 1= Enable

PERFORMANCE **Address: 0x11**
Access: Read/Write Reset Value: 0x01

Bit	7	6	5	4	3	2	1	0
Field	$FMODE_3$	$FMODE_2$	$FMODE_1$	$FMODE_0$	VEL_RUN RATE	POSHI_RUN_ RATE	POSLO_RUN_R ATE_1	POSLO_RUN_ $RATE_0$

Data Type : Bit field

USAGE : Register 0x11 provide configuration to change sensor navigation performance

Field Name	Description
$FMODE_{3-0}$	force modes **0x0: Normal operation**. 0x1: force mode rest 1. 0x2: force mode rest 2. 0x3: force mode rest 3. 0x4: force mode POS Only 0x5: force mode POS Low Only 0x6: force mode POS Hi Only 0x7: Reserved 0x8: force mode VEL Only 0x9: force mode VEL A3L 0xa: force mode VEL A3S 0xb: Reserved ... 0xe: Reserved 0xf: Force awake
VEL_RUNRATE	0x0: **8ms** 0x1: 4ms
POSHI_RUN_RATE	0x0: **8ms** 0x1: 4ms
$POSLO\_RUN\_RATE_{1-0}$	0x0: 8ms 0x1: **4ms** 0x2: 2ms 0x3: Reserved

BURST_READ **Address: 0x12**
Access: Read/Write Reset Value: 0x0b

Bit	7	6	5	4	3	2	1	0
Field	Reserved	$BURST_6$	$BURST_5$	$BURST_4$	$BURST_3$	$BURST_2$	$BURST_1$	$BURST_0$

Data Type : Bit field

USAGE : this register provide feature for burst read setting.

Field Name	Description
$BURST_{6-0}$	Burst data

RESERVED **Address: 0x13 - 0x1a**

RUN_DOWNSHIFT **Address: 0x1b**
Access: Read/Write Reset Value: 0x04

Bit	7	6	5	4	3	2	1	0
Field	RD_7	RD_6	RD_5	RD_4	RD_3	RD_2	RD_1	RD_0

Data Type : Bit field

USAGE : Run to Rest1 time, units are pos mode rate * 8.

REST1_RATE **Address: 0x1c**
Access: Read/Write Reset Value: 0x04

Bit	7	6	5	4	3	2	1	0
Field	$R1R_7$	$R1R_6$	$R1R_5$	$R1R_4$	$R1R_3$	$R1R_2$	$R1R_1$	$R1R_0$

Data Type : Bit field

USAGE : Units are 10ms step.

REST1_DOWNSHIFT **Address: 0x1d**
Access: Read/Write Reset Value: 0x1f

Bit	7	6	5	4	3	2	1	0
Field	$R1D_7$	$R1D_6$	$R1D_5$	$R1D_4$	$R1D_3$	$R1D_2$	$R1D_1$	$R1D_0$

Data Type : Bit field

USAGE : Units are rest1 *16.

REST2_RATE **Address: 0x1e**
Access: Read / Write Reset Value: 0x0a

Bit	7	6	5	4	3	2	1	0
Field	$R2R_7$	$R2R_6$	$R2R_5$	$R2R_4$	$R2R_3$	$R2R_2$	$R2R_1$	$R2R_0$

Data Type : Bit field

USAGE : Units are 10ms step.

REST2_DOWNSHIFT **Address: 0x1f**
Access: Read / Write Reset Value: 0x2f

Bit	7	6	5	4	3	2	1	0
Field	$R2D_7$	$R2D_6$	$R2D_5$	$R2D_4$	$R2D_3$	$R2D_2$	$R2D_1$	$R2D_0$

Data Type : Bit field

USAGE : Units are rest2 * 128.

REST3_RATE **Address: 0x20**
Access: Read / Write Reset Value: 0x32

Bit	7	6	5	4	3	2	1	0
Field	$R3R_7$	$R3R_6$	$R3R_5$	$R3R_4$	$R3R_3$	$R3R_2$	$R3R_1$	$R3R_0$

Data Type : Bit field

USAGE : Units are 10ms step.

RESERVED **Address: 0x21- 0x2c**

OBSERVATION1 **Address: 0x2d**
Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	$MODE_1$	$MODE_0$	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Data Type : Bit field
USAGE : Register 0x2d provides bits that are set every frame. It can be used during EFT/B testing to check that the chip is running correctly, also to verify sensor operating state. Writing anything to this register will clear the bits. Wait for at least one frame before reading the register.

Field Name	Description
$MODE_{1-0}$	Observe that chip is working any write will clear bits [5:0] present mouse state **00 = Run** 01 = Rest 1 10 = Rest 2 11 = Rest 3

RESERVED **Address: 0x2e- 0x34**

PIXEL_GRAB **Address: 0x35**
Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	PG_Valid	PG_6	PG_5	PG_4	PG_3	PG_2	PG_1	PG_0

Data Type : Eight-bit word.

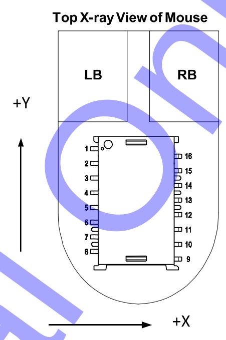
USAGE : Procedure to use Pixel_Grab function for complete pixel image.

1) Write register 0x41 with value 0xba
2) Write register 0x7f with value 0xff
3) Write register 0xb4 with value 0xd7
4) Write register 0x7f with value 0x00
5) Write register 0x41 with value 0xb5
6) Write register 0x32 with value 0x90
7) Write register 0x35 with value 0x01
8) Read register 0x47, make sure bit[1] is set else wait for 10ms and verify again
9) Read register 0x2d, make sure bit[2] is set else wait for 10ms and verify again
10) Read register 0x35
11) Write register 0x2d with value 0x01
    - Repeat step 9-11 for full frame, means 484 times in total
12) Read register 0x47, make sure bit[0] is set which indicate all 484 has been read successfully

Field Name	Description
PG_Valid	Pix grabber data valid
PD_{6-0}	Pixel grab data

First Pixel

462	440	418	396	374	352	330	308	286	264	242	220	198	176	154	132	110	88	66	44	22	0
463	441	419	397	375	353	331	309	287	265	243	221	199	177	155	133	111	89	67	45	23	1
464	442	420	398	376	354	332	310	288	266	244	222	200	178	156	134	112	90	68	46	24	2
465	443	421	399	377	355	333	311	289	267	245	223	201	179	157	135	113	91	69	47	25	3
466	444	422	400	378	356	334	312	290	268	246	224	202	180	158	136	114	92	70	48	26	4
467	445	423	401	379	357	335	313	291	269	247	225	203	181	159	137	115	93	71	49	27	5
468	446	424	402	380	358	336	314	292	270	248	226	204	182	160	138	116	94	72	50	28	6
469	447	425	403	381	359	337	315	293	271	249	227	205	183	161	139	117	95	73	51	29	7
470	448	426	404	382	360	338	316	294	272	250	228	206	184	162	140	118	96	74	52	30	8
471	449	427	405	383	361	339	317	295	273	251	229	207	185	163	141	119	97	75	53	31	9
472	450	428	406	384	362	340	318	296	274	252	230	208	186	164	142	120	98	76	54	32	10
473	451	429	407	385	363	341	319	297	275	253	231	209	187	165	143	121	99	77	55	33	11
474	452	430	408	386	364	342	320	298	276	254	232	210	188	166	144	122	100	78	56	34	12
475	453	431	409	387	365	343	321	299	277	255	233	211	189	167	145	123	101	79	57	35	13
476	454	432	410	388	366	344	322	300	278	256	234	212	190	168	146	124	102	80	58	36	14
477	455	433	411	389	367	345	323	301	279	257	235	213	191	169	147	125	103	81	59	37	15
478	456	434	412	390	368	346	324	302	280	258	236	214	192	170	148	126	104	82	60	38	16
479	457	435	413	391	369	347	325	303	281	259	237	215	193	171	149	127	105	83	61	39	17
480	458	436	414	392	370	348	326	304	282	260	238	216	194	172	150	128	106	84	62	40	18
481	459	437	415	393	371	349	327	305	283	261	239	217	195	173	151	129	107	85	63	41	19
482	460	438	416	394	372	350	328	306	284	262	240	218	196	174	152	130	108	86	64	42	20
483	461	439	417	395	373	351	329	307	285	263	241	219	197	175	153	131	109	87	65	43	21



Last Pixel

Figure 17. Pixel Address Map for 22x22 (sensor looking on the navigation surface through the lens)

FRAME_GRAB — **Address: 0x36**

Access: Read/Write — Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	FG_EN	FG_6	FG_5	FG_4	FG_3	FG_2	FG_1	FG_0

Data Type : 8-bit integer

USAGE : Write bit[7] to enable FRAME_GRAB register, and read this register again for the pixel burst data. Please refer to frame capture for more detail.

Field Name	Description
FG_EN	Note: not readable bit. 0 = frame grab disabled 1 = frame grab enable
FG_{6-0}	Pixel burst register

RESERVED — **Address: 0x37- 0x39**

POWER_UP_RESET — **Address: 0x3a**

Access: Write — Reset Value: NA

Bit	7	6	5	4	3	2	1	0
Field	RST_7	RST_6	RST_5	RST_4	RST_3	RST_2	RST_1	RST_0

Data Type : 8-bit integer

USAGE : Write 0x5a to this register to reset the chip. All settings will revert to default values. Write 0x96 to wake up from shutdown mode which will remain all registers values that configured upon power up sequence.

SHUTDOWN **Address: 0x3b**
Access: Write Reset Value: NA

Bit	7	6	5	4	3	2	1	0
Field	SD_7	SD_6	SD_5	SD_4	SD_3	SD_2	SD_1	SD_0

Data Type : 8-bit integer

USAGE : Write 0xe7 to set the chip to shutdown mode.

RESERVED **Address: 0x3c- 0x3d**

NOT_REV_ID **Address: 0x3e**
Access: Read Reset Value: 0xfe

Bit	7	6	5	4	3	2	1	0
Field	$NRID_7$	$NRID_6$	$NRID_5$	$NRID_4$	$NRID_3$	$NRID_2$	$NRID_1$	$NRID_0$

Data Type : Inverse 8-Bit unsigned integer

USAGE : This value is the inverse of the Revision_ID. It can be used to test the SPI port.

NOT_PROD_ID **Address: 0x3f**
Access: Read Reset Value: 0xc1

Bit	7	6	5	4	3	2	1	0
Field	$NPID_7$	$NPID_6$	$NPID_5$	$NPID_4$	$NPID_3$	$NPID_2$	$NPID_1$	$NPID_0$

Data Type : Inverse 8-Bit unsigned integer

USAGE : This value is the inverse of the Product_ID. It can be used to test the SPI port.

RESERVED **Address: 0x40**

SPI_CLK_ON_REQ **Address: 0x41**

Access: Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	$SCLK_7$	$SCLK_6$	$SCLK_5$	$SCLK_4$	$SCLK_3$	$SCLK_2$	$SCLK_1$	$SCLK_0$

Data Type : Bit field

USAGE : This register configures the SPI clock enable or disable for power saving purpose.

Field Name	Description
$SCLK_{7-0}$	Write 0xba to enable spi clock Write 0xb5 to disable spi clock

RESERVED **Address: 0x42- 0x46**

PRBS_TEST_CTL **Address: 0x47**

Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PIX_GRAB_FIRST	PIXEL_GRAB_DONE

Data Type : Bit field

USAGE : This register configures sensor test features

Field Name	Description
PIX_GRAB_FIRST	First pixel
PIXEL_GRAB_DONE	Pixel grab complete

RESERVED **Address: 0x48 – 0x7e**

SPI_PAGE0 **Address: 0x7f**
Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	$SP0_7$	$SP0_6$	$SP0_5$	$SP0_4$	$SP0_3$	$SP0_2$	$SP0_1$	$SP0_0$

Data Type : Bit field

USAGE : This register configures the SPI page selector, this can only be accessed when register pointer in page 0, address below 0x7f

Field Name	Description
$SPI0_{7\text{-}0}$	writing 0xFF to this register will switch to spi page 1 (spi addr above 0x7f)

RESERVED **Address: 0x80- 0x84**

RES_STEP **Address: 0x85**
Access: Read/Write Reset Value: 0x06

Bit	7	6	5	4	3	2	1	0
Field	SWAPXY	INV_X	INV_Y	RES_4	RES_3	RES_2	RES_1	RES_0

Data Type : Bit field

USAGE : This register configures reporting orientation direction and resolution setting.

w 41 ba -> Write register 0x41 with 0xba to enable spi clock
w 7f ff -> Write register 0x7f with value 0xff, page 1 switch

w 85 XX

w 7f 00 -> Write register 0x7f with 0x00, page 0 switch
w 41 b5 -> Write register 0x41 with value 0xb5 disable spi clock

Field Name	Description
SWAPXY	**0x0 : No swap** 0x1 : Swap between x and y
INV_X	**0x0 : not inverted** 0x1 : inverted X
INV_Y	**0x0 : not inverted** 0x1 : inverted Y

RES 4-0	resolution factor with step size 200cpi 0x1: 200cpi 0x2: 400cpi 0x3: 600cpi 0x4: 800cpi 0x5: 1000cpi **0x6: 1200cpi (default)** ... 0xf: 3000cpi 0x10: 3200cpi

RESERVED **Address: 0x86- 0x9d**

VCSEL_CTL **Address: 0x9e**
Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	COMPL_RBIN_SEL	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Data Type : Bit field

USAGE : This register configure the VCSEL options

Field Name	**Description**
COMPL_RBIN_SEL	-

LSR_CONTROL **Address: 0x9f**
Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	R_BIN_SEL_REG	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LASER_DISABLE

Data Type : Bit field

USAGE : This register configures the VCSEL options.

Field Name	**Description**
R_BIN_SEL_REG	
LASER_DISABLE	Laser force disabled 0: LASER_NEN normal 1: LASER_NEN force disabled

RESERVED **Address: 0xa0- 0xfe**

SPI_PAGE1 **Address: 0xff**
Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	$SP1_7$	$SP1_6$	$SP1_5$	$SP1_4$	$SP1_3$	$SP1_2$	$SP1_1$	$SP1_0$

Data Type : Bit field

USAGE : This register configures the SPI page selector, this can only be accessed when register pointer in page 1, address above 0x80

Field Name	Description
$SPI1_{7-0}$	writing 0x00 to this register will switch to spi page 0 (spi addr below 0x80)