PMW3901MB-TXQT: Optical Motion Tracking Chip

Product Datasheet

General Description

The PMW3901MB-TXQT is PixArt Imaging's latest optical navigation chip designed with far field optics technology that enables navigation in the air. It is housed in a 28-pin land-grid-array (LGA) package that provides X-Y motion information with a wide working range of 80 mm to infinity. It is most suitable for far field application for motion detection.

Key Features

- Wide working range from 80 mm to infinity
- No lens focusing required during lens mounting process
- Power consumption of 6 mA typical @ run mode
- 16-bits motion data registers
- Motion detect pin output
- Internal oscillator – no clock input needed

Applications

- Devices that require far field motion detection, e.g Drone
- Indoor and outdoor X-Y positioning especially in GPS denied environment

Key Parameters

Parameter	Value
Supply Voltage (V)	V_{DD}: 1.8 – 2.1 V_{DDIO}: 1.8 – 3.6
Working Range (mm)	80 to infinity
Frame Rate (fps)	121
Interface	4-Wire SPI @ 2 MHz
Package Type	28-pin LGA Package with L214-ZSZ Lens Assembly: 6 x 6 x 3.08 mm

Ordering Information

Part Number	Package Type
PMW3901MB-TXQT	28-pin LGA Package
L214-ZSZ	Lens Assembly

RoHS compliant

For any additional inquiries, please contact us at http://www.pixart.com/contact.asp

1.0 Signal Description

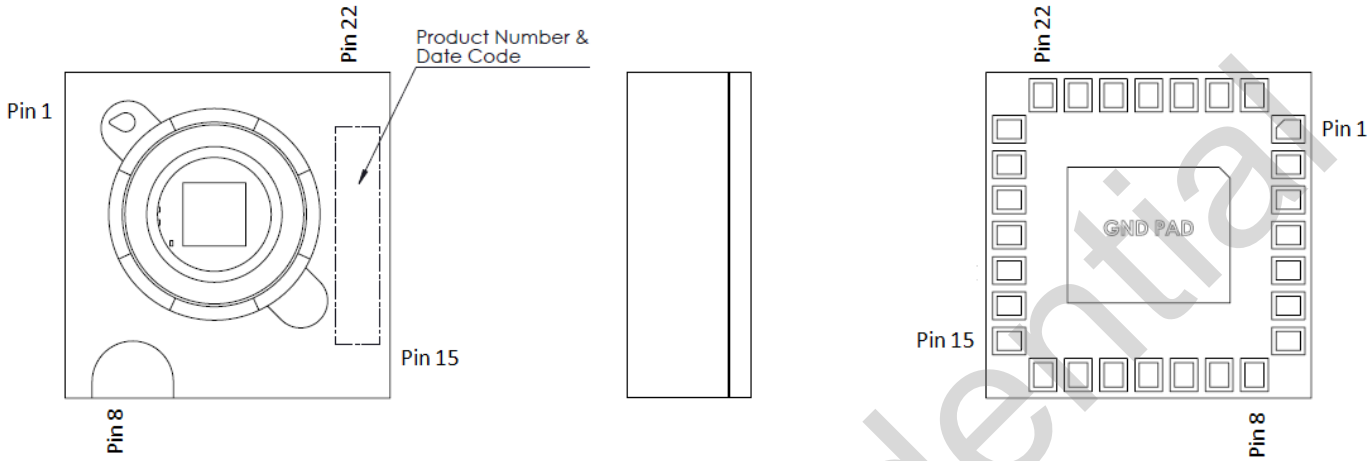


Figure 1. Pin Configuration

Table 1. Signal Pins Description

Pin No.	Signal Name	Type	Description
Functional Group:		Power Supplies	
2	VDD	Power	Input power supply
3	VDDIO	Power	I/O reference voltage
4	VREG	Power	Internal voltage output
1	GND	Ground	Ground
21	GND	Ground	Ground
Functional Group:		Control Interface	
16	MOSI	Input	Serial data input
17	SCLK	Input	Serial data clock
18	MISO	Output	Serial data output
19	NCS	Input	Chip select
Functional Group:		Functional I/O	
7	NRESET	Input	Hardware reset (Active low)
15	MOTION	Output	Motion interrupt (Active low)
20	LED_N	Input	External LED control pin (Active low) (Refer **Appendix A** for more details)
Functional Group:		Special Function Pin	
5 - 6	NC	NC	No connection (float)
8 - 14	NC	NC	No connection (float)
22 - 28	NC	NC	No connection (float)
29*	GND PAD	Ground Pad	Bottom of LGA package must be connected to circuit ground

2.0 Operating Specifications

2.1 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit	Notes
Storage Temperature	T_S	-40	85	°C	
Lead-Free Solder Temperature	T_{SOLDER}		260	°C	
Supply Voltage	V_{DD}	-0.5	2.1	V	
	V_{DDIO}	-0.5	3.6	V	
Input Voltage	V_{IN}	-0.5	3.6	V	All I/O pins
ESD	ESD_{HBM}		2	kV	All pins (Human Body Model)

Notes:

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied.
3. Functional operation should be restricted to the Recommended Operating Conditions.

2.2 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit	Notes
Operating Temperature	T_A	0		60	°C	
Power Supply Voltage	V_{DD}	1.8	2.0	2.1	V	Including supply noise
	V_{DDIO}	1.8	2.0	3.6	V	$V_{DDIO} \geq V_{DD}$
Power Supply Rise Time	t_{RT}	0.15		20	ms	0 to V_{DD} min
Supply Noise (Sinusoidal)	V_{NA}			100	mV_{p-p}	10 kHz – 75 MHz
Serial Port Clock Frequency	f_{SCLK}			2	MHz	50% duty cycle
Working Range	Z	80			mm	
Effective Viewing Angle	V_A		42		°	
Illuminance	Lx	60			lux	Tested under florescent light on crimson carpet, light grey vinyl & light grey cement surfaces.
Frame Rate	F_R		121		fps	
Speed	S			7.4	rad/s	

Note: PixArt does not guarantee the performance of the system beyond the recommended operating condition limits.

2.3 DC Characteristics

Table 4. DC Electrical Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Current	I_{DD_RUN}		6		mA	Average current. No load on MISO, MOTION.
Power Down Current	I_{PD}		12		uA	
Input Low Voltage	V_{IL}			0.3*V_{DDIO}	V	SCLK, MOSI, NCS
Input High Voltage	V_{IH}	0.7*V_{DDIO}			V	SCLK, MOSI, NCS
Input Hysteresis	V_{I_HYS}		100		mV	SCLK, MOSI, NCS
Input Leakage Current	I_{LEAK}		± 1	± 10	uA	V_{in} = V_{DDIO} or 0V, SCLK, MOSI, NCS
Output Low Voltage	V_{OL}			0.45	V	I_{OUT} = 1mA, MISO, MOTION
Output High Voltage	V_{OH}	V_{DDIO} - 0.45			V	I_{OUT} = -1mA, MISO, MOTION

Note: All the parameters are tested under operating conditions: V_{DD} = 2.0V, V_{DDIO} = 2.0V, T_A = 25°C.

2.4 AC Characteristics

Table 5. AC Electrical Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Motion Delay After Reset	$t_{MOT-RST}$	50			ms	From reset to valid motion, assuming motion is present
Shutdown	t_{STDWN}			500	us	From Shutdown mode active to low current
Wake from Shutdown	t_{WAKEUP}	50			ms	From Shutdown mode inactive to valid motion. Notes: A RESET must be asserted after a shutdown. Refer to section "Notes on Shutdown", also note $t_{MOT-RST.}$
MISO Rise Time	t_{r-MISO}		50		ns	C_L = 100pF
MISO Fall Time	t_{f-MISO}		50		ns	C_L = 100pF
MISO Delay After SCLK	$t_{DLY-MISO}$			120	ns	From SCLK falling edge to MISO data valid, no load conditions
MISO Hold Time	$t_{hold-MISO}$	200			ns	Data held until next falling SCLK edge
MOSI Hold Time	$t_{hold-MOSI}$	200			ns	Amount of time data is valid after SCLK rising edge
MOSI Setup Time	$t_{setup-MOSI}$	120			ns	From data valid to SCLK rising edge
SPI Time Between Write Commands	t_{SWW}	10.5			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second data byte.
SPI Time Between Write And Read Commands	t_{SWR}	6			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second address byte.
SPI Time Between Read And Subsequent Commands	t_{SRW} t_{SRR}	1.5			µs	From rising SCLK for last bit of the first data byte, to falling SCLK for the first bit of the address byte of the next command.
SPI Read Address-Data Delay	t_{SRAD}	2			µs	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read.

NCS Inactive After Motion Burst	t_{BEXIT}	500			ns	Minimum NCS inactive time after motion burst before next SPI usage
NCS To SCLK Active	$t_{NCS-SCLK}$	120			ns	From last NCS falling edge to first SCLK rising edge
SCLK To NCS Inactive (For Read Operation)	$t_{SCLK-NCS}$	120			ns	From last SCLK rising edge to NCS rising edge, for valid MISO data transfer
SCLK To NCS Inactive (For Write Operation)	$t_{SCLK-NCS}$	2			µs	From last SCLK rising edge to NCS rising edge, for valid MOSI data transfer
NCS To MISO High-Z	$t_{NCS-MISO}$			500	ns	From NCS rising edge to MISO high-Z state
MOTION Rise Time	$t_{r-MOTION}$		50		ns	C_L = 100pF
MOTION Fall Time	$t_{f-MOTION}$		50		ns	C_L = 100pF
Input Capacitance	C_{in}		50		pF	SCLK, MOSI, NCS
Load Capacitance	C_L			100	pF	MISO, MOTION
Transient Supply Current	I_{DDT}			70	mA	Max supply current during the supply ramp from 0V to V_{DD} with min 150 us and max 20 ms rise time (does not include charging currents for bypass capacitors).
	I_{DDTIO}			70	mA	Max supply current during the supply ramp from 0V to V_{DDIO} with min 150 us and max 20 ms rise time (does not include charging currents for bypass capacitors).

Note: All the parameters are tested under operating conditions: V_{DD} = 2.0V, V_{DDIO} = 2.0V, T_A = 25°C.

3.0 Mechanical Specifications

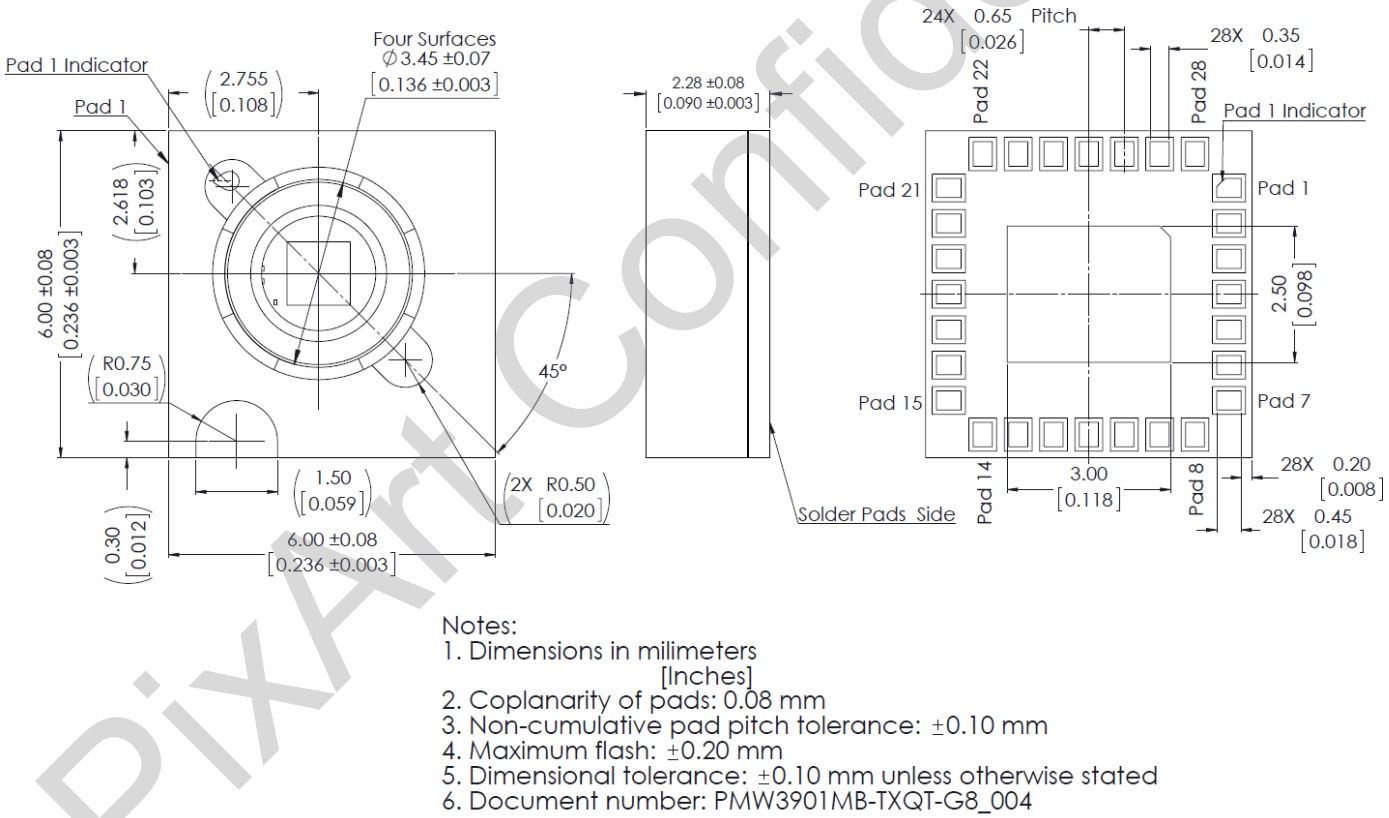
3.1 Package Marking

Refer Figure 1. Pin Configuration for the code marking location on the device package.

Table 6. Code Identification

Code	Marking	Description
Product Number	P3901	Part number label
Lot Code	YWX	Y: Year W: Week X: Reserved as PixArt reference

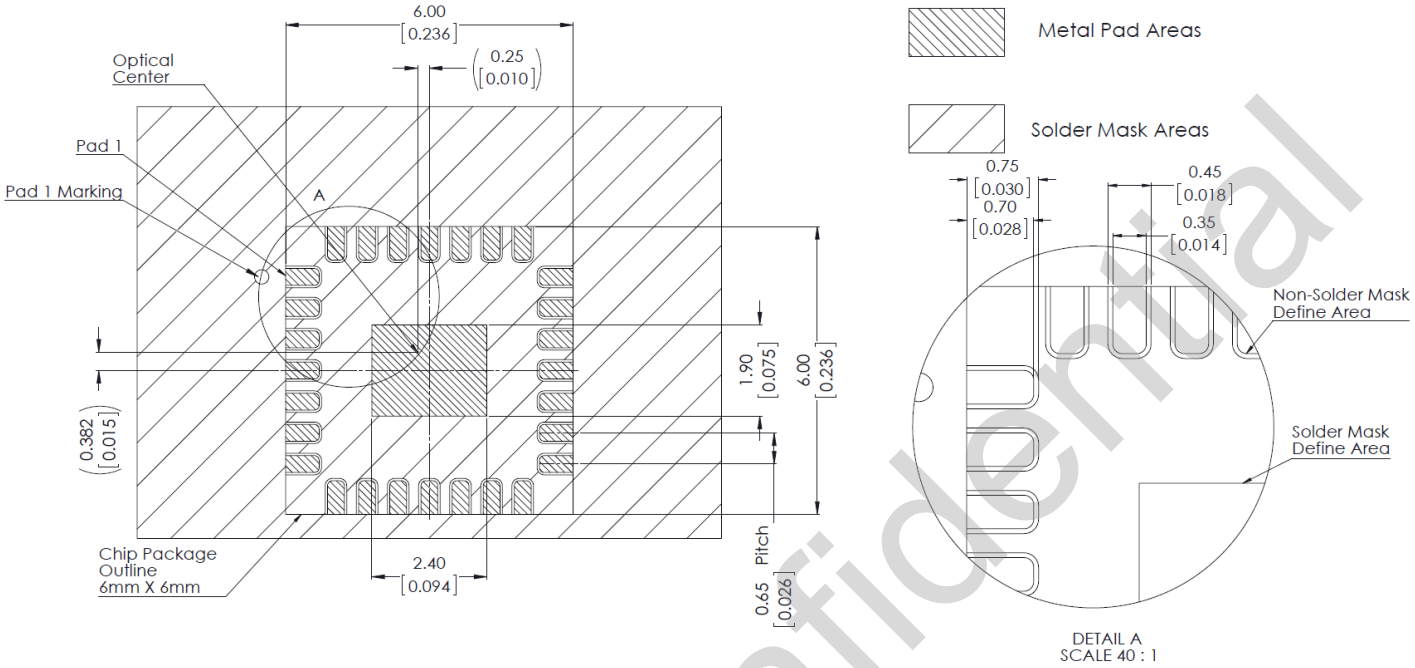
3.2 LGA Package Outline Drawing



Notes:
1. Dimensions in milimeters
[Inches]
2. Coplanarity of pads: 0.08 mm
3. Non-cumulative pad pitch tolerance: ±0.10 mm
4. Maximum flash: ±0.20 mm
5. Dimensional tolerance: ±0.10 mm unless otherwise stated
6. Document number: PMW3901MB-TXQT-G8_004

CAUTION: It is advised that normal static discharge precautions be taken in handling and assembling of this component to prevent damage and/or degradation which may be induced by ESD.

Figure 2. LGA Package Outline Drawing



Note: Bottom center pad of LGA package must be connected to circuit ground.

Figure 3. Recommended PCB Layout

3.3 L214-ZSZ Lens Assembly Drawings

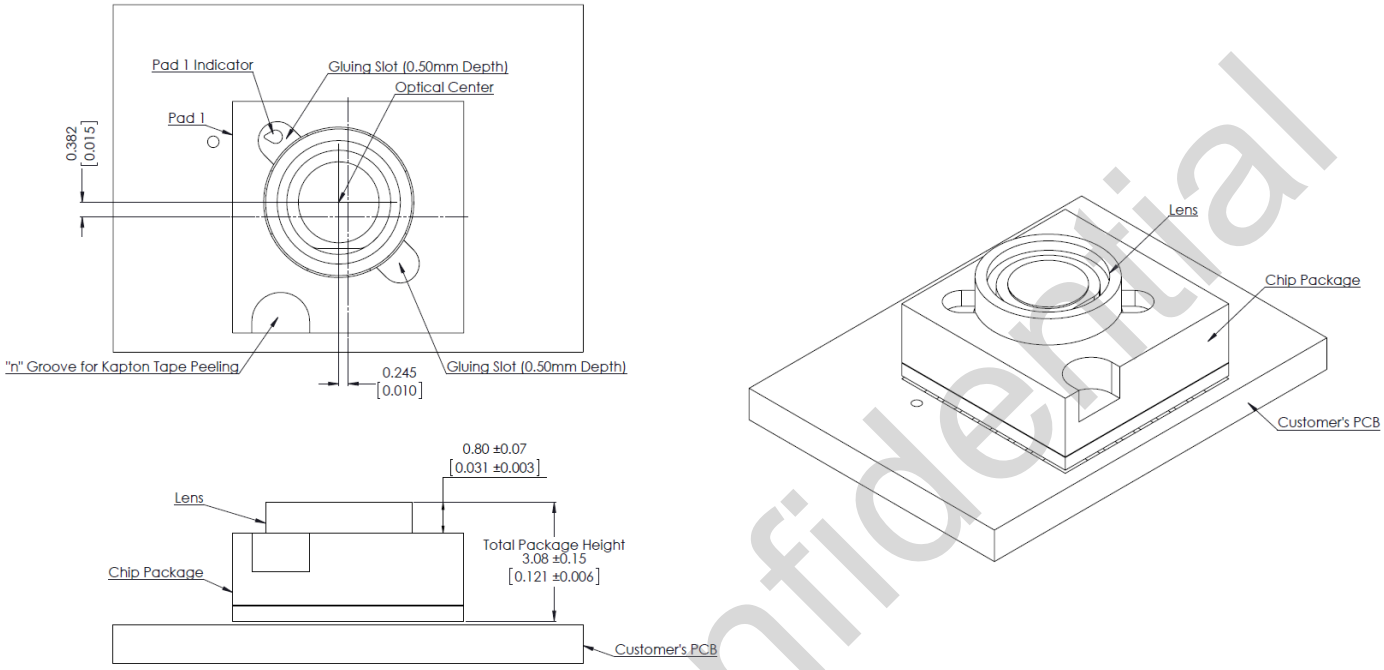


Figure 4. System Assembly View with L214-ZSZ

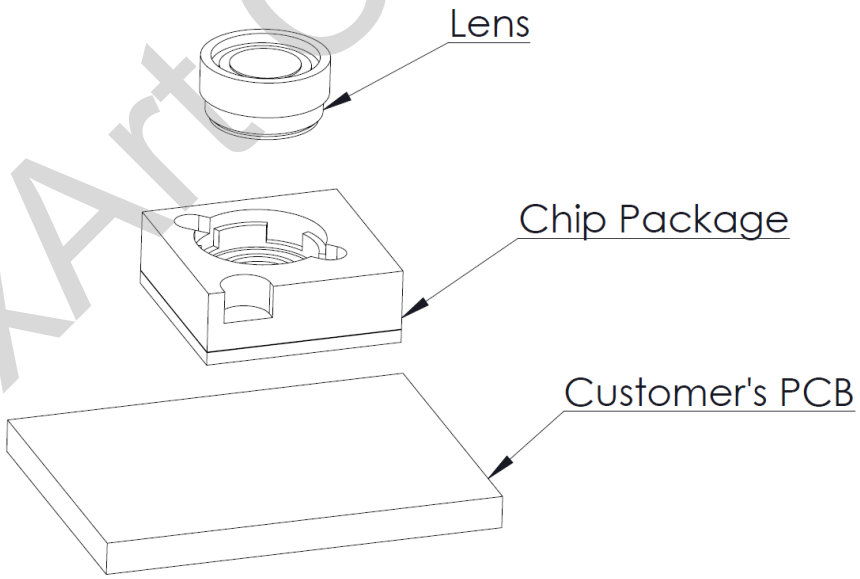


Figure 5. Exploded View of System Assembly

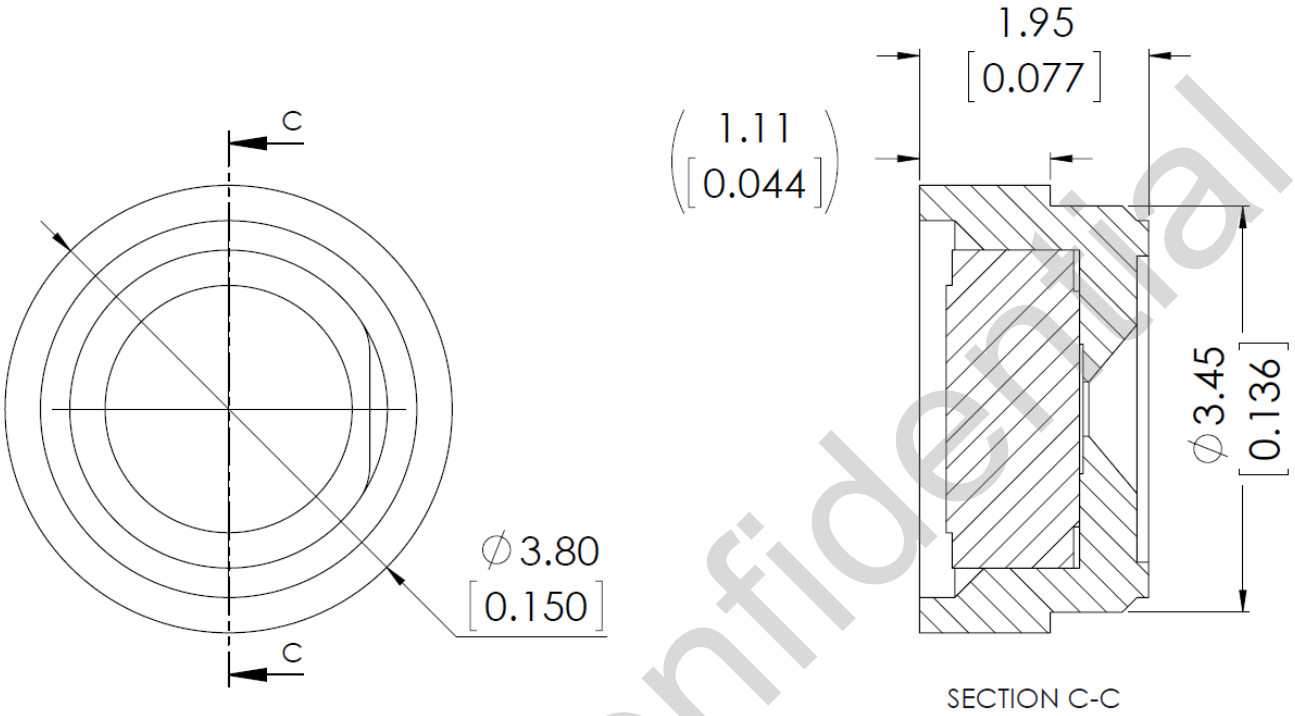
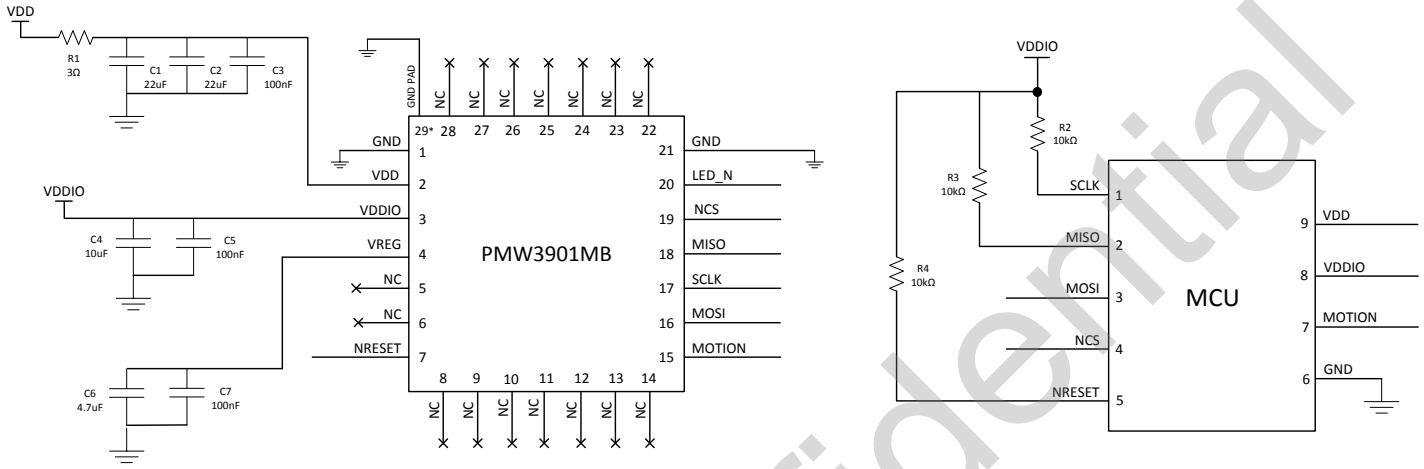


Figure 6. L214-ZSZ Lens Outline Drawing

4.0 System Level Description

4.1 Reference Schematic



Note:
1. All capacitors must be placed as close as possible to VDD, VDDIO & VREG pins.
2. Ceramic non-polarity capacitors are recommended.

Figure 7. PMW3901MB Reference Schematics

5.0 Registers

5.1 Registers List

PMW3901MB registers are accessible via the serial port. The registers are used to read motion data and status as well as to set the device configuration.

Table 7. Register List

Address	Register Name	Access	Reset	Address	Register Name	Access	Reset
0x00	Product_ID	RO	0x49	0x0B	Shutter_Lower	RO	0x00
0x01	Revision_ID	RO	0x00	0x0C	Shutter_Upper	RO	0x00
0x02	Motion	R/W	0x00	0x15	Observation	R/W	0x00
0x03	Delta_X_L	RO	0x00	0x16	Motion_Burst	RO	0x00
0x04	Delta_X_H	RO	0x00	0x3A	Power_Up_Reset	WO	N/A
0x05	Delta_Y_L	RO	0x00	0x3B	Shutdown	WO	N/A
0x06	Delta_Y_H	RO	0x00	0x58	RawData_Grab	R/W	0x00
0x07	Squal	RO	0x00	0x59	RawData_Grab_Status	RO	0x00
0x08	RawData_Sum	RO	0x00	0x5B	Orientation	R/W	0xE0
0x09	Maximum_RawData	RO	0x00	0x5F	Inverse_Product_ID	RO	0xB6
0x0A	Minimum_RawData	RO	0x00				